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Schematics and other handouts serve for informational purposes only!

Design drawn by:	VG
Checked by:	VY
Assembly variant:	P1C-5-A
Created by:	VY
Modified by:	VY
Modified at:	2020-09-30



Title:		
S7Mini - Legal Notices		
A4	Number: TE0890 P1C-5-A	Rev. 02
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A

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REV	Description	
-01	Initial revision	IG
-02	<ul style="list-style-type: none"> <li>1. U2 HyperRAM IS66WVH8M8BLL-100B1LI is EOL replaced with IS66WVH8M8DBLL-100B1LI.</li> <li>2. U6 FLASH N25Q064A13ESE40 is EOL and replaced with IS25LP064D-JBLE.</li> <li>3. U4 DC-DC EP53A7LQI is EOL replaced with MPM3834CGPA.</li> <li>4. U10 DC-DC EP53A7HQI is EOL replaced with MPM3834CGPA.</li> <li>5. Added pull up resistor R3 to signal CS0 (U2 HyperRAM).</li> <li>6. Added pull-up resistor R23 on DC-DC PG signal.</li> <li>7. Added pull-up resistors R25, R26 (U6 Serial Flash).</li> <li>8. Added J5 (JTAG only Enable).</li> <li>9. L1 Ferrit bead BKP0603HS121-T is EOL replaced with MPZ0603S121HT000.</li> <li>10. R5 DNP replaced with 1K.</li> <li>11. Added Test points TP14 - TP19.</li> <li>12. Added serial termination R27 to improve impedance matching .</li> <li>13. Added resistor R28 according to MPM3834CGPA datasheet.</li> </ul>	AL/VY/VG (05.06.2024)

B


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		Title: <b>S7Mini - Revision History</b>	
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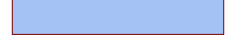
3

4

U\_A-Headers  
A-Headers.SchDoc



U\_FPGA  
FPGA.SchDoc



U\_FPGA\_MISC  
FPGA\_MISC.SchDoc



U\_Flash\_RAM  
Flash\_RAM.SchDoc



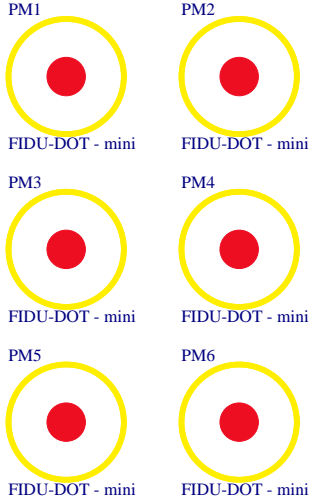
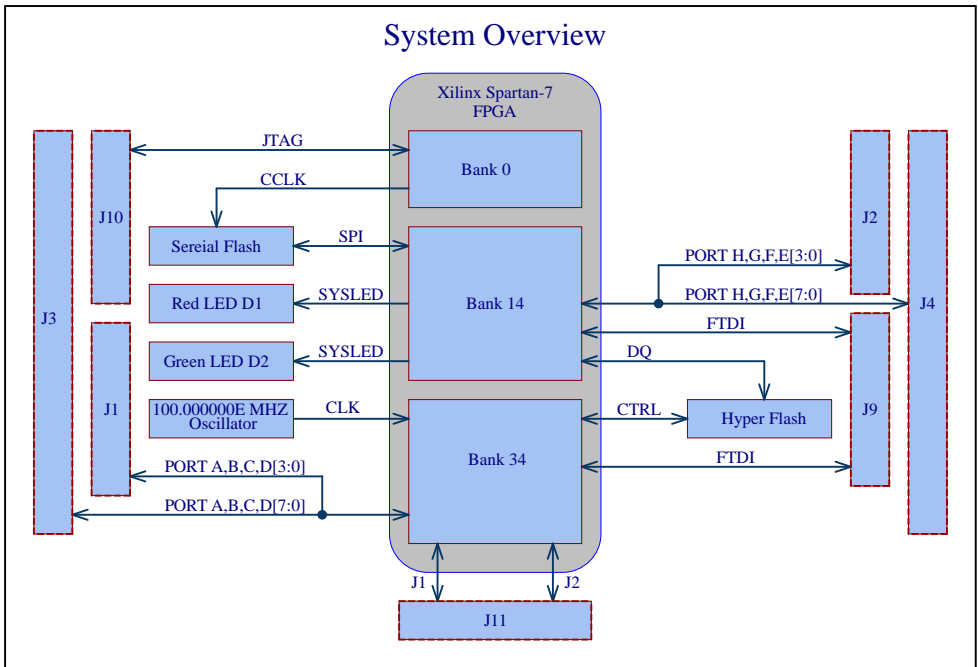
U\_PowerSupply  
PowerSupply.SchDoc



U\_PowerSupply  
Power\_Diagram.SchDoc



Serial  
Serialnumber 6,3 x 6.3mm

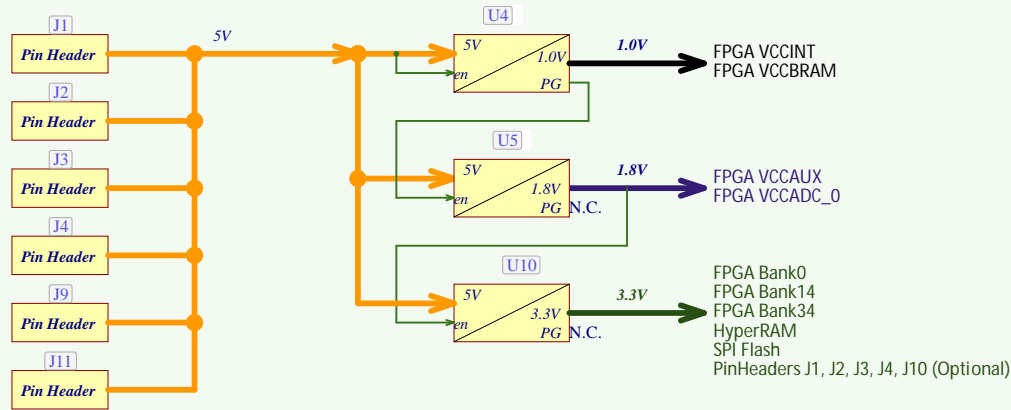


UKCA  
UKCA Logo on Top Overlay  
UKCA-TOPOVERLAY



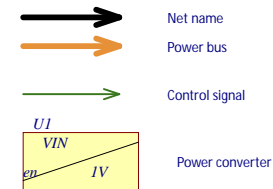
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## Power-on sequencing:



## Supported Voltage Ranges:

Power Rail	Direction	Range	Tolerance	Description	Note
5V	IN	5V	+/-5%	External Power	-
3.3V	OUT	3.3V	+/-3%	From internal DC-DC	-



	Title: <b>S7Mini - Power_Diagram</b>		
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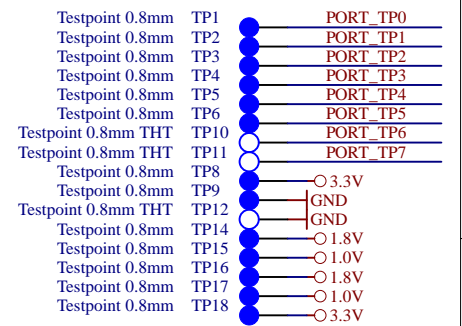
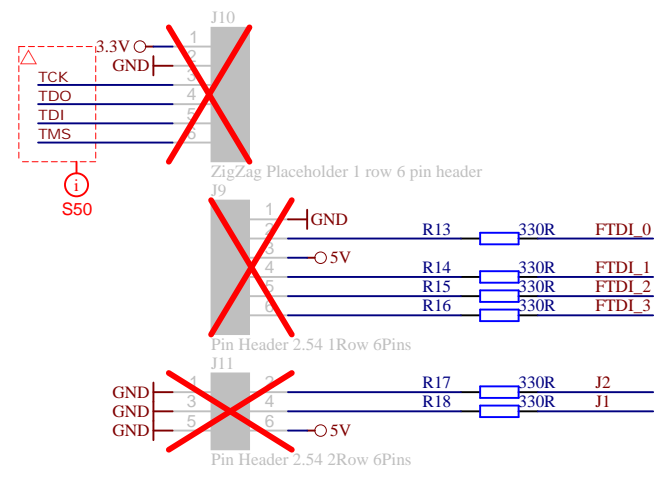
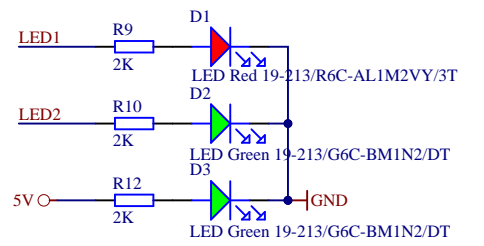
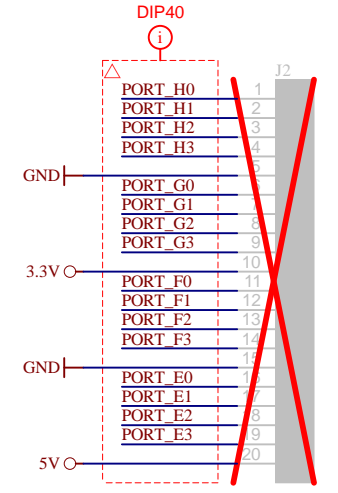
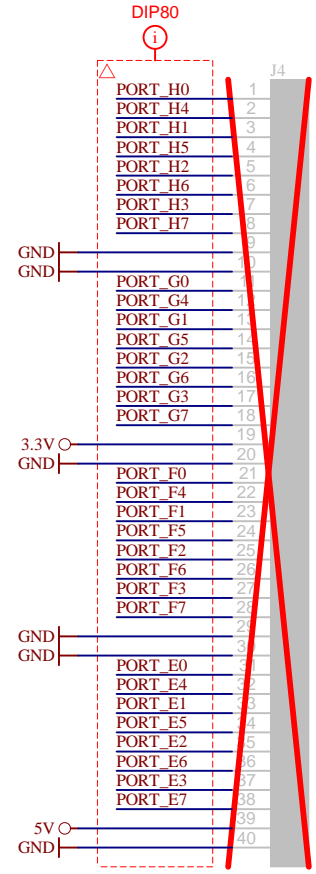
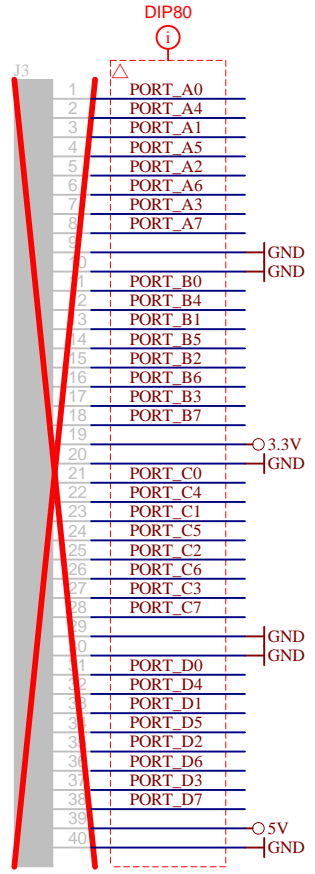
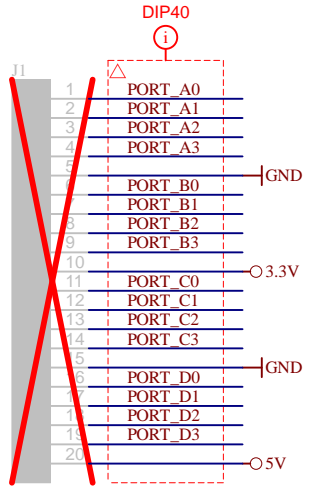
B

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Title: <b>S7Mini - A-Headers</b>		
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BOOTMODE = MASTER SPI

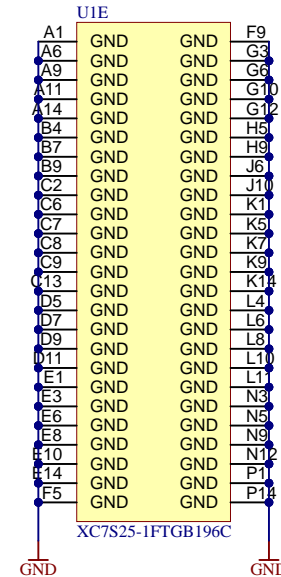
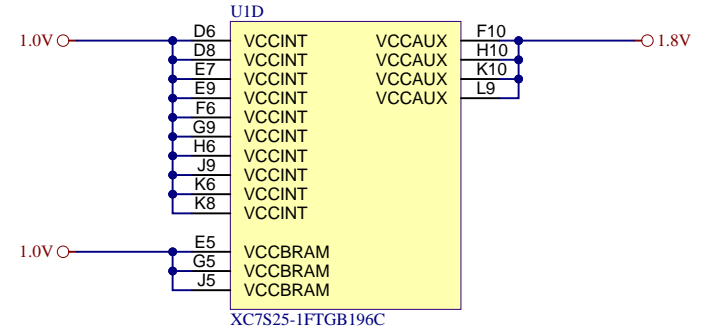
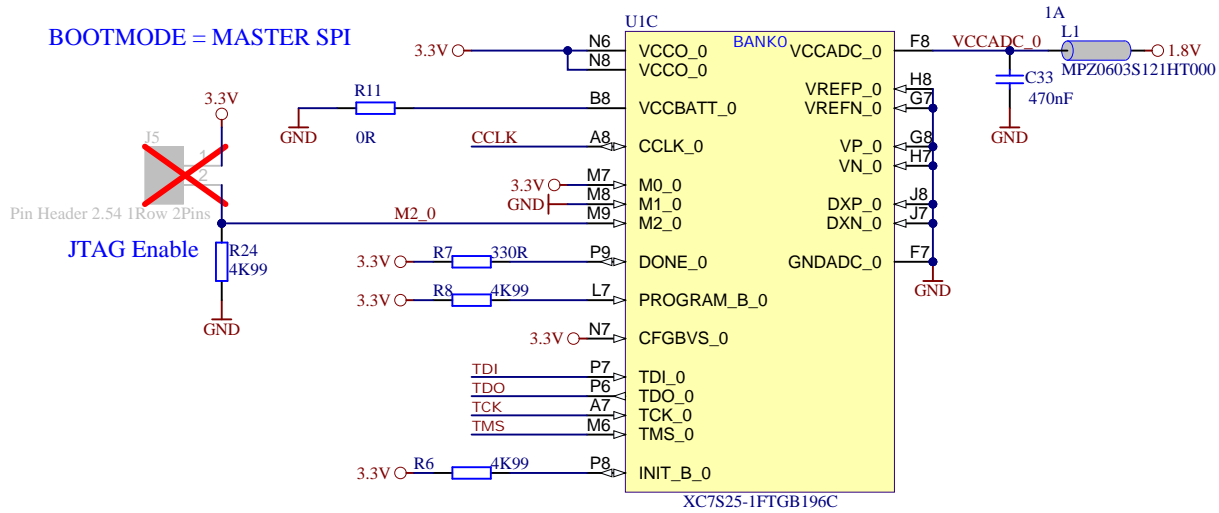
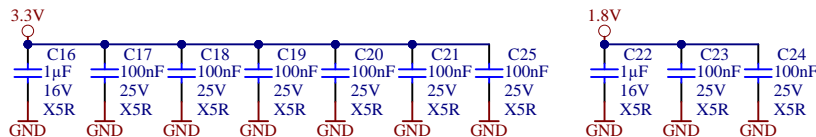
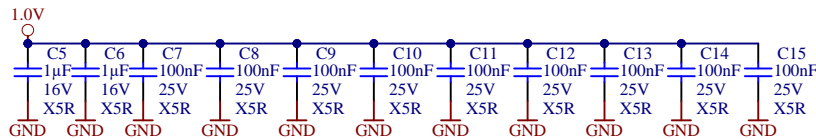


Table 2-1: 7 Series FPGA Configuration Modes

Configuration Mode	M[2:0]	Bus Width	CCLK Direction
Master Serial	000	x1	Output
Master SPI	001	x1, x2, x4	Output
Master BPI	010	x8, x16	Output
Master SelectMAP	100	x8, x16	Output
JTAG	101	x1	Not Applicable
Slave SelectMAP	110	x8, x16, x32 <sup>(1)</sup>	Input
Slave Serial <sup>(2)</sup>	111	x1	Input



Title: **S7Mini - FPGA\_MISC**

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A

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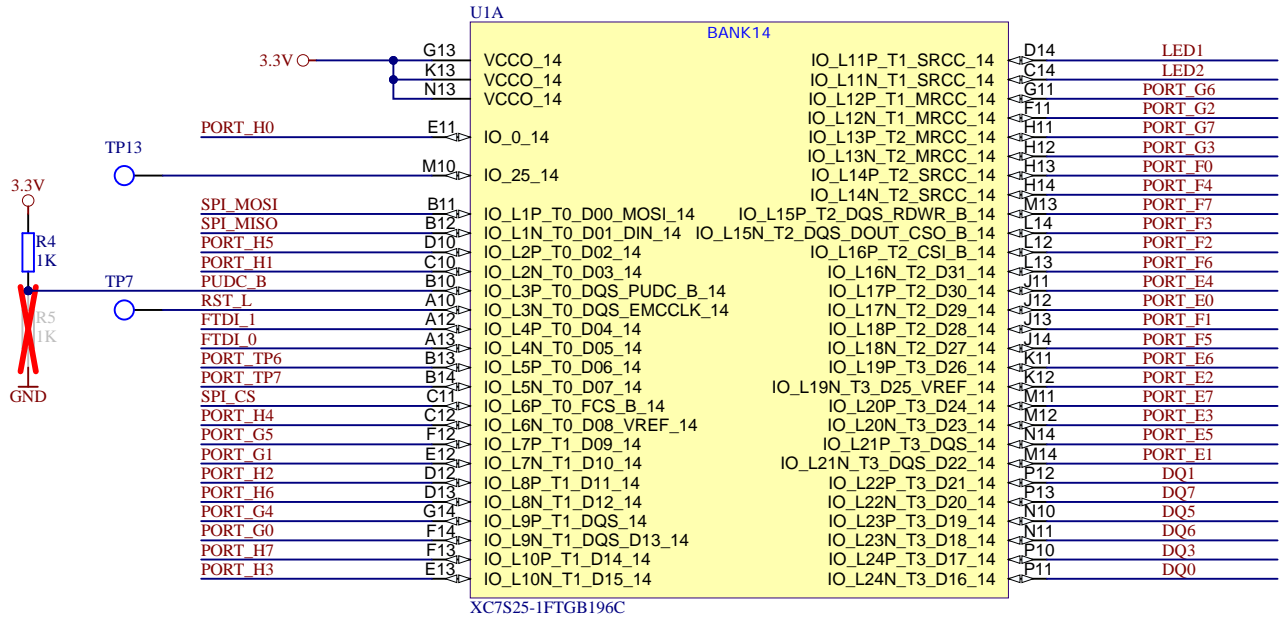
B

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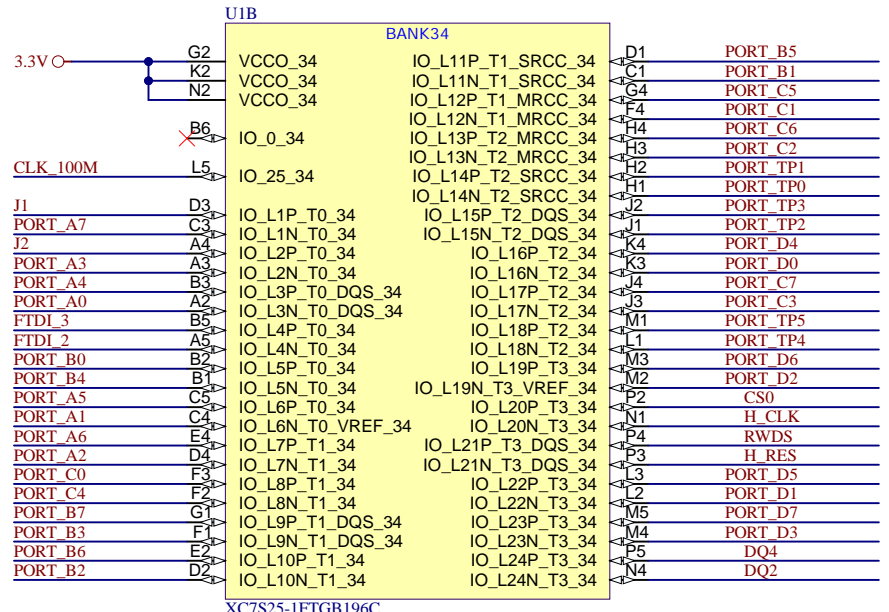
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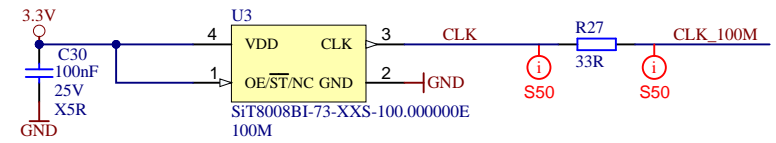
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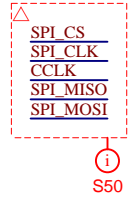
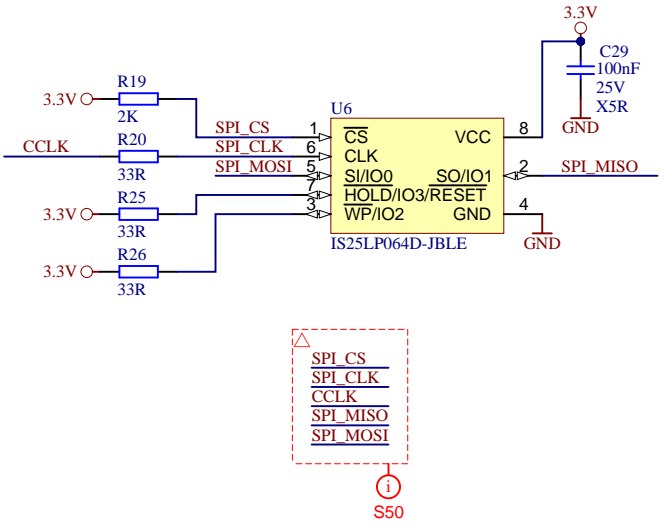
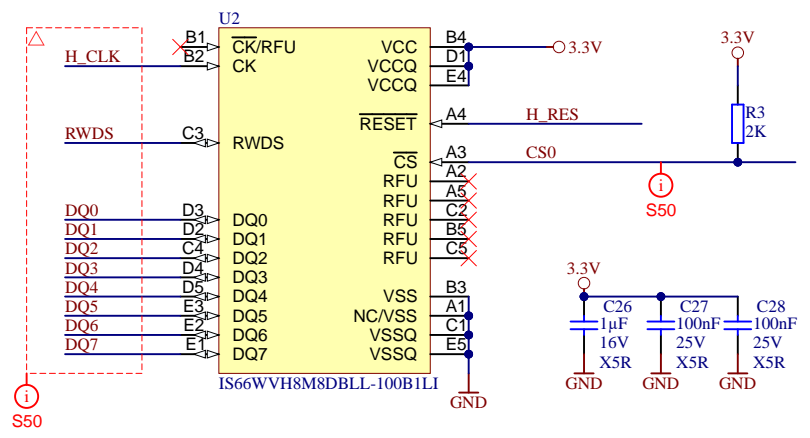
XC7S25-1FTGB196C



XC7S25-1FTGB196C

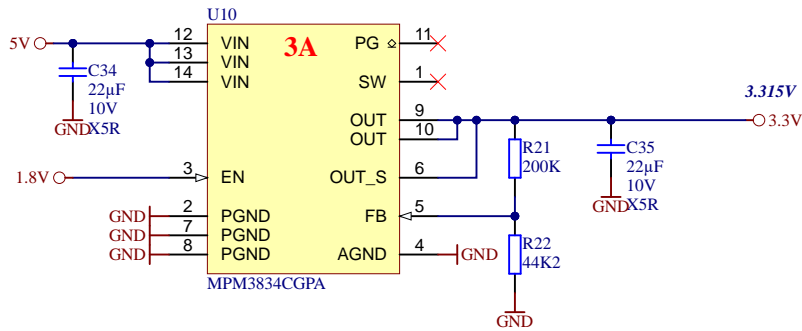
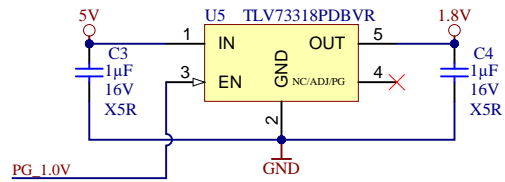
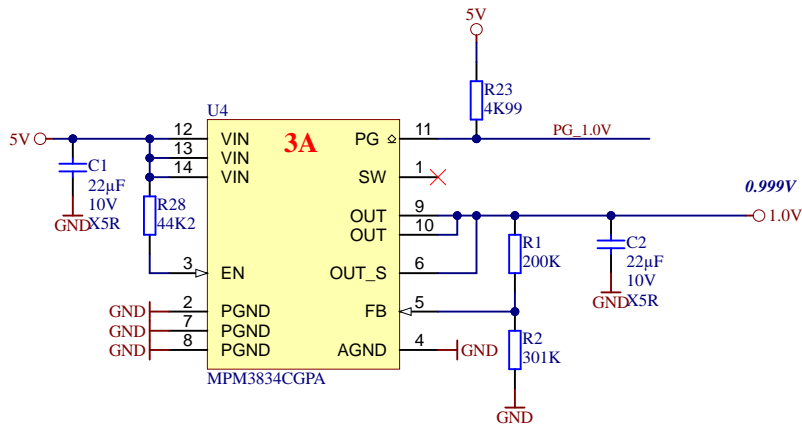



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