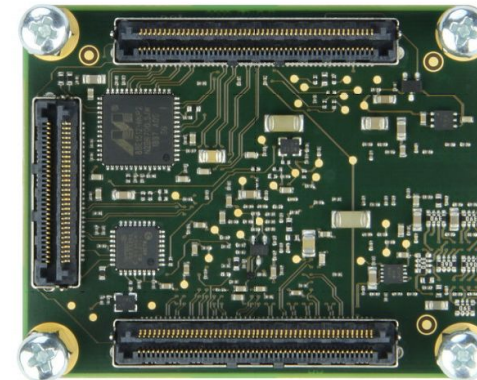
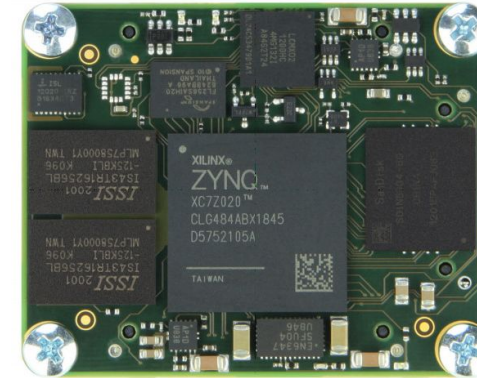




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Project is protected under copyright and we strongly and strictly prohibit the reverse engineering or recreation, even if the design is just adapted or modified. TE0720 is protected under such right and in case of plagiarism we will have to do anything necessary in order to protect our assets.

Schematics and other handouts serve for informational purposes only!

	Title: GigaZee		
	A4	Number: TE0720 61C33MA	Rev. 04
	Date: 2022-01-19	Copyright: Trenz Electronic GmbH / TT	Page 1 of 20
	Filename: Legal Notices Modules.SchDoc		

1		2		3		4	
A	REV		Description				
	-01		Initial revision				
	-02						
	-03						
B	-04		1. Revised power supply circuit, replaced next components: - EN6347QI (U1) by MPM3840GQV-Z, - EP53F8QI (U2, U3) by MPM3834CGPA, - TPS27082LDDCR (Q1) by MP5077GG-Z. 2. Added power supervisor BD39040MUF (U27). Next signal connected to system controller: - PG_All (U27 - U19.C12) with pull-up resistor R67; - WDEN (U27.13 - U19.C6) with pull-down resistor R80; - WDIN (U27.14 - U19.N8); - WDOUT (U27.16 - U19.M3). 3. Signal MIO8 (U5.E5) connected to system controller (U19.N7) 4. Added pull-down resistors R64 (net ON_1V0) and R65 (net ON_1V8) 5. Revised voltage supervisor U26 circuit: U26.6 (VDD) connected to 3.3VIN, Added protection diode D3 to U26.3 (#MR input) 6. Replaced BKP0603HS (L1, L2, L3, L4, L5, L7, L8) by MPZ0603S121HT000 7. Auxiliary information has been added on Samtec B2B connectors page 8. PCB: Revised layout of power supplies 9. PCB: Revised layout of Samtec B2B signals. The length of the tracks has been changed. Pinout of Samtec B2B connectors not affected 10: PCB: Added option to install Heatsink SuperGrip (c) 11. Added capacitors C7, C8 (100uF, 1V) 12. Changed voltage divider resistors (R21, R61) to set the threshold for U26.		VY		
	-04A		1. Added note regarding VCCIO34, page B2B-Connectors		VY		
C							
D							
1		2		3		4	



Title:GigaZee - Revision History

A4

Number:TE072061C33MA

Rev.04

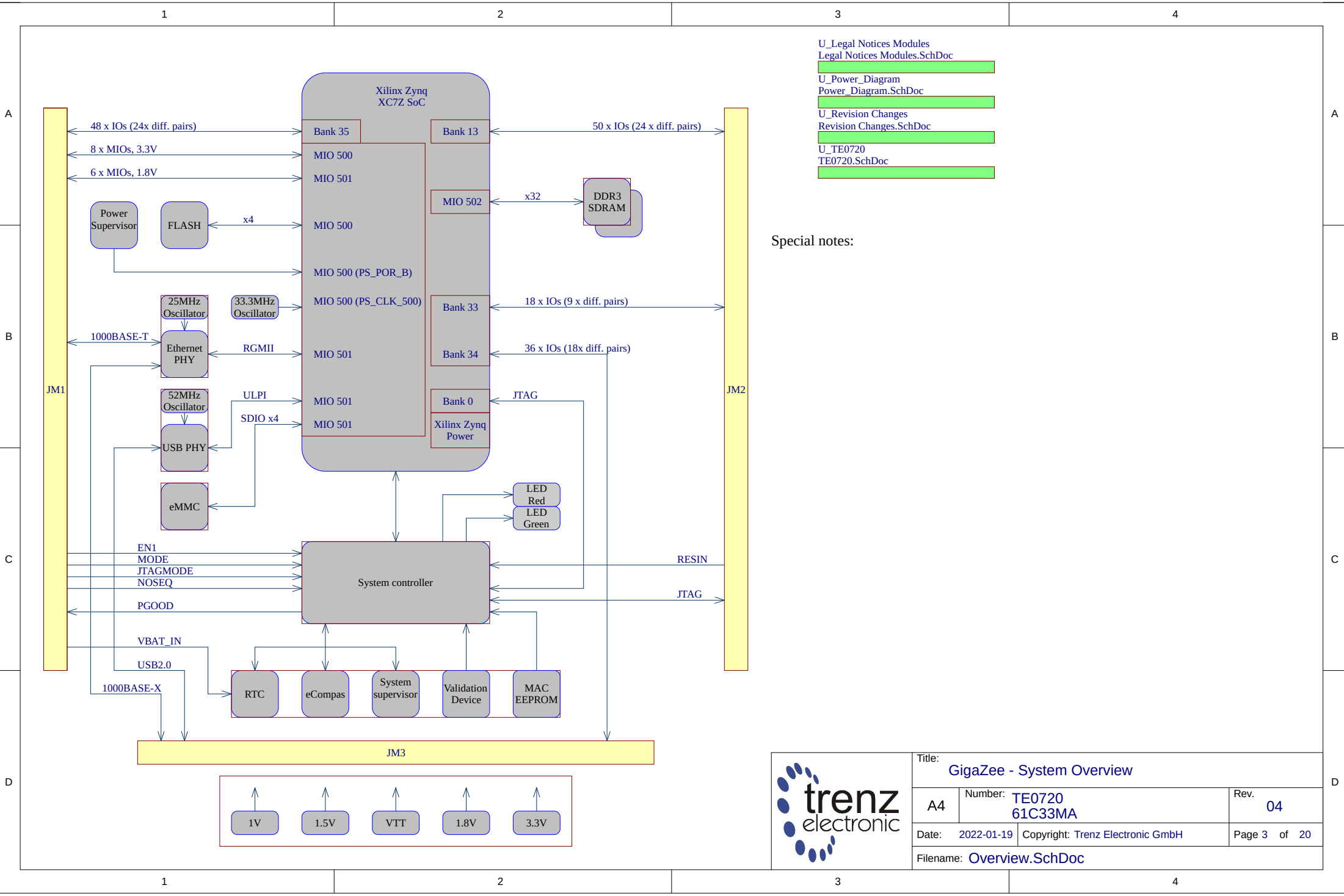
Date:2022-01-19

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Drawn by: VY

Filename: Revision Changes.SchDoc



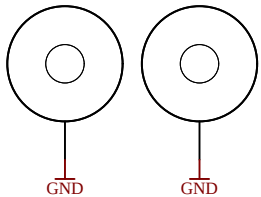
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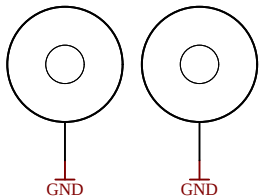
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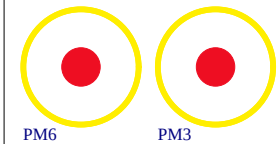
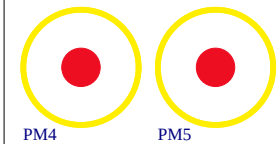
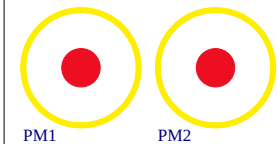
Mount.Hole 3.2mmMount.Hole 3.2mm



Mount.Hole 3.2mmMount.Hole 3.2mm



1V	TP1	Testpoint 0.8mm
VIN	TP2	Testpoint 0.8mm
1.5V	TP3	Testpoint 0.8mm
1.8V	TP4	Testpoint 0.8mm
VTT	TP5	Testpoint 0.8mm
VTTREF	TP6	Testpoint 0.8mm
3.3VIN	TP7	Testpoint 0.8mm
3.3V	TP8	Testpoint 0.8mm
VCCIO13	TP9	Testpoint 0.8mm
VCCIO33	TP10	Testpoint 0.8mm
VCCIO34	TP11	Testpoint 0.8mm
VCCIO35	TP12	Testpoint 0.8mm
AVCC	TP13	Testpoint 0.8mm
AVREF	TP14	Testpoint 0.8mm
AGND	TP15	Testpoint 0.8mm
GND	TP16	Testpoint 0.8mm
GND	TP17	Testpoint 0.8mm
GND	TP18	Testpoint 0.8mm
GND	TP19	Testpoint 0.8mm
GND	TP20	Testpoint 0.8mm



Serial
Serial
Serialnumber 6,3 x 6.3mm

Assembly variant 61C33MA
Created by MR
Modified by MR
Modified at 2021-07-06

SVN Revision Unknown revision



Title: GigaZee - TE0720

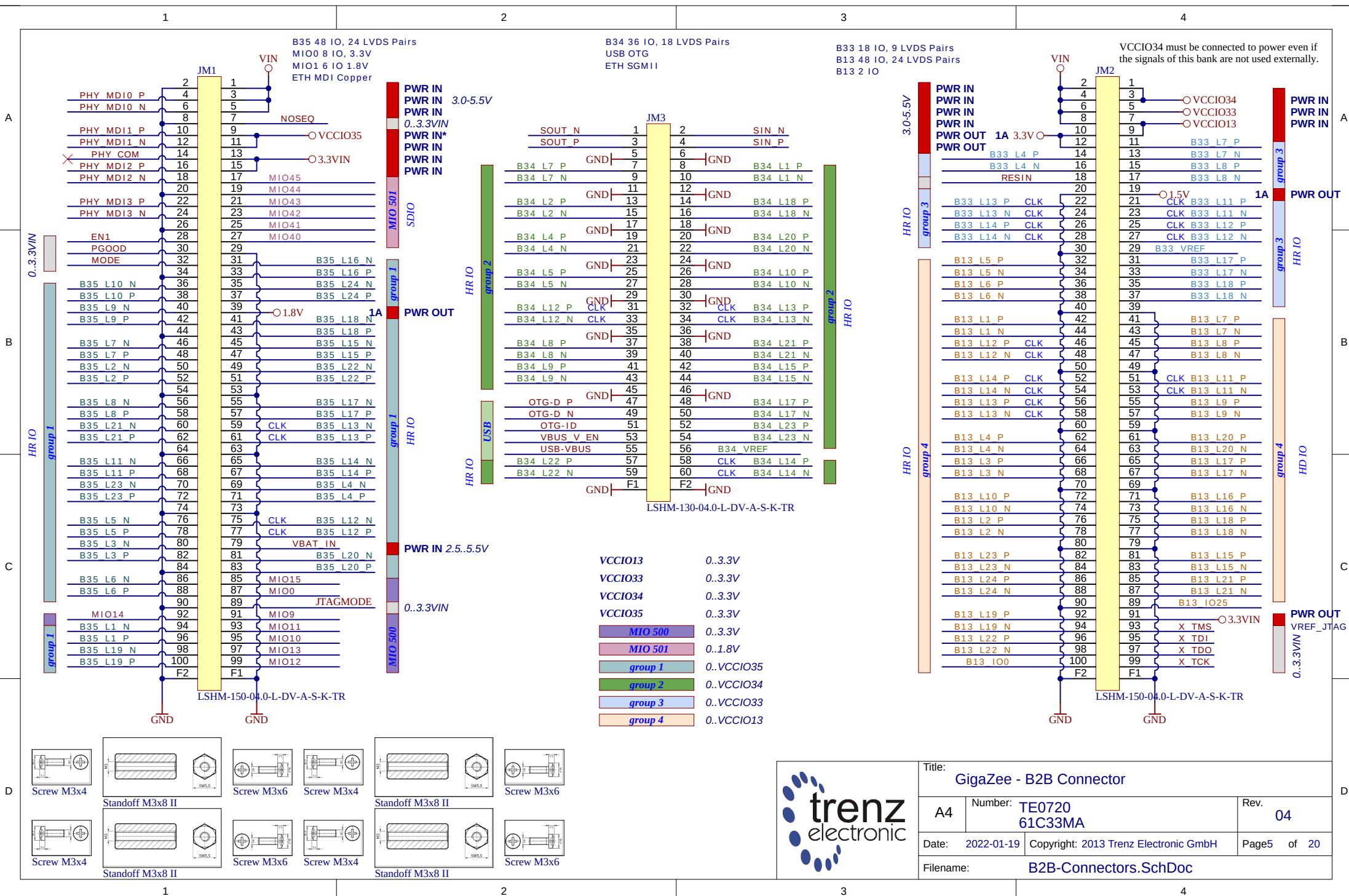
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Date: 2022-01-19	Copyright: 2013 Trenz Electronic GmbH	Page 4 of 20
Drawn by: VY	Filename: TE0720.SchDoc	

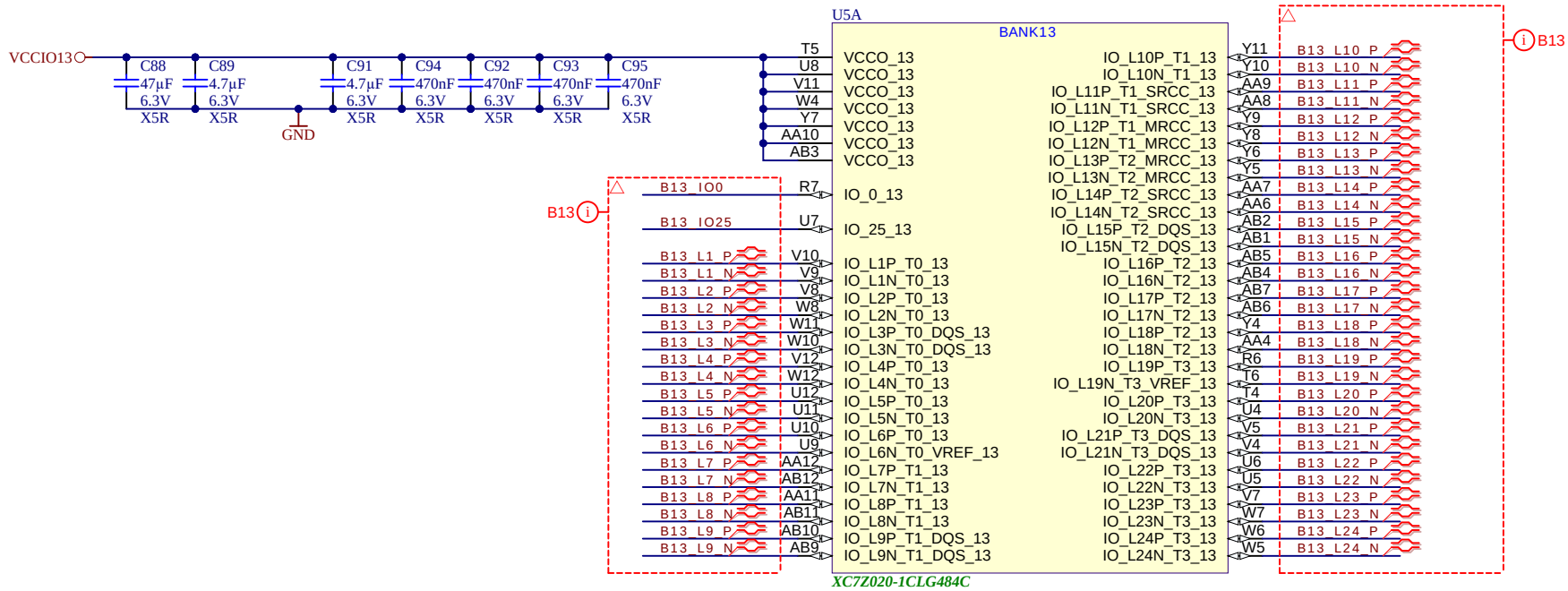
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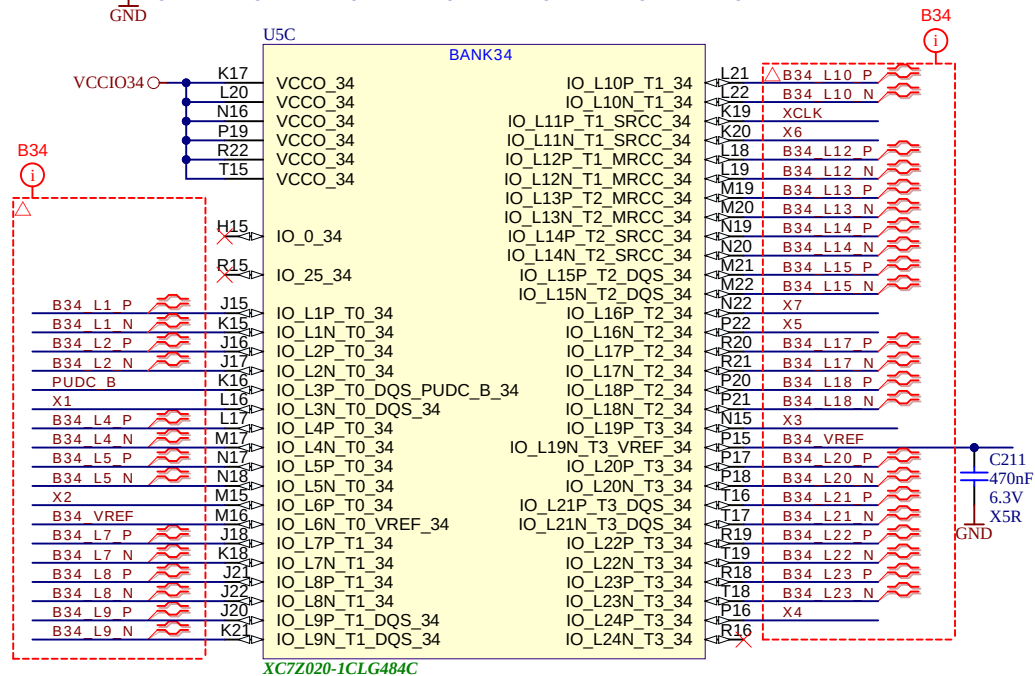
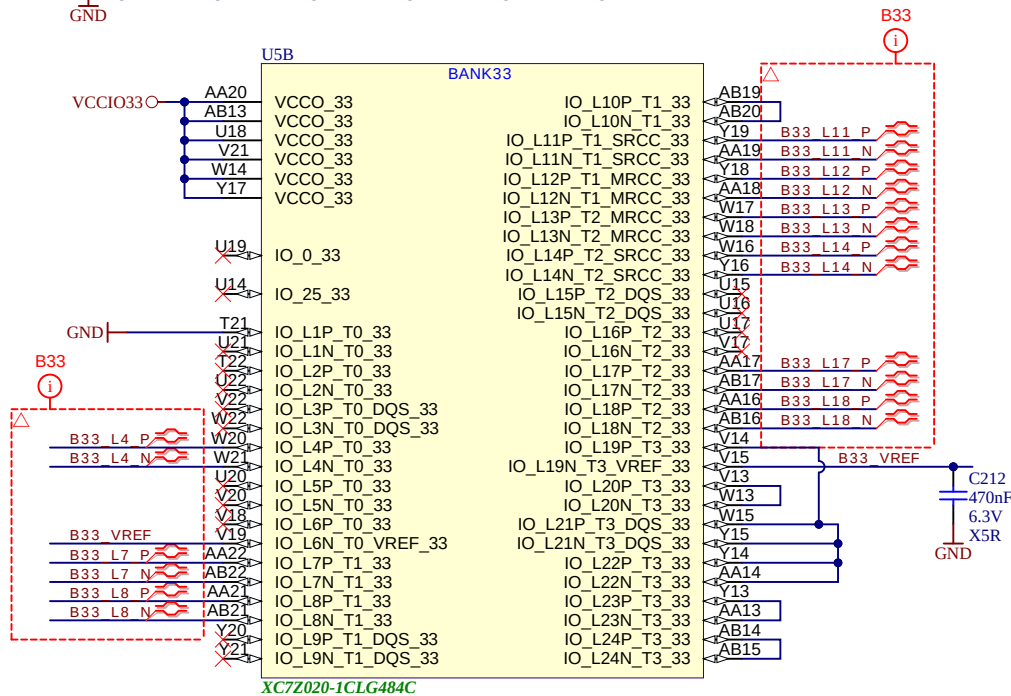
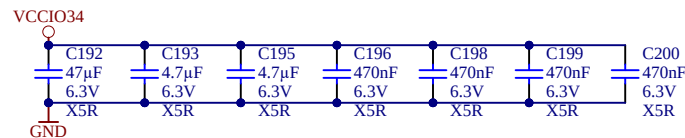
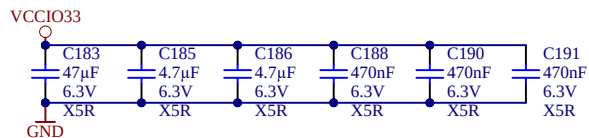
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	A4	Number: TE0720 61C33MA	Rev. 04
	Date: 2022-01-19	Copyright: 2013 Trenz Electronic GmbH	Page6 of 20
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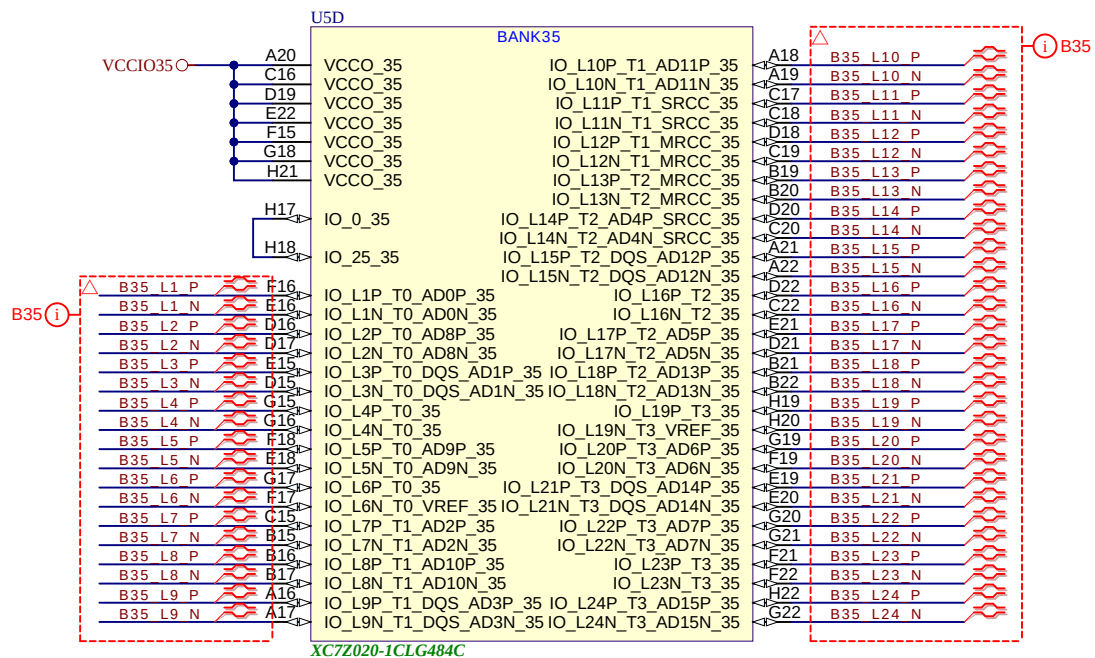
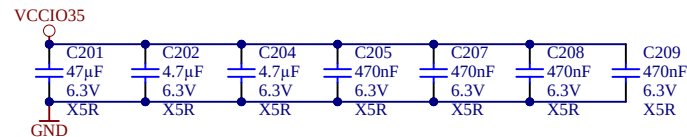
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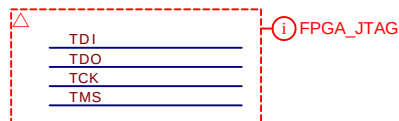
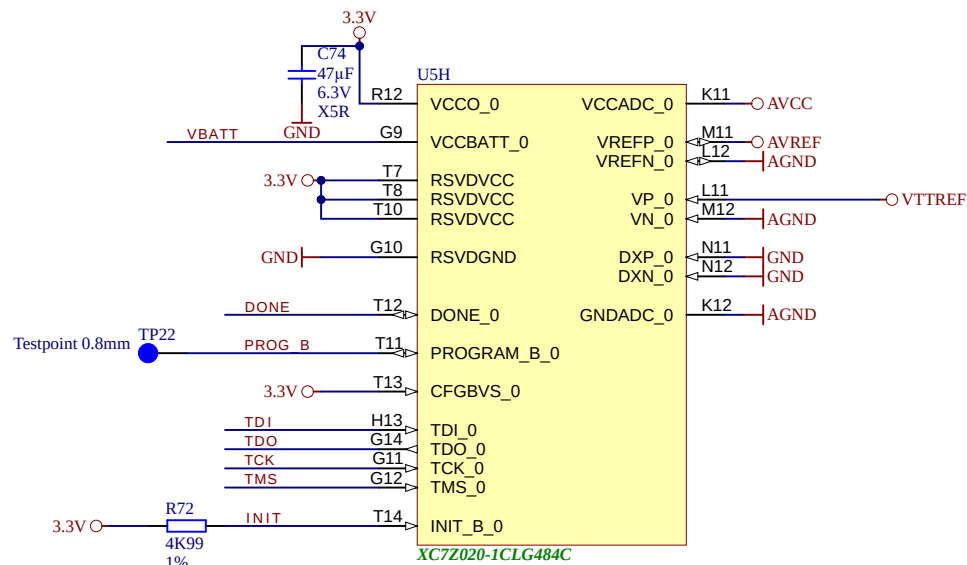
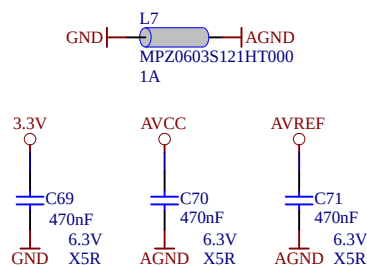
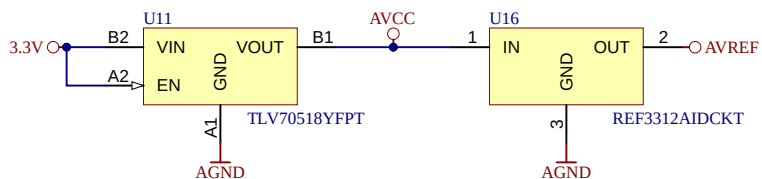
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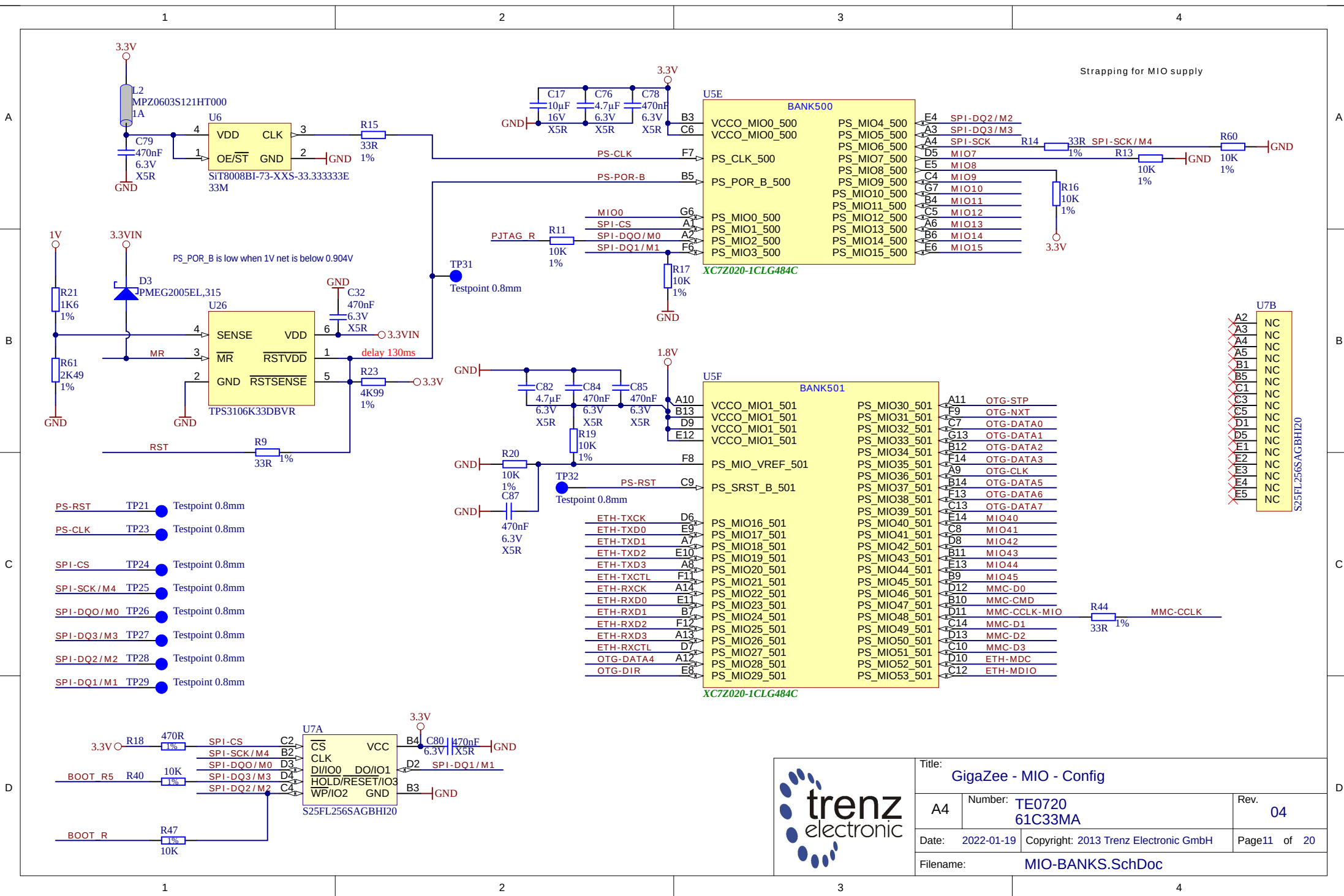
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Date: 2022-01-19	Copyright: 2013 Trenz Electronic GmbH		Page 8 of 20
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		A4	Rev. 04
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Filename: FPGA-MISC.SchDoc			



1

2

3

4

U5G

BANK502

E2
F5
H1
J4
K7
M3
N6
R2
V1

VCCO_DDR_502
VCCO_DDR_502
VCCO_DDR_502
VCCO_DDR_502
VCCO_DDR_502
VCCO_DDR_502
VCCO_DDR_502
VCCO_DDR_502
VCCO_DDR_502

PS_DDR_A0_502
PS_DDR_A1_502
PS_DDR_A2_502
PS_DDR_A3_502
PS_DDR_A4_502
PS_DDR_A5_502
PS_DDR_A6_502
PS_DDR_A7_502
PS_DDR_A8_502
PS_DDR_A9_502

M4 DDR3-A0
M5 DDR3-A1
K4 DDR3-A2
L4 DDR3-A3
K6 DDR3-A4
K5 DDR3-A5
J7 DDR3-A6
J6 DDR3-A7
J5 DDR3-A8
H5 DDR3-A9
J3 DDR3-A10
G5 DDR3-A11
H4 DDR3-A12
F4 DDR3-A13
G4 DDR3-A14

H7
P7

PS_DDR_VREF0_502
PS_DDR_VREF1_502

PS_DDR_A10_502
PS_DDR_A11_502
PS_DDR_A12_502
PS_DDR_A13_502
PS_DDR_A14_502

L7 DDR3-BA0
L6 DDR3-BA1
M6 DDR3-BA2

D1
C3
B2
D3
E3
E1
F2
F1
G2
G1
L1
L2
L3
K1
J1
K3
M1
T3
N3
T1
R3
M2
R1
AA3
U1
AA1
U2
W1
Y3
W3
Y1

PS_DDR_DQ0_502
PS_DDR_DQ1_502
PS_DDR_DQ2_502
PS_DDR_DQ3_502
PS_DDR_DQ4_502
PS_DDR_DQ5_502
PS_DDR_DQ6_502
PS_DDR_DQ7_502
PS_DDR_DQ8_502
PS_DDR_DQ9_502
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PS_DDR_DQ27_502
PS_DDR_DQ28_502
PS_DDR_DQ29_502
PS_DDR_DQ30_502
PS_DDR_DQ31_502

PS_DDR_BA0_502
PS_DDR_BA1_502
PS_DDR_BA2_502

PS_DDR_DM0_502
PS_DDR_DM1_502
PS_DDR_DM2_502
PS_DDR_DM3_502

N4 DDR3-CLK0_P
N5 DDR3-CLK0_N

N7 DDR-VRP
M7 DDR-VRN

P5 DDR3-ODT0
P6 DDR3-S0
V3 DDR3-CKE0
R4 DDR3-WE
P3 DDR3-CAS
R5 DDR3-RAS
F3 DDR3-RESET

C2
D2
H2
J2
N2
P2
V2
W2

PS_DDR_DQS_P0_502
PS_DDR_DQS_N0_502
PS_DDR_DQS_P1_502
PS_DDR_DQS_N1_502
PS_DDR_DQS_P2_502
PS_DDR_DQS_N2_502
PS_DDR_DQS_P3_502
PS_DDR_DQS_N3_502

XC7Z020-1CLG484C

1.5V

C126 100µF 6.3V X5R
C175 4.7µF 6.3V X5R
C176 470nF 6.3V X5R
C177 470nF 6.3V X5R
C179 470nF 6.3V X5R
C182 470nF 6.3V X5R

DDR3-A0	DDR3-BA0
DDR3-A1	DDR3-BA1
DDR3-A2	DDR3-BA2
DDR3-A3	
DDR3-A4	DDR3-WE
DDR3-A5	DDR3-CAS
DDR3-A6	DDR3-RAS
DDR3-A7	
DDR3-A8	DDR3-ODT0
DDR3-A9	DDR3-S0
DDR3-A10	DDR3-CKE0
DDR3-A11	
DDR3-A12	DDR3-CLK0_P
DDR3-A13	DDR3-CLK0_N
DDR3-A14	

LANE0

LANE1

LANE2

LANE3

DDR3-D0
DDR3-D1
DDR3-D2
DDR3-D3
DDR3-D4
DDR3-D5
DDR3-D6
DDR3-D7
DDR3-DM0
DDR3-DQS0_P
DDR3-DQS0_N

DDR3-D8
DDR3-D9
DDR3-D10
DDR3-D11
DDR3-D12
DDR3-D13
DDR3-D14
DDR3-D15
DDR3-DM1
DDR3-DQS1_P
DDR3-DQS1_N

DDR3-D16
DDR3-D17
DDR3-D18
DDR3-D19
DDR3-D20
DDR3-D21
DDR3-D22
DDR3-D23
DDR3-DM2
DDR3-DQS2_P
DDR3-DQS2_N

DDR3-D24
DDR3-D25
DDR3-D26
DDR3-D27
DDR3-D28
DDR3-D29
DDR3-D30
DDR3-D31
DDR3-DM3
DDR3-DQS3_P
DDR3-DQS3_N



Title:

GigaZee - B502

A4

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61C33MA

Rev.

04

Date:

2022-01-19

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Filename:

PS-DDR.SchDoc

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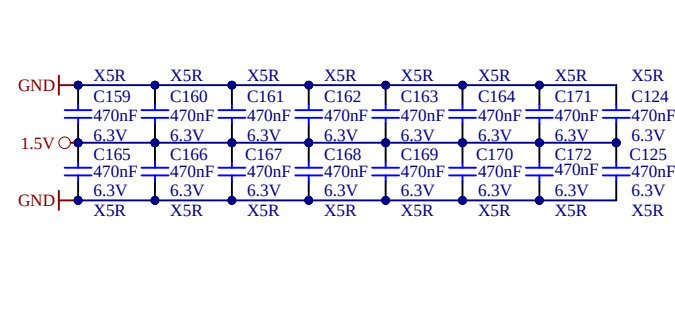
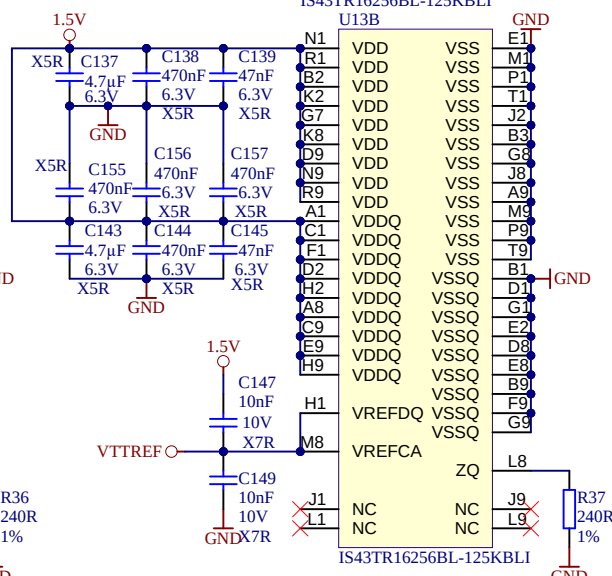
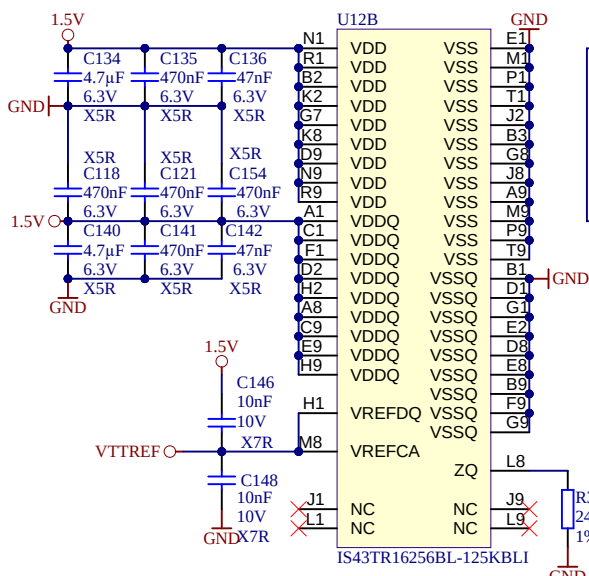
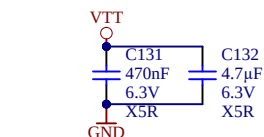
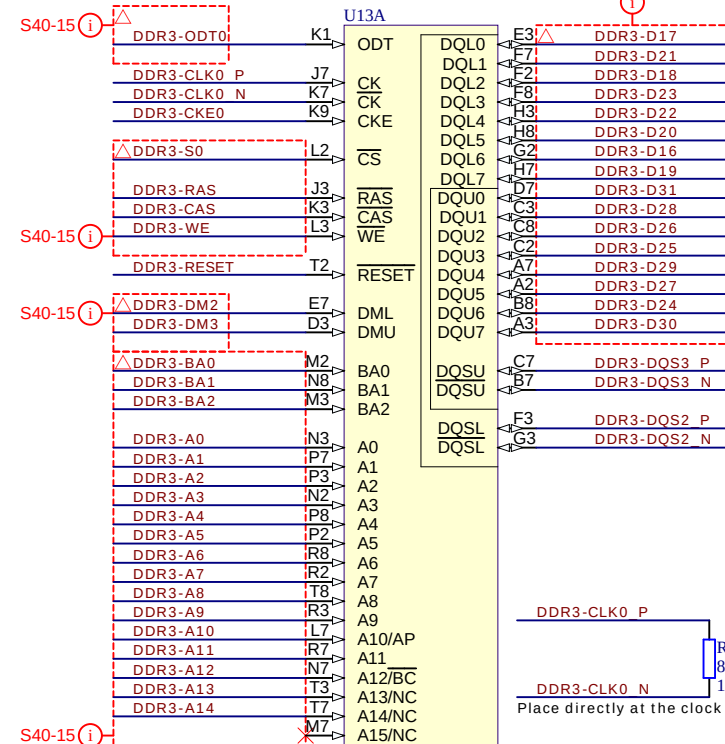
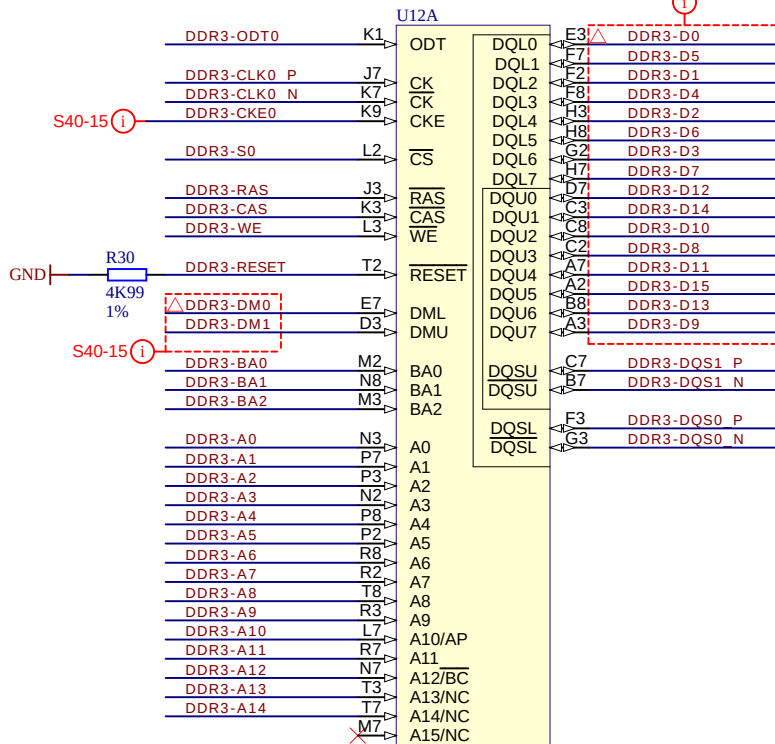
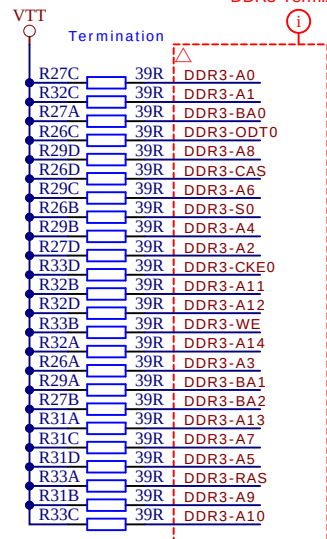
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4

DDR3-Terminator

S40-15

S40-15



Title: GigaZee - DDR3		
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Date: 2022-01-19	Copyright: 2013 Trenz Electronic GmbH	Page13 of 20
Filename: DDR3-RAM.SchDoc		

1

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3

4

1

2

3

4

A

A

B

B

C

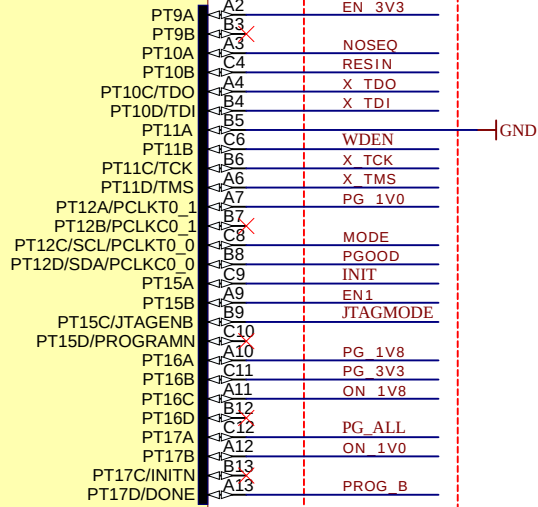
C

D

D

U19A

BANK 0



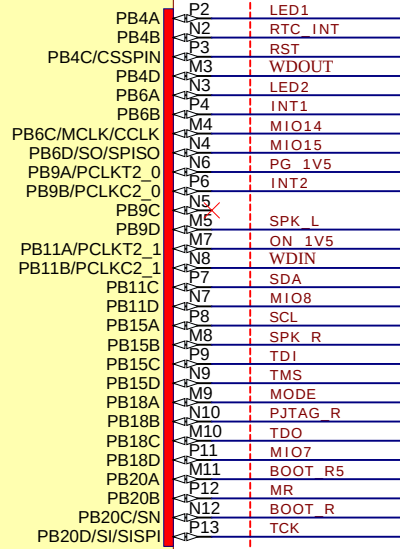
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CPLD_1V8

U19C

BANK 2

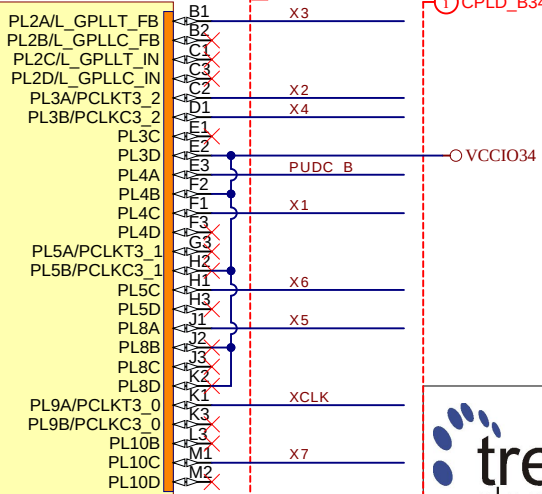


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U19D

BANK 3

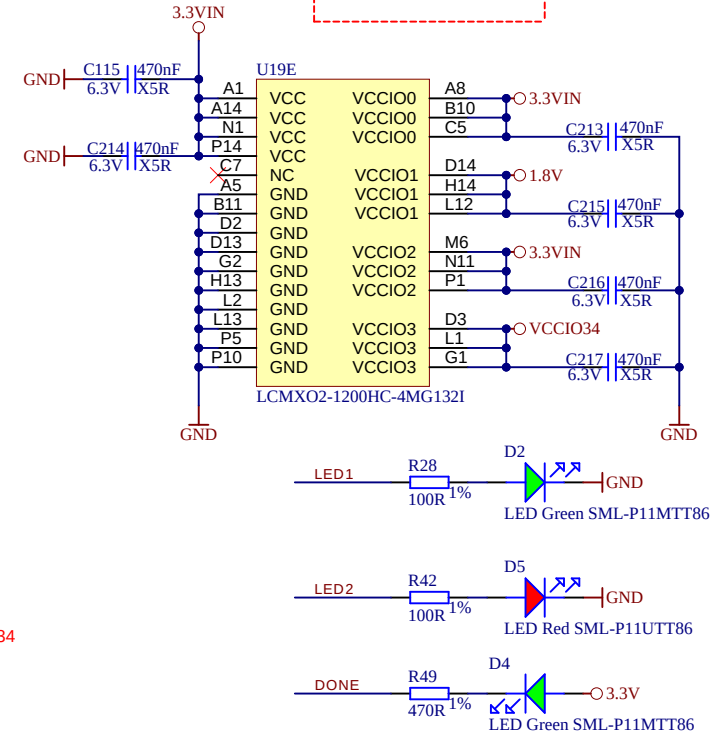


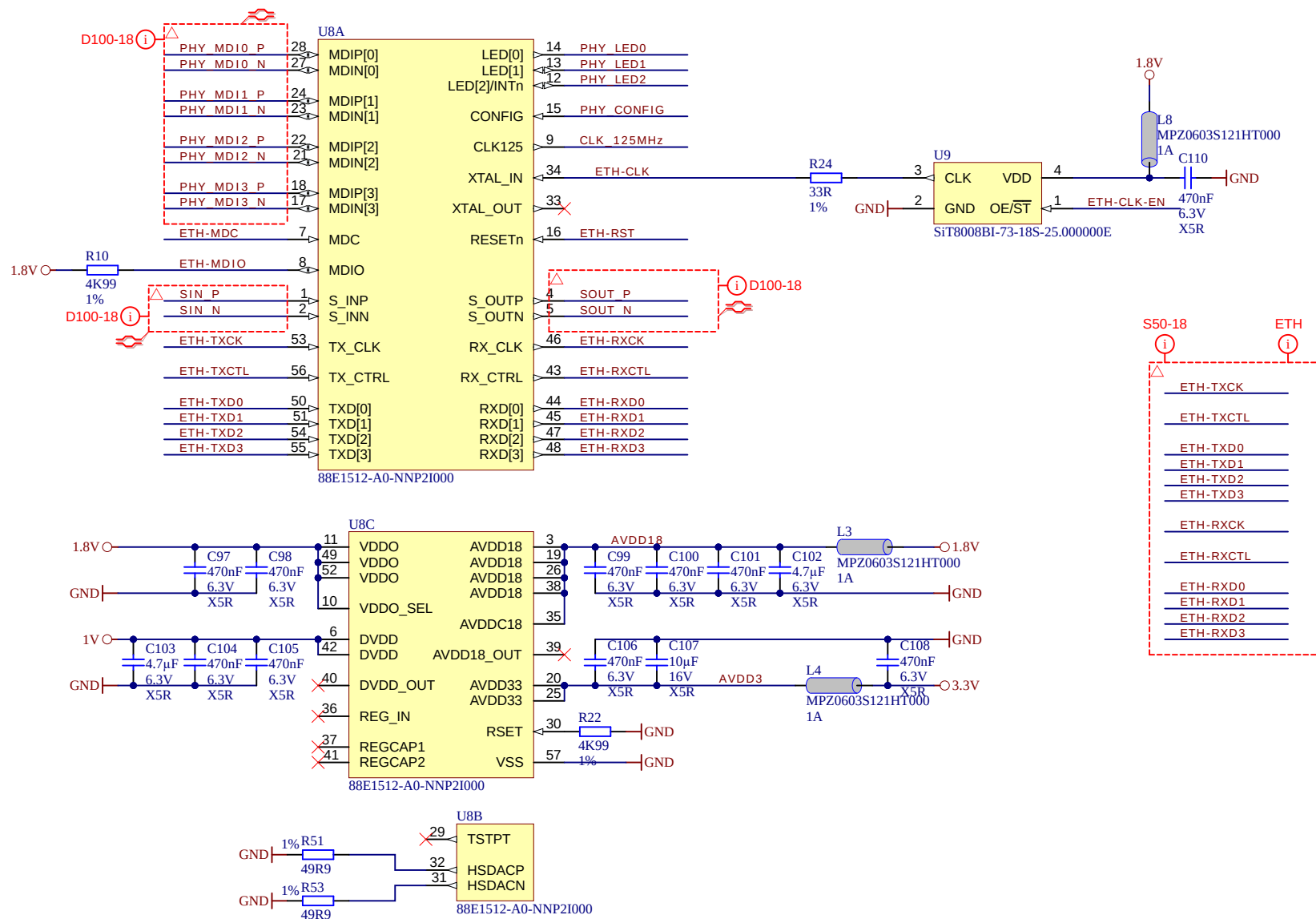
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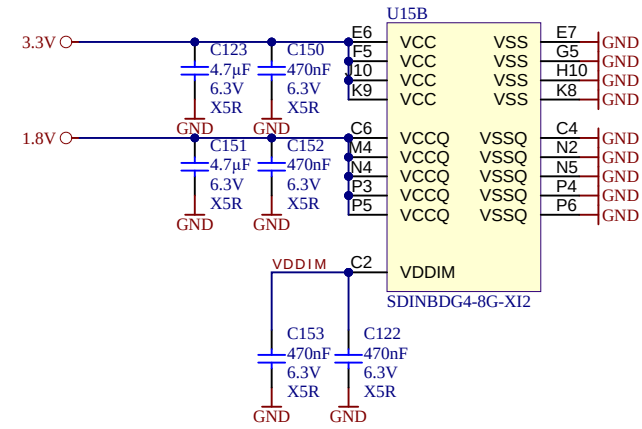
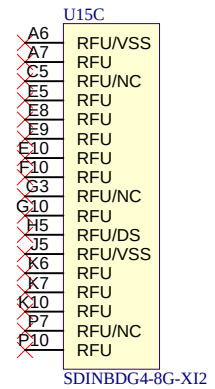
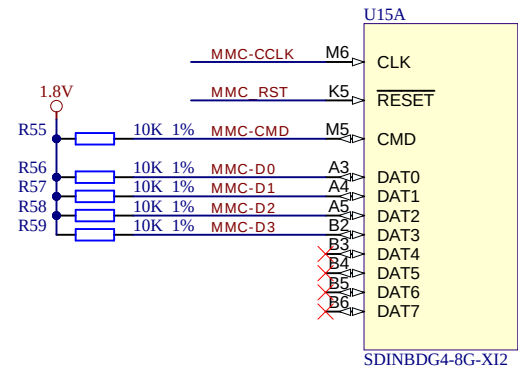
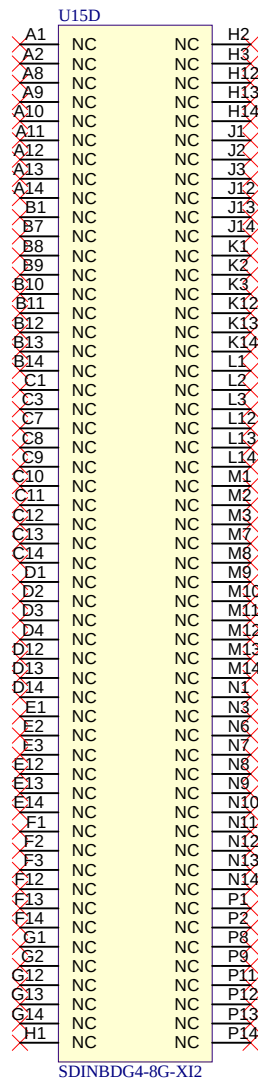
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Date: 2022-01-19	Copyright: 2013 Trenz Electronic GmbH	Page15 of 20
Filename:	SystemController.SchDoc	

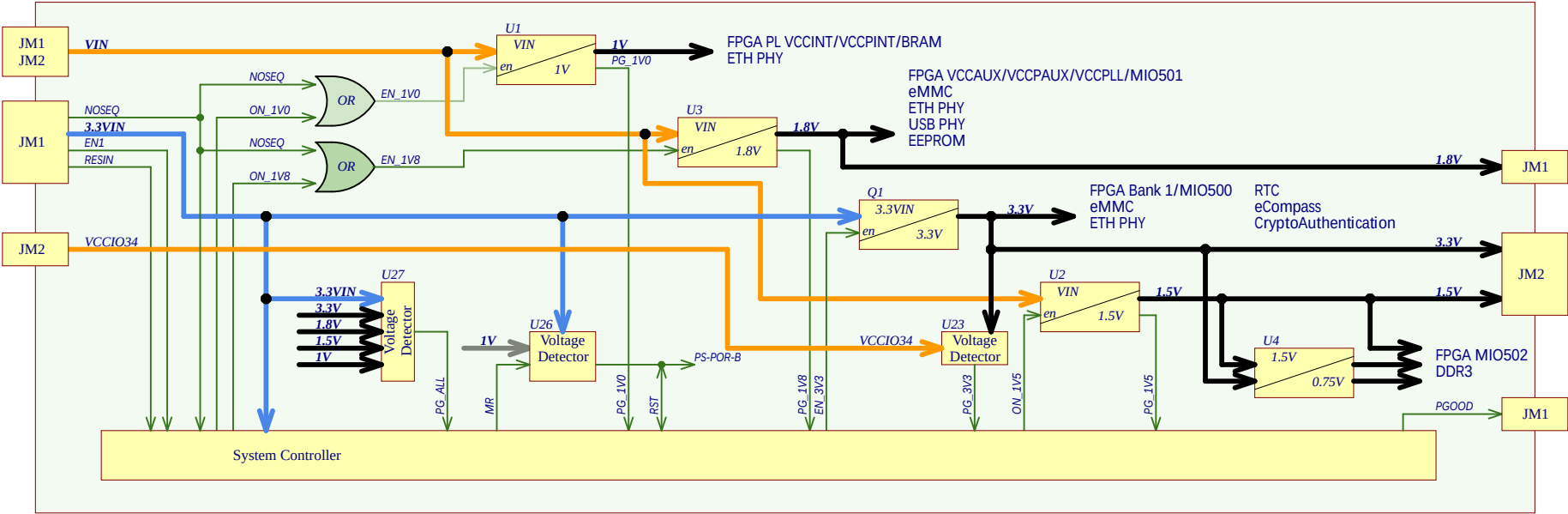




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Filename: ETH-PHY.SchDoc		

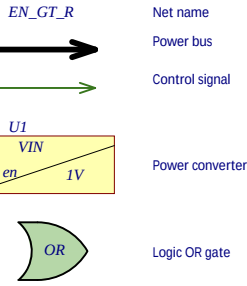


Power-on sequencing:



Recommended Operating Conditions

Power Rail	Direction	Range	Tolerance	Description	Note
VIN	IN	3.3 - 5V	+/-5%	Micromodule Power	Mandatory
3.3VIN	IN	3.3V	+/-5%	Micromodule Power	Mandatory
VCCIO13	IN	1.2 - 3.3V	+/-5%	HR IO Bank13	-
VCCIO33	IN	1.2 - 3.3V	+/-5%	HR IO Bank33	-
VCCIO34	IN	1.5 - 3.3V	+/-5%	HR IO Bank34	Mandatory
VCCIO35	IN	1.2 - 3.3V	+/-5%	HR IO Bank35	-
VBAT_IN	IN	2.5 - 5V	+/-5%	RTC	-
1.8V	OUT	1.8V	+/-5%	For Carrier card Periphery	-
3.3V	OUT	3.3V	+/-5%	For Carrier card Periphery	-
DDR_PWR	OUT	1.5V	+/-5%	For Carrier card Periphery	
VREF_JTAG	OUT	3.3V	+/-5%	For Carrier card Periphery	Connected to 3.3VIN



Title: GigaZee - Power Diagram

A4

Number: TE0720
61C33MA

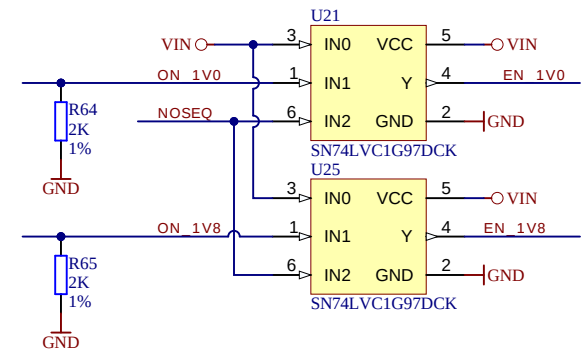
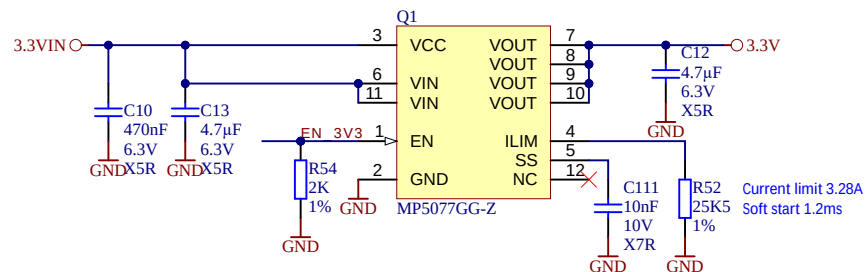
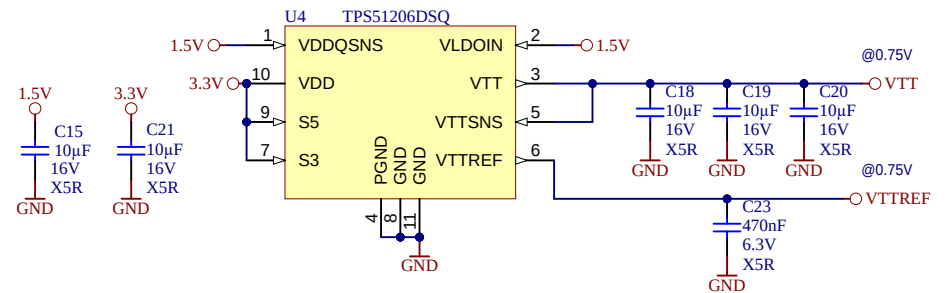
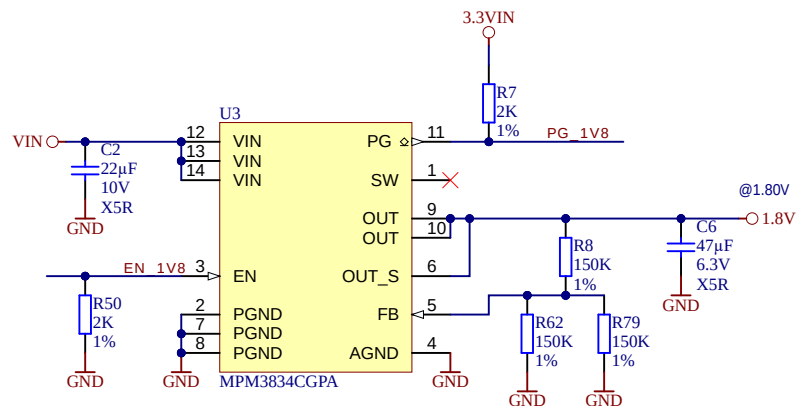
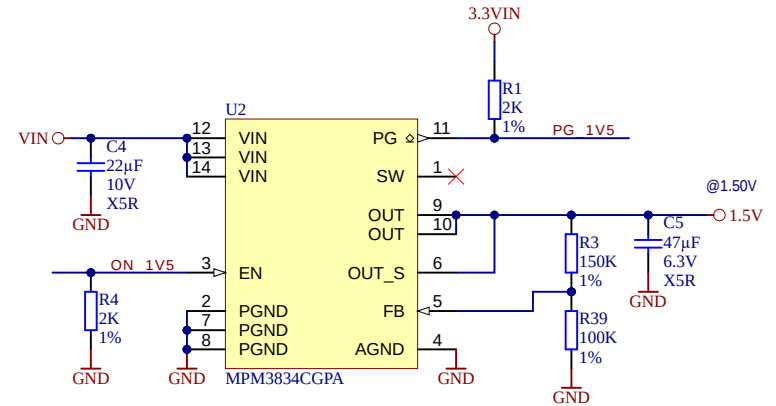
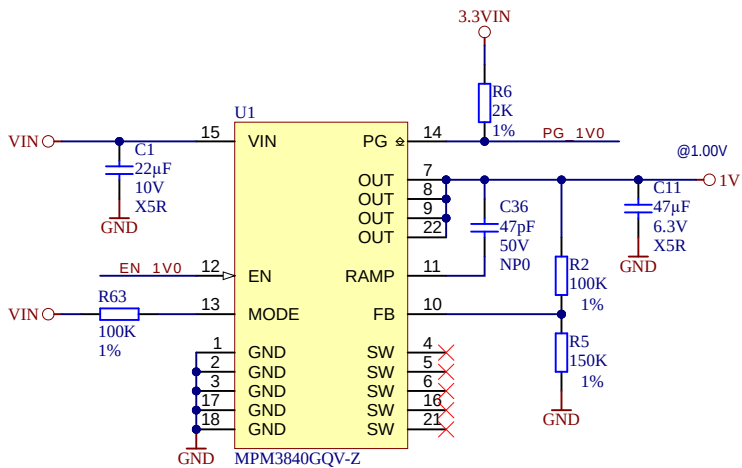
Rev. 04

Date: 23.05.2025

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Filename: Power_Diagram.SchDoc



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