BGM260P Wireless Gecko Bluetooth Module Data Sheet

The BGM260P is a secure, high-performance wireless module optimized for the requirements of battery and line-powered IoT devices running on Bluetooth networks.

Built on the powerful Series 2 EFR32BG26 SoC, the module enables Bluetooth® Low Energy connectivity, delivering exceptional RF performance and energy efficiency, industry-leading Secure Vault® technology, and a comprehensive range of features that address the evolving needs of IoT applications.

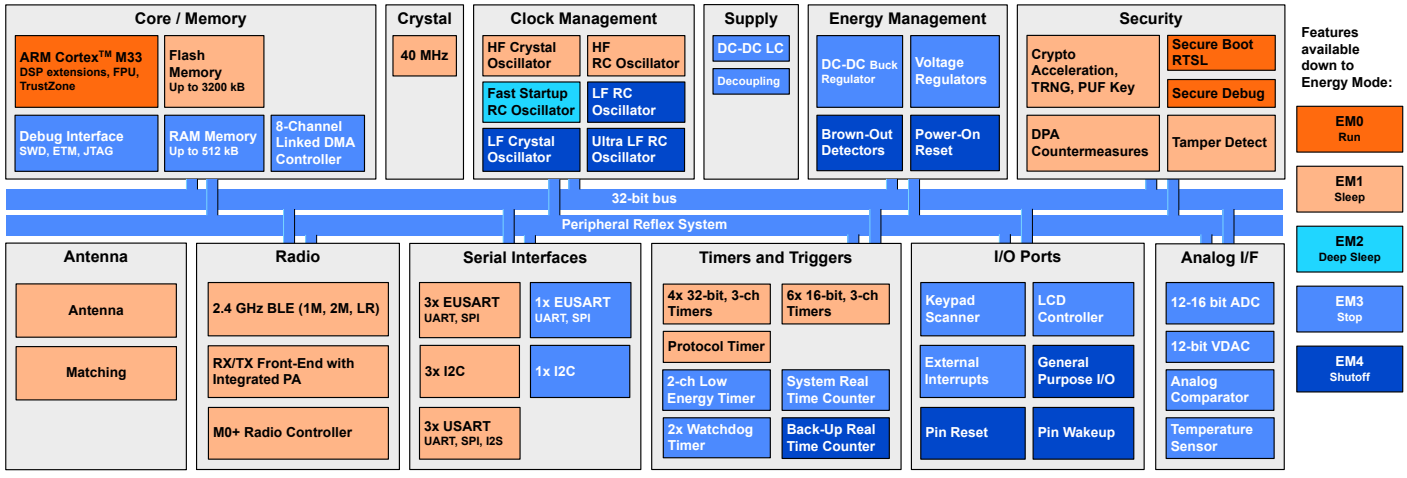
The BGM260P is a complete solution offered with robust and fully-upgradeable software stacks, global regulatory certifications, advanced development and debugging tools, and documentation that simplifies and minimizes the development cycle of your end-product, helping to accelerate its time-to-market.

The BGM260P is targeted for a broad range of applications, including:

- Smart Home Devices
- Lighting
- Gateways and Digital Assistants
- Building Automation and Security

KEY FEATURES

- Bluetooth Low Energy 5.4
- Built-in antenna
- +10 or +19.5 dBm TX output power
- -98.2 dBm Bluetooth Low Energy 1 Mbps RX sensitivity
- 32-bit ARM® Cortex®-M33 core at 80 MHz
- 3200/512 kB of Flash/RAM memory
- Secure Vault®
- Rich set of analog and digital peripherals
- 32 GPIO pins
- -40 °C to 125 °C
- 12.9 mm x 15.0 mm



 Copyright © 2025 by Silicon Laboratories

1. Features

- **Supported Protocols**
  - Bluetooth Low Energy (BLE) 5.4
- **Wireless System-on-Chip**
  - 2.4 GHz radio
  - TX power up to +19.5 dBm
  - High-performance 32-bit 80 MHz ARM Cortex®-M33 with DSP instruction and floating-point unit for efficient signal processing
  - 3200 kB flash program memory
  - 512 kB RAM data memory
- **Receiver Sensitivity**[1]
  - -106.2 dBm (0.1% BER) @ 125 kbps GFSK
  - -101.9 dBm (0.1% BER) @ 500 kbps GFSK
  - -98.2 dBm (0.1% BER) @ 1 Mbps GFSK
  - -95.5 dBm (0.1% BER) @ 2 Mbps GFSK
- **Current Consumption**
  - 5.7 mA RX current @ 1 Mbps GFSK
  - 6.8 mA TX current @ 0 dBm
  - 19.4 mA TX current @ 10 dBm
  - 153 mA TX current @ 19.5 dBm
  - 59.3 µA/MHz in Active Mode (EM0) @ 40 MHz
  - 1.4 µA EM2 DeepSleep current (16 kB RAM retention and RTC running from LFRCO)
- **Regulatory Certifications**
  - CE (EU) and UKCA (UK)
  - FCC (USA) and ISED (Canada)
  - MIC (Japan)
  - KC (South Korea)
  - NCC (Taiwan)
- **Operating Range**
  - 1.8 V to 3.8 V single power supply
  - -40 °C to +125 °C
- **Dimensions**
  - 12.9 mm x 15.0 mm
- **Security**
  - Secure Boot with Root of Trust and Secure Loader (RTSL)
  - Hardware Cryptographic Acceleration for AES128/192/256, ChaCha20-Poly1305, SHA-1, SHA-2/256/384/512, ECDSA +ECDH(P-192, P-256, P-384, P-521), Ed25519 and Curve25519, J-PAKE, PBKDF2
  - True Random Number Generator (TRNG)
  - ARM® TrustZone®
  - Secure Debug Unlock
  - Secure Key Management with PUF
  - Anti-Tamper
  - Secure Attestation
  - PSA L3 certified
- **MCU Peripherals**
  - Analog to Digital Converter (ADC)
    - 12-bit @ 1 Msps
    - 16-bit @ 76.9 ksps
  - 2 × Analog Comparator (ACMP)
  - 2 × Digital to Analog Converter (VDAC)
  - Up to 32 General Purpose I/O pins with output state retention and asynchronous interrupts
  - 8 Channel DMA Controller
  - 20 Channel Peripheral Reflex System (PRS)
  - 6 × 16-bit Timer/Counter with 3 Compare/Capture/PWM channels
  - 4× 32-bit Timer/Counter with 3 Compare/Capture/PWM channels
  - 2 x 32-bit Real Time Counter (SYSRTC/BURTC)
  - 24-bit Low Energy Timer for waveform generation (LETIMER)
  - 16-bit Pulse Counter with asynchronous operation (PCNT)
  - 2 × Watchdog Timer (WDOG)
  - 3× Universal Synchronous/Asynchronous Receiver/Transmitter (USART), supporting UART/SPI/SmartCard (ISO 7816)/IrDA/I^2S
  - 4 × Enhanced Universal Synchronous/Asynchronous Receiver/Transmitter (EUSART) supporting UART/SPI/DALI/IrDA
  - 4× I^2C interface with SMBus support
  - Low-Frequency RC Oscillator with precision mode to replace 32 kHz sleep crystal (LFRCO)
  - Die temperature sensor with +/- 1.5 °C accuracy after single-point calibration

Note:

1. Sensitivity values above are for +10 dBm parts (BGM260P22A).

2. Ordering Information

Table 2.1. Ordering Information

Ordering Code	Protocol Stack	Max TX Power	Security	Antenna	Flash (kB)	RAM (kB)	GPIO	Carrier
BGM260PB22VNA2	• Bluetooth Low Energy 5.4	+10 dBm	Vault High	Built-in	3200	512	32	Cut Tape
BGM260PB22VNA2R	• Bluetooth Low Energy 5.4	+10 dBm	Vault High	Built-in	3200	512	32	Reel
BGM260PB32VNA2	• Bluetooth Low Energy 5.4	+19.5 dBm	Vault High	Built-in	3200	512	32	Cut Tape
BGM260PB32VNA2R	• Bluetooth Low Energy 5.4	+19.5 dBm	Vault High	Built-in	3200	512	32	Reel

Note:

1. BGM260P modules operate in the 2.4 GHz ISM frequency band.
2. The maximum RF TX power allowed by different regional regulatory authorities may differ from the maximum output power a module can produce. End-product manufacturers must then verify that the module is configured to meet the regulatory limits for each region in accordance with the local rules and the formal certification test reports.
3. Throughout this document, the modules may be referred to by their product family/marketing name (e.g. BGM260P), by their model names (BGM260P32A, BGM260P22A or by their full ordering codes as seen in the table above.
4. Radio boards **xGM260P-RB4350**(+10 dBm) and **xGM260P-RB4351**(+19.5 dBm) are available for BGM260P evaluation and development.
5. Devices are pre-programmed with BGAPI UART DFU bootloader version 3.0.0, which uses the pin configuration in Section 5. Reference Diagrams.

Table of Contents

1. Features . . . 2

2. Ordering Information . . . 3

3. System Overview . . . 7

3.1 Block Diagram . . . 7

3.2 EFR32BG26 SoC . . . 9

3.3 Antenna . . . 9

3.4 Power Supply . . . 10

3.4.1 Energy Management Unit (EMU) . . . 10

3.4.2 Voltage Scaling . . . 10

3.4.3 Power Domains . . . 11

3.5 Clocking . . . 12

3.6 General Purpose Input/Output (GPIO) . . . 12

3.7 Keypad Scanner (KEYSCAN) . . . 12

3.8 Counters/Timers and PWM . . . 12

3.8.1 Timer/Counter (TIMER) . . . 12

3.8.2 Low Energy Timer (LETIMER) . . . 13

3.8.3 System Real Time Clock with Capture (SYSRTC) . . . 13

3.8.4 Back-Up Real Time Counter (BURTC) . . . 13

3.8.5 Watchdog Timer (WDOG) . . . 13

3.9 Communications and Other Digital Peripherals . . . 13

3.9.1 Universal Synchronous/Asynchronous Receiver/Transmitter (USART) . . . 13

3.9.2 Enhanced Universal Synchronous/Asynchronous Receiver/Transmitter (EUSART) . . . 13

3.9.3 Inter-Integrated Circuit Interface (I^2C) . . . 13

3.9.4 Peripheral Reflex System (PRS) . . . 13

3.10 Security . . . 14

3.10.1 Secure Boot with Root of Trust and Secure Loader (RTSL) . . . 14

3.10.2 Cryptographic Accelerator . . . 15

3.10.3 True Random Number Generator . . . 15

3.10.4 Secure Debug with Lock/Unlock . . . 15

3.10.5 DPA Countermeasures . . . 15

3.10.6 Secure Key Management with PUF . . . 15

3.10.7 Anti-Tamper . . . 16

3.10.8 Secure Attestation . . . 16

3.11 Analog . . . 16

3.11.1 Analog to Digital Converter (IADC) . . . 16

3.11.2 Analog Comparator (ACMP) . . . 16

3.11.3 Digital to Analog Converter (VDAC) . . . 16

3.11.4 Liquid Crystal Display Driver (LCD) . . . 17

3.12 Core, Memory, and Accelerators . . . 17

3.12.1 Processor Core . . . 17

3.12.2 Memory System Controller (MSC) . . . 17

3.12.3 Linked Direct Memory Access Controller (LDMA) 17
3.13 Memory Map 18
3.14 Configuration Summary 19
4. Electrical Specifications 20
4.1 Absolute Maximum Ratings 20
4.2 General Operating Conditions 21
4.3 Thermal Characteristics 22
4.4 MCU Current Consumption at 3.0 V 23
4.5 Radio Current Consumption with 3.0 V Supply 25
4.6 RF Transmitter General Characteristics for the 2.4 GHz Band 26
4.7 RF Receiver General Characteristics for the 2.4 GHz Band 27
4.8 RF Receiver Characteristics for Bluetooth Low Energy in the 2.4 GHz Band 1 Mbps Data Rate . . . 28
4.9 RF Receiver Characteristics for Bluetooth Low Energy in the 2.4 GHz Band 2 Mbps Data Rate . . . 30
4.10 RF Receiver Characteristics for Bluetooth Low Energy in the 2.4 GHz Band 500 kbps Data Rate . 32
4.11 RF Receiver Characteristics for Bluetooth Low Energy in the 2.4 GHz Band 125 kbps Data Rate . 34
4.12 High-Frequency Crystal (HFXO) 35
4.13 Low Frequency Crystal Oscillator (LFXO) 36
4.14 Precision Low Frequency RC Oscillator (LFRCO) 37
4.15 GPIO Pins 38
4.16 LCD 39
4.17 Microcontroller Peripherals 40
4.18 Antenna Radiation and Efficiency 41
5. Reference Diagrams 44
5.1 Network Co-Processor (NCP) Application with UART Host 44
5.2 SoC Application 45
6. Pin Definitions 46
6.1 Module Pinout 46
6.2 Alternate Pin Functions 48
6.3 Analog Peripheral Connectivity 49
6.4 Digital Peripheral Connectivity 50
7. Design Guidelines 56
7.1 Layout and Placement 56
7.2 Proximity to Other Materials 57
7.3 Proximity to Human Body 57
7.4 Reset 57
7.5 Debug 57
7.6 Packet Trace Interface (PTI) 57

8. Package Specifications 58
8.1 Package Outline 58
8.2 PCB Land Pattern 59
8.3 Package Marking 60
9. Soldering Recommendations 61
10. Tape and Reel 62
11. Certifications 63
11.1 CE and UKCA - EU and UK 63
11.2 FCC - USA 63
11.3 ISED - Canada 66
11.4 MIC - Japan 68
11.5 KC - South Korea 69
11.6 NCC - Taiwan 70
11.7 RF Exposure and Proximity to Human Body 72
11.8 Bluetooth Qualification 72
12. Revision History 73

3. System Overview

3.1 Block Diagram

The BGM260P module is a highly integrated, high-performance system with all the essential hardware components needed to enable 2.4 GHz wireless connectivity and support robust networking capabilities via multiple wireless protocols.

Built around the EFR32BG26 Wireless SoC, the BGM260P includes a built-in antenna, an RF matching network (optimized for transmit power efficiency), supply decoupling and filtering components, an LC tank for DC-DC conversion, a 40 MHz reference crystal, and an RF shield. An integrated 32.768 kHz RC oscillator (LFRCO) for low power operation without an external crystal. Precision mode enables periodic recalibration against the HFXO crystal to improve accuracy to +/- 500 ppm, making it suitable for BLE sleep interval timing. External 32 kHz crystal (LFXO) is supported via GPIO pins for scenarios demanding maximum energy efficiency and accuracy.

The RF matching network is optimized for transmit power efficiency, therefore modules rated for +19.5 dBm will show non-optimal current consumption and performance when operated at a lower output power (e.g. +10 or 0 dBm).

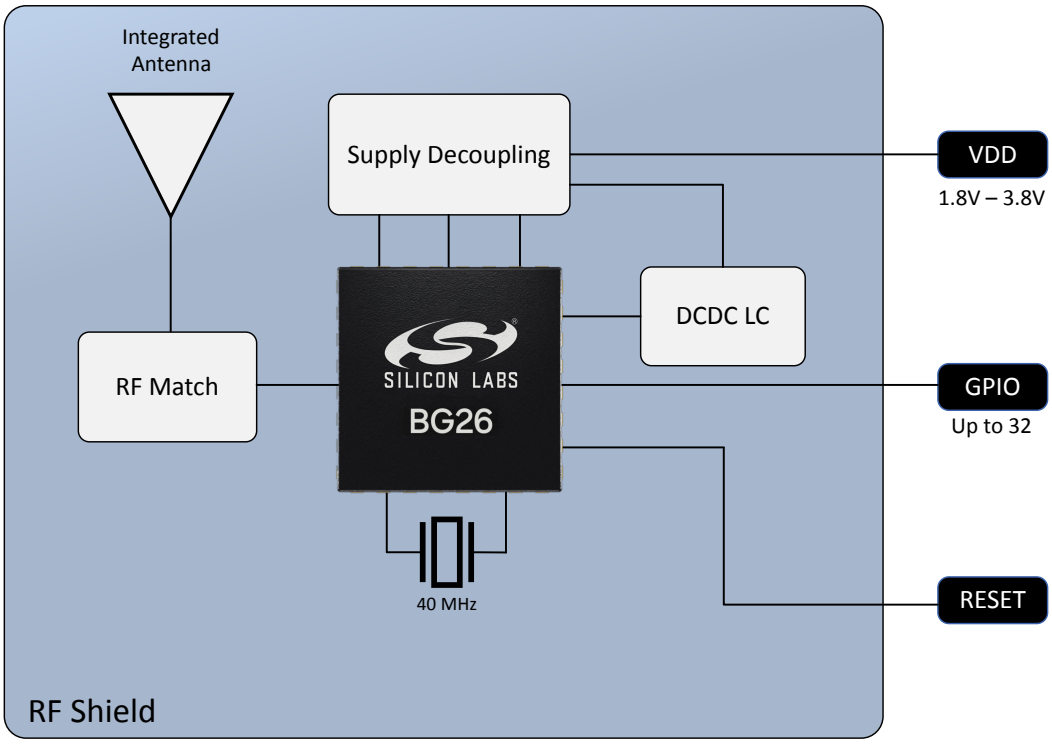


Figure 3.1. BGM260P Block Diagram

A simplified internal schematic for the BGM260P module is shown in Figure 3.2 BGM260P Module Schematic on page 8. On +19.5 dBm devices PAVDD is directly connected to VDD.

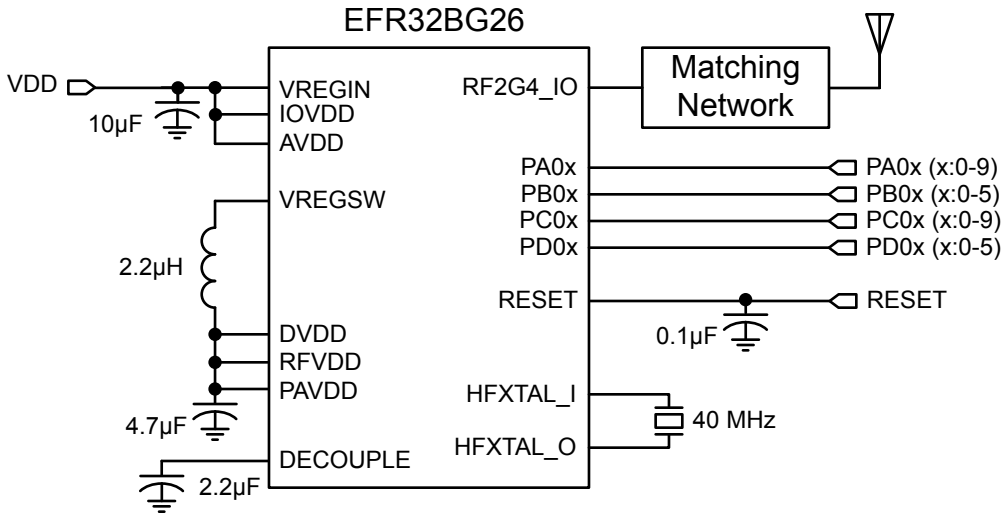


Figure 3.2. BGM260P Module Schematic

3.2 EFR32BG26 SoC

The EFR32BG26 SoC features a 32-bit ARM Cortex M33 core, a 2.4 GHz high-performance radio, 3200 kB of Flash memory, 512 kB of RAM, a dedicated core for security, a rich set of MCU peripherals, and various clock management and serial interfacing options. See the EFR32xG26 Reference Manual and EFR32BG26 Data Sheet for details.

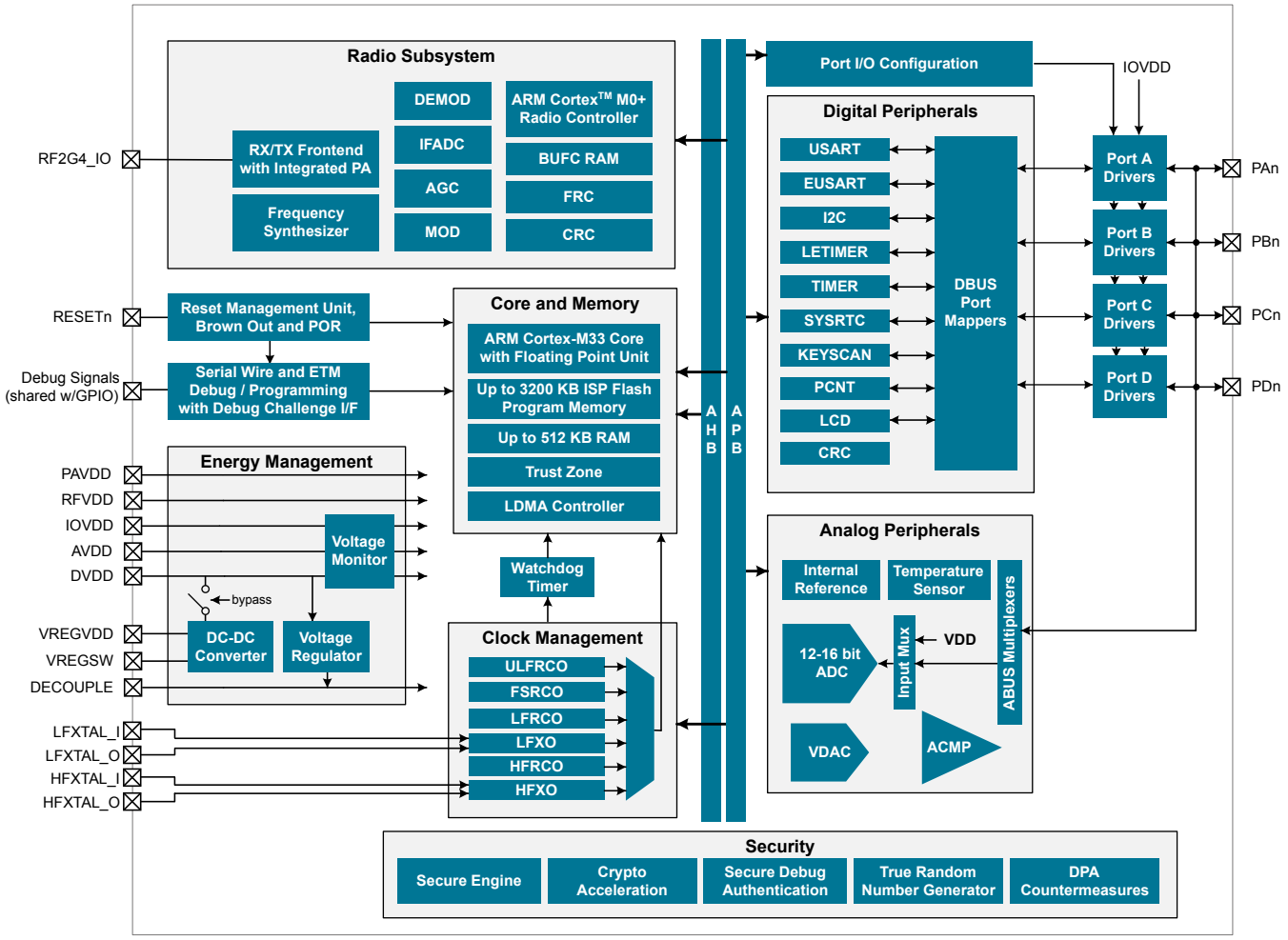


Figure 3.3. Detailed EFR32BG26 Block Diagram

3.3 Antenna

BGM260P modules include a build-in antenna. Typical performance characteristics for the built-in antenna are detailed in the table below. See 4.18 Antenna Radiation and Efficiency for more details.

Table 3.1. Integral Antenna Efficiency and Peak Gain

Parameter	With optimal layout	Note
Efficiency	-1 dB	Antenna efficiency, gain and radiation pattern are highly dependent on the application PCB layout and mechanical design. Refer to for recommendations to achieve optimal antenna performance.
Peak gain	2.87 dBi	

3.4 Power Supply

The BGM260P requires a single nominal supply level (VDD) to operate and supports an operating range of 1.8 to 3.8 V. The nominal level needed for +10 dBm devices (Model: BGM260P22A) is 3.0 V whereas +19.5 dBm devices (Model: BGM260P32A) require 3.3 V in order to achieve higher TX output power. All necessary decoupling, filtering and DC-DC related components are included in the module.

Note: The power amplifier for +10 dBm modules is supplied through an internal LDO, and thus is independent of the VDD supply. Respectively, the power amplifier for +19.5 dBm modules is supplied through the VDD pin with a target level of 3.3 V.

3.4.1 Energy Management Unit (EMU)

The EMU manages transitions of energy modes in the device. Each energy mode defines which peripherals and features are available and the amount of current the device consumes. The EMU can also be used to implement system-wide voltage scaling and turn off the power to unused RAM blocks to optimize the energy consumption in the target application. The DC-DC regulator operation is tightly integrated with the EMU.

3.4.2 Voltage Scaling

The BGM260P supports supply voltage scaling for the LDO powering DECOUPLE, with independent selections for EM0 / EM1 and EM2 / EM3. Voltage scaling helps to optimize the energy efficiency of the system by operating at lower voltages when possible. The EM0 / EM1 voltage scaling level defaults to VSCALE2, which allows the core to operate in active mode at full speed. The intermediate level, VSCALE1, allows operation in EM0 and EM1 at up to 40 MHz. The lowest level, VSCALE0, can be used to conserve power further in EM2 and EM3. The EMU will automatically switch the target voltage scaling level when transitioning between energy modes.

3.4.3 Power Domains

Peripherals may exist on one of several independent power domains which are powered down to minimize supply current when not in use. Power domains are managed automatically by the EMU.

The lowest-energy power domain is the "high-voltage" power domain (PDHV), which supports extremely low-energy infrastructure and peripherals. Circuits powered from PDHV are always on and available in all energy modes down to EM4.

The next power domain is the low power domain (PD0), which is further divided to power subsets of peripherals. All PD0 power domains are shut down in EM4. Circuits powered from PD0 power domains may be available in EM0, EM1, EM2, and EM3.

Low power domain A (PD0A) is the base power domain for EM2 and EM3 and will always remain on in EM0-EM3. It powers the most commonly-used EM2 and EM3-capable peripherals and infrastructure required to operate in EM2 and EM3. Auxiliary PD0 power domains (PD0B, PD0C, PD0D, PD0E) power additional EM2 and EM3-capable peripherals on demand. If any peripherals on one of the auxiliary power domains is enabled, that power domain will be active in EM2 and EM3. Otherwise, the auxiliary PD0 power domains will be shut down to reduce current.

Note: Power domain PD0E is also turned on when peripherals on PD0B, PD0C, or PD0D are used.

The active power domain (PD1) powers the rest of the device circuitry, including the CPU core and EM0 / EM1 peripherals. PD1 is always powered on in EM0 and EM1. PD1 is always shut down in EM2, EM3, and EM4.

Table 3.2 Peripheral Power Subdomains on page 11 shows the peripherals on the PDHV and PD0x domains. Any peripheral not listed is on PD1.

Table 3.2. Peripheral Power Subdomains

Always On in EM2/EM3		Selectively On in EM2/3			
PDHV[1]	PD0A	PD0B[2]	PD0C[2]	PD0D[2]	PD0E
LFRCO (Non-precision Mode)	SYSRTC	LETIMER0	LFRCO (Precision Calibration Mode)	DEBUG	GPIO
LFXO	FSRCO	IADC0	HFRCOEM23	WDOG0/1	KEYSCAN
BURTC		PCNT0	HFXO	EUSART0	PRS
BURAM		ACMP0/1		I2C0	
ULFRCO		VDAC0/1			

Note:

1. Peripherals on PDHV are also available in EM4.
2. If any of PD0B, PD0C, or PD0D are enabled, PD0E will also be automatically enabled.

3.5 Clocking

The Clock Management Unit (CMU) controls oscillators and clocks in the BGM260P. Individual enabling and disabling of clocks to all peripheral modules is performed by the CMU. The CMU also controls enabling and configuration of the oscillators. A high degree of flexibility allows software to optimize energy consumption in any specific application by minimizing power dissipation in unused peripherals and oscillators.

The BGM260P integrates one crystal oscillator, supports two crystal oscillators (one internal, one external) and fully integrates four RC oscillators, listed below.

- Integrated high frequency crystal oscillator (HFXO) running at 40.0 MHz provides a precise timing reference for the MCU and the radio.
- Optional external 32.768 kHz crystal oscillator (LFXO) provides an accurate timing reference for low energy modes. An external LFXO enhances energy efficiency during BLE sleep intervals by reducing the listening window and eliminating the need for periodic recalibration against the HFXO in EM2.
- An integrated high frequency RC oscillator (HFRCO) is available for the MCU system, when crystal accuracy is not required. The HFRCO employs fast start-up at minimal energy consumption combined with a wide frequency range, from 1 MHz to 80 MHz.
- An integrated fast start-up RC oscillator (FSRCO) that runs at a fixed 20 MHz.
- An integrated low frequency 32.768 kHz RC oscillator (LFRCO). Precision mode enables periodic recalibration against the 40.0 MHz HFXO crystal to improve accuracy to +/- 500 ppm, suitable for BLE sleep interval timing.
- An integrated ultra-low frequency 1 kHz RC oscillator (ULFRCO) is available to provide a timing reference at the lowest energy consumption in low energy modes.

3.6 General Purpose Input/Output (GPIO)

The BGM260P has up to 32 General Purpose Input/Output pins. Each GPIO pin can be individually configured as either an output or input. More advanced configurations including open-drain, open-source, and glitch-filtering can be configured for each individual GPIO pin. The GPIO pins can be overridden by peripheral connections, like SPI communication. Each peripheral connection can be routed to several GPIO pins on the device. The input value of a GPIO pin can be routed through the Peripheral Reflex System to other peripherals. The GPIO subsystem supports asynchronous external pin interrupts.

All of the pins on ports A and port B are EM2 capable. These pins may be used by Low-Energy peripherals in EM2/3 and may also be used as EM2/3 pin wake-ups. Pins on ports C and D are latched/retained in their current state when entering EM2 until EM2 exit upon which internal peripherals could once again drive those pads.

A few GPIOs also have wake functionality down to EM4. These pins are listed in the Table 6.2 GPIO Alternate Functions Table on page 48 with the function GPIO.EM4WU.

3.7 Keypad Scanner (KEYSCAN)

A low-energy keypad scanner (KEYSCAN) is included, which can scan up to a 6 x 8 matrix of keyboard switches. The KEYSCAN peripheral contains logic for debounce and settling time, allowing it to scan through the switch matrix autonomously in EM0 and EM1, and interrupt the processor when a key press is detected. A wake-on-keypress feature is also supported, allowing for the detection of any key press down to EM3.

3.8 Counters/Timers and PWM

3.8.1 Timer/Counter (TIMER)

TIMER peripherals keep track of timing, count events, generate PWM outputs, and trigger timed actions in other peripherals through the Peripheral Reflex System (PRS). The core of each TIMER is a 16-bit or 32-bit counter with up to 3 compare/capture channels. Each channel is configurable in one of three modes. In capture mode, the counter state is stored in a buffer at a selected input event. In compare mode, the channel output reflects the comparison of the counter to a programmed threshold value. In PWM mode, the TIMER supports generation of pulse-width modulation (PWM) outputs of arbitrary waveforms defined by the sequence of values written to the compare registers. In addition, some timers offer dead-time insertion.

See 3.14 Configuration Summary for information on the feature set of each timer.

3.8.2 Low Energy Timer (LETIMER)

The unique LETIMER is a 24-bit timer that is available in energy mode EM0 Active, EM1 Sleep, EM2 Deep Sleep, and EM3 Stop. This allows it to be used for timing and output generation when most of the device is powered down, allowing simple tasks to be performed while the power consumption of the system is kept at an absolute minimum. The LETIMER can be used to output a variety of waveforms with minimal software intervention. The LETIMER is connected to the Peripheral Reflex System (PRS), and can be configured to start counting on compare matches from other peripherals such as the Real Time Clock.

3.8.3 System Real Time Clock with Capture (SYSRTC)

The System Real Time Clock (SYSRTC) is a 32-bit counter providing timekeeping down to EM3. The SYSRTC can be clocked by any of the on-board low-frequency oscillators, and it is capable of providing system wake-up at user defined intervals.

3.8.4 Back-Up Real Time Counter (BURTC)

The Back-Up Real Time Counter (BURTC) is a 32-bit counter providing timekeeping in all energy modes, including EM4. The BURTC can be clocked by any of the on-board low-frequency oscillators, and it is capable of providing system wake-up at user-defined intervals.

3.8.5 Watchdog Timer (WDOG)

The watchdog timer can act both as an independent watchdog or as a watchdog synchronous with the CPU clock. It has windowed monitoring capabilities, and can generate a reset or different interrupts depending on the failure mode of the system. The watchdog can also monitor autonomous systems driven by the Peripheral Reflex System (PRS).

3.9 Communications and Other Digital Peripherals

3.9.1 Universal Synchronous/Asynchronous Receiver/Transmitter (USART)

The Universal Synchronous/Asynchronous Receiver/Transmitter is a flexible serial I/O module. It supports full duplex asynchronous UART communication with hardware flow control as well as RS-485, SPI, MicroWire, and 3-wire. It can also interface with devices supporting:

- ISO7816 SmartCards
- IrDA
- I^2S

3.9.2 Enhanced Universal Synchronous/Asynchronous Receiver/Transmitter (EUSART)

The Enhanced Universal Synchronous/Asynchronous Receiver/Transmitter supports full duplex asynchronous UART communication with hardware flow control, RS-485, and IrDA support. The EUSART also supports high-speed SPI. In EM0 and EM1, the EUSART provides a high-speed, buffered communication interface.

When routed to GPIO ports A or B, the EUSART0 may also be used in a low-energy mode and operate in EM2. A 32.768 kHz clock source allows full duplex UART communication up to 9600 baud. EUSART0 can also act as a SPI secondary device in EM2 and EM3, and wake the system when data is received from an external bus controller.

3.9.3 Inter-Integrated Circuit Interface (I^2C)

The I^2C module provides an interface between the MCU and a serial I^2C bus. It is capable of acting as a main or secondary interface and supports multi-drop buses. Standard-mode, fast-mode, and fast-mode plus speeds are supported, allowing transmission rates from 10 kbit/s up to 1 Mbit/s. Bus arbitration and timeouts are also available, allowing implementation of an SMBus-compliant system. The interface provided to software by the I^2C module allows precise timing control of the transmission process and highly automated transfers. Automatic recognition of addresses is provided in active and low energy modes. Not all instances of I^2C are available in all energy modes.

3.9.4 Peripheral Reflex System (PRS)

The Peripheral Reflex System provides a communication network between different peripheral modules without software involvement. Peripheral modules producing Reflex signals are called producers. The PRS routes Reflex signals from producers to consumer peripherals which in turn perform actions in response. Edge triggers and other functionality, such as simple logic operations (AND, OR, NOT), can be applied by the PRS to the signals. The PRS allows peripherals to act autonomously without waking the MCU core, saving power.

3.10 Security

BGM260P modules support Secure Vault High.

Secure Vault is a PSA Level 3 certified collection of technologies that deliver state-of-the-art security and upgradability features to protect and future-proof IoT devices against costly threats, attacks, and tampering. A dedicated security CPU enables the Secure Vault functions and isolates cryptographic functions and data from the Cortex-M33 core.

Table 3.3. Secure Vault Features

Feature	Secure Vault High
True Random Number Generator (TRNG)	Yes
Secure Boot with Root of Trust and Secure Loader (RTSL)	Yes
Secure Debug with Lock/Unlock	Yes
DPA Countermeasures	Yes
Anti-Tamper	Yes
Secure Attestation	Yes
Secure Key Management	Yes
Symmetric Encryption	• AES 128 / 192 / 256 bit • ECB, CTR, CBC, CFB, CCM, GCM, CBC-MAC, and GMAC • ChaCha20
Public Key Encryption - ECDSA / ECDH / EdDSA	• p192, p256, p384 and p521 • Curve25519 (ECDH) • Ed25519 (EdDSA)
Key Derivation	• ECJ-PAKE p192, p256, p384, and p521 • PBKDF2 • HKDF
Hashes	• SHA-1 • SHA-2 256, 384, and 512 • Poly1305

3.10.1 Secure Boot with Root of Trust and Secure Loader (RTSL)

The Secure Boot with RTSL authenticates a chain of trusted firmware that begins from an immutable memory (ROM).

It prevents malware injection, prevents rollback, ensures that only authentic firmware is executed, and protects Over The Air updates.

For more information about this feature, see AN1218: Series 2 Secure Boot with RTSL.

3.10.2 Cryptographic Accelerator

The Cryptographic Accelerator is an autonomous hardware accelerator with Differential Power Analysis (DPA) countermeasures to protect keys.

It supports AES encryption and decryption with 128/192/256-bit keys, ChaCha20 encryption, and Elliptic Curve Cryptography (ECC) to support public key operations and hashes.

Supported block cipher modes of operation for AES include:

- Electronic Code Book (ECB)
- Counter Mode (CTR)
- Cipher Block Chaining (CBC)
- Cipher Feedback (CFB)
- Galois Counter Mode (GCM)
- Counter with CBC-MAC (CCM)
- Cipher Block Chaining Message Authentication Code (CBC-MAC)
- Galois Message Authentication Code (GMAC)

The Cryptographic Accelerator accelerates Elliptical Curve Cryptography and supports the National Institute of Standards and Technology (NIST) recommended curves including P-192, P-256, P-384, and P-521 for Elliptic Curve Diffie-Hellman (ECDH) key derivation, and Elliptic Curve Digital Signature Algorithm (ECDSA) sign and verify operations. Also supported is the non-NIST Curve25519 for ECDH and Ed25519 for Edwards-curve Digital Signature Algorithm (EdDSA) sign and verify operations.

Secure Vault also supports Elliptic Curve variant of Password Authenticated Key Exchange by Juggling (ECJ-PAKE) and Password-Based Key Derivation Function 2 (PBKDF2).

Supported hashes include SHA-1, SHA-2/256/384/512 and Poly1305.

This implementation provides a fast and energy efficient solution to state of the art cryptographic needs.

3.10.3 True Random Number Generator

The TRNG module is a non-deterministic random number generator that harvests entropy from a thermal energy source. It includes start-up health tests for the entropy source as required by NIST SP800-90B and AIS-31, as well as online health tests required for NIST SP800-90C.

The TRNG is suitable for periodically generating entropy to seed an approved pseudo random number generator.

3.10.4 Secure Debug with Lock/Unlock

For obvious security reasons, it is critical for a product to have its debug interface locked before being released in the field.

Secure Vault also provides a secure debug unlock function that allows authenticated access based on public key cryptography. This functionality is particularly useful for supporting failure analysis while maintaining confidentiality of IP and sensitive end-user data.

For more information about this feature, see AN1190: Series 2 Secure Debug.

3.10.5 DPA Countermeasures

The AES and ECC accelerators have Differential Power Analysis (DPA) countermeasures support. This makes it very expensive from a time and effort standpoint to use DPA to recover secret keys.

3.10.6 Secure Key Management with PUF

Key material in Secure Vault High products is protected by "key wrapping" with a standardized symmetric encryption mechanism. This method has the advantage of protecting a virtually unlimited number of keys, limited only by the storage that is accessible by the Cortex-M33, which includes off-chip storage as well. The symmetric key used for this wrapping and unwrapping must be highly secure because it can expose all other key materials in the system. The Secure Vault Key Management system uses a Physically Unclonable Function (PUF) to generate a persistent device-unique seed key on power up to dynamically generate this critical wrapping/unwrapping key which is only visible to the AES encryption engine and is not retained when the device loses power.

3.10.7 Anti-Tamper

Secure Vault High devices provide internal tamper protection which monitors parameters such as voltage, temperature, and electromagnetic pulses as well as detecting tamper of the security sub-system itself. Additionally, 8 external configurable tamper pins support external tamper sources, such as enclosure tamper switches.

For each tamper event, the user is able to select the severity of the tamper response ranging from an interrupt, to a reset, to destroying the PUF reconstruction data which will make all protected key materials un-recoverable and effectively render the device inoperable. The tamper system also has an internal resettable event counter with programmable trigger threshold and refresh periods to mitigate false positive tamper events.

For more information about this feature, see AN1247: Anti-Tamper Protection Configuration and Use.

3.10.8 Secure Attestation

Secure Vault High products support Secure Attestation, which begins with a secure identity that is created during the Silicon Labs manufacturing process. During device production, each device generates its own public/private keypair and securely stores the wrapped private key into immutable OTP memory and this key never leaves the device. The corresponding public key is extracted from the device and inserted into a binary DER-encoded X.509 device certificate, which is signed into a Silicon Labs CA chain and then programmed back into the chip into an immutable OTP memory.

The secure identity can be used to authenticate the chip at any time in the life of the product. The production certification chain can be requested remotely from the product. This certification chain can be used to verify that the device was authentically produced by Silicon Labs. The device unique public key is also bound to the device certificate in the certification chain. A challenge can be sent to the chip at any point in time to be signed by the device private key. The public key in the device certificate can then be used to verify the challenge response, proving that the device has access to the securely-stored private key, which prevents counterfeit products or impersonation attacks.

For more information about this feature, see AN1268: Authenticating Silicon Labs Devices Using Device Certificates.

3.11 Analog

3.11.1 Analog to Digital Converter (IADC)

The IADC is a hybrid architecture combining techniques from both SAR and Delta-Sigma style converters. Flexible controls allow fine-tuned performance and speed to meet the needs of a wide variety of applications. Hardware oversampling reduces system-level noise over multiple front-end samples. The IADC includes integrated voltage reference options. Inputs are selectable from a wide range of sources, including pins configurable as either single-ended or differential.

The IADC supports one operational mode:

- Normal Mode: Flexible speed and performance, 12-16 bits output resolution
  - 11.7 bits ENOB performance at 1 Msps (OSR = 2)
  - 14.3 bits ENOB performance at 76.9 ksps (OSR = 32)

3.11.2 Analog Comparator (ACMP)

The ACMP is used to compare the voltage of two analog inputs, with a digital output indicating which input voltage is higher. Inputs are selected from among internal references and external pins. The tradeoff between response time and current consumption is configurable by software. Two 6-bit reference dividers allow for a wide range of internally-programmable reference sources. The ACMP can also be used to monitor the supply voltage. An interrupt can be generated when the supply falls below or rises above the programmable threshold.

3.11.3 Digital to Analog Converter (VDAC)

The VDAC can convert a digital value to an analog output voltage. The VDAC is a fully differential, 500 ksps, 12-bit converter. The VDAC may be used for a number of different applications such as sensor interfaces or sound output. The VDAC can generate high-resolution analog signals while the MCU is operating at low frequencies and with low total power consumption. Using DMA and a timer, the VDAC can be used to generate waveforms without any CPU intervention. The VDAC is available in all energy modes down to and including EM3.

3.11.4 Liquid Crystal Display Driver (LCD)

The LCD driver is capable of driving a segmented LCD with up to 4x23 segments. A voltage boost function enables it to provide the LCD with higher voltage than the supply voltage for the device. A patented charge redistribution driver can reduce the LCD peripheral supply current by up to 40%. In addition, an animation feature can run custom animations on the LCD without any CPU intervention. The LCD driver can also remain active even in Energy Mode 2 and provides a Frame Counter interrupt that can wake-up the device on a regular basis for updating data.

3.12 Core, Memory, and Accelerators

3.12.1 Processor Core

The ARM Cortex-M processor includes a 32-bit RISC processor integrating the following features and tasks in the system:

- ARM Cortex-M33 RISC processor achieving 1.50 Dhrystone MIPS/MHz
- ARM TrustZone security technology
- Embedded Trace Macrocell (ETM) for real-time trace and debug
- Up to 3200 kB flash program memory
- Up to 512 kB RAM data memory
- Configuration and event handling of all modules
- 2-pin Serial-Wire debug interface

3.12.2 Memory System Controller (MSC)

The MSC is the program memory unit of the microcontroller. The flash memory is readable and writable from both the Cortex-M33 and LDMA. In addition to the main flash array where program code is normally written, the MSC also provides an information block where additional information, such as special user information or flash-lock bits, is stored. There is also a read-only page in the information block containing system and device calibration data. Read and write operations are supported in energy modes EM0 Active and EM1 Sleep.

3.12.3 Linked Direct Memory Access Controller (LDMA)

The LDMA controller allows the system to perform memory operations independently of software. This reduces both energy consumption and software workload. The LDMA allows operations to be linked together and staged, enabling sophisticated operations to be implemented.

3.13 Memory Map

The BGM260P memory map is shown in the figures below. RAM and flash sizes are for the largest memory configuration.

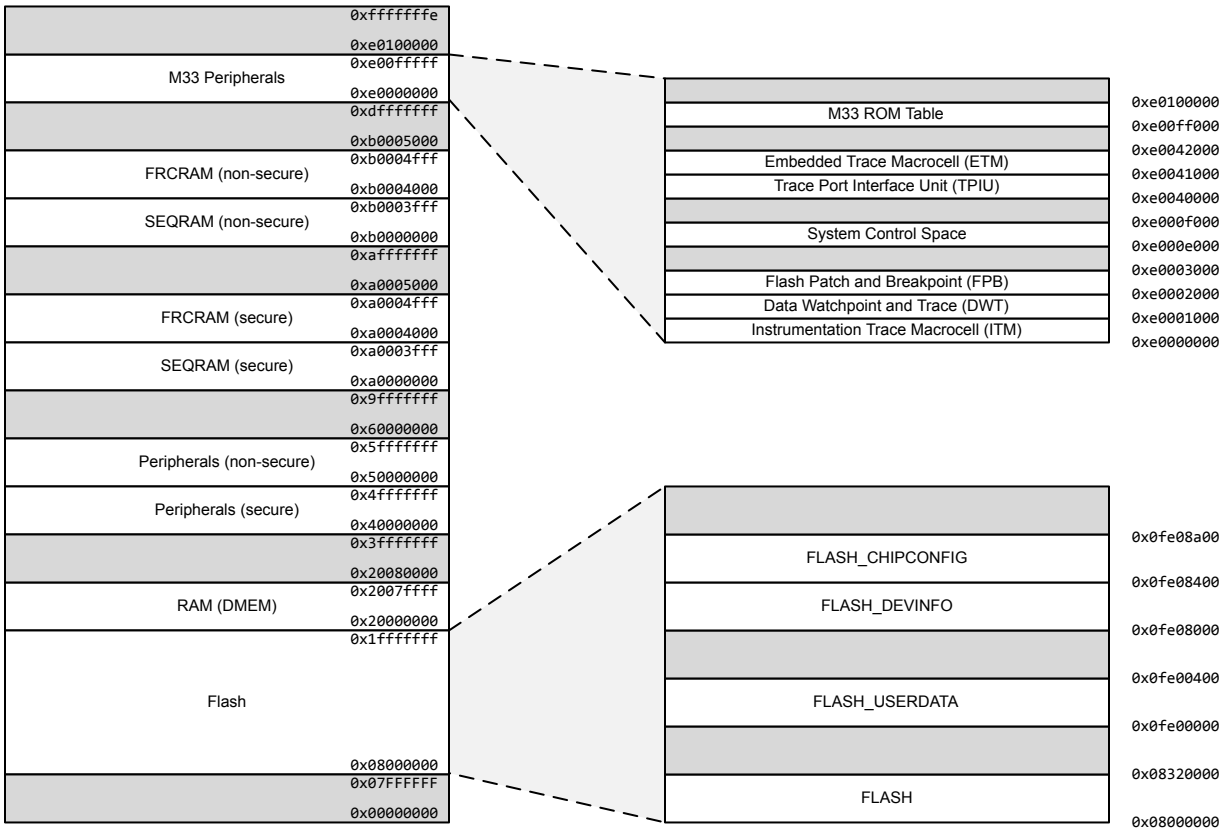


Figure 3.4. BGM260P Memory Map — Core Peripherals and Code Space

3.14 Configuration Summary

The features of the BGM260P are a subset of the feature set described in the device reference manual. The table below describes device specific implementation of the features. Remaining modules support full configuration. Refer to the Energy Modes table in the BGM260P Reference Manual EMU Chapter for a more comprehensive list of energy mode support for all device peripherals.

Table 3.4. Configuration Summary

Module	Lowest Energy Mode	Configuration
I2C0	EM1 - Full functionality EM2/3[1] - Functionality limited to receive address recognition	
I2C1	EM1 - Full functionality	
I2C2	EM1 - Full functionality	
I2C3	EM1 - Full functionality	
LETIMER0	EM2/3[1]	24-bit, 2-channels
TIMER0	EM1	32-bit, 3-channels, +DTI
TIMER1	EM1	32-bit, 3-channels, +DTI
TIMER2	EM1	16-bit, 3-channels, +DTI
TIMER3	EM1	16-bit, 3-channels, +DTI
TIMER4	EM1	16-bit, 3-channels, +DTI
TIMER5	EM1	16-bit, 3-channels, +DTI
TIMER6	EM1	16-bit, 3-channels, +DTI
TIMER7	EM1	16-bit, 3-channels, +DTI
TIMER8	EM1	32-bit, 3-channels, +DTI
TIMER9	EM1	32-bit, 3-channels, +DTI
EUSART0	EM1 - Full high-speed operation, all modes EM2[1] - Low-energy UART operation, 9600 Baud EM2/3[1] - Low-energy SPI secondary receiver	UART, SPI, IrDA, DALI
EUSART1	EM1	UART, SPI, IrDA, DALI
EUSART2	EM1	UART, SPI, IrDA, DALI
EUSART3	EM1	UART, SPI, IrDA, DALI
USART0	EM1	UART, SPI, IrDA, I2S, SmartCard
USART1	EM1	UART, SPI, IrDA, I2S, SmartCard
USART2	EM1	UART, SPI, IrDA, I2S, SmartCard

Note:

1. EM2 and EM3 operation is only supported for digital peripheral I/O on Port A and Port B. All GPIO ports support digital peripheral operation in EM0 and EM1.

4. Electrical Specifications

All electrical parameters in all tables are specified under the following conditions, unless stated otherwise:

- Typical values are based on T_A=25 °C and VDD supply at 3.0 V, by production test and/or technology characterization.
- Radio performance numbers are measured in conducted mode, based on Silicon Laboratories reference designs using output power-specific external RF impedance-matching networks for interfacing to a 50 Ω antenna.
- Minimum and maximum values represent the worst conditions across supply voltage, process variation, and operating temperature, unless stated otherwise.

4.1 Absolute Maximum Ratings

Table 4.1. Absolute Maximum Ratings

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Storage temperature range	T_{STG}		-40	—	+125	°C
Voltage on any supply pin	V_{DDMAX}		-0.3	—	3.8	V
Junction temperature	T_{JMAX}		—	—	+125	°C
Voltage ramp rate on any supply pin	$V_{DDRAMPMAX}$		—	—	1.0	V / µs
DC voltage on any GPIO pin[1]	V_{DIGPIN}		-0.3	—	V_{VDD} + 0.3	V
DC voltage on RESETn pin[2]	V_{RESETn}		-0.3	—	3.8	V
Total current into VDD pin	I_{VDDMAX}	Source	—	—	200	mA
Total current into GND pin	I_{VSSMAX}	Sink	—	—	200	mA
Current per I/O pin	I_{IOMAX}	Sink	—	—	50	mA
		Source	—	—	50	mA
Current for all I/O pins	$I_{IOALLMAX}$	Sink	—	—	200	mA
		Source	—	—	200	mA

Note:

1. When operating as an LCD driver, the output voltage on a GPIO may safely exceed this specification except on PA00, where the the maximum voltage is VDD. The pin output voltage may be up to 3.8 V in this case.
2. The RESETn pin has a pull-up device to the internal DVDD supply. For minimum leakage, RESETn should not exceed the voltage at DVDD, which is generated by the DC-DC converter. DVDD is equal to 1.8 V when DC-DC is active and bypassed to VDD when DC-DC is inactive.

4.2 General Operating Conditions

Table 4.2. General Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Operating ambient temperature range[1]	T_A		-40	—	+125	°C
VDD operating supply voltage	V_{VDD}	10 dBm Module, DC-DC in regulation	2.2	3.0	3.8	V
		19.5 dBm Module, DC-DC in regulation	2.2	3.3	3.8	V
		10 dBm Module, DC-DC in bypass	1.8	3.0	3.8	V
		19.5 dBm Module, DC-DC in bypass	1.8	3.3	3.8	V
HCLK and SYSCLK frequency	f_{HCLK}	VSCALE2, MODE = WS1	—	—	80	MHz
		VSCALE2, MODE = WS0	—	—	40	MHz
		VSCALE1, MODE = WS1	—	—	40	MHz
		VSCALE1, MODE = WS0	—	—	20	MHz
PCLK frequency	f_{PCLK}	VSCALE2 or VSCALE1	—	—	40	MHz
EM01 Group A clock frequency	$f_{EM01GRPACLK}$	VSCALE2	—	—	80	MHz
		VSCALE1	—	—	40	MHz
EM01 Group C clock frequency	$f_{EM01GRPCCLK}$	VSCALE2	—	—	80	MHz
		VSCALE1	—	—	40	MHz
Radio HCLK frequency	f_{RHCLK}	VSCALE2 or VSCALE1	—	40	—	MHz
DPLL Reference Clock	$f_{DPLLREFCLK}$	VSCALE2 or VSCALE1	—	—	40	MHz

Note:

1. The device may operate continuously at the maximum allowable ambient T_A rating as long as the absolute maximum T_{JMAX} is not exceeded. For an application with significant power dissipation, the allowable T_A may be lower than the maximum T_A rating. T_A = T_{JMAX} - ($THETA_{JA}$ x PowerDissipation). Refer to the 4.1 Absolute Maximum Ratings table and the 4.3 Thermal Characteristics table for T_{JMAX} and $THETA_{JA}$.

4.3 Thermal Characteristics

Table 4.3. Thermal Characteristics

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Thermal Resistance, Junction to Ambient	$THETA_{JA}$	2-Layer PCB, under Natural Convection[1]	—	48.5	—	°C/W
		4-Layer PCB, under Natural Convection[1]	—	24.5	—	°C/W
Thermal Resistance, Junction to Board	PSI_{JT}	2-Layer PCB, under Natural Convection[1]	—	8.6	—	°C/W
		4-Layer PCB, under Natural Convection[1]	—	8.3	—	°C/W

Note:

1. Measured according to JEDEC standard JESD51-2A. Integrated Circuit Thermal Test Method Environmental Conditions - Natural Convection (Still Air).

4.4 MCU Current Consumption at 3.0 V

Unless otherwise indicated, typical conditions are: VDD = 3.0 V, DC-DC in regulation. Voltage scaling level = VSCALE1. T_A = 25 °C. Minimum and maximum values in this table represent the worst conditions across process variation at T_A = 25 °C.

Table 4.4. MCU Current Consumption at 3.0 V

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in EM0 mode with all peripherals disabled	I_{ACTIVE}	80 MHz HFRCO w/ DPLL referenced to 40 MHz crystal, CPU running Prime from flash, VSCALE2	—	53.5	—	µA/MHz
		80 MHz HFRCO w/ DPLL referenced to 40 MHz crystal, CPU running while loop from flash, VSCALE2	—	53.8	—	µA/MHz
		80 MHz HFRCO w/ DPLL referenced to 40 MHz crystal, CPU running CoreMark loop from flash, VSCALE2	—	72.4	—	µA/MHz
		40 MHz crystal, CPU running Prime from flash	—	59.4	—	µA/MHz
		40 MHz crystal, CPU running while loop from flash	—	59.3	—	µA/MHz
		40 MHz crystal, CPU running CoreMark loop from flash	—	76.9	—	µA/MHz
		38 MHz HFRCO, CPU running while loop from flash	—	55	—	µA/MHz
Current consumption in EM1 mode with all peripherals disabled	I_{EM1}	80 MHz HFRCO w/ DPLL referenced to 40 MHz crystal, VSCALE2	—	39.9	—	µA/MHz
		40 MHz crystal	—	45.7	—	µA/MHz
		38 MHz HFRCO	—	41.5	—	µA/MHz
Current Consumption in EM2 mode, VSCALE0	I_{EM2_VS}	512 kB RAM and full Radio RAM retention, RTC running from LFXO[1]	—	5	—	µA
		512 kB RAM and full Radio RAM retention, RTC running from LFRCO[1]	—	5	—	µA
		512 kB RAM and full Radio RAM retention, RTC running from LFRCO in precision mode[1]	—	5.75	—	µA
		16 kB RAM and full Radio RAM retention, RTC running from LFXO[1]	—	1.4	—	µA
		16 kB RAM and full Radio RAM retention, RTC running from LFRCO[1]	—	1.4	—	µA
		16 kB RAM and full Radio RAM retention, RTC running from LFRCO in precision mode[1]	—	2.15	—	µA

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in EM3 mode, VSCALE0	I_{EM3_VS}	512 kB RAM and full Radio RAM retention, RTC running from ULFRCO[1]	—	4.7	—	µA
		16 kB RAM and full Radio RAM retention, RTC running from ULFRCO[1]	—	1.2	—	µA
Change in current consumption for retained RAM bank in EM2 or EM3	I_{EM3_RAM}	Per 16 kB RAM bank	—	0.12	—	µA
Current consumption in EM4 mode[2]	I_{EM4}	No BURTC, no LF oscillator	—	0.23	—	µA
		BURTC with LFRCO	—	0.66	—	µA
Current consumption during reset	I_{RST}	Hard pin reset held	—	480	—	µA

Note:

1. CPU cache retained, EM0/1 peripheral states retained
2. Note that the DCDC will be disabled in EM4.

4.5 Radio Current Consumption with 3.0 V Supply

RF current consumption measured with MCU in EM1 and all MCU peripherals disabled. Unless otherwise indicated, typical conditions are: VDD = 3.0 V, DC-DC in regulation. T_A = 25 °C.

Table 4.5. Radio Current Consumption with 3.0 V Supply

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Current consumption in receive mode, active packet reception	I_{RX_ACTIVE}	125 kbit/s, 2GFSK, f = 2.4 GHz, VSCALE1, EM1P	—	6	—	mA
		125 kbit/s, 2GFSK, f = 2.4 GHz, VSCALE2	—	7.2	—	mA
		500 kbit/s, 2GFSK, f = 2.4 GHz, VSCALE1, EM1P	—	6.1	—	mA
		500 kbit/s, 2GFSK, f = 2.4 GHz, VSCALE2	—	7.2	—	mA
		1 Mbit/s, 2GFSK, f = 2.4 GHz, VSCALE1, EM1P	—	5.7	—	mA
		1 Mbit/s, 2GFSK, f = 2.4 GHz, VSCALE2	—	6.8	—	mA
		2 Mbit/s, 2GFSK, f = 2.4 GHz, VSCALE1, EM1P	—	6.5	—	mA
		2 Mbit/s, 2GFSK, f = 2.4 GHz, VSCALE2	—	7.6	—	mA
Current consumption in receive mode, listening for packet	I_{RX_LISTEN}	125 kbit/s, 2GFSK, f = 2.4 GHz, VSCALE1, EM1P	—	6	—	mA
		125 kbit/s, 2GFSK, f = 2.4 GHz, VSCALE2	—	7.2	—	mA
		500 kbit/s, 2GFSK, f = 2.4 GHz, VSCALE1, EM1P	—	6.1	—	mA
		500 kbit/s, 2GFSK, f = 2.4 GHz, VSCALE2	—	7.2	—	mA
		1 Mbit/s, 2GFSK, f = 2.4 GHz, VSCALE1, EM1P	—	5.7	—	mA
		1 Mbit/s, 2GFSK, f = 2.4 GHz, VSCALE2	—	6.8	—	mA
		2 Mbit/s, 2GFSK, f = 2.4 GHz, VSCALE1, EM1P	—	6.5	—	mA
		2 Mbit/s, 2GFSK, f = 2.4 GHz, VSCALE2	—	7.7	—	mA
Current consumption in transmit mode, VSCALE2	I_{TX}	f = 2.442 GHz, CW, 19.5 dBm output power, VDD = 3.3 V	—	154.8	—	mA
		f = 2.442 GHz, CW, 10 dBm output power	—	19.4	—	mA
		f = 2.442 GHz, CW, 0 dBm output power	—	6.8	—	mA

4.6 RF Transmitter General Characteristics for the 2.4 GHz Band

Unless otherwise indicated, typical conditions are: VDD = 3.0 V, DC-DC in regulation. RF center frequency 2.45 GHz. T_A = 25 °C.

Table 4.6. RF Transmitter General Characteristics for the 2.4 GHz Band

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
RF tuning frequency range	F_{RANGE}		2402	—	2480	MHz
Maximum TX power[1]	$POUT_{MAX}$	19.5 dBm, VDD = 3.3 V	—	19.5	—	dBm
		10 dBm	—	10	—	dBm
		0 dBm	—	-0.1	—	dBm
Minimum active TX power	$POUT_{MIN}$	19.5 dBm, VDD = 3.3 V	—	-33	—	dBm
		10 dBm	—	-30	—	dBm
		0 dBm	—	-24	—	dBm
Output power step size	$POUT_{STEP}$	0 dBm, Output Power < -5 dBm	2.7	6	10.2	dB
		0 dBm, Output Power > -5 dBm	0.1	0.4	1.6	dB
		10 dBm, Output Power < -5 dBm	2.2	6	12.7	dB
		10 dBm, -5 dBm < Output power < 0 dBm	0.9	1.4	2.1	dB
		10 dBm, Output power > 0 dBm	0.1	0.3	1.1	dB
		19.5 dBm, VDD = 3.3 V, Output power < -5 dBm	14.3	6.5	2.5	dB
		19.5 dBm, VDD = 3.3 V, -5 dBm < Output power < 0 dBm	1.1	1.4	1.8	dB
		19.5 dBm, VDD = 3.3 V, 0 dBm < Output power < 10 dBm	0.1	0.4	1	dB
		19.5 dBm, VDD = 3.3 V, Output power > 10 dBm	0.1	0.1	0.4	dB
Output power variation vs supply voltage variation	$POUT_{VAR_V}$	19.5 dBm output power with VDD voltage swept from 1.8 V to 3.8 V	—	5	—	dB
		10 dBm output power with VDD voltage swept from 1.8 V to 3.8 V	—	0.02	—	dB
		0 dBm output power with VDD voltage swept from 1.8 V to 3.8 V	—	0.02	—	dB
Output power variation vs temperature	$POUT_{VAR_T}$	19.5 dBm, VDD = 3.3 V, (-40 to +125 °C)	—	0.9	—	dB
		10 dBm, (-40 to +125 °C)	—	0.8	—	dB
		0 dBm, (-40 to +125 °C)	—	1.2	—	dB
Output power variation over the RF tuning frequency range	$POUT_{VAR_F}$	19.5 dBm, VDD = 3.3 V	—	0.2	—	dB
		10 dBm	—	0.2	—	dB
		0 dBm	—	0.2	—	dB

Note:

1. Supported transmit power levels are determined by the ordering part number (OPN). Transmit power ratings for all devices covered in this data sheet can be found in the TX Power column of the Ordering Information Table.

4.7 RF Receiver General Characteristics for the 2.4 GHz Band

Unless otherwise indicated, typical conditions are: VDD = 3.0 V, DC-DC in regulation. RF center frequency 2.442 GHz. T_A = 25 °C.

Table 4.7. RF Receiver General Characteristics for the 2.4 GHz Band

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
RF tuning frequency range	F_{RANGE}		2402	—	2480	MHz

4.8 RF Receiver Characteristics for Bluetooth Low Energy in the 2.4 GHz Band 1 Mbps Data Rate

Unless otherwise indicated, typical conditions are: VDD = 3.0 V, DC-DC in regulation. RF center frequency 2.442 GHz. T_A = 25 °C.

Table 4.8. RF Receiver Characteristics for Bluetooth Low Energy in the 2.4 GHz Band 1 Mbps Data Rate

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Rx Max Strong Signal Input Level for 0.1% BER	RX_{SAT}	Signal is reference signal, packet length is 37 bytes[1]	—	10	—	dBm
Sensitivity	SENS	10 dBm Module, Signal is reference signal, 37 byte payload[1]	—	-98.2	—	dBm
		10 dBm Module, Signal is reference signal, 255 byte payload[2]	—	-96.7	—	dBm
		10 dBm Module, With non-ideal signals, 37 byte payload[3] [1]	—	-97.9	—	dBm
		19.5 dBm Module, Signal is reference signal, 37 byte payload[1]	—	-97.7	—	dBm
		19.5 dBm Module, Signal is reference signal, 255 byte payload[2]	—	-96.1	—	dBm
		19.5 dBm Module, With non-ideal signals, 37 byte payload[3] [1]	—	-97.3	—	dBm
Signal to co-channel interferer	C/I_{CC}	(see notes), 37 byte payload[1] [4]	—	6.4	—	dB
N ± 1 Adjacent channel selectivity	C/I_1	Interferer is reference signal at +1 MHz offset, 37 byte payload[1] [5] [4] [6]	—	-7.2	—	dB
		Interferer is reference signal at -1 MHz offset, 37 byte payload[1] [5] [4] [6]	—	-7.4	—	dB
N ± 2 Alternate channel selectivity	C/I_2	Interferer is reference signal at +2 MHz offset, 37 byte payload[1] [5] [4] [6]	—	-44.7	—	dB
		Interferer is reference signal at -2 MHz offset, 37 byte payload[1] [5] [4] [6]	—	-46.7	—	dB
N ± 3 Alternate channel selectivity	C/I_3	Interferer is reference signal at +3 MHz offset, 37 byte payload[1] [5] [4] [6]	—	-49.9	—	dB
		Interferer is reference signal at -3 MHz offset, 37 byte payload[1] [5] [4] [6]	—	-49.6	—	dB
Selectivity to image frequency	C/I_{IM}	Interferer is reference signal at image frequency with 1 MHz precision, 37 byte payload[1] [6]	—	-25.2	—	dB
Selectivity to image frequency ± 1 MHz	C/I_{IM_1}	Interferer is reference signal at image frequency +1 MHz with 1 MHz precision, 37 byte payload[1] [6]	—	-44.7	—	dB
		Interferer is reference signal at image frequency -1 MHz with 1 MHz precision, 37 byte payload[1] [6]	—	-7.2	—	dB

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit

Note:

1. 0.1% Bit Error Rate.
2. 0.017% Bit Error Rate.
3. With non-ideal signals as specified in Bluetooth Test Specification RF-PHY.TS.5.0.1 section 4.7.1
4. Desired signal -67 dBm.
5. Desired frequency 2402 MHz ≤ Fc ≤ 2480 MHz.
6. With allowed exceptions.

4.9 RF Receiver Characteristics for Bluetooth Low Energy in the 2.4 GHz Band 2 Mbps Data Rate

Unless otherwise indicated, typical conditions are: VDD = 3.0 V, DC-DC in regulation. RF center frequency 2.442 GHz. T_A = 25 °C.

Table 4.9. RF Receiver Characteristics for Bluetooth Low Energy in the 2.4 GHz Band 2 Mbps Data Rate

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Rx Max Strong Signal Input Level for 0.1% BER	RX_{SAT}	Signal is reference signal, packet length is 37 bytes[1]	—	10	—	dBm
Sensitivity	SENS	10 dBm Module, Signal is reference signal, 37 byte payload[1]	—	-95.5	—	dBm
		10 dBm Module, Signal is reference signal, 255 byte payload[2]	—	-93.9	—	dBm
		10 dBm Module, With non-ideal signals, 37 byte payload[3] [1]	—	-95.3	—	dBm
		19.5 dBm Module, Signal is reference signal, 37 byte payload[1]	—	-94.8	—	dBm
		19.5 dBm Module, Signal is reference signal, 255 byte payload[2]	—	-93.3	—	dBm
		19.5 dBm Module, With non-ideal signals, 37 byte payload[3] [1]	—	-94.6	—	dBm
Signal to co-channel interferer	C/I_{CC}	(see notes), 37 byte payload[1] [4]	—	6.6	—	dB
N ± 1 Adjacent channel selectivity	C/I_1	Interferer is reference signal at +2 MHz offset, 37 byte payload[1] [5] [4] [6]	—	-7.1	—	dB
		Interferer is reference signal at -2 MHz offset, 37 byte payload[1] [5] [4] [6]	—	-7.5	—	dB
N ± 2 Alternate channel selectivity	C/I_2	Interferer is reference signal at +4 MHz offset, 37 byte payload[1] [5] [4] [6]	—	-43.8	—	dB
		Interferer is reference signal at -4 MHz offset, 37 byte payload[1] [5] [4] [6]	—	-45.8	—	dB
N ± 3 Alternate channel selectivity	C/I_3	Interferer is reference signal at +6 MHz offset, 37 byte payload[1] [5] [4] [6]	—	-49.8	—	dB
		Interferer is reference signal at -6 MHz offset, 37 byte payload[1] [5] [4] [6]	—	-50.8	—	dB
Selectivity to image frequency	C/I_{IM}	Interferer is reference signal at image frequency with 1 MHz precision, 37 byte payload[1] [6]	—	-24.6	—	dB
Selectivity to image frequency ± 2 MHz	C/I_{IM_1}	Interferer is reference signal at image frequency +2 MHz with 1 MHz precision, 37 byte payload[1] [6]	—	-43.8	—	dB
		Interferer is reference signal at image frequency -2 MHz with 1 MHz precision, 37 byte payload[1] [6]	—	-7.1	—	dB

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit

Note:

1. 0.1% Bit Error Rate.
2. 0.017% Bit Error Rate.
3. With non-ideal signals as specified in Bluetooth Test Specification RF-PHY.TS.5.0.1 section 4.7.1
4. Desired signal -64 dBm.
5. Desired frequency 2402 MHz ≤ Fc ≤ 2480 MHz.
6. With allowed exceptions.

4.10 RF Receiver Characteristics for Bluetooth Low Energy in the 2.4 GHz Band 500 kbps Data Rate

Unless otherwise indicated, typical conditions are: VDD = 3.0 V, DC-DC in regulation. RF center frequency 2.442 GHz. T_A = 25 °C.

Table 4.10. RF Receiver Characteristics for Bluetooth Low Energy in the 2.4 GHz Band 500 kbps Data Rate

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Rx Max Strong Signal Input Level for 0.1% BER	RX_{SAT}	Signal is reference signal, packet length is 37 bytes[1]	—	10	—	dBm
Sensitivity	SENS	10 dBm Module, Signal is reference signal, 37 byte payload[1]	—	-101.9	—	dBm
		10 dBm Module, Signal is reference signal, 255 byte payload[2]	—	-100.6	—	dBm
		10 dBm Module, With non-ideal signals, 37 byte payload[3] [1]	—	-101.2	—	dBm
		19.5 dBm Module, Signal is reference signal, 37 byte payload[1]	—	-101.2	—	dBm
		19.5 dBm Module, Signal is reference signal, 255 byte payload[2]	—	-99.9	—	dBm
		19.5 dBm Module, With non-ideal signals, 37 byte payload[3] [1]	—	-100.6	—	dBm
Signal to co-channel interferer	C/I_{CC}	(see notes), 37 byte payload[1] [4]	—	2.0	—	dB
N ± 1 Adjacent channel selectivity	C/I_1	Interferer is reference signal at +1 MHz offset, 37 byte payload[1] [5] [4] [6]	—	-8.8	—	dB
		Interferer is reference signal at -1 MHz offset, 37 byte payload[1] [5] [4] [6]	—	-8.9	—	dB
N ± 2 Alternate channel selectivity	C/I_2	Interferer is reference signal at +2 MHz offset, 37 byte payload[1] [5] [4] [6]	—	-49.4	—	dB
		Interferer is reference signal at -2 MHz offset, 37 byte payload[1] [5] [4] [6]	—	-51.4	—	dB
N ± 3 Alternate channel selectivity	C/I_3	Interferer is reference signal at +3 MHz offset, 37 byte payload[1] [5] [4] [6]	—	-52.0	—	dB
		Interferer is reference signal at -3 MHz offset, 37 byte payload[1] [5] [4] [6]	—	-55.5	—	dB
Selectivity to image frequency	C/I_{IM}	Interferer is reference signal at image frequency with 1 MHz precision, 37 byte payload[1] [6]	—	-52.4	—	dB
Selectivity to image frequency ± 1 MHz	C/I_{IM_1}	Interferer is reference signal at image frequency +1 MHz with 1 MHz precision, 37 byte payload[1] [6]	—	-52.4	—	dB
		Interferer is reference signal at image frequency -1 MHz with 1 MHz precision, 37 byte payload[1] [6]	—	-49.8	—	dB

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit

Note:

1. 0.1% Bit Error Rate.
2. 0.017% Bit Error Rate.
3. With non-ideal signals as specified in Bluetooth Test Specification RF-PHY.TS.5.0.1 section 4.7.1
4. Desired signal -72 dBm.
5. Desired frequency 2402 MHz ≤ Fc ≤ 2480 MHz.
6. With allowed exceptions.

4.11 RF Receiver Characteristics for Bluetooth Low Energy in the 2.4 GHz Band 125 kbps Data Rate

Unless otherwise indicated, typical conditions are: VDD = 3.0 V, DC-DC in regulation. RF center frequency 2.442 GHz. T_A = 25 °C.

Table 4.11. RF Receiver Characteristics for Bluetooth Low Energy in the 2.4 GHz Band 125 kbps Data Rate

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Rx Max Strong Signal Input Level for 0.1% BER	RX_{SAT}	Signal is reference signal, packet length is 37 bytes[1]	—	10	—	dBm
Sensitivity	SENS	10 dBm Module, Signal is reference signal, 37 byte payload[1]	—	-106.2	—	dBm
		10 dBm Module, Signal is reference signal, 255 byte payload[2]	—	-105.8	—	dBm
		10 dBm Module, With non-ideal signals, 37 byte payload[3] [1]	—	-105.8	—	dBm
		19.5 dBm Module, Signal is reference signal, 37 byte payload[1]	—	-105.6	—	dBm
		19.5 dBm Module, Signal is reference signal, 255 byte payload[2]	—	-105.2	—	dBm
		19.5 dBm Module, With non-ideal signals, 37 byte payload[3] [1]	—	-105.2	—	dBm
Signal to co-channel interferer	C/I_{CC}	(see notes), 37 byte payload[1] [4]	—	0.8	—	dB
N ± 1 Adjacent channel selectivity	C/I_1	Interferer is reference signal at +1 MHz offset, 37 byte payload[1] [5] [4] [6]	—	-13	—	dB
		Interferer is reference signal at -1 MHz offset, 37 byte payload[1] [5] [4] [6]	—	-13.1	—	dB
N ± 2 Alternate channel selectivity	C/I_2	Interferer is reference signal at +2 MHz offset, 37 byte payload[1] [5] [4] [6]	—	-54.2	—	dB
		Interferer is reference signal at -2 MHz offset, 37 byte payload[1] [5] [4] [6]	—	-55.9	—	dB
N ± 3 Alternate channel selectivity	C/I_3	Interferer is reference signal at +3 MHz offset, 37 byte payload[1] [5] [4] [6]	—	-55.9	—	dB
		Interferer is reference signal at -3 MHz offset, 37 byte payload[1] [5] [4] [6]	—	-59.6	—	dB
Selectivity to image frequency	C/I_{IM}	Interferer is reference signal at image frequency with 1 MHz precision, 37 byte payload[1] [6]	—	-55.2	—	dB
Selectivity to image frequency ± 1 MHz	C/I_{IM_1}	Interferer is reference signal at image frequency +1 MHz with 1 MHz precision, 37 byte payload[1] [6]	—	-55.9	—	dB
		Interferer is reference signal at image frequency -1 MHz with 1 MHz precision, 37 byte payload[1] [6]	—	-54.2	—	dB

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Note: 1. 0.1% Bit Error Rate. 2. 0.017% Bit Error Rate. 3. With non-ideal signals as specified in Bluetooth Test Specification RF-PHY.TS.5.0.1 section 4.7.1 4. Desired signal -79 dBm. 5. Desired frequency 2402 MHz ≤ Fc ≤ 2480 MHz. 6. With allowed exceptions.						

4.12 High-Frequency Crystal (HFXO)

Table 4.12. High-Frequency Crystal (HFXO)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Crystal frequency	f_{HFXTAL}		—	40	—	MHz
Initial calibrated accuracy	ACC_{HFXTAL}		-5	+/-3	5	ppm
Temperature drift	$DRIFT_{HFXTAL}$	Across specified temperature range	-32	—	32	ppm

4.13 Low Frequency Crystal Oscillator (LFXO)

Table 4.13. Low Frequency Crystal Oscillator (LFXO)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Crystal Frequency	F_{LFXO}		—	32.768	—	kHz
Supported Crystal equivalent series resistance (ESR)	ESR_{LFXO}	GAIN = 0	—	—	80	kΩ
		GAIN = 1 to 3	—	—	100	kΩ
Supported range of crystal load capacitance [1]	C_{L_LFXO}	GAIN = 0	4	—	6	pF
		GAIN = 1	6	—	10	pF
		GAIN = 2 (see note[2])	10	—	12.5	pF
		GAIN = 3 (see note[2])	12.5	—	18	pF
Current consumption	I_{CL12p5}	ESR = 70 kΩ, C_L = 12.5 pF, GAIN[3] = 2, AGC[4] = 1	—	294	—	nA
Startup Time	$T_{STARTUP}$	ESR = 70 kΩ, C_L = 7 pF, GAIN[3] = 1, AGC[4] = 1	—	52	—	ms
On-chip tuning cap step size	SS_{LFXO}		—	0.26	—	pF
On-chip tuning capacitor value at minimum setting[5]	C_{LFXO_MIN}	CAPTUNE = 0	—	5.2	—	pF
On-chip tuning capacitor value at maximum setting[5]	C_{LFXO_MAX}	CAPTUNE = 0x4F	—	26.2	—	pF

Note:

1. Total load capacitance seen by the crystal
2. Crystals with a load capacitance of greater than 12 pF require external load capacitors.
3. In LFXO_CAL Register
4. In LFXO_CFG Register
5. The effective load capacitance seen by the crystal will be $C_{LFXO}/2$. This is because each XTAL pin has a tuning cap and the two caps will be seen in series by the crystal

4.14 Precision Low Frequency RC Oscillator (LFRCO)

Table 4.14. Precision Low Frequency RC Oscillator (LFRCO)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Nominal oscillation frequency	F_{LFRCO}		—	32.768	—	kHz
Frequency accuracy	F_{LFRCO_ACC}	Normal mode	-3	—	3	%
		Precision mode[1], across operating temperature range[2]	-500	—	500	ppm
Startup time	$t_{STARTUP}$	Normal mode	—	204	—	µs
		Precision mode[1]	—	11.7	—	ms
Current consumption	I_{LFRCO}	Normal mode	—	189.9	—	nA
		Precision mode[1], T = stable at 25 °C [3]	—	649.8	—	nA

Note:

1. The LFRCO operates in high-precision mode when CFG_HIGHPRECEN is set to 1. High-precision mode is not available in EM4.
2. Includes ± 40 ppm frequency tolerance of the HFXO crystal.
3. Includes periodic re-calibration against HFXO crystal oscillator.

4.15 GPIO Pins

Table 4.15. GPIO Pins

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Leakage current	I_{LEAK_IO}	MODEx = DISABLED, VDD = 3.0 V	—	2.5	—	nA
Input low voltage[1]	V_{IL}	Any GPIO pin	—	—	0.3 * V_{VDD}	V
		RESETn	—	—	0.3 * V_{DVDD}	V
Input high voltage[1]	V_{IH}	Any GPIO pin	0.7 * V_{VDD}	—	—	V
		RESETn	0.7 * V_{DVDD}	—	—	V
Hysteresis of input voltage	V_{HYS}	Any GPIO pin	0.05 * V_{VDD}	—	—	V
		RESETn	0.05 * V_{DVDD}	—	—	V
Output high voltage	V_{OH}	Sourcing 20 mA, VDD = 3.0 V	0.8 * V_{VDD}	—	—	V
Output low voltage	V_{OL}	Sinking 20 mA, VDD = 3.0 V	—	—	0.2 * V_{VDD}	V
GPIO rise time	T_{GPIO_RISE}	VDD = 3.0 V, C_{load} = 50pF, SLEWRATE = 4, 10% to 90%	—	8.4	—	ns
GPIO fall time	T_{GPIO_FALL}	VDD = 3.0 V, C_{load} = 50pF, SLEWRATE = 4, 90% to 10%	—	7.1	—	ns
Pull up/down resistance[2]	R_{PULL}	Any GPIO pin. Pull-up to VDD: MODEn = DISABLE DOUT=1. Pull-down to GND: MODEn = WIREDORPULLDOWN DOUT = 0.	33	44	55	kΩ
		RESETn pin. Pull-up to DVDD	33	44	55	kΩ
Maximum filtered glitch width	T_{GF}	MODE = INPUT, DOUT = 1	—	27	—	ns
RESETn low time to ensure pin reset	T_{RESET}		100	—	—	ns

Note:

1. GPIO input thresholds are proportional to the VDD pin. RESETn input thresholds are proportional to the internal DVDD supply, which is generated by the DC-DC converter. DVDD is equal to 1.8 V when DC-DC is active and bypassed to VDD when DC-DC is inactive.
2. GPIO pull-ups connect to VDD supply, pull-downs connect to GND. RESETn pull-up connects to internal DVDD supply, which is generated by the DC-DC converter. DVDD is equal to 1.8 V when DC-DC is active and bypassed to VDD when DC-DC is inactive.

4.16 LCD

Table 4.16. LCD

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
LCD Temperature Range	T_{RANGE}		-40	—	105	°C
Frame rate	f_{LCDFR}		30	—	100	Hz
LCD supply range[1]	V_{LCDIN}		1.8	—	3.8	V
LCD output voltage range[2] [3]	V_{LCD}	Step-down mode with external LCD capacitor	2.4	—	MIN(3.6, V_{LCDIN} - 0.1)	V
		Charge pump mode with external LCD capacitor	2.4	—	MIN(3.6, 1.9 * V_{LCDIN})	V
Contrast control step size	$STEP_{CONTRAST}$	Charge pump or Step-down mode	—	50	—	mV
Contrast control step accuracy[4]	$ACC_{CONTRAST}$		—	+/- 1.5	—	%

Note:

1. V_{LCDIN} is selectable between the VDD or DVDD supply pins, depending on EMU_PWRCTRL_ANASW.
2. V_{LCD} should be a maximum of 2 V above V_{VDD} to avoid additional leakage through the GPIO pins used for LCD functions.
3. Maximum voltage for PA00 is V_LCDIN.
4. Step size accuracy is measured relative to the typical step size, and typ value represents one standard deviation.

4.17 Microcontroller Peripherals

The MCU peripherals set available in BGM260P modules includes:

- Analog to Digital Converter (IADC)
- Analog Comparator (ACMP)
- Digital to Analog Converter (VDAC)
- Brown Out Detectors (BOD)
- Oscillators
  - High Frequency RC Oscillator (HFRCO)
  - Fast Start-Up RC Oscillator (FSRCO)
  - Ultra Low Frequency RC Oscillator (ULFRCO)
- Counters/Timers and PWM
  - Timer/Counter (TIMER)
  - Low Energy Timer (LETIMER)
  - System Real Time Clock with Capture (SYSRTC)
  - Back-Up Real Time Counter (BURTC)
  - Watchdog Timer (WDOG)
  - Pulse Counter (PCNT)
- USART (UART/SPI/SmartCards/IrDA/I2S)
- EUSART (UART/IrDA)
- I^2C peripheral interfaces
- Peripheral Reflex System (PRS)
- Flash Characteristics
- Temperature Sensor
- Crypto Operation Timing for SE Manager API
- Crypto Operation Average Current for SE Manager API

For details on their electrical performance, consult the relevant portions of Section 4 in the EFR32BG26 Data Sheet.

To learn which GPIO ports provide access to every peripheral, consult 6.3 Analog Peripheral Connectivity and 6.4 Digital Peripheral Connectivity.

4.18 Antenna Radiation and Efficiency

Typical BGM260P radiation patterns for the built-in antenna under optimal operating conditions are plotted in the figures that follow. Antenna gain and radiation patterns have a strong dependence on the size and shape of the application PCB the module is mounted on, as well as on the proximity of any mechanical design to the antenna.

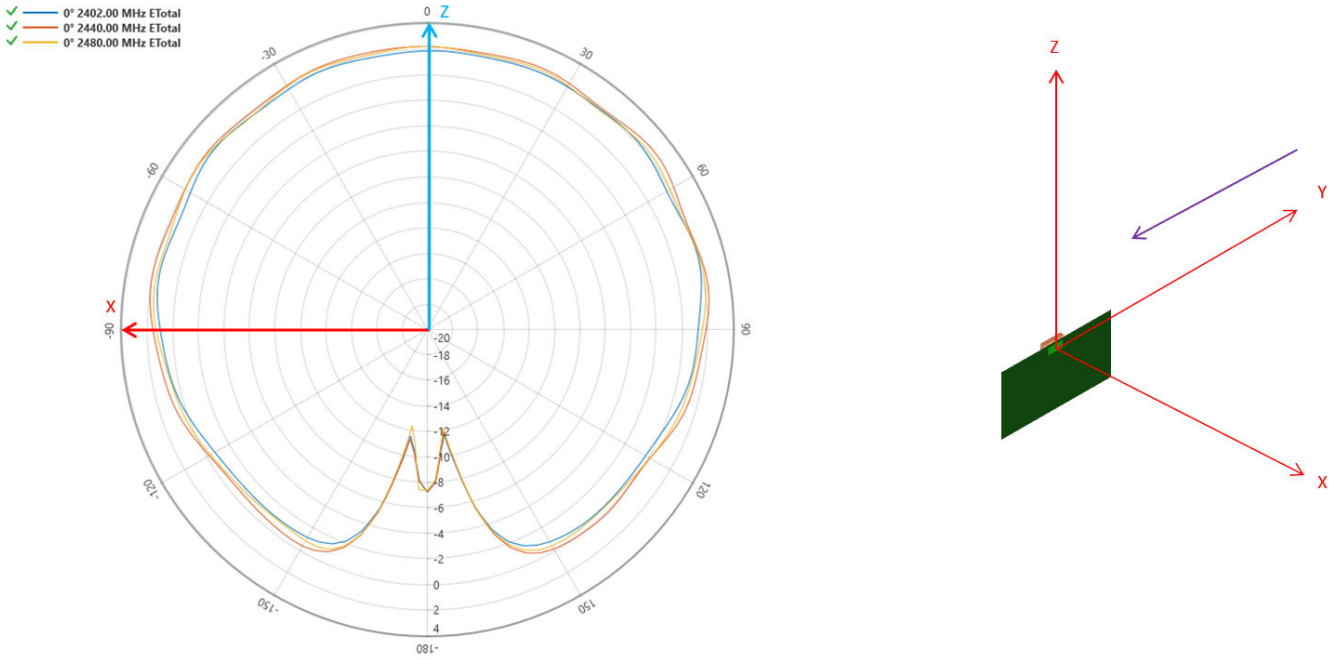


Figure 4.1. Typical 2D Antenna Radiation Patterns - Phi 0° (Side View) Gain (dBi)

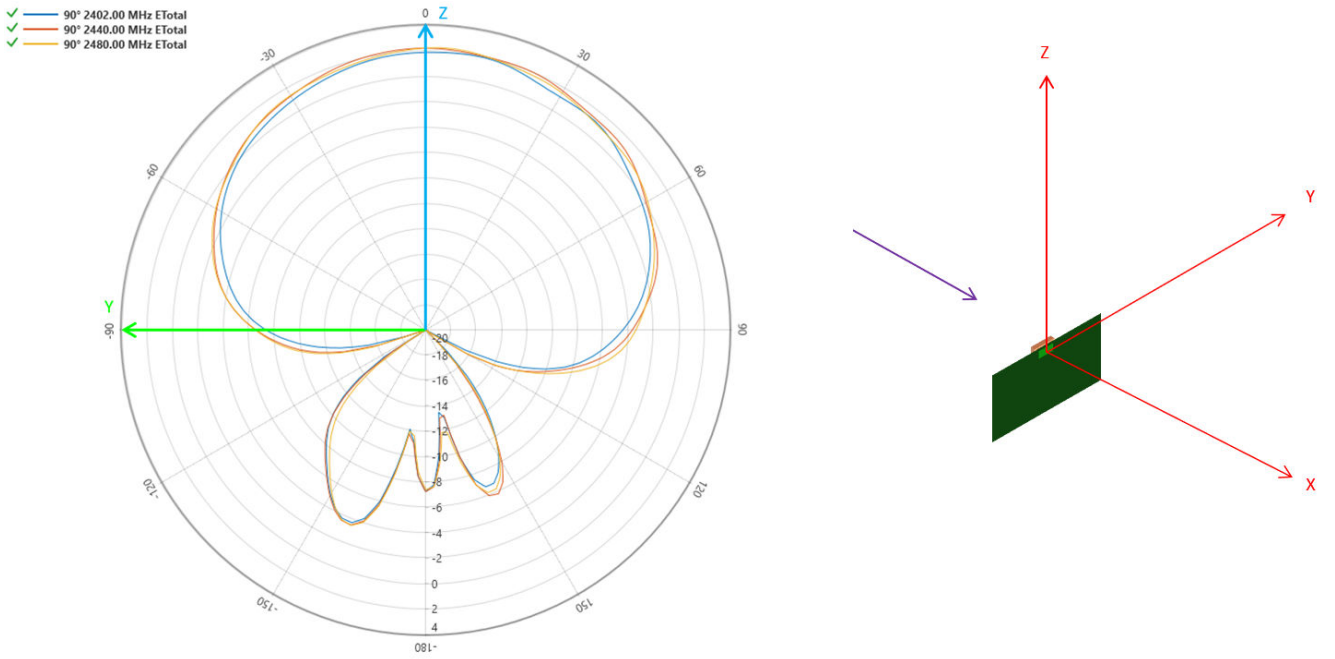


Figure 4.2. Typical 2D Antenna Radiation Patterns - Phi 90° (Top View) Gain (dBi)

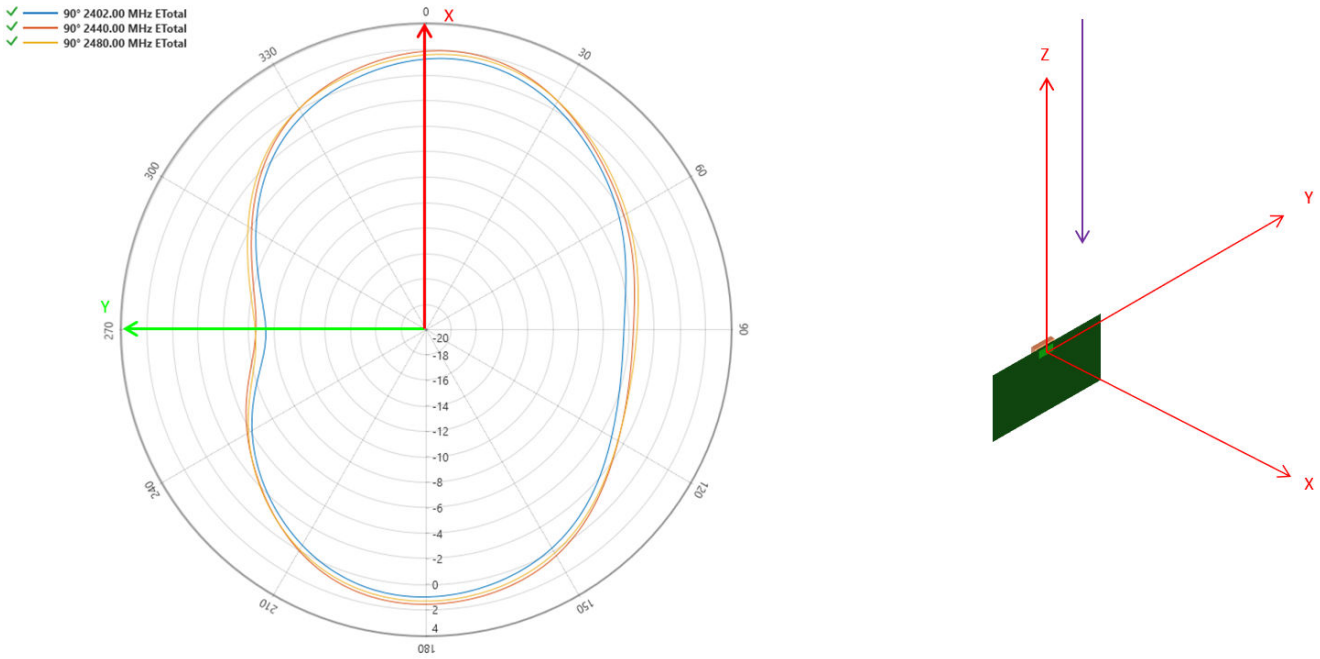


Figure 4.3. Typical 2D Antenna Radiation Patterns - Theta 90^{o} (Front View) Gain (dBi)

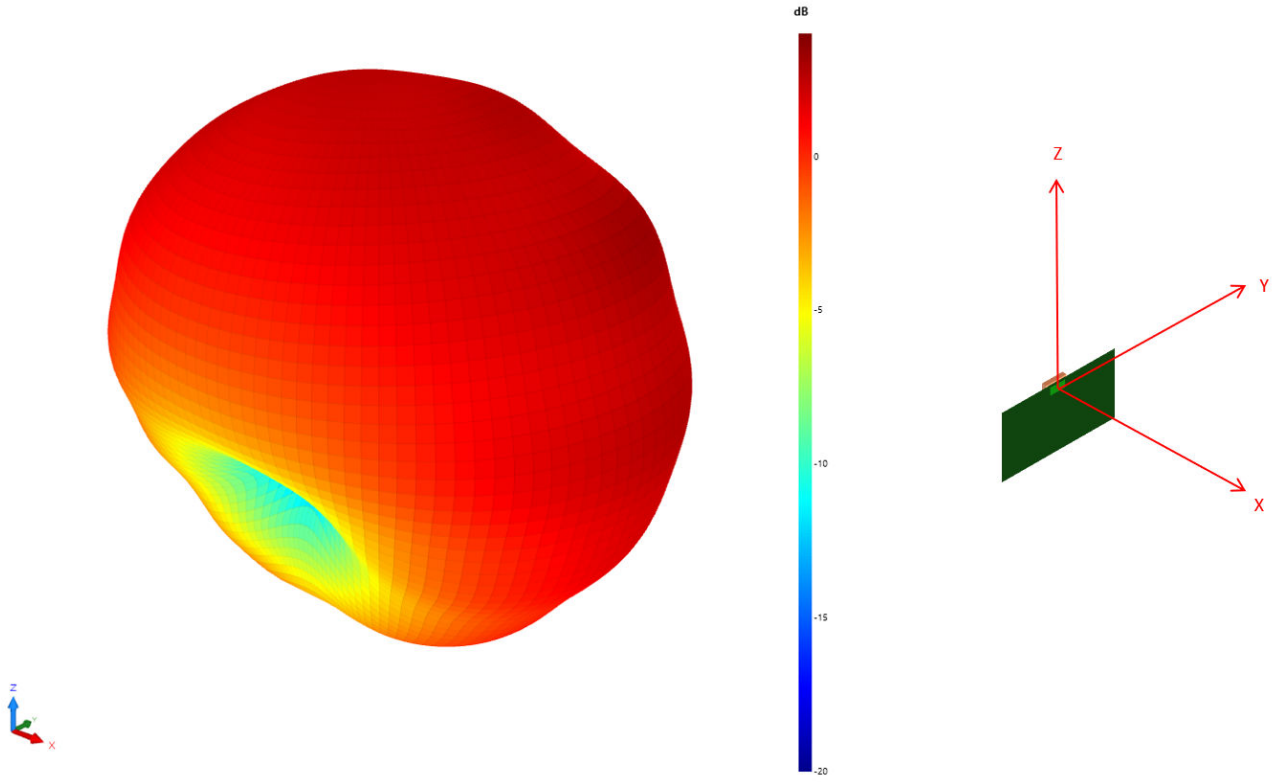


Figure 4.4. 3D Radiation Pattern at 2440MHz View 1

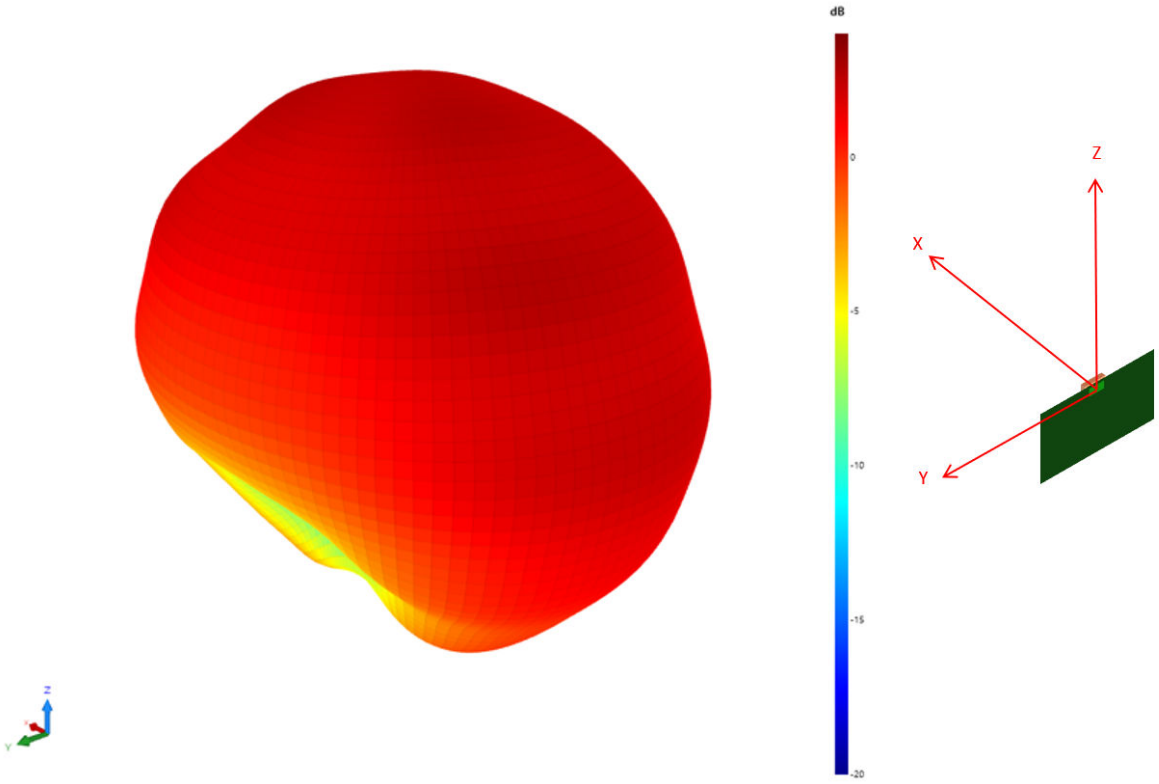


Figure 4.5. 3D Radiation Pattern at 2440MHz View 2

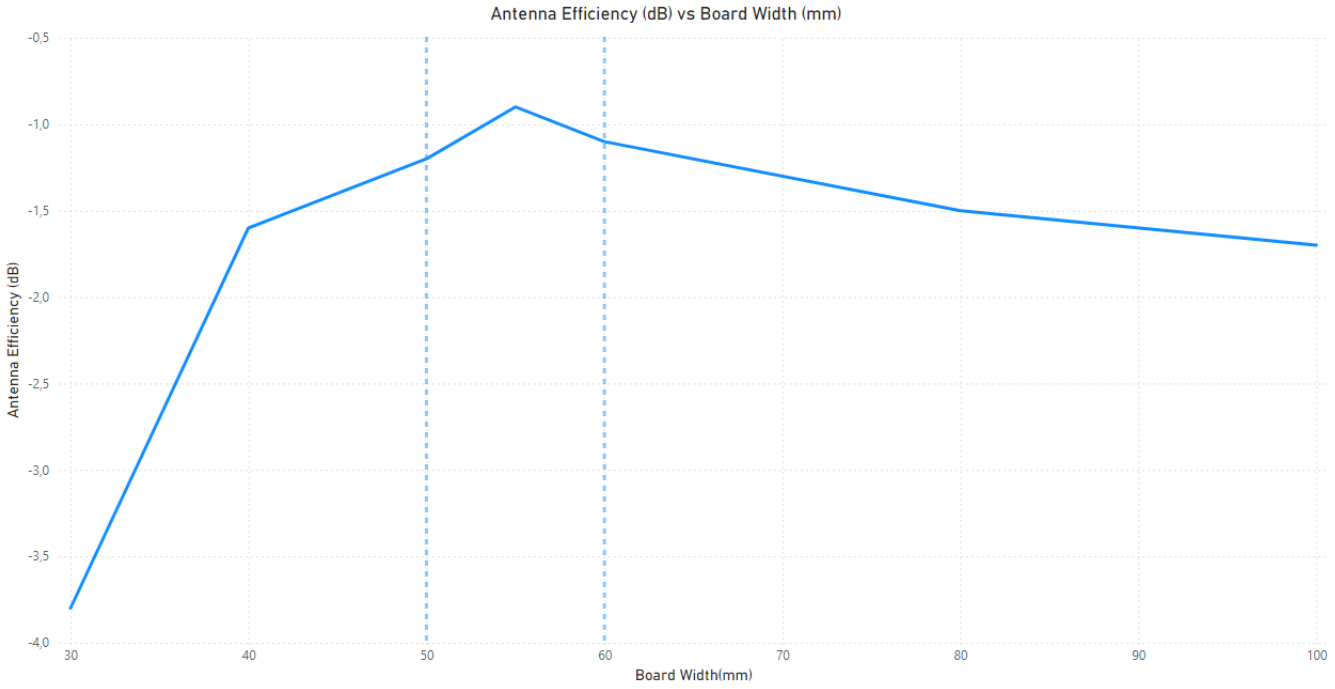


Figure 4.6. Efficiency of the Built-in Antenna as Function of the Carrier Board Width (mm)

5. Reference Diagrams

5.1 Network Co-Processor (NCP) Application with UART Host

The BGM260P can be controlled over the UART interface as a peripheral to an external host processor. Typical power supply, programming/debug interface, and host interface connections are shown in the figure below. For more details, refer to AN958: Debugging and Programming Interfaces for Custom Designs.

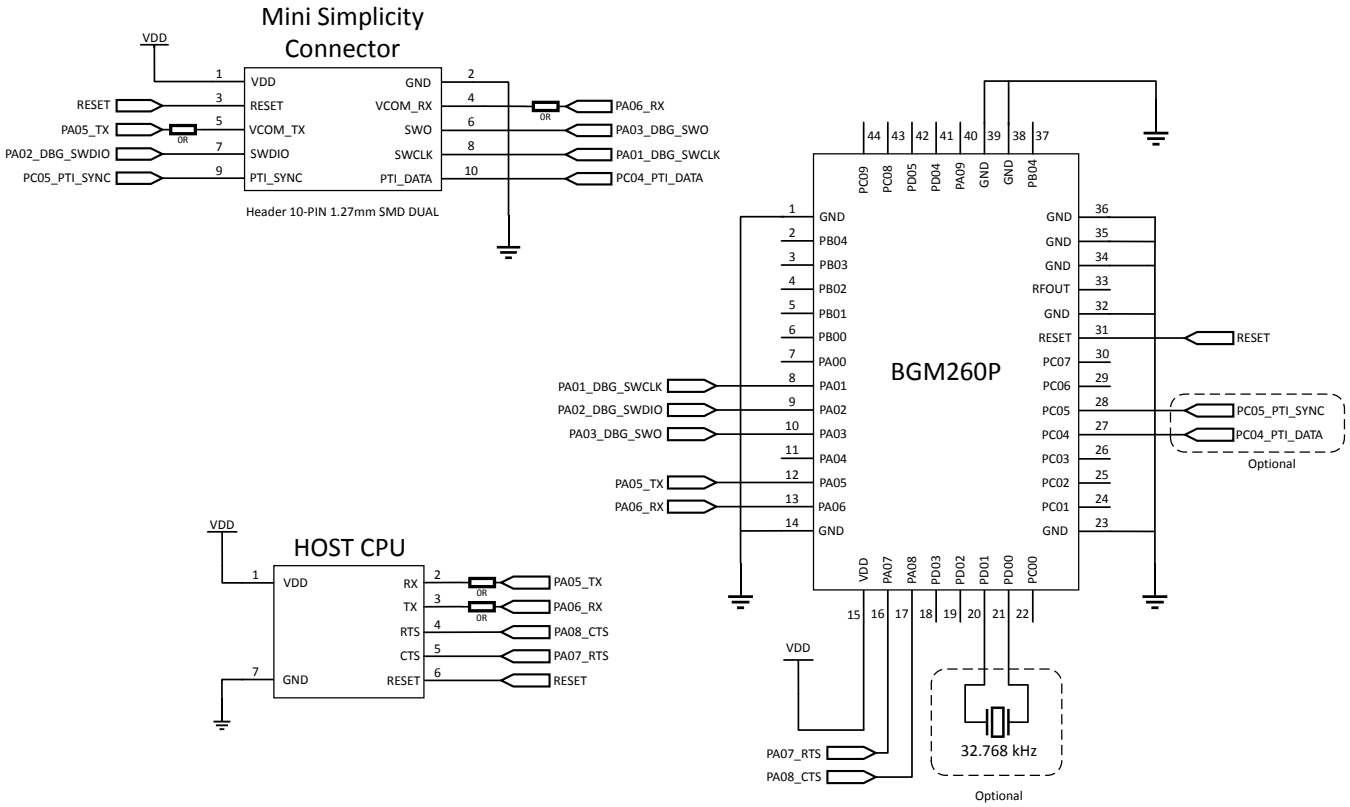


Figure 5.1. UART NCP Configuration

5.2 SoC Application

The BGM260P can be used in a stand-alone SoC configuration without an external host processor. Typical power supply and programming/debug interface connections are shown in the figure below. For more details, refer to AN958: Debugging and Programming Interfaces for Custom Designs.

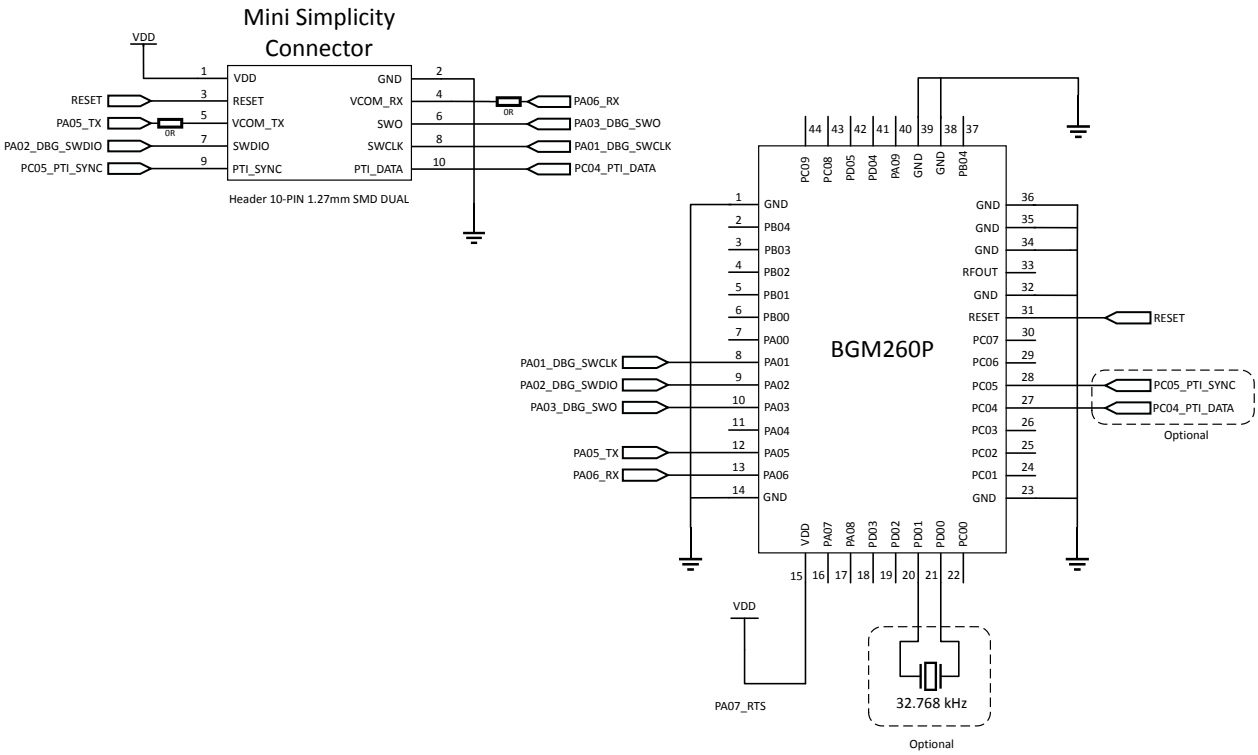


Figure 5.2. Stand-Alone SoC Configuration

6. Pin Definitions

6.1 Module Pinout

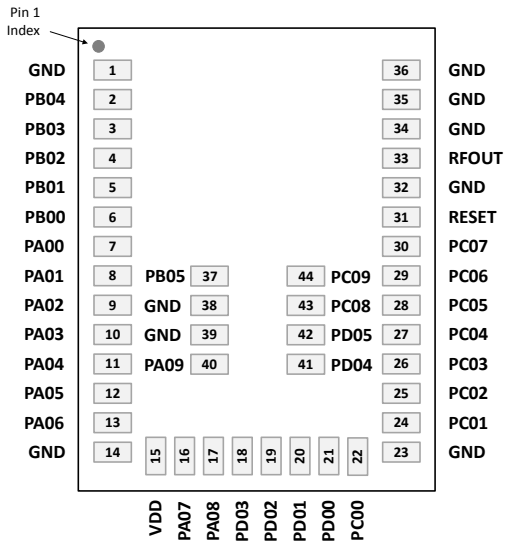


Figure 6.1. BGM260P Module Pinout

The next table shows the BGM260P pinout and general descriptions for each pin. Refer to 6.2 Alternate Pin Functions, 6.3 Analog Peripheral Connectivity, and 6.4 Digital Peripheral Connectivity for details on functions and peripherals supported by each GPIO pin.

Table 6.1. BGM260P Module Pin Definitions

Pin Name	No.	Description	Pin Name	No.	Description
GND	1	Ground	PB04	2	GPIO
PB03	3	GPIO	PB02	4	GPIO
PB01	5	GPIO	PB00	6	GPIO
PA00	7	GPIO	PA01	8	GPIO
PA02	9	GPIO	PA03	10	GPIO
PA04	11	GPIO	PA05	12	GPIO
PA06	13	GPIO	GND	14	Ground
VDD	15	Power supply	PA07	16	GPIO
PA08	17	GPIO	PD03	18	GPIO
PD02	19	GPIO	PD01	20	GPIO
PD00	21	GPIO	PC00	22	GPIO
GND	23	Ground	PC01	24	GPIO
PC02	25	GPIO	PC03	26	GPIO
PC04	27	GPIO	PC05	28	GPIO
PC06	29	GPIO	PC07	30	GPIO

Pin Name	No.	Description	Pin Name	No.	Description
RESETn	31	Reset Pin. The RESETn pin is pulled up to an internal DVDD supply. An external pull-up is not recommended. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released. The RESETn pin can be left unconnected if no external reset switch or source is used.	GND	32	Ground
RFOUT	33	No Connect	GND	34	Ground
GND	35	Ground	GND	36	Ground
PB05	37	GPIO	GND	38	Ground
GND	39	Ground	PA09	40	GPIO
PD04	41	GPIO	PD05	42	GPIO
PC08	43	GPIO	PC09	44	GPIO

6.2 Alternate Pin Functions

Some GPIOs support alternate functions like debugging, wake-up from EM4, external low frequency crystal access, etc.. The following table shows which module pins have alternate capabilities and the functions they support. Refer to the EFR32xG26 Reference Manual for more details.

Table 6.2. GPIO Alternate Functions Table

GPIO	Alternate Functions		
PA00	IADC0.VREFP	LCD.SEG8	
PA01	GPIO.SWCLK	LCD.SEG9	
PA02	GPIO.SWDIO		
PA03	GPIO.SWV	GPIO.TDO	GPIO.TRACEDATA0
PA04	GPIO.TDI	GPIO.TRACECLK	LCD.SEG10
PA05	GPIO.TRACEDATA1	GPIO.EM4WU0	LCD.SEG11
PA06	GPIO.TRACEDATA2	LCD.LCD_CP	
PA07	GPIO.TRACEDATA3	LCD.SEG12	
PA08	LCD.SEG13		
PA09	LCD.SEG20		
PB00	VDAC0.VDAC_CH0_MAIN_OUTPUT	LCD.SEG14	
PB01	GPIO.EM4WU3	VDAC0.VDAC_CH1_MAIN_OUTPUT	LCD.SEG15
PB02	VDAC1.VDAC_CH0_MAIN_OUTPUT	LCD.SEG16	
PB03	GPIO.EM4WU4	VDAC1.VDAC_CH1_MAIN_OUTPUT	LCD.SEG17
PB04	LCD.SEG26		
PB05	LCD.SEG27		
PC00	GPIO.EM4WU6	LCD.SEG0	
PC01	GPIO.EFP_TX_SDA	LCD.SEG1	
PC02	GPIO.EFP_TX_SCL	LCD.SEG2	
PC03	LCD.SEG3		
PC04	LCD.SEG4		
PC05	GPIO.EFP_INT	GPIO.EM4WU7	LCD.SEG5
PC06	LCD.SEG6		
PC07	GPIO.EM4WU8	LCD.SEG7	
PC08	LCD.SEG18		
PC09	GPIO.THMSW_EN	GPIO.THMSW_HALFSWITCH	LCD.SEG19
PD00	LFXO.LFXTAL_O		
PD01	LFXO.LFXTAL_I	LFXO.LF_EXTCLK	
PD02	GPIO.EM4WU9	LCD.COM0	

GPIO	Alternate Functions		
PD03	LCD.COM1		
PD04	LCD.COM2		
PD05	GPIO.EM4WU10	LCD.COM3	

6.3 Analog Peripheral Connectivity

Many analog resources are routable and can be connected to numerous GPIO's. The table below indicates which peripherals are available on each GPIO port. When a differential connection is being used positive inputs are restricted to the EVEN pins and negative inputs are restricted to the ODD pins. When a single ended connection is being used positive input is avaliable on all pins. See the EFR32xG26 Reference Manual for more details on the ABUS and analog peripherals.

Table 6.3. ABUS Routing Table

Peripheral	Signal	PA		PB		PC		PD	
		EVEN	ODD	EVEN	ODD	EVEN	ODD	EVEN	ODD
ACMP0	ANA_NEG	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	ANA_POS	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
ACMP1	ANA_NEG	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	ANA_POS	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
IADC0	ANA_NEG	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	ANA_POS	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
VDAC0	VDAC_CH0_ABUS_OUT-PUT	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	VDAC_CH1_ABUS_OUT	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
VDAC1	VDAC_CH0_ABUS_OUT-PUT	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	VDAC_CH1_ABUS_OUT	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes

6.4 Digital Peripheral Connectivity

Many digital resources are routable and can be connected to numerous GPIO's. The table below indicates which peripherals are available on each GPIO port.

Table 6.4. DBUS Routing Table

Peripheral.Resource	PORT			
	PA	PB	PC	PD
ACMP0.DIGOUT	Available	Available	Available	Available
ACMP1.DIGOUT	Available	Available	Available	Available
CMU.CLKIN0			Available	Available
CMU.CLKOUT0			Available	Available
CMU.CLKOUT1			Available	Available
CMU.CLKOUT2	Available	Available		
CMU.CLKOUTHIDDEN	Available	Available		
EUSART0.CS	Available	Available		
EUSART0.CTS	Available	Available		
EUSART0.RTS	Available	Available		
EUSART0.RX	Available	Available		
EUSART0.SCLK	Available	Available		
EUSART0.TX	Available	Available		
EUSART1.CS	Available	Available	Available	Available
EUSART1.CTS	Available	Available	Available	Available
EUSART1.RTS	Available	Available	Available	Available
EUSART1.RX	Available	Available	Available	Available
EUSART1.SCLK	Available	Available	Available	Available
EUSART1.TX	Available	Available	Available	Available
EUSART2.CS	Available	Available	Available	Available
EUSART2.CTS	Available	Available	Available	Available
EUSART2.RTS	Available	Available	Available	Available
EUSART2.RX	Available	Available	Available	Available
EUSART2.SCLK	Available	Available	Available	Available
EUSART2.TX	Available	Available	Available	Available
EUSART3.CS	Available	Available	Available	Available
EUSART3.CTS	Available	Available	Available	Available
EUSART3.RTS	Available	Available	Available	Available
EUSART3.RX	Available	Available	Available	Available
EUSART3.SCLK	Available	Available	Available	Available
EUSART3.TX	Available	Available	Available	Available

Peripheral.Resource	PORT			
	PA	PB	PC	PD
FRC.DCLK			Available	Available
FRC.DFRAME			Available	Available
FRC.DOUT			Available	Available
HFXO0.BUFOUT_REQ_IN_ASYNC	Available	Available		
I2C0.SCL	Available	Available	Available	Available
I2C0.SDA	Available	Available	Available	Available
I2C1.SCL			Available	Available
I2C1.SDA			Available	Available
I2C2.SCL	Available	Available		
I2C2.SDA	Available	Available		
I2C3.SCL			Available	Available
I2C3.SDA			Available	Available
KEYSCAN.COL_OUT_0	Available	Available	Available	Available
KEYSCAN.COL_OUT_1	Available	Available	Available	Available
KEYSCAN.COL_OUT_2	Available	Available	Available	Available
KEYSCAN.COL_OUT_3	Available	Available	Available	Available
KEYSCAN.COL_OUT_4	Available	Available	Available	Available
KEYSCAN.COL_OUT_5	Available	Available	Available	Available
KEYSCAN.COL_OUT_6	Available	Available	Available	Available
KEYSCAN.COL_OUT_7	Available	Available	Available	Available
KEYSCAN.ROW_SENSE_0	Available	Available		
KEYSCAN.ROW_SENSE_1	Available	Available		
KEYSCAN.ROW_SENSE_2	Available	Available		
KEYSCAN.ROW_SENSE_3	Available	Available		
KEYSCAN.ROW_SENSE_4	Available	Available		
KEYSCAN.ROW_SENSE_5	Available	Available		
LETIMER0.OUT0	Available	Available		
LETIMER0.OUT1	Available	Available		
MODEM.ANT0	Available	Available	Available	Available
MODEM.ANT1	Available	Available	Available	Available
MODEM.ANT_ROLL_OVER			Available	Available
MODEM.ANT_RR0			Available	Available
MODEM.ANT_RR1			Available	Available
MODEM.ANT_RR2			Available	Available
MODEM.ANT_RR3			Available	Available
MODEM.ANT_RR4			Available	Available

Peripheral.Resource	PORT			
	PA	PB	PC	PD
MODEM.ANT_RR5			Available	Available
MODEM.ANT_SW_EN			Available	Available
MODEM.ANT_SW_US			Available	Available
MODEM.ANT_TRIG			Available	Available
MODEM.ANT_TRIG_STOP			Available	Available
MODEM.DCLK	Available	Available		
MODEM.DIN	Available	Available		
MODEM.DOUT	Available	Available		
PCNT0.S0IN	Available	Available		
PCNT0.S1IN	Available	Available		
PRS.ASYNCH0	Available	Available		
PRS.ASYNCH1	Available	Available		
PRS.ASYNCH2	Available	Available		
PRS.ASYNCH3	Available	Available		
PRS.ASYNCH4	Available	Available		
PRS.ASYNCH5	Available	Available		
PRS.ASYNCH6			Available	Available
PRS.ASYNCH7			Available	Available
PRS.ASYNCH8			Available	Available
PRS.ASYNCH9			Available	Available
PRS.ASYNCH10			Available	Available
PRS.ASYNCH11			Available	Available
PRS.ASYNCH12	Available	Available		
PRS.ASYNCH13	Available	Available		
PRS.ASYNCH14	Available	Available		
PRS.ASYNCH15	Available	Available		
PRS.SYNCH0	Available	Available	Available	Available
PRS.SYNCH1	Available	Available	Available	Available
PRS.SYNCH2	Available	Available	Available	Available
PRS.SYNCH3	Available	Available	Available	Available
RAC.LNAEN	Available	Available	Available	Available
RAC.PAEN	Available	Available	Available	Available
TIMER0.CC0	Available	Available	Available	Available
TIMER0.CC1	Available	Available	Available	Available
TIMER0.CC2	Available	Available	Available	Available
TIMER0.CDTI0	Available	Available	Available	Available

Peripheral.Resource	PORT			
	PA	PB	PC	PD
TIMER0.CDTI1	Available	Available	Available	Available
TIMER0.CDTI2	Available	Available	Available	Available
TIMER1.CC0	Available	Available	Available	Available
TIMER1.CC1	Available	Available	Available	Available
TIMER1.CC2	Available	Available	Available	Available
TIMER1.CDTI0	Available	Available	Available	Available
TIMER1.CDTI1	Available	Available	Available	Available
TIMER1.CDTI2	Available	Available	Available	Available
TIMER2.CC0	Available	Available		
TIMER2.CC1	Available	Available		
TIMER2.CC2	Available	Available		
TIMER2.CDTI0	Available	Available		
TIMER2.CDTI1	Available	Available		
TIMER2.CDTI2	Available	Available		
TIMER3.CC0			Available	Available
TIMER3.CC1			Available	Available
TIMER3.CC2			Available	Available
TIMER3.CDTI0			Available	Available
TIMER3.CDTI1			Available	Available
TIMER3.CDTI2			Available	Available
TIMER4.CC0	Available	Available		
TIMER4.CC1	Available	Available		
TIMER4.CC2	Available	Available		
TIMER4.CDTI0	Available	Available		
TIMER4.CDTI1	Available	Available		
TIMER4.CDTI2	Available	Available		
TIMER5.CC0	Available	Available	Available	Available
TIMER5.CC1	Available	Available	Available	Available
TIMER5.CC2	Available	Available	Available	Available
TIMER5.CDTI0	Available	Available	Available	Available
TIMER5.CDTI1	Available	Available	Available	Available
TIMER5.CDTI2	Available	Available	Available	Available
TIMER6.CC0	Available	Available	Available	Available
TIMER6.CC1	Available	Available	Available	Available
TIMER6.CC2	Available	Available	Available	Available
TIMER6.CDTI0	Available	Available	Available	Available

Peripheral.Resource	PORT			
	PA	PB	PC	PD
TIMER6.CDTI1	Available	Available	Available	Available
TIMER6.CDTI2	Available	Available	Available	Available
TIMER7.CC0	Available	Available	Available	Available
TIMER7.CC1	Available	Available	Available	Available
TIMER7.CC2	Available	Available	Available	Available
TIMER7.CDTI0	Available	Available	Available	Available
TIMER7.CDTI1	Available	Available	Available	Available
TIMER7.CDTI2	Available	Available	Available	Available
TIMER8.CC0	Available	Available	Available	Available
TIMER8.CC1	Available	Available	Available	Available
TIMER8.CC2	Available	Available	Available	Available
TIMER8.CDTI0	Available	Available	Available	Available
TIMER8.CDTI1	Available	Available	Available	Available
TIMER8.CDTI2	Available	Available	Available	Available
TIMER9.CC0	Available	Available	Available	Available
TIMER9.CC1	Available	Available	Available	Available
TIMER9.CC2	Available	Available	Available	Available
TIMER9.CDTI0	Available	Available	Available	Available
TIMER9.CDTI1	Available	Available	Available	Available
TIMER9.CDTI2	Available	Available	Available	Available
USART0.CLK	Available	Available	Available	Available
USART0.CS	Available	Available	Available	Available
USART0.CTS	Available	Available	Available	Available
USART0.RTS	Available	Available	Available	Available
USART0.RX	Available	Available	Available	Available
USART0.TX	Available	Available	Available	Available
USART1.CLK	Available	Available	Available	Available
USART1.CS	Available	Available	Available	Available
USART1.CTS	Available	Available	Available	Available
USART1.RTS	Available	Available	Available	Available
USART1.RX	Available	Available	Available	Available
USART1.TX	Available	Available	Available	Available
USART2.CLK	Available	Available	Available	Available
USART2.CS	Available	Available	Available	Available
USART2.CTS	Available	Available	Available	Available
USART2.RTS	Available	Available	Available	Available

Peripheral.Resource	PORT			
	PA	PB	PC	PD
USART2.RX	Available	Available	Available	Available
USART2.TX	Available	Available	Available	Available

7. Design Guidelines

7.1 Layout and Placement

For optimal performance of the BGM260P,

- Place the module aligned with the center of an edge of the application PCB, as illustrated in the figures below.
- Leave the antenna clearance area void of any traces, components, or copper on all layers of the application PCB.
- Connect all ground pads directly to a solid ground plane.
- Place the ground vias as close to the ground pads as possible.
- Avoid plastic or any other dielectric material in contact with the antenna.
- The outer row footprint is backward compatible with BGM240P module footprint, and the inner row pins are optional.

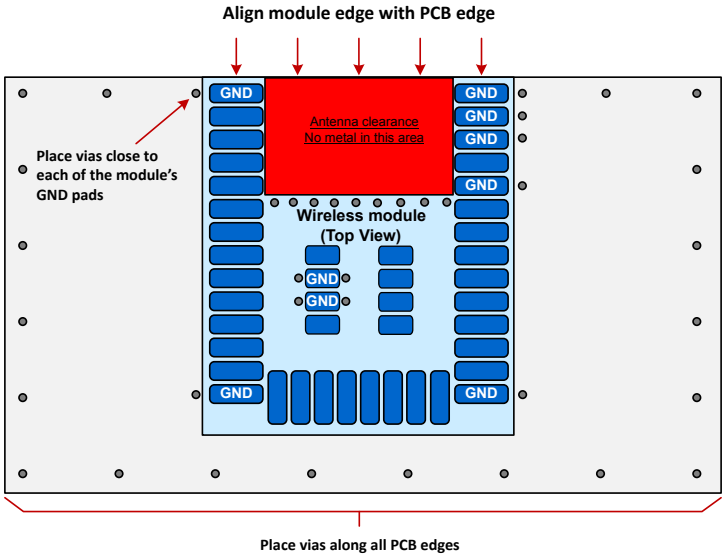


Figure 7.1. Recommended Layout for BGM260P Using Built-in Antenna

The figure below illustrates layout scenarios that will lead to severely degraded RF performance for the module with integrated antenna.

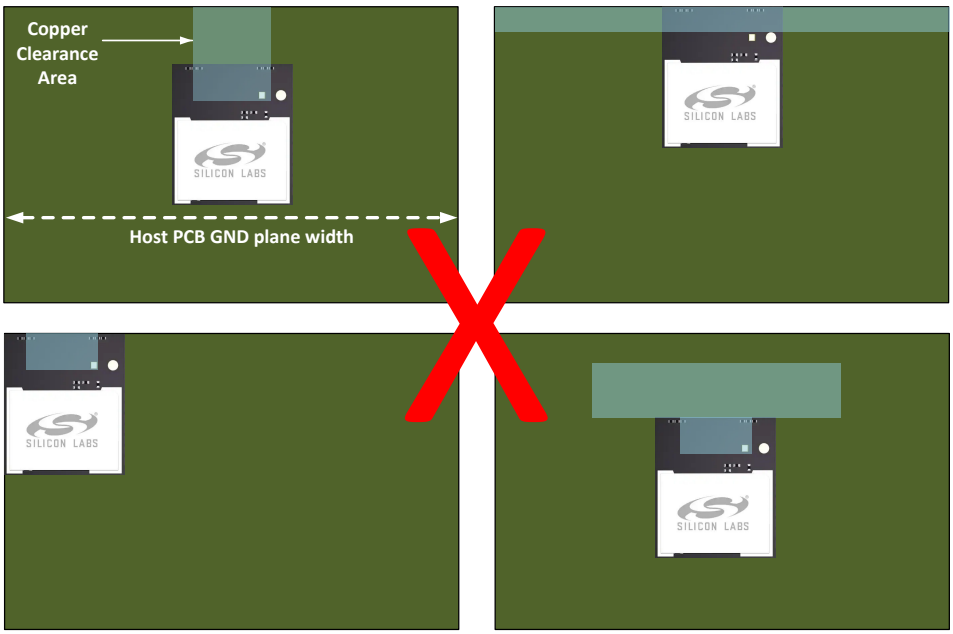


Figure 7.2. Non-Optimal Layout Examples

The width of the GND plane to the sides of the module will impact the efficiency of the built-in antenna. To achieve optimal performance, a total GND plane width of 50 - 60 mm is recommended. Narrower or wider ground planes can be used but will result in compromised RF performance. See 4.18 Antenna Radiation and Efficiency for reference.

7.2 Proximity to Other Materials

Avoid placing plastic or any other dielectric material in close proximity to the antenna, as this is likely to cause RF performance degradation. Solder mask, conformal coating, and/or other thin dielectric layers are acceptable directly on top of the antenna region, however these might also negatively impact antenna efficiency and reduce range.

Any metallic object in close proximity to the antenna will prevent the antenna from radiating freely. The minimum recommended distance of metallic and/or conductive objects is 10 mm in any direction from the antenna except in the directions of the application PCB ground planes.

7.3 Proximity to Human Body

Placing the module in contact with, or very close to the human body will negatively impact antenna efficiency and reduce range. Furthermore, additional certification work may be required if the module is integrated in a wearable device: please refer to chapter 11.7 RF Exposure and Proximity to Human Body.

7.4 Reset

The Reset Management Unit (RMU) is responsible for handling reset of the BGM260P. A wide range of reset sources are available, including several power supply monitors, pin reset, software controlled reset, core lockup reset, and watchdog reset.

The reset state does not provide power saving functionality and it is not recommended as a means to conserve power.

7.5 Debug

See AN958: Debugging and Programming Interfaces for Custom Designs.

The BGM260P supports hardware debugging via 4-pin JTAG or 2-pin serial-wire debug (SWD) interfaces. It is recommended to expose the debug pins in your own hardware design for firmware update and debug purposes. The table below lists the required pins for JTAG and SWD debug interfacing, which are also presented in Section 6.2 Alternate Pin Functions.

If JTAG interfacing is enabled, the module must be power cycled to return to a SWD debug configuration if necessary.

Table 7.1. Debug Pins

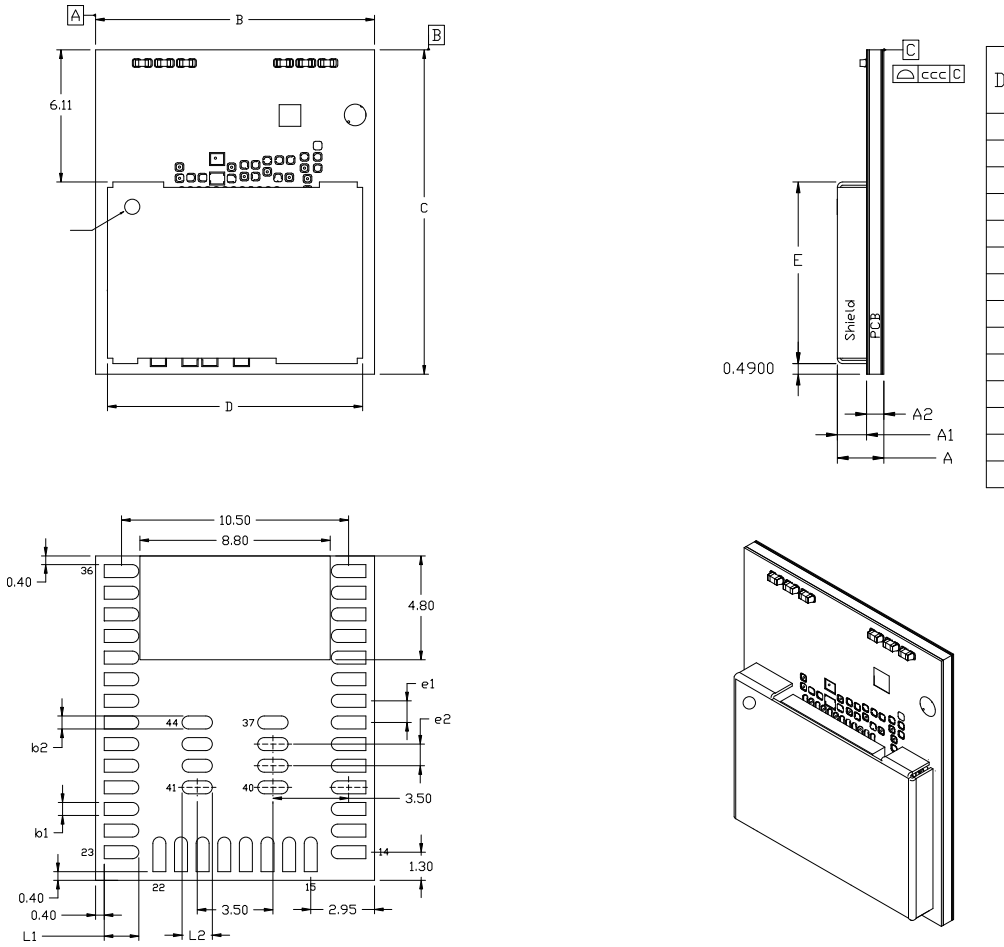
Pin Name	JTAG Signal	SWD Signal	Comments
PA04	TDI	N/A	This pin is disabled after reset. Once enabled the pin has a built-in pull-up.
PA03	TDO	N/A	This pin is disabled after reset.
PA02	TMS	SWDIO	Pin is enabled after reset and has a built-in pull-up.
PA01	TCK	SWCLK	Pin is enabled after reset and has a built-in pull-down.

7.6 Packet Trace Interface (PTI)

The BGM260P integrates a true PHY-level packet trace interface (PTI) peripheral that can capture packets non-intrusively to monitor and log device and network traffic without burdening processing resources in the module's SoC. The PTI generates two output signals that can serve as a powerful debugging tool, especially in conjunction with other hardware and software development tools available from Silicon Labs. The PTI_DATA and PTI_FRAME signals can be accessed through any GPIO on ports C and D (see FRC.DOUT and FRC.DFRAME peripheral resources in 6. Pin Definitions).

8. Package Specifications

8.1 Package Outline



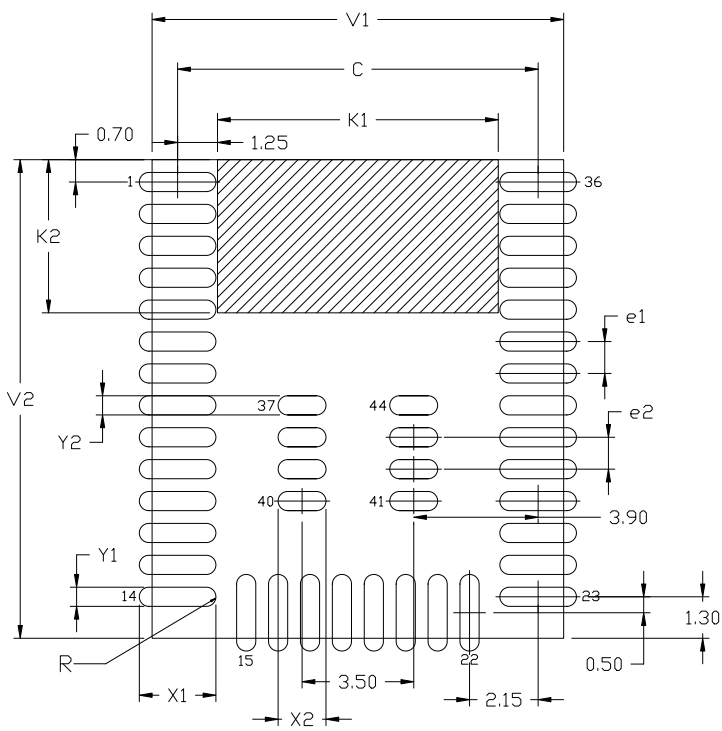
Dimension	MIN	NOM	MAX
A	1.950	2.150	2.350
A1	1.250	1.350	1.450
A2	0.700	0.800	0.900
B	12.700	12.900	13.100
C	14.800	15.000	15.200
D	11.700	11.800	11.900
E	8.300	8.400	8.500
e1		1.00 BSC	
e2		1.00 BSC	
L1	1.500	1.600	1.700
L2	1.300	1.400	1.500
b1	0.500	0.600	0.700
b2	0.500	0.600	0.700
ccc	--	--	0.100

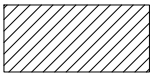
Figure 8.1. Package Outline

Note:

1. All dimensions are in mm.
2. All dimensions are measured after singulation.
3. Solder paste thickness is expected to contribute to the overall package height but must be within the specified tolerance.
4. No burrs or sharp edges are allowed.

8.2 PCB Land Pattern





Antenna keep out zone

Dimension	mm
V1	12.90
V2	15.00
K1	8.80
K2	4.80
C	11.30
e1	1.00
e2	1.00
X1	2.40
X2	1.50
Y1	0.60
Y2	0.60
R	0.30

Figure 8.2. Recommended Land Pattern for Modules with a Built-in Antenna

Note:

1. All dimensions are in mm.
2. Refer to the technical documentation of the specific solder paste for profile configuration.
3. Avoid using more than two reflow cycles.
4. A no-clean, type-3 solder paste is recommended.
5. A stainless steel, laser-cut, and electro-polished stencil with trapezoidal walls should be used to ensure good solder paste release.
6. The recommended stencil thickness is 0.100 mm (4 mils).
7. For further recommendations, refer to the JEDEC J-STD-020, IPC-SM-782, and IPC-7351 guidelines.
8. The outer row footprint is backward compatible with BGM240P module footprint, and the inner row pins are optional.

8.3 Package Marking

The figure below shows the module markings engraved on the RF shield.

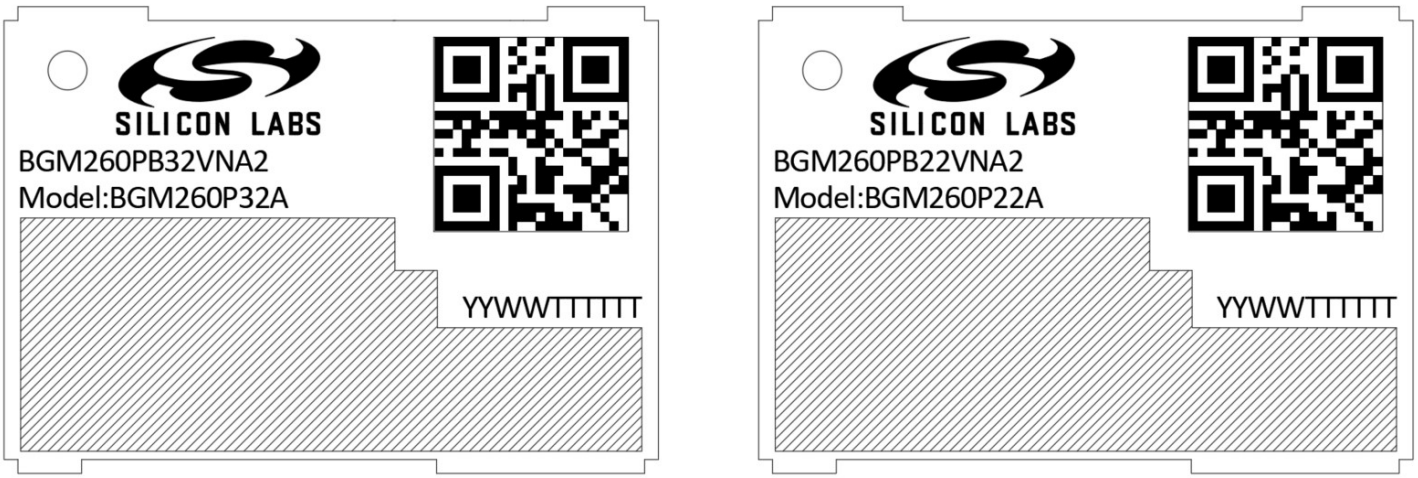


Figure 8.3. BGM260P Top Marking

Mark Description

The package marking consists of:

- BGM260Pxxxxxxx - Orderable Part Number designation
- Model: BGM260Pxxx - Model Number designation
- QR Code: YYWWMMABCDE
  - YY – Last two digits of the assembly year
  - WW – Two-digit workweek when the device was assembled
  - MMABCDE – Silicon Labs unit code
- YYWWTTTTTT
  - YY – Last two digits of the assembly year
  - WW – Two-digit workweek when the device was assembled
  - TTTTTT – Manufacturing trace code. The first letter is the device revision
- All certification-related information (such as the CE compliance mark, or the FCC and IC IDs, etc.) is being engraved on the hatched-out area, in accordance with the requirements by regional regulatory bodies.

9. Soldering Recommendations

It is recommended that final PCB assembly of the BGM260P follows the industry standard as identified by the Institute for Printed Circuits (IPC). This product is assembled in compliance with the J-STD-001 requirements and the guidelines of IPC-AJ-820. Surface mounting of this product by the end user is recommended to follow IPC-A-610 to meet or exceed class 2 requirements.

CLASS 1 General Electronic Products

Includes products suitable for applications where the major requirement is function of the completed assembly.

CLASS 2 Dedicated Service Electronic Products

Includes products where continued performance and extended life is required, and for which uninterrupted service is desired but not critical. Typically the end-use environment would not cause failures.

CLASS 3 High Performance/Harsh Environment Electronic Products

Includes products where continued high performance or performance-on-demand is critical, equipment downtime cannot be tolerated, end-use environment may be uncommonly harsh, and the equipment must function when required, such as life support or other critical systems.

Note: General SMT application notes are provided in the AN1223: LGA Manufacturing Guidance.

10. Tape and Reel

BGM260P modules are delivered to the customer in cut tape (100 pcs) or reel (1000 pcs) packaging having the dimensions below. All dimensions are given in mm unless otherwise indicated.

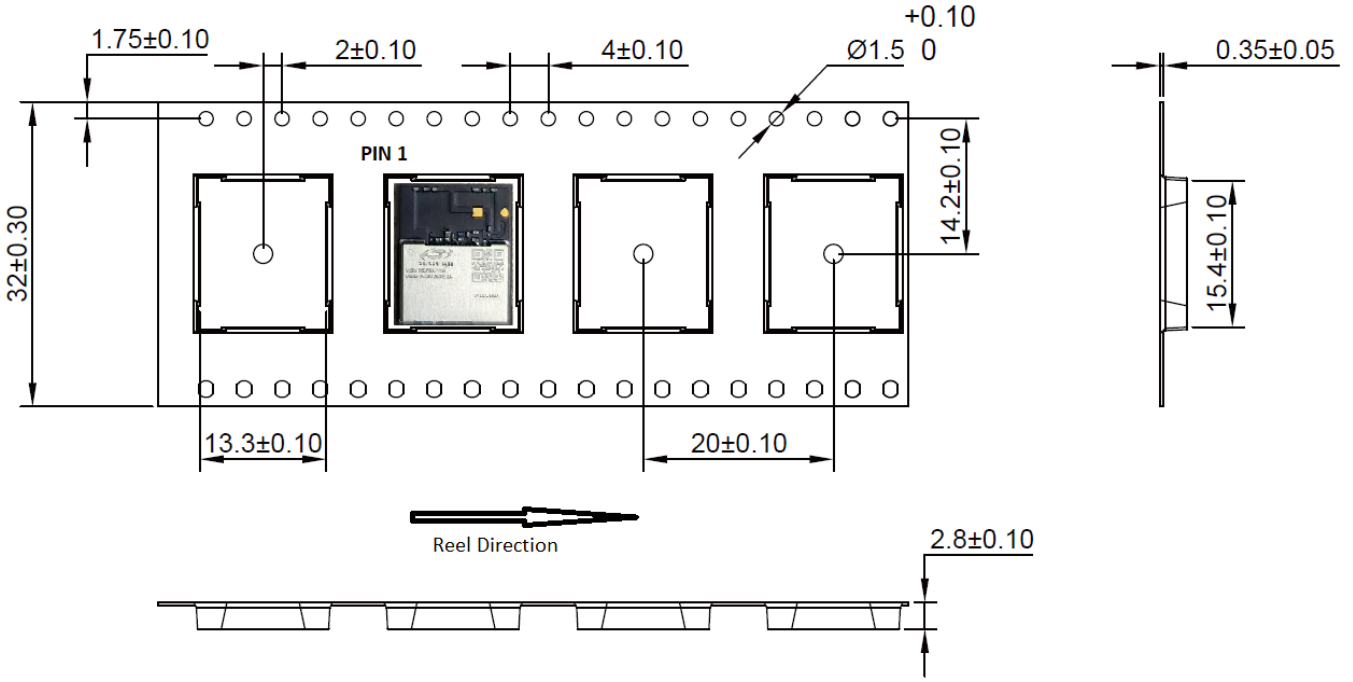


Figure 10.1. Carrier Tape Dimensions

Figure 10.1. Carrier Tape Dimensions

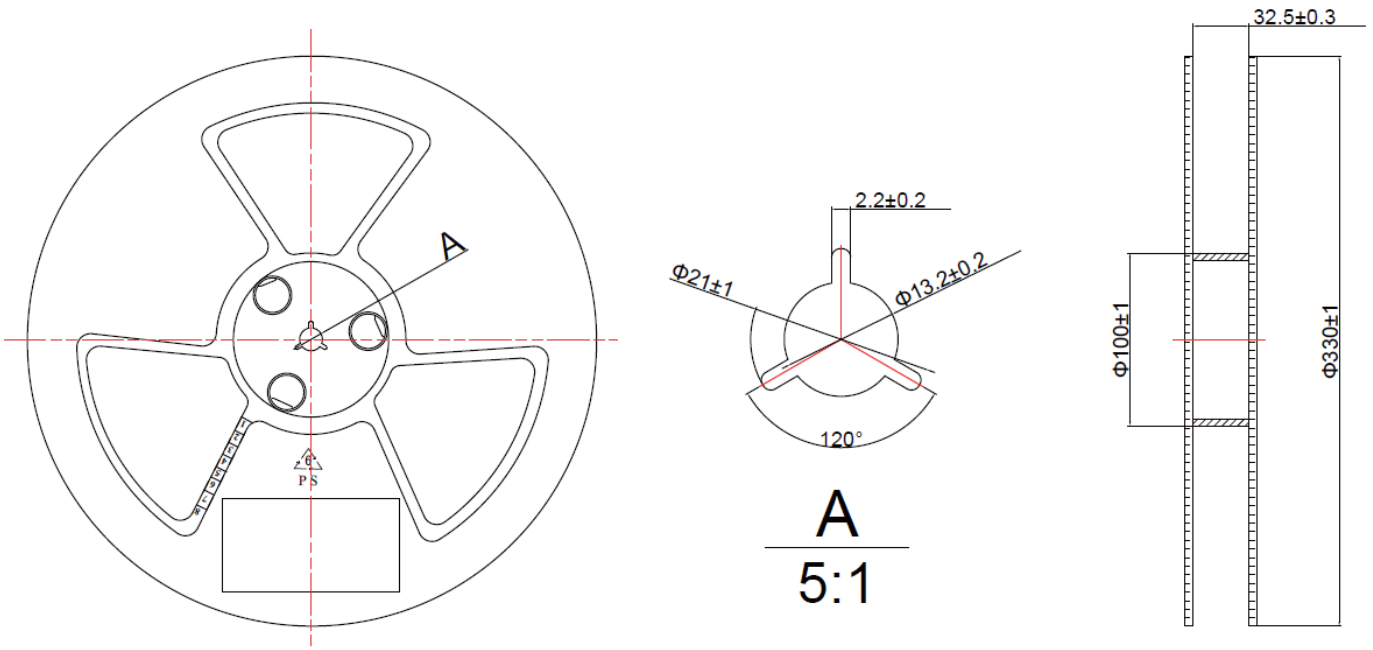


Figure 10.2. Reel Dimensions

11. Certifications

This section details the certification status of the modules with regards to regional regulatory radio approvals. Where applicable, the status with the qualifications against the specifications of the supported global industrial wireless standards is given too.

The address of the module manufacturer (technology owner) and certification applicant/holder is:

SILICON LABS / SILICON LABORATORIES FINLAND OY
Alberga Business Park, Bertel Jungin aukio 3,
02600 Espoo, Finland

The BGM260P modules have brand name of "SILICON LABS". For certifications and qualifications purposes, the modules are referred to by their formal Model Name(s) of BGM260P22A and BGM260P32A.

"SILICON LABS" (and "Silicon Labs") is a trademark globally owned by the Silicon Laboratories Inc. corporation, and all branches and subsidiaries, including the above applicant, holds the right to use it.

For any clarification on regulatory certifications, or if you need to discuss topics such as Permissive Changes or Change in ID requests, please contact your Sales Representative or our Technical Support. You can get started by visiting Contact Us.

11.1 CE and UKCA - EU and UK

The BGM260P modules have been tested against the relevant harmonized/designated standards and are in conformity with the essential requirements and other relevant requirements of the EU's Radio Equipment Directive (RED) (2014/53/EU) and of the UK's Radio Equipment Regulations (RER) (S.I. 2017/1206).

Table 11.1. Operating Frequencies and Maximum Transmitted Power per the EN 300 328 RF test report

Model name	Operating Frequencies	Maximum EIRP BLE
BGM260P22A	2402 - 2480 MHz (BLE)	12.94 dBm
BGM260P32A	2405 - 2480 MHz (15.4)	19.75 dBm

Please notice that every end-product integrating a BGM260P module will need to perform the radio EMC tests on the whole assembly, according to the ETSI 301 489-x relevant standards.

Furthermore, it is ultimately the responsibility of the manufacturers to ensure the compliance of their end-products as a whole. The specific product assembly is likely to have an impact to RF radiated characteristics, when compared to the bare module. Hence, manufacturers should carefully consider RF radiated testing with the final product assembly, and the possible deviations in the PSD, EIRP and spurious emissions measurements, as defined in the ETSI EN 300 328 standard.

The modules are entitled to carry the CE and UKCA compliance marks, and the respective formal Declarations of Conformity (DoC) are available at the product web page which is reachable starting from https://www.silabs.com/.

Each OEM must also consider applying the compliance marks to a visible location on their end-products. In general, module customers assume full responsibility with regards to learning the guidelines and meeting the requirements for the compliance in each member country where their end-products are marketed.

11.2 FCC - USA

This device complies with FCC's e-CFR Title 47, Part 15, Subpart C, Section 15.247 (and related relevant parts of the ANSI C63.10 standard) when operating with the built-in integral antenna.

Operation is subject to the following two conditions:

1. This device may not cause harmful interference, and
2. This device must accept any interference received, including interference that may cause undesirable operation.

Any changes or modifications not expressly approved by Silicon Labs could void the user's authority to operate the equipment.

FCC RF Radiation Exposure Statement

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. End users must follow the specific operating instructions for satisfying RF exposure compliance.

This transmitter meets the Mobile requirements at a distance of 20 cm and above from the human body, in accordance with the evaluation exposed in the RF Exposure test report(s). This transmitter also meets the Portable requirements at distances equal or above 11.6 mm for the BGM260P22A and 35.1 mm for the BGM260P32A in the case of Bluetooth Low Energy. These distances are reported for convenience also in Table 11.2 Minimum Separation Distances for SAR Evaluation Exemption on page 72.

This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter except in accordance with FCC multi-transmitter product procedures.

OEM Responsibilities to comply with FCC Regulations

This module has been tested for compliance to FCC Part 15.

OEM integrators are responsible for testing their end-product for any additional compliance requirements needed with this module installed (for example, digital device emissions, PC peripheral requirements, etc.).

Additionally, investigative measurements and spot-check testing (with all transmitters active, if other co-located radios than the module itself exist on the host), are strongly recommended in order to verify that the full system's compliance is maintained when the module is integrated, even with the module having a full modular approval, in accordance with the "Host Product Testing Guidance" in FCC's KDB 996369 D04 Module Integration Guide.

- **General Considerations**

  This transmitter module is tested as a subsystem and its certification does not cover the FCC Part 15 Subpart B (unintentional radiator) rule requirement, which is typically applicable to the final host. The final host will still need to be assessed for compliance to this portion of the rule requirements, if applicable.

- **Manual Information to the End User**

  The OEM integrator has to be aware not to provide information to the end-user regarding how to install or remove this RF module, or how to change RF related parameters, in the user's manual of the final product which integrates this module.

  The end-user manual shall include all required regulatory information/warnings as shown in this manual.

- **Host Manufacturer Responsibilities**

  A host manufacturer is ultimately responsible for the full compliance of their host system. The final product is supposed to be assessed against all the essential requirements of the FCC rules, such as FCC Part 15 Subpart B, before it can be placed on the US market. This includes re-assuring the compliance of the radio transmitter with the RF and EMF essential requirements of the FCC rules. The modular radio transmitter must not be incorporated into any other radio-equipped device or system without retesting for compliance as multi-radio and combined equipment.

  For more details about integrating the Single Modular Transmitter, refer to the following FCC document:

  • KDB 996369 D04 Module Integration Guide

  For understanding better the process leading to obtaining a Full Modular Approval, see the following documents instead:

  • KDB 996369 D01 Transmitter Module Equipment Authorization Guide

  • KDB 996369 D02 Frequently Asked Questions and Answers about Modules

  The two documents above give an insight of the FCC requirements from the module manufacturer's perspective, and will help to realize the need by the integrators to follow the integration instructions and design guidance, and to take into account for example the RF Exposure limitations, if any. Should a deviation occur, keep in mind the possible need to work with the manufacturer in order to proceed with a permissive change (following a *Change in ID*), in accordance with the FCC guidelines found in the following documents:

  • KDB 178919 D01 Permissive Change Policy

  • KDB 178919 D02 Permissive Change Frequently-Asked Questions

Separation

- To meet the SAR exemption for portable conditions, the minimum separation distance indicated in must be maintained between the human body and the radiator (antenna) at all times. In particular, in the use case of Bluetooth Low Energy the minimum distance must be 11.6 mm for the BGM260P22A and 35.1 mm for the BGM260P32A.
- This transmitter module is tested in a standalone RF Exposure condition, and in case of any co-located radio transmitter being allowed to transmit simultaneously, or in case of portable use at closer distances from the human body than those allowing the exceptions rules to be applied, a separate additional SAR evaluation, or a reduction in the max output power or in the duty-cycle, might be required for the host, ultimately leading to a Class II Permissive Change, or more rarely to a new grant.
- **Important Note:** In the event that the conditions for the exemption cannot be met, the final product will likely have to undergo additional testing to evaluate the RF Exposure, or go through some re-configuration of the max output power and/or duty-cycle in order for the FCC authorization to remain valid, and a permissive change will have to be applied. The SAR evaluation (and/or reconfiguration) is in the responsibility of the end-product's manufacturer, as well as the permissive change that can be carried out with the help of the customer's own Telecommunication Certification Body, following a Change in ID authorization by the module's original grant holder.

End Product Labeling

BGM260P modules are labeled with their own FCC ID. In all those cases when the FCC ID is not visible after the module is installed inside another device, then the outside of the device into which the module is installed must also display a label referring to the enclosed module. In that case, the final product must be labeled in a visible area with the following:

"Contains Transmitter Module FCC ID: QOQ-GM260P"

or

"Contains FCC ID: QOQ-GM260P"

Final note: As long as all the conditions in this and all the above chapters are met, further RF testing of the transmitter will not be strictly required. However, still consider the good practice and the FCC strong recommendation to ensure the compliance of the host by spot-checking. Nevertheless, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements which might be mandatory with this module installed.

Class B Device Notice

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna
- Increase the separation between the equipment and receiver
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected
- Consult the dealer or an experienced radio/TV technician for help

11.3 ISED - Canada

This radio transmitter (with IC: 5123A-GM260P) has been approved by *Innovation, Science and Economic Development Canada (ISED Canada, formerly Industry Canada*) to operate with the built-in integral antenna.

This radio-equipped device complies with ISED's license-exempt RSS standards. Operation is subject to the following two conditions:

1. This device may not cause interference; and
2. This device must accept any interference, including interference that may cause undesired operation of the device

RF Exposure Statement

Exception from routine SAR evaluation limits are given in RSS-102 Issue 6.

The module meets the requirements for Mobile use cases when the minimum separation distance from the human body is 20 cm or greater, in accordance with the evaluation exposed in the RF Exposure test report(s).

For Portable use cases, RF exposure or SAR evaluation is not required when the separation distances from the human body are equal or above 16.9 mm for the BGM260P22A and 41.9 mm for the BGM260P32A in the case of Bluetooth Low Energy.

If the separation distance from the human body is less than the values stated above, which are also reported in for convenience, then the OEM integrator is responsible for evaluating the SAR with the end-product, or for the re-configuration of the radio module in the host in terms of lowering the max RF TX power and/or the duty-cycle. A permissive change would be required too, under the responsibility of the host manufacturer, following a Multiple Listing authorization by the original module's certificate holder.

OEM Responsibilities to comply with IC Regulations

The BGM260P modules have been certified for integration into products only by OEM integrators, under the following conditions:

- The module must be installed in such a way that the intended minimum separation distances are maintained between the radiator (antenna) and all persons at all times. Table 11.2 indicates these distances in accordance to the use cases.
- The transmitter module must not be co-located or operating in conjunction with any other antenna or transmitter.

Important Note: In the event that the above conditions cannot be met, the final product will have to undergo additional testing to evaluate the RF Exposure, or go through some re-configuration of the max output power and/or duty-cycle in order for the ISED authorization to remain valid - a permissive change will have to be applied too**.** The RF Exposure evaluation (SAR, or possibly a re-configuration) is in the responsibility of the end-product's manufacturer, as well as the permissive change that can be carried out with the help of the customer's own Certification Body, following a Multiple Listing authorization by the module's original grant holder.

End Product Labeling

The BGM260P modules are labeled with their own IC ID. In all those cases when the module's own label is not visible after a module is installed inside another device, then the outside of the device into which the module is installed must also display a label referring to the enclosed module. In that case, the final product must be labeled in a visible area with the following:

“**Contains Transmitter Module IC: 5123A-GM260P** ”

or

“**Contains IC: 5123A-GM260P”**

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module or change RF related parameters in the user manual of the end-product.

As long as all the conditions above are met, further transmitter testing will not be required. However, the OEM integrator is still responsible for testing their end-product for the fulfillment of any additional compliance requirements required with this module installed (for example, digital device emissions, PC peripheral requirements, etc.).

CAN ICES-003 (B)

This Class B digital apparatus complies with Canadian ICES-003.

ISED (Français)

Le présent émetteur radio (IC: 5123A-GM260P) a été approuvé par Innovation, Sciences et Développement Économique Canada (ISED Canada, anciennement Industrie Canada) pour fonctionner avec l'antenne intégrée.

L'émetteur/récepteur exempt de licence contenu dans le présent appareil est conforme aux CNR d'Innovation, Sciences et Développement économique Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes:

1. L'appareil ne doit pas produire de brouillage;
2. L'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptibled'en compromettre le fonctionnement.

Déclaration d'exposition RF

L'exception tirée des limites courantes d'évaluation SAR est donnée dans le document RSS-102 Issue 6.

Le module répond aux exigences pour les cas d'utilisation Mobile lorsque la distance minimale de séparation du corps humain est de 20 cm ou plus, conformément à la (aux) limite(s) exposée(s) dans l'analyse de l'exposition RF.

Pour les cas d'utilisation Portables, l'exposition aux fréquences radio ou l'évaluation du SAR n'est pas nécessaire lorsque les distances de séparation du corps humain sont égales ou supérieures à 16.9 mm pour le BGM260P22A et à 41.9 mm pour le BGM260P32A dans le cas de Bluetooth Low Energy.

Si la distance de séparation du corps humain est inférieure aux valeurs indiquées ci-dessus, également indiquées dans le tableau 11.2 pour des raisons de commodité, l'intégrateur OEM est responsable de l'évaluation du SAR avec le produit final, ou de la reconfiguration du module radio dans l'hôte en termes de réduction de la puissance RF TX maximale et/ou du rapport cyclique. Une modification permissive serait également nécessaire, sous la responsabilité du fabricant de l'hôte, suite à une autorisation de cotation multiple par le titulaire du certificat du module d'origine.

Responsabilités du fabricant de se conformer à la réglementation IC

Le module a été certifié pour l'intégration dans les produits uniquement par les intégrateurs OEM dans les conditions suivantes:

- L'antenne doit être installée de manière à maintenir une distance de séparation minimale, comme indiqué ci-dessus, entre le radiateur (antenne) et toutes les personnes.
- Le module émetteur ne doit pas être localisé ou fonctionner conjointement avec une autre antenne ou un autre émetteur.

Remarque Importante: au cas où ces conditions ne pourraient pas être remplies, le produit final devra être soumis à des tests supplémentaires pour évaluer l'exposition RF, ou passer par une reconfiguration de la puissance de sortie maximale et/ou du rapport cyclique, afin que l'autorisation ISED reste valable; une modification permissive devra également être appliqué. L'évaluation de l'exposition aux radiofréquences (SAR, ou éventuellement une reconfiguration) est sous la responsabilité du fabricant du produit final, ainsi que le changement permissif qui peut être effectué avec l'aide de l'organisme de certification des télécommunications du client, après autorisation de cotation multiple par le titulaire de la certification du module.

Étiquetage des produits finis

Les modules BGM260P est étiqueté avec son propre ID de certification.Si l'ID de certification n'est pas visible lorsque le module est installé dans un autre appareil, l'extérieur de l'appareil dans lequel le module est installé doit également afficher une étiquette faisant référence au module inclus. Dans ce cas, le produit final doit être étiqueté dans une zone visible avec les éléments suivants:

"**Contient le module transmetteur IC: 5123A-GM260P** "

ou

"**Contient IC: 5123A-GM260P"**

L'intégrateur OEM doit être conscient de ne pas fournir à l'utilisateur final d'informations sur la procédure d'installation ou de retrait de ce module RF ni sur la modification des paramètres liés à la RF dans le manuel d'utilisation du produit final.

Tant que toutes les conditions ci-dessus sont remplies, aucun test supplémentaire de l'émetteur ne sera nécessaire. Toutefois, l'intégrateur OEM reste responsable de l'essai de son produit final pour déterminer les exigences de conformité supplémentaires requises avec ce module installé (par exemple, émissions d'appareils numériques, exigences relatives aux périphériques PC, etc.)

CAN ICES-003 (B)

Cet appareil numérique de classe B est conforme à la norme canadienne ICES-003.

11.4 MIC - Japan

The BGM260P modules are certified in Japan with following certification numbers:

- Low-power (+10 dBm) parts with model name BGM260P22A: 020-240374
- High-power (+19.5 dBm) parts with model name BGM260P32A: 020-240376

While the module manufacturer takes all reasonable steps to prevent non-compliant operation, it is still the end-product manufacturer's responsibility to ensure that a module is configured to meet the compliance requirements, for example in relation to the maximum allowed RF TX power. When applicable, refer to the SDK documentation and/or API reference manuals and/or integration and certification guides, to learn how to configure (limit) the maximum RF TX power for ensuring the compliance of the end-product during regular operation, if need be. Refer as well to the power setting table(s) and measurements in the test report(s) in order to realize the maximum output power levels allowed for the regulatory compliance in Japan, especially with the high-power variant(s).

Manufacturers integrating a radio module into their host equipment are supposed to make the certification mark and the certification number visible on the outside of the host equipment. This combination of mark and number, and their relative placement, is depicted in Figure 11.1, and depending on the overall size it might also appear among the top shield markings of the radio module. The compliance mark and certification number must be placed close to the text in the Japanese language which is provided below. This requirement in the Radio Law has been made in order to enable users of the combination of host and radio module to verify if they are actually using a radio device which is approved for use in Japan.

Certification Text to be Placed on the Outside Surface of the Host Equipment:

当該機器には電波法に基づく、技術基準適合証明等を受けた特定無線設備を装着している。

Translation of the text:

“This equipment contains specified radio equipment that has been certified to the Technical Regulation Conformity Certification under the Radio Law.”

The "Giteki" Mark shown in the following figures must be affixed to an easily noticeable section of the specified radio-enabled host equipment. Note that such section may be required to contain additional information if the end-device embedding the module is also subject to a Telecom approval.

The manufacturer of the final product is also responsible to provide a Japanese language version of the User Manual and/or Installation Instructions as a companion document coming with the final product when placed on the market in Japan. Such a document will have to mention the integrated radio component and the related certification information.

Figure 11.1. Example of GITEKI Mark with placeholder for actual Certification Number

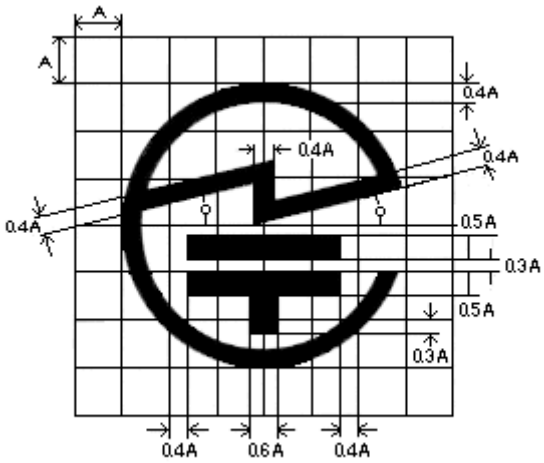


Figure 11.2. Detail of the GITEKI Compliance Mark

11.5 KC - South Korea

The low-power variant of the BGM260P modules, with model name BGM260P22A, has a RF registration for import and use in South Korea.

Registration number is R-R-BGT-GM260P.

These modules are meant to be integrated into end-products, which then become exempted from doing the RF emission testing, as long as the recommended design guidance is followed, and as long as, where applicable, any additional transmit power back-off is implemented in accordance with the measurements and configurations seen in the formal test report(s).

EMC testing and any other relevant test applicable to the end-product as a whole, plus appropriate labeling of the end-product, might still be required for the full regulatory compliance in the country.

11.6 NCC - Taiwan

The BGM260P modules are certified in Taiwan with NCC certification number as follows:

BGM260P 系列模組已取得台灣認證，NCC 認證號碼如下：

BGM260P22A: CCAI25Y1005AT0

BGM260P32A: CCAI25Y1006AT0

Manufacturers are required to mark their end-products with the following sentence: *"This product contains a radio frequency module with certification number CCAI25Y100x0Tx"*, where CCAI25Y100x0Tx corresponds to the above-listed certification number of the embedded module.

系統製造商應在平台上放置以下聲明： *“本產品包含認證編號為 CCAI25Y100x0Tx 的無線電模組”*，其中 CCAI25Y100x0Tx 對應於上面列出的嵌入式模組的認證編號。

Note: The outer packaging of the final product must also be marked with the NCC conformity mark by the manufacturer

注意：最終產品的外包裝也必須由製造商打上 NCC 合格標誌。

Additionally, the final product will have to be listed in the NCC database of approved radio-equipped devices. Consequently, the end manufacturer is also supposed to contact a certification body or the certification house that originally released the modular approval and apply for the registration of their platform under the applicable certification number above. Fees might apply, and an authorization by the module manufacturer might be required too.

此外，最終產品必須列入 NCC 的核准無線電設備資料庫中。因此，最終製造商也應聯繫最初協助頒發模組化核准的認證機構或認證公司，並申請在上述適用的認證編號下註冊其平台。可能需要列出費用和模組製造商的授權。

NCC Statement
- For low-power radio frequency equipment that has been certified, companies, firms, or users are not allowed to change the frequency, increase the power, or change the characteristics and functions of the original design without further NCC approval.
- The use of low-power radio frequency equipment shall not affect flight safety and interfere with legal communications.
- If interference is found, it shall be immediately stopped, and the equipment can be brought back into use only after it has been improved, so that interference is found no more.
- The aforementioned legal communication refers to radio communications operating in accordance with the provisions of the Telecommunications Management Act.
- Low-power radio frequency equipment must withstand interference from legitimate communications or radiating electrical equipment for industrial, scientific, and medical applications.

NCC 警語
取得審驗證明之低功率射頻器材，非經核准，公司、商號或使用者均不得擅自變更頻率、加大功率或變更原設計之特性及功能。 低功率射頻器材之使用不得影響飛航安全及干擾合法通信。 經發現有干擾現象時，應立即停用，並改善至無干擾時方得繼續使用。 前述合法通信，指依電信管理法規定作業之無線電通信。 低功率射頻器材須忍受合法通信或工業、科學及醫療用電波輻射性電機設備之干擾。

11.7 RF Exposure and Proximity to Human Body

When using the BGM260P modules in an application where the radio-equipped end-product is located close to the human body, the human RF Exposure must be taken into account. FCC, ISED, and CE/UKCA all have different standards and rules for evaluating the RF Exposure. In particular, each regulator has different requirements when it comes to the exemption from having to perform RF Exposure and SAR (Specific Absorption Rate) measurements, and the minimum separation distances between the module's antenna and the human body varies accordingly. The properties of the BGM260P modules allow for the minimum separation distances detailed below in Table 11.2 Minimum Separation Distances for SAR Evaluation Exemption on page 72 for the SAR measurement exemption in Portable use cases (less than 20 cm from human body). These modules are approved for the Mobile use case (more than 20 cm) without any need for RF Exposure evaluation.

Table 11.2. Minimum Separation Distances for SAR Evaluation Exemption

Certification	BGM260P22A	BGM260P32A
FCC	Bluetooth: 11.6 mm	Bluetooth: 35.1 mm
ISED	Bluetooth: 16.9 mm	Bluetooth: 41.9 mm
CE	In general, the RF exposure should always be evaluated with the end-product when transmitting with EIRP power levels higher than 20 mW (13 dBm) while operating at distances closer than 20 cm from the human body.	

The exemption distances above, calculated for reference in the full output power use case, are based on the rules in force at the time of writing this data sheet. Even though changes happen rarely, always ensure to apply the rules in force at the time of placing the end-product into the market.

In the cases of FCC and ISED, it is allowed to use a module at its max RF TX power in an end-product where the typical separation distance from the human body is smaller than mentioned above, but it requires evaluating the RF Exposure in the final assembly and applying for a Class 2 Permissive Change to the FCC and ISED approvals of the module. In order to proceed with any permissive change, first the module manufacturer should be asked for an authorization to do an FCC's Change in ID and/or an ISED's Multiple Listing; then, the new Portable condition will be added to the new parallel FCC grant and/or ISED certificate owned by the end-product manufacturer, for extending the approvals to their unique host under their unique configuration and mode of use.

For those end-products where the embedded module supporting multiple wireless protocols is configured to implement only a single one of them, which would allow for the exemption at a shorter distance than the overall minimum distance, there would be no need to the evaluate the RF Exposure at such a shorter distance and above. However, a permissive change would still be needed as a mean to notify the FCC / ISED of the reason why in the field the module is allowed to operate at a shorter distance than in the table above.

An example of another use case where the module could operate at a shorter distance than in the table above, without having to do the RF Exposure evaluation / SAR measurement, is when the power or the duty-cycle is reduced during normal operation. However, the new minimum distance for the exemption should be re-calculated, and still a permissive change would be needed to notify the regulators of the new conditions.

For the CE/UKCA compliance, RF Exposure must be considered and evaluated by the OEM in all cases when the end-product is transmitting at higher power level than indicated in the table above.

Note: Placing the module in touch or very close to the human body will have a negative impact on the efficiency of the antenna thus a reduced range is to be expected.

11.8 Bluetooth Qualification

The BGM260P modules are included in a pre-qualified Bluetooth Low Energy RF-PHY design based on Core Specification 5.4 having DN of **Q306497**.

The RF-PHY design should be imported and combined with the latest Wireless Gecko Link Layer and Host qualified design(s) by Silicon Labs when qualifying a Product (Core-Complete Configuration Design) that embeds the BGM260P, using the Bluetooth SIG's Qualification Workspace tool.

Please find out more about Bluetooth Qualification on docs.silabs.com.

12. Revision History

Revision 1.1

April, 2025

- Added certification number in section 11.6 NCC - Taiwan.
- Added registration number in section 11.5 KC - South Korea.
- Removed "certification pending" statement from Note in section 1. Features.

Revision 1.0

February, 2025

- Updated remaining TBDs in Electrical Characteristics tables
- Updated 11.8 Bluetooth Qualification chapter
- Updated Figure 10.1 Carrier Tape Dimensions on page 62
- Updated 11.7 RF Exposure and Proximity to Human Body

Revision 0.5

December, 2024

- Initial draft

Simplicity Studio

One-click access to MCU and wireless tools, documentation, software, source code libraries & more. Available for Windows, Mac and Linux!

IoT Portfolio
www.silabs.com/IoT

SW/HW
www.silabs.com/simplicity

Quality
www.silabs.com/quality

Support & Community
www.silabs.com/community

Disclaimer
Silicon Labs intends to provide customers with the latest, accurate, and in-depth documentation of all peripherals and modules available for system and software implementers using or intending to use the Silicon Labs products. Characterization data, available modules and peripherals, memory sizes and memory addresses refer to each specific device, and "Typical" parameters provided can and do vary in different applications. Application examples described herein are for illustrative purposes only. Silicon Labs reserves the right to make changes without further notice to the product information, specifications, and descriptions herein, and does not give warranties as to the accuracy or completeness of the included information. Without prior notification, Silicon Labs may update product firmware during the manufacturing process for security or reliability reasons. Such changes will not alter the specifications or the performance of the product. Silicon Labs shall have no liability for the consequences of use of the information supplied in this document. This document does not imply or expressly grant any license to design or fabricate any integrated circuits. The products are not designed or authorized to be used within any FDA Class III devices, applications for which FDA premarket approval is required or Life Support Systems without the specific written consent of Silicon Labs. A "Life Support System" is any product or system intended to support or sustain life and/or health, which, if it fails, can be reasonably expected to result in significant personal injury or death. Silicon Labs products are not designed or authorized for military applications. Silicon Labs products shall under no circumstances be used in weapons of mass destruction including (but not limited to) nuclear, biological or chemical weapons, or missiles capable of delivering such weapons. Silicon Labs disclaims all express and implied warranties and shall not be responsible or liable for any injuries or damages related to use of a Silicon Labs product in such unauthorized applications.

Trademark Information
Silicon Laboratories Inc.®, Silicon Laboratories®, Silicon Labs®, SiLabs® and the Silicon Labs logo®, Bluegiga®, Bluegiga Logo®, EFM®, EFM32®, EFR, Ember®, Energy Micro, Energy Micro logo and combinations thereof, "the world's most energy friendly microcontrollers", Redpine Signals®, WiSeConnect , n-Link, EZLink®, EZRadio®, EZRadioPRO®, Gecko®, Gecko OS, Gecko OS Studio, Precision32®, Simplicity Studio®, Telegesis, the Telegesis Logo®, USBXpress® , Zentri, the Zentri logo and Zentri DMS, Z-Wave®, and others are trademarks or registered trademarks of Silicon Labs. ARM, CORTEX, Cortex-M3 and THUMB are trademarks or registered trademarks of ARM Holdings. Keil is a registered trademark of ARM Limited. Wi-Fi is a registered trademark of the Wi-Fi Alliance. All other products or brand names mentioned herein are trademarks of their respective holders.

SILICON LABS

Silicon Laboratories Inc.
400 West Cesar Chavez
Austin, TX 78701
USA

www.silabs.com