VSC7227

Multirate 14.5 Gbps 12-Channel Adaptive Channel Extender with All-Rate CRU

Datasheet

VMDS-10374
Revision 4.0
July 2014

Vitesse

www.vitesse.com

Contents

Figures

Tables

Revision History

This section describes the changes that were implemented in this document. The changes are listed by revision, starting with the most current publication.

Revision 4.0

Revision 4.0 of this datasheet was published in July 2014. There were no changes to the technical content of the document. The revision number and publication date were updated to reflect the latest release.

Revision 2.5

Revision 2.5 of this datasheet was published in January 2014. The following is a summary of the changes implemented in the datasheet:

- It is recommended that Loss of Lock de-assertion be combined with other off-chip system indicators.
- The R frequency synthesizer co-efficient setting at 4.25 Gbps was clarified.
- Information about using the ADC reading to obtain the die temperature, including clarifying the register name for the reading, was added. The alternate method of obtaining the die temperature was clarified.

Revision 2.4

Revision 2.4 of this datasheet was published in September 2013. The following is a summary of changes implemented in the datasheet:

- Several electrical specifications were updated based on characterization results.
- The VCOSEL settings were updated.
- The recommended bit setting when using DFE in adaptation mode at data rates above 11.5 Gbps was added to the DFECRU_ERRIMODE register (0*n*_9F).
- Bits 5:4 in the DFEAUTOLOL_CTRL register are now reserved.
- Information about channel crossover when the LOS status function is asserted was added.
- Device storage temperature is –55 °C to 125 °C.
- It was clarified that adaptation timeout typical supply current is 2250 mA and typical power dissipation is 2700 mW.
- The F and R frequency synthesizer coefficient settings were updated.

Revision 2.3

Revision 2.3 of this datasheet was published in July 2013. The following is a summary of changes implemented in the datasheet:

- The data rates supported by the DFE internal delay adjust feature were clarified.
- It is recommended to use HALFCLK mode for VScope operation.
- Information about an internal PRBS error counter was added.
- Information about reference clock support was added.
- Frequency synthesizer coefficient settings for the reference clock were updated.
- Information about additional power down savings was added.
- When using the two-wire serial interface for external microcontroller operation, the MODE0 and MODE1 pins must be set low.
- The typical differential output swing voltage was updated.
- The second-level interconnect lead-free (Pb-free) device, VSC7227XKV, is no longer available. The lead-free device, VSC7227YKV, remains available.
- Several register bits are now reserved, because they are Vitesse test bits and must not be modified.
- In the CHIPID register (40_C2), the default value for REVID [3:0] was updated.
- In the SQCTRL register (0*n*_A9), reserved bit [0] must always be set to 1.
- In the EQSETG45 register (0*n*_81), EQ_ENVGA [6:0] set the input VGA gain settings.
- In the FSYNTST register (3*f*_85), the default value for PD [3] was updated to reflect the default value at page 30_85 and at page 31_85.
- Several DFECRU registers were updated to reflect the upper and lower registers for error count and internal clock count functionality.
- The DFECRU_ERRC0 register (0*n*_D3) was updated to match the register functionality.
- In the DFECRU_TRMN_ERRI register (0*n*_9A), settings for PRBS_GATE [4:1] were updated.
- In the DFECRU_DFEMODE register (0*n*_9C), functionality for pattern inversion to bit [12] (PRBS_INVERT) and for switching between DFE adaptation modes in bit [10] (DFE_LOOP_SEL) was added.
- The DFECRU_LENMAX register (0*n*_9D), previously a reserved register, was updated to reflect functionality for LATCH_CNT [11].
- The DFECRU_ERRIMODE register (0*n*_9F), previously a reserved register, was updated to reflect functionality for ERRIMODE [0].
- In the DFECRU_CFDC_ENAP register (0*n*_96), it was clarified that to enable DFE DC offset restore, DCOFF_ADAP [10] and DFEMODE [1:0] must also be set.

- In the DFECRU_DFEAUTO register (0*n*_97), the default values for DEFEAUTOLOS_CTRL [7:6] and DFEAUTOEQDONE_CTRL [3:2] were corrected to 0x0.
- In the INBUFCTRL register (0*n*_8D), DC offset load functionality was added to DCOFF_LOAD [7]. Additionally, bits [3:0] are now reserved.
- In the CHPD_FCOVR register (0*n*_AA), CRUDIVSQSEL [14:13] was updated to reflect squelch selection functionality, and bit [0] is now a reserved bit.
- In the ANMUXSEL register (40_80), ANMUX_COREBLK_SEL [15:12] bit settings were updated.
- The DGMUXCTRL register (40_81) was updated to reflect digital multiplexer functionality.
- In the RCKMUXSEL register (40_88), DGMUX_LAT_SEL [5:4] was updated to reflect latch select functionality.
- In the EQSETG45 register (0*n*_81), EQ_ENVGA [6:0] now reflect input VGA gain settings.
- In the EQVGAREAD register (0*n*_CD), previously a reserved register, EQVGA_READ [7:0] set the EQ_VGA active gain.
- In the ADAPT_TIMER_EN register (0*n*_B0), functionality to disable input EQ adaptation was added to TIMEOUT_INEQ_DIS [0] and TIMEOUT_DFELMS_DIS [1].
- In the ADAPTPD_VGASET register (0*n*_88), USE_HPFN [2] adjusts how the EQVGA adapts.
- In the VGATARGET register (0*n*_8A), bit [13] was corrected to be a reserved bit, and VGA_TARGET [12:0] settings were updated.
- In the DCOFF12 register (0n_86), the input buffer offset injection point settings were clarified. These settings are valid only when DCOFF_ADAP = 0 and DCOFF_LOAD = 1.
- Descriptions for the following bits were updated or clarified: BTMAX and BFMAX (0*n*_98); DXMAX (0*n*_99); MAINTAP (0*n*_A1); CGVF_READ (0*n*_CE); EQ_TABLE (0*n*_84); CFBF_SIGN and CFBF (0*n*_93); VCOSEL (0*n*_9E, 0*n*_B8, 0*n*_EF, and 0*n*_F9); and CFDC (0*n*_96).
- It was clarified that the values for the following bits are sign magnitude: DC_READ0 and DCREAD1 (0*n*_C3); DC_READ2 (0*n*_C4); CFD1 (0*n*_94); CFD2 and CFD3 (0*n*_95); CGD1_READ and CGD2_READ (0*n*_D1); and CGD3_READ (0*n*_D2).
- It was clarified that the device has two on-die frequency synthesizers.
- Copper channel-loss compensation capabilities were clarified.
- The typical performance curve for input equalization transfer function was updated to reflect actual device measurement.

Revision 2.2

Revision 2.2 of this datasheet was published in January 2013. The following is a summary of changes implemented in the datasheet:

- Moisture sensitivity level (MSL) is level 4.
- ESD (electrostatic discharge) was added. For human body model (HBM), it is a Class 2 rating. For charged device model (CDM), it is ±250 V.
- Bit descriptions for various registers were updated.
- Capacitor values for the analog pins were updated.
- The VSC7227YKV part order number was added to reflect the availability of a device with lead-free bumps. The device is now available with leaded or lead-free bumps.

Revision 2.1

Revision 2.1 of this datasheet was published in May 2012. The following is a summary of changes implemented in the datasheet:

- Information about the data rate detection feature was added.
- Register and bit descriptions were added.
- CMOS output high voltage specifications were updated.
- Thermal specifications were updated.

Revision 2.0

Revision 2.0 of this datasheet was published in February 2012. This was the first publication of the document.

1 Product Overview

The VSC7227 device is part of the EQNOX™ family and uses advanced technology to equalize deteriorated input signals while dissipating the lowest possible power.

The VSC7227 device is a 12-channel uni-directional lane adaptive channel extender with a CRU. This device incorporates analog and digital input equalization, clock and data recovery, and output de-emphasis. It operates with data rates from 1 Gbps to 14.5 Gbps.

The VSC7227 device provides electrical compensation to cable, copper, and backplane environments to increase system margin and media driving distances. The device supports all data rates.

Both input equalization and output de-emphasis can be controlled directly from package pins without the need for an optional external microcontroller. An optional external microcontroller can be used to enhance system performance. The input equalization coefficients can also be set automatically with the on-die proprietary adaptation algorithm.

The VSC7227 device uses advanced technology to equalize deteriorated input signals while dissipating the lowest possible power. The device is available in a 144-pin, flip chip ball grid array (FCBGA) package. It operates on a single supply of 1.2 volts.

The VSC7227 device supports data rates up to 14.5 Gbps. The following protocols and environments are supported:

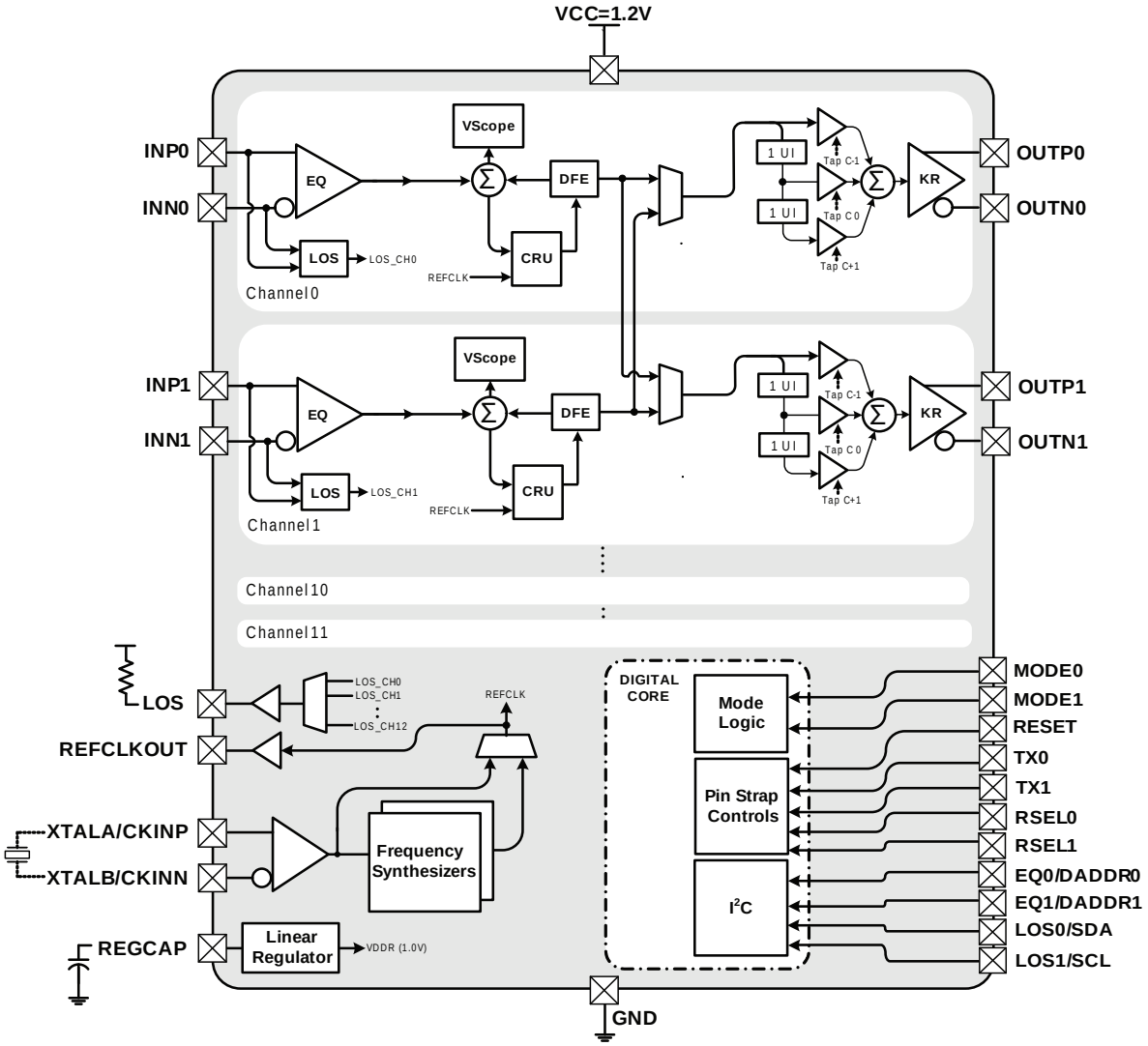
- Supports greater than 65 inches of FR-4 at 10 Gbps when used as a signal driver and receiver
- Supports greater than 10 meters of 24AWG of SFP+ copper direct attached cable at 10 Gbps when used as a signal driver and receiver
- 10/1 Gbps Ethernet, SFP+, IEEE 802.3ap KR IO electrical compatible
- 40/100 Gbps Ethernet IEEE 802.3ba
- 16G/10G/8G/4G/2G/1G Fibre Channel
- 10/5/2 Gbps Infiniband
- SONET and OTN data rates
- 6.25 Gbps RXAUI and 3.125 Gbps XAUI
- SFP+, QSFP+, CFP, and CXP optical and electrical modules

1.1 Block Diagram

The VSC7227 device is a simple to use copper media receiver/driver. It is designed to provide an easy to use, low power, signal cleanup device that supports numerous environments and protocols.

The following illustration shows a simplified block diagram for the VSC7227 device.

Figure 1. Block Diagram



1.2 Features and Benefits

The following table lists the features and benefits of the VSC7227 device.

Table 1. Features and Benefits

Feature	Benefit
Minimum external components	Extremely simple to use device.
Low pin count device	Simple to use device for equalizing non-ideal electrical environments. Requires no microcontroller to operate basic modes.
Low power dissipation device	Low module and system power.
Adaptive or programmable input equalization	Auto adapts the equalizer settings for compensation of copper losses in backplanes, copper traces, and cables. Additional control options through pin strapping or two-wire serial interface.
Adaptive or programmable DFEs	Auto adapts the DFE tap settings to compensate for crosstalk and reflections. Additional control options through pin strapping or two-wire serial interface.
CRU referenceless operation	No external reference clock needed. A low-cost 25 MHz crystal along with two on-chip frequency synthesizers allows for CRU operation at any data rate.
Wide CRU frequency range	Allows for clock recovery unit from 1 Gbps up to 14.5 Gbps.
Programmable output de-emphasis	Package pin strappable or an optional two-wire serial interface allows for compensation of copper losses in cables, copper trace, and backplanes.
Two-wire serial interface port	Optional device control using the two-wire serial interface. This interface can be used to optimize performance and to set the device to various modes.
Pin strap mode	No microcontroller needed.
Channel power down	Ability to power down unused channels to optimize system power.
VScope input signal monitoring integrated circuit	Optimum eye opening and lower BER.
Data polarity multiplexer	Allows for a simple data inversion if necessary to optimize board and system layout.
144-pin 13 mm × 13 mm FCBGA package	Fits into small form factor modules and has excellent thermal and RF performance.
Loss of Signal (LOS) detection	Alerts the user when the incoming signal strength goes below the programmed value.
Adaptation power down	Allows the user to power down adaptation circuitry to optimize power dissipation.
DFE bypass mode	Allows the user to shutdown the DFE to optimize power for a given application.
Adaptation timeout	Allows the user to program a timeout for adaptation after the device powers up. Simplifies usability.
Adjacent channel crossover	Allows the user to crossover data from one adjacent channel to the next. Enhances redundancy in system designs.

1.3 Applications

Some of the applications for the VSC7227 device are as follows:

- Wideband signal switching, clean-up and retimer
- Line driver/retimer/receiver
- Backplane driver/retimer/receiver
- Copper cable driver/retimer/receiver
- PCB signal enhancement
- Optical module retimer/receiver

1.3.1 Without External Microcontroller (Pin Strap Mode)

The VSC7227 device can be used without an external microcontroller. In this application, the input equalization can either be adaptive or set. The amount of input equalization is set through the EQ0/DADDR0 and EQ1/DADDR1 pins. For more information, see "Input Equalization Retimer Mode Settings," page 28.

In this application, the output de-emphasis of all 12 lanes is the same and is controlled by the state of the die pins, TX0/RST and TX1, respectively. These pins are tri-level logic pins that can be programmed to low, float, and high logic levels. For more information about output de-emphasis, see "Output De-Emphasis Retimer Mode Settings," page 29.

The Clock Recovery Unit (CRU) and the frequency synthesizers in this pin strappable application are used with nine possible settings that require an external crystal, or an optional bypass mode can be selected for use with an external reference clock. The pins that select the nine rate select settings are RSEL1 and RSEL0. For more information about the nine total settings, see "Rate Select Settings," page 28.

The Loss of Signal (LOS) settings can be adjusted and set through the two LOS0/SDA and LOS1/SCK tri-level pins. For more information, see "LOS Pin Strap Mode Settings," page 28.

1.3.2 With External Microcontroller (Two-Wire Serial Interface Mode)

The VSC7227 device can be used with an external microcontroller. In this application, all of the features of the device can be controlled and monitored through the two-wire serial port. To operate in this mode, the MODE0 and MODE1 pins must be set to low. The address of the two-wire serial device is controlled by the state of the tri-level pins, EQ0/DADDR0 and EQ1/DADDR1. The VSC7227 device supports eight unique two-wire serial addresses. For more information, see "Two-Wire Serial Programming Addresses," page 33.

The VSC7227 device has two frequency synthesizers. This allows flexibility for configuring data rates on each channel independently. In most applications, the second synthesizer can be powered down because a single frequency synthesizer is all that is needed. In other cases, such as the 16G Fibre Channel mode, the second frequency

synthesizer ensures backward compatibility to 8G and 4G Fibre Channel. Full customization of routing reference clocks to channels is available using the two-wire serial interface.

1.4 Specifications

Specifications for the device are as follows:

- 1.2 V single power supply
- Supports data rates from 1 Gbps to 14.5 Gbps
- 165 mW per channel in retimer mode typical power consumption
- 50 mVpp differential input sensitivity
- 30 dB of input line equalization
- Four-tap Decision Feedback Equalizer (DFE)
- Referenceless CRU operation with an external low cost crystal
- 1000 mV nominal differential output swing with AC-coupled 100 Ω differential load
- –40 °C ambient to 110 °C junction operating temperature range
- 144-pin 13 mm × 13 mm, 1 mm pin pitch, FCBGA package

2 Functional Descriptions

The VSC7227 device is a 12-channel unidirectional channel extender supporting data rates from 1 Gbps to 14.5 Gbps. This device is designed to be extremely easy to use while having the provisions for an optional external microcontroller. Both the input equalization and output de-emphasis can be programmed to various levels with no external components or devices. More precise access to all of the devices features is available with the use of an external microcontroller.

2.1 Input Stage

The inputs are terminated on-chip to a 100 Ω differential load, with an internal bias voltage of 0.6 V. The INPx and INNx pins have internal 0.1 µF AC-coupling capacitors.

2.1.1 Input Equalization

The VSC7227 device features a front end adaptive or programmable input equalizer stage. The input signal equalization on the VSC7227 device helps to combat the Inter Symbol Interference (ISI) of high-speed data as it passes through lossy media. This is accomplished by increasing the relative sensitivity of the receive circuits to the high frequency components of the data edges, which works to reverse, in part or in whole, the degradation of signal quality due to propagation through the transmission media.

Discontinuities and losses in the transmission media act as low-pass filters and attenuate the high frequency components of a signal. The cut-off frequency and slope of the filter depend on the specifics of the discontinuities and the losses of the data path. Typically, electrically short discontinuities, such as solder pads and connectors, have a high cutoff frequency. Lossy media, such as transmission lines or backplanes, have a lower cutoff frequency bandwidth. The electrical length of the transmission line or the size of a discontinuity affects the magnitude of the attenuation.

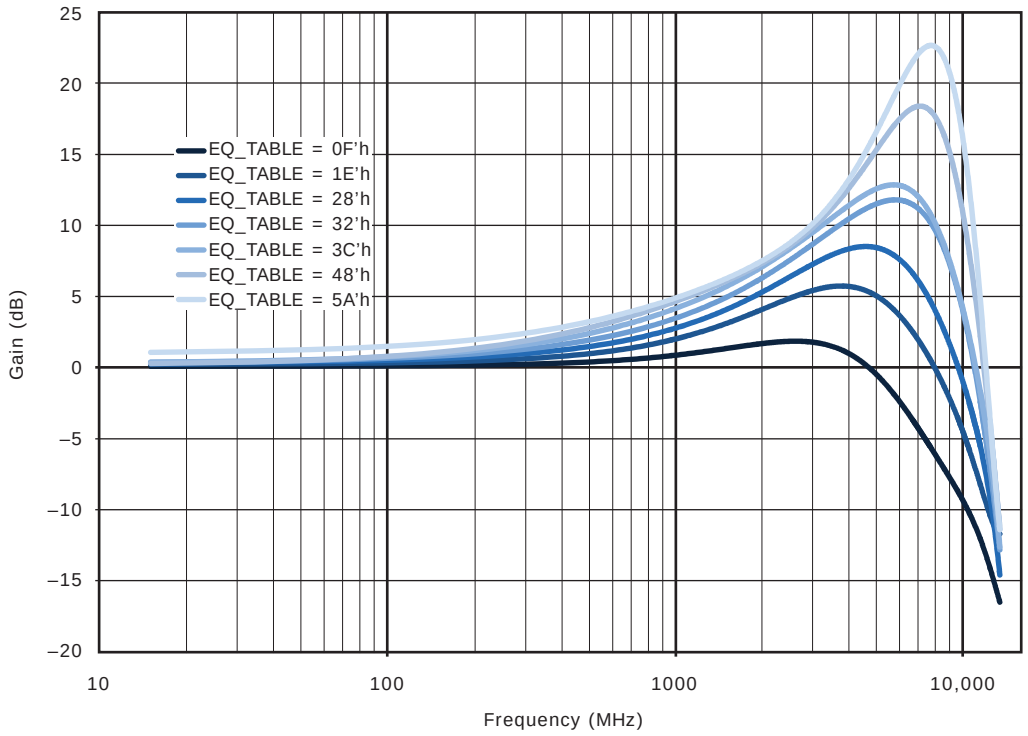
Without a microcontroller, the input equalization levels can be optimized adaptively and for different loss profiles. With the optional external microcontroller, the input equalization level can be controlled using the registers. For more information, see Table 10, page 28.

The VSC7227 device provides flexibility in correcting for transmission losses by providing six independent equalization stages. These six equalization stages can be controlled in three ways:

- The input equalizer can be put into adaptation mode (EQ_ADAP_EN = 1), where all six equalization stages are automatically optimized to compensate for the high frequency loss from the incoming signal.
- The input equalizer can be tuned using a 7-bit bus (EQ_TABLE[6:0]), which controls the equalization strength of all six stages.
- The input equalization stages can be controlled individually.

The following illustration shows the input equalizer transfer function for various EQ_TABLE[6:0] settings. The recommended minimum EQ_TABLE value is 8. For more information about how to control the input equalizer, see “Input Stage Registers,” page 38.

Figure 2. Input Equalizer (typical) Transfer Function



2.1.2 Input Adaptation

The VSC7227 device has autonomous input adaptation capabilities. The adaptation algorithm is enabled in the default setting. The adaptation algorithm optimizes the eye opening. For optimal performance, coefficients can also be manually adjusted using the two-wire serial port.

2.1.3 EQ Adaptation Power Down

The VSC7227 device includes the ability to power down adaptation circuitry in various different blocks to lower power consumption. The INEQ adaptation block can be powered down by setting PD_INBUF_ADAP bit in the ADAPTPD_VGASET register.

2.1.4 EQ VGA

This variable gain amplifier located inside the EQ circuit block has autonomous adaptation capabilities. The adaptation algorithm is enabled by default. Register EQVGA_ADAP can be set for manual mode.

2.1.5 Input Variable Gain Amplifier (VGA)

The front end input linear variable gain amplifier can be operated in adaptive mode or manual mode by programming register VGA_ADAP.

2.2 Loss of Signal (LOS)

The VSC7227 device has a dedicated Loss of Signal (LOS) open drain package pin. The LOS assert and de-assert threshold levels can be set using the LOS registers (LOSASSRT and LOSDASSRT). Incoming data is compared to the LOS assertion and de-assertion threshold level and the LOS signal is asserted accordingly. During normal operation, an input signal greater than the decision threshold will pull the LOS low. If the input signal falls below the decision threshold, the LOS pin is floated and the external LOS resistor pull-up pulls the LOS signal high. The minimum hysteresis on the LOS pin is approximately 2 dB.

Assertion of LOS can be used to control the state of the device output data DOUT and DOUTN. The default mode is to squelch the output on LOS assertion. With an external microcontroller, the state of DOUT*x*/DOUTN*x* on LOS assertion can be programmed with the registers.

In addition to detecting a loss of signal condition, the user has the ability to digitally monitor the differential peak-to-peak amplitude of the incoming signal using the LOS_AMP_PP[11:0] bits in the LOSAMPPP register.

The LOS output pin is an open drain pin. The pin is designed to sink up to 2 mA of current. The recommended external load resistor is 4.7 kΩ.

2.3 Clock Recovery Unit

The VSC7227 device performs clock recovery on the incoming 1 Gbps to 14.5 Gbps signals from the INP*x* and INN*x* pins. The recovered clock is used by the data recovery block to regenerate the data by sampling the output of the summing circuit. The data recovery section samples the waveform at the optimal phase and sets the output bit either high or low. The CRU can be adjusted for desired data rates using the VCOSEL[7:6] and VCODIVSEL[5:4] bits in the two-wire serial interface mode. The following table lists the registers settings for some common data rates.

Table 2. CRU Data Rate Settings

Data Rate (Gbps)	VCOSEL	VCODIVSEL	Description
3.125	0x0	0x2	XAUI
4.25	0x2	0x1	4 GFC
5	0x2	0x1	Infiniband DDR
6.25	0x0	0x1	RXAUI
8.5	0x2	0x0	8 GFC
9.95328	0x2	0x0	OC-192
10	0x2	0x0	Infiniband QDR
10.3125	0x1	0x0	10 GbE
10.52	0x1	0x0	10 GFC

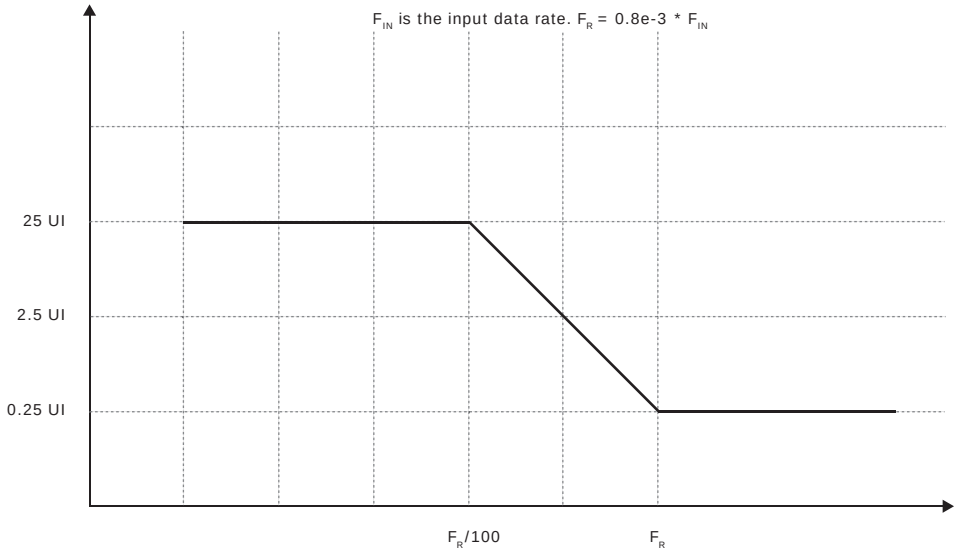
Table 2. CRU Data Rate Settings *(continued)*

Data Rate (Gbps)	VCOSEL	VCODIVSEL	Description
10.709	0x1	0x0	OC-192 + FEC
11.5	0x1	0x0	10 GFC + FEC
14.025	0x0	0x0	16 GFC
14.0625	0x0	0x0	Infiniband FDR

2.3.1 Jitter Tolerance

Jitter tolerance is the ability of the CRU to track timing variations in the received data stream. The amount of jitter that can be tolerated is a function of the frequency of the jitter. At high frequencies, the targeted applications do not require the VSC7227 device to tolerate large amounts of jitter, whereas, at low frequencies, many unit intervals (bit times) of jitter have to be tolerated. The following illustration shows the jitter tolerance for the VSC7227 device.

Figure 3. Jitter Tolerance Mask



2.3.2 Loss of Lock (LOL)

The Loss of Lock (LOL) signal is an alarm state that is asserted in any of the following conditions:

- No valid input signal
- Reference clock frequency and data rate differ too much
- Division ratio for the reference clock through the frequency synthesizer has been chosen incorrectly

When asserted, the LOL alarm reliably indicates an issue has occurred. It is recommended that LOL de-assertion be combined with other off-chip system indicators to confirm an issue was resolved.

The LOL state can be monitored through the two-wire serial interface; it can also be selected through the LOS pin.

2.4 Decision Feedback Equalizer (DFE)

The VSC7227 device features a four-tap Decision Feedback Equalizer (DFE). The DFE assists the linear input equalizer to combat inter-symbol interference.

2.4.1 Adaptive DFE

The VSC7227 device has autonomous DFE tap coefficient adaptation capabilities. The adaptation algorithm is enabled in the default setting. The adaptation algorithm optimizes the eye opening. For optimal performance, coefficients can also be manually adjusted using the two-wire serial port.

2.4.2 DFE Adaptation Power Down

The VSC7227 device includes the ability to power down adaptation circuitry in various different blocks to lower power consumption. The DFE adaptation block can be powered down by setting the PD_DFEADAPT bit in the DFECRU_CTRL register.

2.5 VScope Input Signal Monitoring Integrated Circuit

VScope™ is an integrated input signal monitoring integrated circuit. VScope enables design engineers and system developers to readily evaluate the effectiveness of the equalization capability for a given application environment. Additionally, signals can be monitored remotely without disrupting the data integrity of a live data path. By monitoring the health of a given link, optical or electrical, various types of signal degradation can be identified and corrected.

The input signal can be observed at two points: after the EQ block and after the summing point of the DFE chain. The selection can be made using the VSCOPE_INSEL register. It is recommended that HALFCLK mode be used for VScope operation.

2.6 Output Stage

The VSC7227 device has high-speed outputs (OUTPx, OUTNx) that are back terminated to 50 Ω resistors per side to V_{CC}. The outputs must be AC-coupled. The recommended AC-coupling capacitor value is 100 nF. The nominal output common mode is 0.75 V. Place a high quality V_{CC} to ground bypass capacitor as close to the package pins as practical.

2.6.1 Output Polarity Select

The VSC7227 device offers high speed outputs with selectable output polarity that can be controlled only through the two-wire serial port. In normal operation, a high voltage on INPx results in a high voltage on OUTP*x*.

If an external microcontroller is used, the polarity can be switched using the TX_INV bit in the OUTDRVCTRL register. TX_INV is set LOW by default. If TX_INV is set HIGH, the data path is inverted.

2.6.2 Output Squelching

The VSC7227 device outputs are squelched by default on the assertion of loss of signal. This default setting can be overridden through register settings in the two-wire serial interface mode. Loss of lock can also be utilized to enable output squelching.

The VSC7227 device output squelch can be programmed to set OUTP*x*/OUTN*x* to be squelch LOW/HIGH or HIGH/LOW through the OD_SQ_HLN register bit.

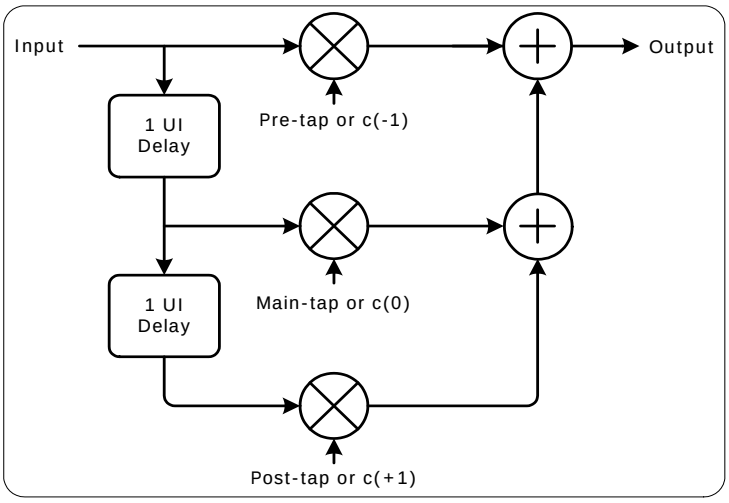
2.6.3 Output De-Emphasis Control

The VSC7227 device features a programmable output de-emphasis stage.

2.6.3.1 Retimer Mode Output De-Emphasis

The output driver architecture is based on the IEEE802.3ap standard (section 72.7.1.10). This is a three-tap (pre, main, and post) finite impulse response (FIR) architecture as shown in the following illustration (figure 72-11 in IEEE 802.3ba).

Figure 4. Transmit Equalizer Three-Tap FIR Architecture



The setting of the output de-emphasis levels can be accomplished without a microcontroller in retimer pin strap mode. Device pins TX1 and TX0/RST are tri-level input pins that control the output de-emphasis level. The tri-level inputs pads provide

nine fixed settings of output de-emphasis that can be applied to all 12 lanes. For more information about the nominal settings, see "Output De-Emphasis Retimer Mode Settings," page 29.

With the optional external microcontroller, the output de-emphasis level can be controlled using registers. For more information, see Table 77, page 57, Table 78, page 57, and Table 79, page 57. An external microcontroller provides finer control of the output de-emphasis.

2.7 Reference Clock

The reference clock is used by the VSC7227 device as a hint clock only; it is not used to retime the signal. A low-cost 25 MHz crystal or other external reference clock can be used. The supplied reference clock frequency must be accurate within ±100 ppm.

When using other than the 25 MHz crystal, the frequency of the clock must be below 200 MHz. It is recommended to have an AC-coupling capacitor at the CLKIN pin.

To supply a single-ended reference clock, terminate the unused pin with a 100 pF capacitor to ground.

If more than one VSC7227 device is on the same board, the reference clock can be daisy-chained by connecting the REFCLKOUT pin of the first device to the CLKIN pin of the second device, and so on.

2.8 Frequency Synthesizers

A frequency synthesizer allows for multiplication, division, and mixing of frequencies to create an output signal with the desired frequency. With two on-die frequency synthesizers, the VSC7227 device has the flexibility to modify the frequency of any reference clock to match the application.

The frequency synthesizers are programmed using four coefficients: N[7:0], M[7:0], F[23:0], and R[23:0]. These four coefficients can be programmed to obtain the desired output reference clock. The following equation shows the frequency synthesizer transfer function.

$$\text{Output} = \text{Input} \times \frac{N}{M} \times \left(\frac{64}{64 + \alpha} \right) \quad \text{Where } \alpha = \frac{F}{R}$$

Note It is highly recommended to keep the ratio 'α' close to 0.5.

The frequency synthesizers can be used with a low cost 25 MHz external crystal to enable reference-less operation of the CRU. The CRU and the frequency synthesizers can be controlled using the two-wire serial interface or the pin strap mode using the RSEL1 and RSEL0 pins.

The following table lists some example data rates and the appropriate frequency synthesizer coefficient settings.

Table 3. Frequency Synthesizer Coefficient Settings

Gbps	MHz	N[7:0]	M[7:0]	F[23:0]	R[23:0]	Description
3.125	25	0x41	0x21	0x8C000	0x101D00	XAUI
4.25	25	0x4B	0x38	0xA0000	0x129800	4 GFC
5	25	0x4A	0x2F	0x90000	0x125C00	Infiniband DDR
6.25	25	0x41	0x21	0x8C000	0x101D00	RXAUI
8.5	25	0x4B	0x38	0xA0000	0x129800	8 GFC
9.95328	25	0x45	0x2C	0xB2800	0x14E200	OC-192
10	25	0x4A	0x2F	0x90000	0x125C00	Infiniband QDR
10.3125	25	0x41	0x28	0x8C000	0x101D00	10 GbE
10.52	25	0x44	0x29	0xC2000	0x150F80	10 GFC
10.709	25	0x40	0x26	0xA6200	0x18D678	OC-192 + FEC
11.5	25	0x43	0x25	0x84000	0x109F00	10 GFC + FEC
14.025	25	0x40	0x1D	0xE6000	0x1FC680	16 GFC

2.9 Data Rate Detection

The VSC7227 device supports data rate detection for systems that require channels to run at different data rates. Data rate detection can be used to program the device to switch from one data rate to another, as required. Up to four different data rates may be programmed at one time without the use of hardware resources to detect and switch the configuration of a channel. Data rate detection is enabled by setting the DRD_ENABLE bit in the DRD_CTRL register. The following table shows the registers used to configure the four different data rates into different look-up tables (LUTs). For more information about the specific controls available within each register, see the bit descriptions for the specific register.

Table 4. Data Rate Detection Configuration Registers

Register	Description
EQ_ADAP_LUT	Adaptive input equalization algorithm control
EQ_DIFF_LUT	Sets the difference between target high-pass and low-pass filter values in Adaptive mode
EQ_TABLE_LUT	Input equalizer look-up table for equalization settings
DFE_AVG_LUT	DFE adaptation rate
DFEMODE_LUT	DFE adaptation mode
DFE_DELAY_LUT	DFE function internal delay adjust
VCOSEL_LUT	VCO select
VCODIVSEL_LUT	VCO clock divider ratio select
RCKSEL_LUT	Channel reference clock select
OD_IND_BYP_LUT	Output peaking inductor bypass select
OD_SLEW_LUT	Output slew rate select

2.10 Mode Package Pin

The Mode pin state determines the mode of operation of the VSC7227 device, which has the following four comprehensive modes:

- Two-wire serial interface mode: mode state 0
- Fibre Channel mode: mode state 1
- Pin strap modes: mode states 6 and 8
- Infiniband modes: mode states 2 and 7

The following table lists the available mode pin settings.

Table 5. Mode Pin Settings

MODE State	MODE1	MODE0	Mode
0	0	0	Two-wire serial interface mode
1	0	Float	Fibre Channel mode
2	0	1	Infiniband0 mode
3	Float	0	Reserved (do not use)
4	Float	Float	Reserved (do not use)
5	Float	1	Reserved (do not use)
6	1	0	Retimer pin strap with crystal mode
7	1	Float	Infiniband1 mode
8	1	1	Retimer pin strap with external reference clock

The MODE0 and MODE1 mode pins are tri-level input pins that can be set to V_{CC}, GND, or left floating.

2.11 Fibre Channel Modes

The VSC7227 device has a Fibre Channel mode to support dedicated external rate select hardware pins for each channel. The ASIC controlling the VSC7227 device is able to set up each channel's data rate and rise/fall time through a single pin by pulling it high or low per FC-PI-2 (4G Fibre Channel), FC-PI-4 (8G Fibre Channel), and FC-PI-5 (16G Fibre Channel) standards.

Program the values for VCOSEL, VCODIVSEL, and slew rate in a LUT that corresponds to the state of the Fibre Channel rate select pin for that channel. For example, for 8G Fibre Channel mode, program the LUTs to set the channel for 8.5 Gbps data rate with a rise/fall time of 45 ps when the rate select pin is set high, and 4.0 Gbps data rate with a rise/fall time of 60 ps when the rate select pin is set low. The host can use the two-wire serial port to change any settings for optimization.

The following table lists the channel mode rate select pins.

Table 6. Channel Mode Rate Select Pins

Channel	Pin Name
0	FCSEL0

Table 6. Channel Mode Rate Select Pins *(continued)*

Channel	Pin Name
1	FCSEL1
2	FCSEL2
3	FCSEL3
4	FCSEL4
5	FCSEL5
6	FCSEL6
7	FCSEL7
8	FCSEL8
9	FCSEL9
10	FCSEL10
11	FCSEL11

For information about data rate detection register bit controls, see Table 4, page 25.

2.12 Infiniband Rate Select

The VSC7227 device supports Infiniband rate selection with external rate select pins that set up the channels for the required standard. Utilizing programmable LUTs, the channels can be set up to use the needed VCO, VCODIV, and slew rate selection. The following tables show the rate select pins for the two Infiniband modes.

Table 7. Infiniband0 Rate Select Pins

Channels	Control Pins
All	FCSEL0, FCSEL1

Table 8. Infiniband1 Rate Select Pins

Channels	Control Pins
0, 1, 2, 3	FCSEL0, FCSEL1
4, 5, 6, 7	FCSEL2, FCSEL3
8, 9, 10, 11	FCSEL4, FCSEL5

The following table shows the channels set by the control pin settings for both Infiniband0 and Infiniband1 modes.

Table 9. Infiniband Channel Settings

FCSEL1, FCSEL3, FCSEL5	FCSEL0, FCSEL2, FCSEL4	Mode (LUT select)
0	0	A
0	1	B
1	0	C
1	1	D

2.13 Pin-Strap Modes

The following tables list the recommended input equalization and output de-emphasis settings in the pin-strappable mode (no external microcontroller) for the VSC7227 device. For information about mode states, see Table 5, page 26.

Table 10. Input Equalization Retimer Mode Settings

MODE State	EQ State	EQ1 Pin	EQ0 Pin	EQ (dB)	DFE	Comment
6/8	0	0	0	Auto	Auto	Full auto.
6/8	1	0	Float	Off	Auto	DFE only.
6/8	2	0	1	Auto	Off	INEQ only.
6/8	3	Float	0	6	Auto	Pin strappable mode. Monotonically increasing amounts of input equalization.
6/8	4	Float	Float	12	Auto	Pin strappable mode. Monotonically increasing amounts of input equalization.
6/8	5	Float	1	18	Auto	Pin strappable mode. Monotonically increasing amounts of input equalization.
6/8	6	1	0	24	Auto	Pin strappable mode. Monotonically increasing amounts of input equalization.
6/8	7	1	Float	30	Auto	Pin strappable mode. Monotonically increasing amounts of input equalization.
6/8	8	1	1	4	Off	SFI nominal.

Table 11. LOS Pin Strap Mode Settings

MODE State	State	LOS1	LOS0	LOS Amplitude (mVpp)	LOS Hysteresis (dB)
6/8	0	0	0	3.8	2
6/8	1	0	Float	6	2
6/8	2	0	1	8	2
6/8	3	Float	0	10	2
6/8	4	Float	Float	20	2
6/8	5	Float	1	35	2
6/8	6	1	0	45	2
6/8	7	1	Float	100	2
6/8	8	1	1	200	2

Table 12. Rate Select Settings

MODE State	Rate Select State	RSEL 1 Pin	RSEL 0 Pin	Reference Clock Generated (MHz)	Data Rate (Gbps)	Description
6/8	0	0	0	156.25	10.3125	10 GbE
6/8	1	0	Float	212.5	14.025	16 GFC

Table 12. Rate Select Settings *(continued)*

MODE State	Rate Select State	RSEL 1 Pin	RSEL 0 Pin	Reference Clock Generated (MHz)	Data Rate (Gbps)	Description
6/8	2	0	1	106.25	8.5	8 GFC
6/8	3	Float	0	106.25	4.25	4 GFC
6/8	4	Float	Float	159.393939	10.52	10 GFC
6/8	5	Float	1	125	10	Infiniband QDR
6/8	6	1	0	125	5	Infiniband DDR
6/8	7	1	Float	156.25	3.125	XAUI
6/8	8	1	1	156.25	6.25	RXAUI

Table 13. Output De-Emphasis Retimer Mode Settings

MODE State	DE State	TX1	TX0	PRE c(-1) (mA)	MAIN c(0) (mA)	POST c(+1) (mA)	DC Amplitude (mV)	De-Emphasis (dB)	Comment
6/8	0	0	0	0	16	0	800	0	KR preset
6/8	1	0	Float	0	10	–1	450	–1.74	Clean eye optics
6/8	2	0	1	–1	16	–2	650	–3.3	
6/8	3	Float	0	–1	15	–4	500	–6.02	
6/8	4	Float	Float	–1	13.5	–5.5	350	–9.12	KR Initialize
6/8	5	Float	1	–1	12.5	–6.5	250	–12.04	
6/8	6	1	0	–0.5	11.5	–8	150	–16.48	
6/8	7	1	Float	–0.25	11	–8.75	100	–20	
6/8	8	1	1	–0.25	10.5	–9	62.5	–23.97	

2.14 Adjacent Channel Crossover

To allow for redundancy in system-level design, the VSC7227 device features a crossover of adjacent channels, allowing the user to broadcast data from one channel to two channels, switch data from one channel to another, and so on. This feature is the equivalent to a 2 × 2 crosspoint switch, which can be enabled by setting register CH_CP. The two adjacent channel pairs are channel *n* and channel *n*+1, where *n* is an even number. For example, channel 0 and channel 1, channel 2 and channel 3, and so on.

By default, the VSC7227 device squelches the output upon LOS assertion, which will affect the crossover function when if is no signal at the input of the channel on which the crossover is enabled (CH_CP = 1). To disable the squelch function, set the SQ_DIS bit to 1 in the SQCTRL (0*n*_A9) register.

2.15 Power Down and Power Savings Modes

The two-wire serial port can be used to control the VSC7227 device for maximum power savings. Channels can be powered down individually by setting the PD_CH bit in

the CHPD_FCOVR register. For additional power savings, individual circuit blocks such as input buffer, VScope, LOS, output driver, and DFE can also be powered down individually. For example, when the channel crossover from channel 0 to channel 1 is enabled, channel 1's input buffer, EQ, DFE, and CRU can be powered down.

2.16 Power on Reset

The VSC7227 device utilizes an on-die power-on-reset. All of the on-die control registers are reset to zero unless otherwise noted. For more information, see "Registers," page 37.

2.17 Adaptation Timeout

The VSC7227 device contains a timeout feature to allow the user to easily control the power down of adaptation. The time from power on of the VSC7227 device to power down of the adaptation can be set by the user anywhere from 5 ms to 20 seconds using a 16-bit register, TIMERMAX. When the counter times out, the adaptation of the INEQ and DFE blocks are shut down.

2.18 Analog-to-Digital Converter

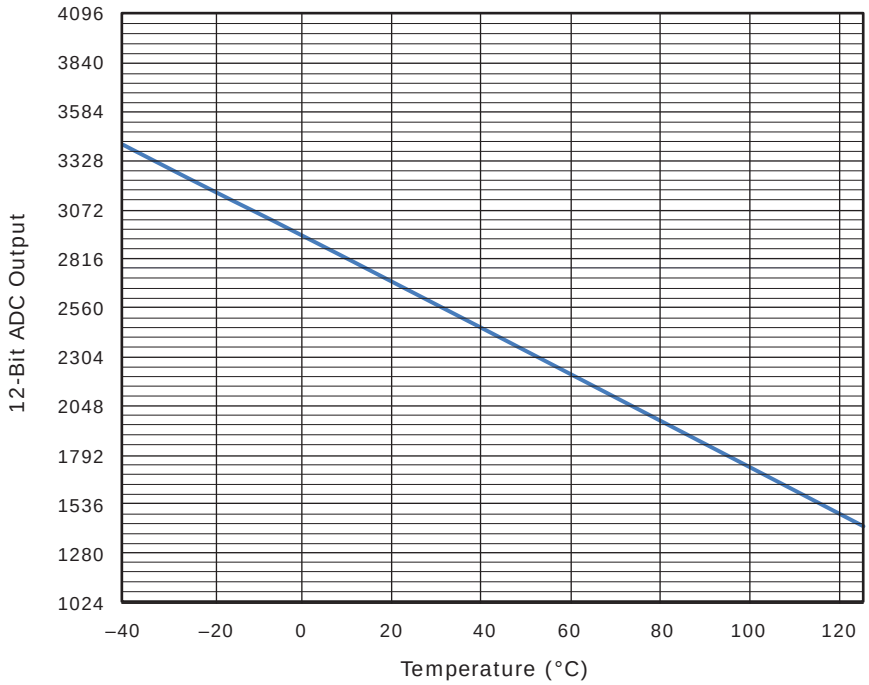
The VSC7227 device has an on-die, 12-bit ADC to provide digital monitoring of analog signals. The ADC has a nominal full-scale measurement range from 0.3 V to 0.9 V. The ADC is capable of monitoring the on-die temperature, power supply voltage, and the band gap voltage. The output format of the ADC is straight binary. The LSB of the 12-bit value is approximately 0.6 V /4096 = 146 µV.

2.19 Die Temperature Monitor

The VSC7227 device has an on-die temperature monitor. For normal operation, the temperature monitoring can be accessed only using the two-wire serial port. A 12-bit digital reading of the on-die operating junction temperature is available from the ADC_DOUT registers by first setting ANMUX_COREBLK_SEL to 0xC to select the temperature monitor output (VTEMP). An initial 1-point calibration is highly recommended to attain greater accuracy. The following illustration plots the temperature versus the 12-bit ADC output.

An alternate method to obtain the die temperature is to use the internal diodes by connecting TD_ANODE and TD_CATHODE pins to an external temperature monitor device.

Figure 5. Temperature vs. 12-Bit ADC Output ($ADCOUT_{10}$)



2.20 Internal Error Counter

To check for errors, perform the following steps:

1. Set the PRBS pattern using PRBS_SEL bits [7:5] in the DFECRU_TRMN_ERRI register 0*n*_9A.
2. Set for continuous checking by setting PRBS_GATE bits [4:1] to 0xF in the DFECRU_TRMN_ERRI register 0*n*_9A.
3. Enable the checker by setting PRBS_EN bit [0] to 1 in the DFECRU_TRMN_ERRI register 0*n*_9A.
4. Clear the error counter and the clock counter by setting ERRIMODE bit [0] to 1, then setting it back to 0, in the DFECRU_ERRIMODE register 0*n*_9F.
5. Read PRBS_NOSYNC bit [15] in the DFECRU_ERRC2 register 0*n*_E8.
6. Check for inversion in PRBS_INVERT bit [12] in the DFECRU_DFEMODE register 0*n*_9C.
7. When synchronization is achieved (PRBS_NOSYNC bit [15] = 0), counting begins.
8. Set LATCH_CNT bit [11] from 0 to 1 in the DFECRU_LENMAX register 0*n*_9D to lock in both clock and error counter values. The ERRCNT and CLKCNT registers are ready for a read. Internally, the counter continues to accumulate error and clock counts.

9. Read the following registers for clock and error counter values:
   ERRCNT2 register 0*n*_E8 (bits 13:0)
   ERRCNT1 register 0*n*_E9
   ERRCNT0 register 0*n*_D3 [13:0]
   CLKCNT1 register 0*n*_FC [15:0]
   CLKCNT0 register 0*n*_FD [15:0]
10. Using the values from step 9, calculate the BER using the formula: BER = ((ERRCNT2, ERRCNT1, ERRCNT0)/3) / ((CLKCNT1, CLKCNT0) × 16384)
11. Set LATCH_CNT bit [11] from 1 to 0 in the DFECRU_LENMAX register 0*n*_9D.
12. Repeat steps 8 through 11 as necessary.
13. To exit, disable the checker by setting PRBS_EN bit [0] to 1 in the DFECRU_TRMN_ERRI register 0*n*_93.

The error counter increments three times for each corrupted bit. The BER calculation is only valid for the window of time between latches. The error counter saturates when it is full. However, the clock counter rolls over, so the clock counter must be latched and read before the clock counter rolls over. For example, for 10.3125 Gbps, the clock counter rolls over after 1.8 hours. The BER calculation shown in step 10 is valid only if the clock counter rollover events are properly accounted for. Clock counts can be accumulated within software by polling often enough to identify when the current value read is less than the previous value read, which implies a rollover, and thus adding a value of 0x100000000(4,294,967,296 decimal) per rollover event. This is to say the BER calculation is not cumulative.

2.21 Two-Wire Serial Interface

The VSC7227 device supports a slave mode two-wire serial interface where an external master device controls the VSC7227 slave device. The two-wire serial interface operates in both standard mode (up to 100 kbps) and fast mode (up to 400 kbps) data transfer rates. Forcing the mode pin to ground enables the two-wire serial mode for the device. When enabled, the internal registers can be programmed and read.

A master device generates a start condition <S> by transitioning SDA high to low while SCK is high. Data is then transferred on the SDA line with the most significant bit (MSB) first and the SCK line clocking each bit. Data transitions occur when the SCK is low and is valid (read) or stable (write) when on the high to low transition of the SCK. Data transfers are acknowledged (ACK or <A>) by the receiving device (VSC7227 for data writes and the master device for data reads) by holding the SDA signal low while strobing SCK high then low (NACK or <NA> is the opposite). The master generates a stop condition <P> (terminates the data transfer) with a low to high transition on the SDA signal while SCK is high. For more information, see Figure 7, page 35.

2.21.1 Serial Write

A serial write starts with the master sending a byte to the VSC7227 device. The first seven bits represent the serial interface address, and the eighth must be a 0 to indicate a write operation. The VSC7227 device compares its serial interface address to the one transmitted. Acknowledge is generated only if they match.

Without issuing a start or stop condition, the master then sends a second byte to the VSC7227 device. The VSC7227 device interprets this byte as the register address. The VSC7227 device consists of 16-bit (two byte) registers. The master sends a third byte to the VSC7227 device to write the 8 MSB bits, followed by a fourth byte to write the 8 LSB bits. This is interpreted as the data for the 16-bit register write. At this point, the write has taken effect.

The following is an example of the write sequence (assuming the serial interface address is set to 0x10).

```
<S><0x20><A><Address><A><8 bit MSB data><A><8 bit LSB data><A><P>
```

2.21.2 Serial Read

A read cycle starts similarly to the serial write. The master sends the serial interface address again but this time uses a 1 in the LSB to indicate a read operation. After the acknowledge cycle from the VSC7227 device, the master stops driving the SDA line. At this point, the VSC7227 device outputs one bit at a time on the falling edge of SCK, transmitting the MSB first until the first 8 MSB bits of the 16-bit register are transmitted. Followed by the acknowledgement, the 8 LSB bits of the 16-bit register are transmitted.

After the eighth falling edge of the SCK, the VSC7227 device releases control of the SDA bus and the master issues the clock for the acknowledge cycle. After the master issues the acknowledge cycle, the master issues a stop condition that signals the end of the transmission.

The following is an example sequence (assuming the serial interface address is set to 0x10).

```
<S><0x20><A><Address><A><S><0x21><A><8 bit MSB data><A><8 bit LSB
data><NA><P>
```

2.21.3 Serial Addressing

The VSC7227 device two-wire serial interface supports a 7-bit slave address. This address may be set through the EQ1/DADDR1 and EQ0/DADDR0 pins. These pins are tri-level pins. The following table lists the programming addresses for the two-wire serial interface. For information about mode states, see Table 5, page 26.

Table 14. Two-Wire Serial Programming Addresses

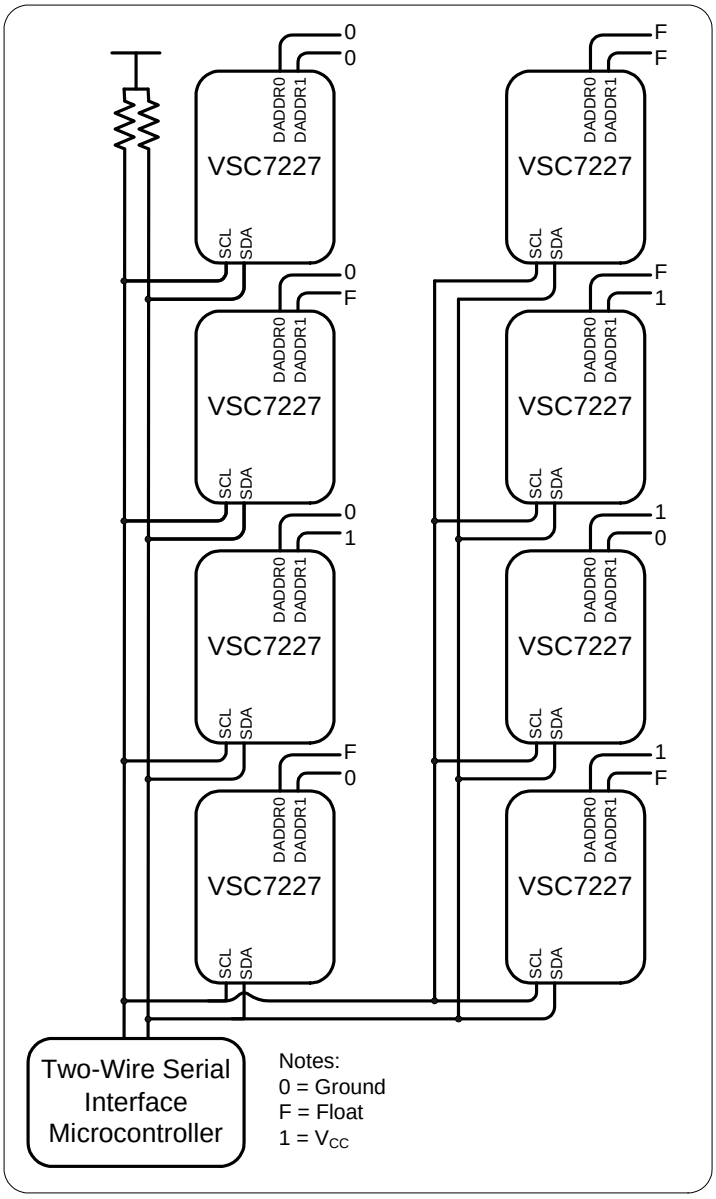
MODE State	EQ1/DADDR1 Pin	EQ0/DADDR0 Pin	Two-Wire Serial Address
0/1/7	0	0	0x10
0/1/7	0	Float	0x11
0/1/7	0	1	0x12
0/1/7	Float	0	0x13
0/1/7	Float	Float	0x14
0/1/7	Float	1	0x15
0/1/7	1	0	0x16
0/1/7	1	Float	0x17

Table 14. Two-Wire Serial Programming Addresses *(continued)*

MODE State	EQ1/DADDR1 Pin	EQ0/DADDR0 Pin	Two-Wire Serial Address
0/1/7	1	1	Reserved

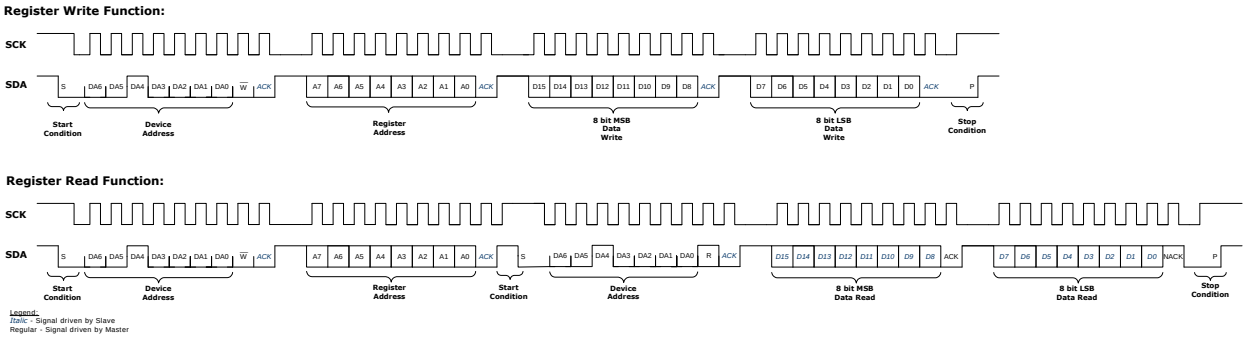
The following illustration shows the multiple addressing using the two-wire serial interface.

Figure 6. Multiple Two-Wire Serial Device Addressing



The following illustration shows the two-wire serial interface timing diagram.

Figure 7. Two-Wire Serial Timing



2.22 Write Bit Masking

Write bit masking allows users to mask bits they do not want to change. Normally, changing a single bit requires the user to re-write the bits that are not to be changed. This requires additional housekeeping, which burdens the external microcontroller. With write bit masking, the user asserts the bit(s) that they might want to change through register address 0x7E. A 1 in the 16-bit register enables a bit write, while a 0 disables writing to the respective bits.

2.23 Page-Based Programming

The VSC7227 device uses page-based register programming to configure the features and functions of the device. Pages are grouped according to function; each page typically has a maximum of 128 addresses and a potential address space of 128 16-bit words. A specific page is selected by programming the value for the desired page into the page register at address 0x7F.

Registers 0x00 to 0x7F, including the write bit mask register (0x7E) and the page select register (0x7F), are not linked to a specific page and can be programmed regardless of the value in the page select register (address 0x7F). The following tables highlight the two-wire interface register scheme and the page select scheme. For information about mode states, see Table 5, page 26.

Table 15. Register Scheme

MODE State	Register Address	Function	Comments
0/1/2/7	0x00 – 0x7D	Reserved	Reserved
0/1/2/7	0x7E	Write Bit Mask register	1: Enable bit write 0: Enable bit masking
0/1/2/7	0x7F	Page Select register	
0/1/2/7	0x80 – 0xFF	Page registers	Individual page registers

Table 16. Page Select Scheme

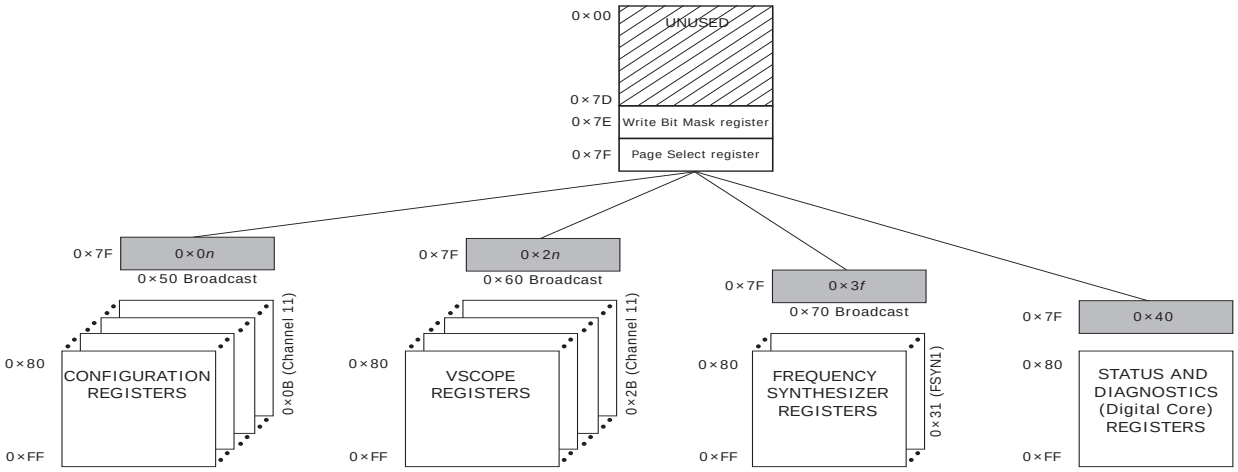
MODE State	Page Select Register Value	Function	Comments
0/1/2/7	0x00 – 0x0B	Channel *n* control	Enables write/read to channel 0 through channel 11 registers
0/1/2/7	0x20 – 0x2B	Channel *n* VScope control	Enables write/read to channel 0 through channel 11 VScope registers
0/1/2/7	0x30	Frequency synthesizer 0 control	Enables write/read to frequency synthesizer 0 registers
0/1/2/7	0x31	Frequency synthesizer 1 control	Enables write/read to frequency synthesizer 1 registers
0/1/2/7	0x40	Digital core block control	Enables write/read to digital core registers
0/1/2/7	0x50	Channel broadcast	Enables write to all channel registers
0/1/2/7	0x60	Channel VScope broadcast	Enables write to all channel VScope registers
0/1/2/7	0x70	Frequency synthesizer broadcast	Enables write to all frequency synthesizer registers
0/1/2/7	0x80	Reserved	For internal testing purposes only

3 Registers

This section provides the register information for the VSC7227 device. The registers can only be accessed using the two-wire serial port and an optional external microcontroller.

The first part of a register address, “XX_”, refers to the page while the second part, “_YY”, refers to the register address in hexadecimal notation. Register bit numbers use hexadecimal notation. A range of bits is indicated with a colon. For example, a reference to bits 5 through 0 is shown as 5:0. Bit 15 is the most significant bit (MSB), with bit 0 being the least significant bit (LSB) unless otherwise noted. The following illustration shows the register spaces.

Figure 8. Register Space Diagram



3.1 Configuration Registers

The following sections provide information about the registers for all 12 channels. These registers can be accessed by programming page select register (0x7F) with a value of 0*n,* where *n* goes from 0x0 through 0xB. These registers can also be written to all channels (broadcast) by setting the page select register to 0x50.

3.1.1 Input Stage Registers

This section provides information about the input equalizer registers for the VSC7227 device.

Table 17. EQSET0123 (0*n*_80)

Bit	Name	Access	Description	Default
15:12	EQ_SET0	RW	Input equalizer first stage boost setting when in EQ Manual mode 0x0: Minimum 0xF: Maximum These settings are valid only when EQ_ADAP_EN = 0 or if LD_EQ_TABLE = 0	0x2
11:8	EQ_SET1	RW	Input equalizer second stage boost setting when in EQ Manual mode 0x0: Minimum 0xF: Maximum These settings are valid only when EQ_ADAP_EN = 0 or if LD_EQ_TABLE = 0	0x2
7:4	EQ_SET2	RW	Input equalizer third stage boost setting when in EQ Manual mode 0x0: Minimum 0xF: Maximum These settings are valid only when EQ_ADAP_EN = 0 or if LD_EQ_TABLE = 0	0x1
3:0	EQ_SET3	RW	Input equalizer fourth stage boost setting when in EQ Manual mode 0x0: Minimum 0xF: Maximum These settings are valid only when EQ_ADAP_EN = 0 or if LD_EQ_TABLE = 0	0x1

Table 18. EQSETG45 (0*n*_81)

Bit	Name	Access	Description	Default
15:12	EQ_SET4	RW	Input equalizer fifth stage boost setting when in EQ Manual mode 0x0: Minimum 0xF: Maximum These settings are valid only when EQ_ADAP_EN = 0 or if LD_EQ_TABLE = 0	0x1
11:8	EQ_SET5	RW	Input equalizer sixth stage boost setting when in EQ Manual mode 0x0: Minimum 0xF: Maximum These settings are valid only when EQ_ADAP_EN = 0 or if LD_EQ_TABLE = 0	0x1
7	RESERVED	RW	Must be set to its default	0x0
6:0	EQ_ENVGA	RW	Input VGA gain settings 0x00: Minimum 0x7F: Maximum These settings are valid only when VGA_ADAP = 0.	0x7F

Table 19. EQBUFZONE (0*n*_82)

Bit	Name	Access	Description	Default
15:14	RESERVED	RW	Must be set to its default.	0x0
13:0	EQ_BUFF	RW	Sets the buffer zone between target high pass filter and low pass filter values (EQ_DIFF). Valid if EQ_DIFF – EQ_BUFF < HPF – LPF < EQ_DIFF + EQ_BUFF. These values are two's complement, and are valid only when EQ_ADAP_EN = 1 or if LD_EQ_TABLE = 0.	0x0021

Table 20. EQADAPTEN_DIFF (0*n*_83)

Bit	Name	Access	Description	Default
15	EQ_ADAP_EN	RW	Adaptive input equalization (EQ) algorithm control. 0: EQ Manual mode 1: EQ Adaptive mode	0x1
14	RESERVED	RW	Must be set to its default.	0x0
13:0	EQ_DIFF	RW	Sets the difference between target high pass and low pass filter values when in Adaptive mode. These values are two's complement, and each LSB is 0.15 mV. These settings are valid only when EQ_ADAP_EN = 1 or if LD_EQ_TABLE = 0.	0x0021

Table 21. EQTABLE (0*n*_84)

Bit	Name	Access	Description	Default
15:7	RESERVED	RW	Must be set to its default	0x000
6:0	EQ_TABLE	RW	Input equalizer on-chip look-up table for equalization settings 0x00: Minimum 0x5A: Maximum These settings are valid only when EQ_ADAP_EN = 0 or if LD_EQ_TABLE = 1	0x08

Table 22. DCOFF0 (0*n*_85)

Bit	Name	Access	Description	Default
15:8	RESERVED	RW	Must be set to its default	0x00
7:0	DCI0	RW	Input buffer first offset injection point setting 0x80: Maximum negative offset 0x00: Zero offset 0x7F: Maximum positive offset These settings are valid only when DCOFF_ADAP = 0	0x00

Table 23. DCOFF12 (0*n*_86)

Bit	Name	Access	Description	Default
15:8	DCI1	RW	Input buffer second offset injection point setting 0x80: Maximum negative offset 0x00: Zero offset 0x7F: Maximum positive offset These settings are valid only when DCOFF_ADAP = 0 and DCOFF_LOAD = 1.	0x00
7:0	DCI2	RW	Input buffer third offset injection point setting 0x80: Maximum negative offset 0x00: Zero offset 0x7F: Maximum positive offset These settings are valid only when DCOFF_ADAP = 0 and DCOFF_LOAD = 1	0x00

Table 24. DCOFF3_EQVGASET (0*n*_87)

Bit	Name	Access	Description	Default
15:8	DCI3	RW	Input buffer fourth offset injection point setting 0x80: Maximum negative offset 0x00: Zero offset 0x7F: Maximum positive offset These settings are valid only when DCOFF_ADAP = 0	0x00
7	RESERVED	RW	Must be set to its default.	0x0
6:0	EQVGA_SET	RW	EQ VGA (Variable Gain Amplifier) gain settings when in EQ VGA Manual mode 0x00: Minimum 0x7F: Maximum These settings are valid only when EQVGA_ADAP = 0	0x60

Table 25. ADAPTPD_VGASET (0*n*_88)

Bit	Name	Access	Description	Default
15	PD_INBUF_ADAP	RW	Input adaptation power down control 0: Normal operation 1: Power down	0x0
14:8	VGA_SET	RW	Input VGA (Variable Gain Amplifier) gain settings when in VGA Manual mode 0x00: Minimum 0x7F: Maximum These settings are valid only when VGA_ADAP = 0	0x30
7:3	RESERVED	RW	Must be set to its default	0x00
2	USE_HPFN	RW	Use High Pass Filter Negate 0: Use HPF and LPF for EQ adaptation 1: Use LPF and EQ buffer for EQ adaptation	0x0
1:0	RESERVED	RW	Must be set to its default	0x0

Table 26. VGABUFZONE (0*n*_89)

Bit	Name	Access	Description	Default
15:14	RESERVED	RW	Must be set to its default.	0x0
13:0	VGA_BUFF	RW	Sets the buffer zone for VGA_TARGET when in VGA Adaptive mode. Valid if VGA_TARGET – VGA_BUFF < VGA amplitude < VGA_TARGET + VGA_BUFF. These values are two's complement, and each LSB is 0.15 mV. These settings are valid only when VGA_ADAP = 1.	0x0021

Table 27. VGATARGET (0*n*_8A)

Bit	Name	Access	Description	Default
15:13	RESERVED	RW	Must be set to its default.	0x0
12:0	VGA_TARGET	RW	Sets the target value for VGA output amplitude when in VGA Adaptive mode. These values are two's complement, and each LSB is 0.15 mV. These settings are valid only when VGA_ADAP = 1. 0x00: Minimum 0x7F: Maximum	0x01AA

Table 28. EQVGATARGET (0*n*_8B)

Bit	Name	Access	Description	Default
15:14	RESERVED	RW	Must be set to its default.	0x0
13:0	EQVGA_TARGET	RW	Sets the target value for the EQ VGA output amplitude when in EQVGA Adaptive mode. These values are two's complement, and each LSB is 0.15 mV. These settings are valid only when EQVGA_ADAP = 1.	0x01AA

Table 29. EQVGABUFF (0*n*_8C)

Bit	Name	Access	Description	Default
15:14	RESERVED	RW	Must be set to its default.	0x0
13:0	EQVGA_BUFF	RW	Sets the buffer zone for EQ VGA_TARGET when in EQVGA Adaptive mode. Valid if EQVGA_TARGET – EQVGA_BUFF < EQVGA amplitude < EQVGA_TARGET + EQVGA_BUFF. These values are two's complement, and each LSB is 0.15 mV. These settings are valid only when EQVGA_ADAP = 1.	0x0021

Table 30. INBUFCTRL (0*n*_8D)

Bit	Name	Access	Description	Default
15:13	RESERVED	RW	Must be set to its default.	0x0
12	EQVGA_ADAP	RW	EQ VGA adaptive algorithm control. 0: EQ VGA Manual mode. 1: EQ VGA Adaptive mode.	0x1
11	VGA_ADAP	RW	VGA adaptive algorithm control. 0: VGA Manual mode. 1: VGA Adaptive mode.	0x1
10	DCOFF_ADAP	RW	DC offset correction adaptive algorithm control. 0: DC Offset Manual mode. 1: DC Offset Adaptive mode.	0x1
9	LD_EQ_TABLE	RW	Input equalizer load settings control. 0: Utilizes equalizer settings from registers EQBUFSTG0123 and EQBUFSTG45. 1: Utilizes equalizer settings from EQ_TABLE. Set to 1 when using data rate detect functionality.	0x1
8	PD_INBUF	RW	Input buffer power down control. 0: Normal operation. 1: Power down.	0x0
7	DCOFF_LOAD	RW	DC offset load. 0: DC offset DACs are frozen. 1: DC offset set by DCI1, DCI2, and DCI3. **Note** DCOFF_ADAP must be set to 0; otherwise DC offset will be in adaptive mode.	0x0
6	USE_LPF	RW	VGA0 adaptation using LPF. 0: VGA0 adaptation done with buffer. 1: VGA0 adaptation done with LPF.	0x1
5	USE_UNIT_GAIN	RW	EQVGA unity gain select. 0: EQVGA set using EQVGA_TARGET (EQ output amplitude = EQ VGA TARGET). 1: EQVGA setup for unity gain (EQ output amplitude = VGA output).	0x0
4	USE_EQVGAMAX	RW	EQVGA adaptation override. This bit is only effective when EQVGA_ADAP is set high. 0: VGA controls EQ output amplitude and EQVGA is set to maximum. 1: VGA controls VGA output amplitude.	0x1
3:0	RESERVED	RW	Do not modify.	0x0

Table 31. VGA_ADAPTLIMIT (0*n*_8E)

Bit	Name	Access	Description	Default
15:14	RESERVED	RW	Must be set to its default	0x0
13:7	INB_VGA_MAX	RW	Sets the maximum value the VGA adaptation algorithm can go to	0x60
6:0	INB_VGA_MIN	RW	Sets the minimum value the VGA adaptation algorithm can go to	0x06

Table 32. EQVGA_ADAPTLIMIT (0*n*_8F)

Bit	Name	Access	Description	Default
15:14	RESERVED	RW	Must be set to its default	0x0
13:7	INB_EQVGA_MAX	RW	Sets the maximum value the EQ VGA adaptation algorithm can go to	0x60
6:0	INB_EQVGA_MIN	RW	Sets the minimum value the EQ VGA adaptation algorithm can go to	0x06

Table 33. EQ_ADAPTLIMIT (0*n*_90)

Bit	Name	Access	Description	Default
15	RATESEL_OVR	RW	Override Data Rate Detect (DRD) LUT for INEQ registers 0: DRD normal operation 1: Override DRD LUT for INEQ registers	0x0
14	RESERVED	RW	Must be set to its default	0x0
13:7	INB_EQ_MAX	RW	Sets the maximum value the EQ adaptation algorithm can go to	0x48
6:0	INB_EQ_MIN	RW	Sets the minimum value the EQ adaptation algorithm can go to	0x00

Table 34. INEQ_RST (0*n*_B1)

Bit	Name	Access	Description	Default
15	INEQ_RST_FORCE	RW	Force INEQ adaptation reset 0: Normal operation 1: Force INEQ adaptation reset	0x0
14	INEQ_RST_LOLEN	RW	INEQ adaptation reset on LOL 0: Disabled 1: Enabled	0x0
13	INEQ_RST_LOSEN	RW	INEQ adaptation reset on LOS 0: Disabled 1: Enabled	0x0
12	INEQ_RST_MAXEQEN	RW	INEQ adaptation reset on Max EQ setting 0: Disabled 1: Enabled	0x0
11	INEQ_RST_MAXVGAEN	RW	INEQ adaptation reset on Max VGA setting 0: Disabled 1: Enabled	0x0
10	INEQ_RST_EN	RW	INEQ adaptation reset enable 0: Disabled 1: Enabled	0x0
9:0	RESERVED	RW	Must be set to its default	0x000

Table 35. EQSETREAD0123 (0*n*_C0)

Bit	Name	Access	Description	Default
15:12	EQ_SET_READ0	RO	Input equalizer first stage boost setting output	X
11:8	EQ_SET_READ1	RO	Input equalizer second stage boost setting output	X
7:4	EQ_SET_READ2	RO	Input equalizer third stage boost setting output	X
3:0	EQ_SET_READ3	RO	Input equalizer fourth stage boost setting output	X

Table 36. EQSETREAD45_DIAG (0*n*_C1)

Bit	Name	Access	Description	Default
15:12	EQ_SET_READ4	RO	Input equalizer fifth stage boost setting output	X
11:8	EQ_SET_READ5	RO	Input equalizer sixth stage boost setting output	X
7:6	RESERVED	RO	Reserved	X
5	EQVGA_DONE	RO	Output indicates when EQ VGA adaptive algorithm is done 0: Adaptation in progress 1: Adaptation is done	X
4	EQMAXED	RO	Output indicates if EQ adaptation has maxed out 0: Maximum not reached 1: Maximum reached	X
3	VGA0MAXED	RO	Output indicates if VGA has reached INB_VGA_MAX 0: VGA setting < INB_VGA_MAX 1: VGA = INB_VGA_MAX	X
2	VGA_DONE	RO	Output indicates when VGA adaptive algorithm is done 0: Adaptation in progress 1: Adaptation is done	X
1	EQ_DONE	RO	Output indicates when the input equalizer adaptive algorithm has converged 0: Adaptation in progress 1: Adaptation is done	X
0	RESERVED	RO	Reserved	X

Table 37. EQDCOFFO1 (0*n*_C3)

Bit	Name	Access	Description	Default
15:8	DC_READ0	RO	Input buffer first offset injection point setting output. Sign magnitude.	X
7:0	DC_READ1	RO	Input buffer second offset injection point setting output. Sign magnitude.	X

Table 38. EQDCOFFO2_VGASET (0*n*_C4)

Bit	Name	Access	Description	Default
15:8	DC_READ2	RO	Input buffer third offset injection point setting output. Sign magnitude.	X
7	RESERVED	RO	Reserved.	X
6:0	VGA_READ	RO	Outputs the VGA gain settings.	X

Table 39. EQCODE (0*n*_C5)

Bit	Name	Access	Description	Default
15:0	RESERVED	RO	Reserved	X

Table 40. EQHPFOUT (0*n*_C6)

Bit	Name	Access	Description	Default
15:13	RESERVED	RO	Reserved	X
12:0	HPFADC_READ	RO	High frequency digital value from ADC. Peak amplitude = (HPFADC_READ) – (HPFDCADC_READ) x 0.15 mV	X

Table 41. EQLPFOUT (0*n*_C7)

Bit	Name	Access	Description	Default
15:13	RESERVED	RO	Reserved	X
12:0	LPFADC_READ	RO	Low frequency digital value from ADC. Peak amplitude = (LPFADC_READ) – (VDCADC_READ) x 0.15 mV	X

Table 42. EQDCOUT (0*n*_C8)

Bit	Name	Access	Description	Default
15:13	RESERVED	RO	Reserved	X
12:0	VDCADC_READ	RO	Common mode voltage of EQ output from ADC. It is used to calculate the peak amplitude of LPF and EQVGA peak detectors.	X

Table 43. EQVGAOUT (0*n*_C9)

Bit	Name	Access	Description	Default
15:13	RESERVED	RO	Reserved	X

Table 43. EQVGAOUT (0*n*_C9) *(continued)*

Bit	Name	Access	Description	Default
12:0	EQVGAADC_READ	RO	EQVGA output from ADC. Peak amplitude = (EQVGAADC_READ) – (VDCADC_READ) x 0.15 mV.	X

Table 44. EQVGA0OUT (0*n*_CA)

Bit	Name	Access	Description	Default
15:13	RESERVED	RO	Reserved	X
12:0	VGA0ADC_READ	RO	VGA0 output from ADC. Peak amplitude (VGA0ADC_READ) – (VDC0ADC_READ) x 0.15 mV.	X

Table 45. EQDC0OUT (0*n*_CB)

Bit	Name	Access	Description	Default
15:13	RESERVED	RO	Reserved	X
12:0	VDC0ADC_READ	RO	Common mode voltage of VGA0 output from ADC. It is used to calculate the peak amplitude of the VGA0 peak detector.	X

Table 46. EQHPFDCOUT (0*n*_CC)

Bit	Name	Access	Description	Default
15:13	RESERVED	RO	Reserved	X
12:0	HPFDCADC_READ	RO	Common mode voltage of HPF output from ADC. It is used to calculate the peak amplitude of the HPF peak detector.	X

Table 47. EQVGAREAD (0*n*_CD)

Bit	Name	Access	Description	Default
15:8	RESERVED	RO	Reserved	X
7:0	EQVGA_READ	RO	EQ VGA active gain setting	X

3.1.2 Decision Feedback Equalizer (DFE) and CRU Registers

This section provides information about the DFE and CRU registers for all 12 channels. These registers can be accessed by programming page select register (0x7F) from 0x00

through 0x0B. These registers can also be written to all channels (broadcast) by setting the page select registers to 0x50.

Table 48. DFECRU_CTRL (0*n*_91)

Bit	Name	Access	Description	Default
15	DFECRU_LTR	RW	CRU lock to reference enable 0: Lock to incoming data 1: Force lock to reference	0x0
14	RSTN_FDET	RW	Frequency detector reset 0: Reset 1: Normal operation	0x1
13	ER_PDET	RW	Enables CRU rising edge detection 0: Ignore rising edges 1: Normal operation	0x1
12	EF_PDET	RW	Enables CRU falling edge detection 0: Ignore falling edges 1: Normal operation	0x1
11	RESERVED	RW	Must be set to its default	0x0
10	PD_DFECRU	RW	DFE and CRU power down control 0: Normal operation 1: Power down	0x0
9	PD_DFE	RW	Power down DFE only 0: DFE enabled 1: DFE powered down	0x0
8	RESERVED	RW	Must be set to its default	0x0
7	LOL_INV	RW	Loss of lock signal polarity select 0: Normal 1: Inverted	0x0
6	LOL_SRC	RW	Loss of lock signal source select 0: Loss of Lock signal 1: State of LOL_FRC bit	0x0
5	LOL_FRC	RW	Loss of lock signal force 0: If LOL_SRC = 1, LOL output = 0 1: If LOL_SRC = 1, LOL output = 1	0x0
4:1	RESERVED	RW	Must be set to its default	0x0
0	PD_DFEADAPT	RW	Power down DFE adaptation circuitry 0: Normal operation 1: DFE adaptation circuitry powered down	0x0

Table 49. DFECRU_CFVF_CFAP (0*n*_92)

Bit	Name	Access	Description	Default
15:8	CFVF	RW	DFE input amplitude coefficient	0x40
7:0	CFAP	RW	DFE target input amplitude	0x60

Table 50. DFECRU_CFBT_CFBF (0*n*_93)

Bit	Name	Access	Description	Default
15	CFBT_SIGN	RW	DFE tap 0 sign. 0: Positive sign. 1: Negative sign. These values are sign magnitude and are valid only when DFEMODE = 0x2.	0x0
14:8	CFBT	RW	DFE tap 0 magnitude. 0x00: Minimum. 0x7F: Maximum. These values are sign magnitude and are valid only when DFEMODE = 0x2.	0x00
7	CFBF_SIGN	RW	DFE tap 0 sign inverse (signed magnitude). 0: Positive sign. 1: Negative sign. These values are sign magnitude and are valid only when DFEMODE = 0x2. Set CFBF to –CFBT.	0x0
6:0	CFBF	RW	DFE tap 0 magnitude inverse (signed magnitude). 0x00: Minimum. 0x7F: Maximum. These values are sign magnitude and are valid only when DFEMODE = 0x2. Set CFBF to –CFBT.	0x00

Table 51. DFECRU_CFD1 (0*n*_94)

Bit	Name	Access	Description	Default
15:8	RESERVED	RW	Reserved.	0x00
7:0	CFD1	RW	DFE tap 1 setting. These settings are sign magnitude and are valid only when DFEMODE = 0x2.	0x00

Table 52. DFECRU_CFD2_CFD3 (0*n*_95)

Bit	Name	Access	Description	Default
15:8	CFD2	RW	DFE tap 2 setting. These values are sign magnitude and are valid only when DFEMODE = 0x02.	0x00
7:0	CFD3	RW	DFE tap 3 setting. These values are sign magnitude and are valid only when DFEMODE = 0x02.	0x00

Table 53. DFECRU_CFDC_ENAP (0*n*_96)

Bit	Name	Access	Description	Default
15:8	CFDC	RW	DFE DC offset correction. 0x80: Maximum negative offset. 0x00: Zero offset. 0x7F: Maximum positive offset. These values are sign magnitude and valid only when DFEMODE = 0x2 and DFEDCOFF_EN = 0x1.	0x00
7	DFETARG_EN	RW	DFE target amplitude enable. 0: Disabled. 1: Enabled.	0x1
6	DFE0_EN	RW	DFE tap 0 enable. 0: Disabled. 1: Enabled.	0x1
5	DFE0_INV_EN	RW	DFE tap 0 inverse enable. 0: Disabled. 1: Enabled.	0x1
4	DFE0TARG_EN	RW	DFE tap 0 target enable. 0: Disabled. 1: Enabled.	0x1
3	DFE1_EN	RW	DFE tap 1 enable. 0: Disabled. 1: Enabled.	0x1
2	DFE2_EN	RW	DFE tap 2 enable. 0: Disabled. 1: Enabled.	0x1
1	DFE3_EN	RW	DFE tap 3 enable. 0: Disabled. 1: Enabled.	0x1
0	DFEDCOFF_EN	RW	DFE DC offset restore enable. 0: Disabled. 1: Enabled. DCOFF_ADAP [10] (0*n*_8D) must be set to 1, and DFEMODE [1:0] (0*n*_9C) must be set to 0x1 to enable DFC DC offset restore.	0x1

Table 54. DFECRU_DFEAUTO (0*n*_97)

Bit	Name	Access	Description	Default
15:8	RESERVED	RW	Must be set to its default.	0x00
7:6	DFEAUTOLOS_CTRL	RW	LOS condition control. 0x0: Ignore. 0x1: Freeze taps. 0x2: Reset tap settings. 0x3: Reserved. These settings are only valid when DFEMODE = 0x1.	0x0
5:4	RESERVED	RW	Do not modify.	0x0

Table 54. DFECRU_DFEAUTO (0*n*_97) *(continued)*

Bit	Name	Access	Description	Default
3:2	DFEAUTOEQDONE_CTRL	RW	EQ_DONE bit condition control when not asserted. 0x0: Ignore. 0x1: Freeze taps. 0x2: Reset tap settings. 0x3: Reserved. These settings are only valid when DFEMODE = 0x1.	0x0
1:0	DFEAUTOVGADONE_CTRL	RW	VGA_DONE bit condition control when not asserted. 0x0: Ignore. 0x1: Freeze taps. 0x2: Reset tap settings. 0x3: Reserved. These settings are only valid when DFEMODE = 0x1.	0x1

Table 55. DFECRU_BTMX_BFMX (0*n*_98)

Bit	Name	Access	Description	Default
15:8	BTMAX	RW	Clip limit for DFE tap 0 coefficient when in DFE Adaptive mode (DFEMODE = 0x1) 0x0: Minimum 0x7F: Maximum	0x20
7:0	BFMAX	RW	Clip limit for DFE tap 0 inverse coefficient when in DFE Adaptive mode (DFEMODE = 0x1) 0x0: Minimum 0x7F: Maximum	0x20

Table 56. DFECRU_DXMX_TRMX (0*n*_99)

Bit	Name	Access	Description	Default
15:8	DXMAX	RW	Clip limit for DFE tap 1 through 3 coefficients when in DFE Adaptive mode (DFEMODE = 0x1) 0x0: Minimum 0x7F: Maximum	0x08
7:0	TRMAX	RW	Clip limit for maximum DFE target amplitude coefficient when in DFE Adaptive mode (DFEMODE = 0x1)	0x60

Table 57. DFECRU_TRMN_ERRI (0*n*_9A)

Bit	Name	Access	Description	Default
15:8	TRMIN	RW	Clip limit for minimum DFE target amplitude coefficient when in DFE Adaptive mode (DFEMODE = 0x1)	0x60

Table 57. DFECRU_TRMN_ERRI (0*n*_9A) *(continued)*

Bit	Name	Access	Description	Default
7:5	PRBS_SEL	RW	PRBS pattern select 0x0: PRBS 2^7 0x1: PRBS 2^9 0x2: PRBS 2^{11} 0x3: PRBS 2^{15} 0x4: PRBS 2^{23} 0x5: PRBS 2^{31} 0x6 - 0x7: Reserved	0x0
4:1	PRBS_GATE	RW	PRBS gate select 0xF: Infinite gate time Others: Reserved	0x0
0	PRBS_EN	RW	PRBS error check enable 0: Disabled 1: Enabled	0x0

Note Register 0*n*_9B is reserved read-write and must be set to its default (0x0000).

Table 58. DFECRU_DFEMODE (0*n*_9C)

Bit	Name	Access	Description	Default
15:13	RESERVED	RW	Must be set to its default	0x0
12	PRBS_INVERT	RW	Pattern inversion for error counter 0: Disabled 1: Enabled	0x0
11	RESERVED	RW	Do not modify	0x00
10	DFE_LOOP_SEL	RW	DFE loop mode select 0x0: CFVF is the target amplitude 0x1: CFAP is the target amplitude For more information, see Table 49, page 47.	0x0
9:6	RESERVED	RW	Do not modify	0x00
5:4	DFE_AVG	RW	DFE adaptation rate 0x0: Fastest 0x3: Slowest (recommended)	0x0
3:2	RESERVED	RW	Must be set to its default	0x0
1:0	DFEMODE	RW	DFE Adaptation mode 0x0: Freeze DFE tap settings 0x1: DFE auto adaptation enabled 0x2: DFE taps set through registers 0x3: Reset all DFE taps	0x1

Table 59. DFECRU_LENMAX (0*n*_9D)

Bit	Name	Access	Description	Default
15:12	RESERVED	RW	Must be set to its default.	0x0

Table 59. DFECRU_LENMAX (0*n*_9D) *(continued)*

Bit	Name	Access	Description	Default
11	LATCH_CNT	RW	Latch the internal error count and clock count values to the readable error and clock counter registers. 0: No action. 1: Update the readable registers (not self-clearing). See "Internal Error Counter," page 31.	0x0
10:0	RESERVED	RW	Do not modify.	0x000

Table 60. DFECRU_RATESEL (0*n*_9E)

Bit	Name	Access	Description	Default
15:8	DFE_DELAY	RW	DFE function internal delay adjust 0x55: Data rates higher than 10.50 Gbps 0x57: Data rates between 9.33 Gbps and 10.50 Gbps 0x56: Data rates between 8.25 Gbps and 9.33 Gbps 0x5E: Data rates between 7.75 Gbps and 8.25 Gbps 0x5A: Data rates between 7.20 Gbps and 7.75 Gbps 0xDA: Data rates between 6.25 Gbps and 7.20 Gbps 0x9A: Data rates below 6.25 Gbps	0xDE
7:6	VCOSEL	RW	Selects one of the three on-chip VCOs 0x0: 11.2 Gbps to 14.5 Gbps 0x1: 8.8 Gbps to 13.5 Gbps 0x2: 7.2 Gbps to 11 Gbps 0x3: 7.2 Gbps to 11 Gbps	0x1
5:4	VCODIVSEL	RW	Selects VCO clock divider ratio 0x0: Divide by 1 0x1: Divide by 2 0x2: Divide by 4 0x3: Divide by 8	0x0
3:2	RESERVED	RW	Must be set to its default	0x0
1:0	RCKSEL	RW	Channel reference clock select 0x0: Internal reference clock from FSYN0 0x1: Internal reference clock equal to external reference clock 0x2: Internal reference clock from FSYN1 0x3: Internal reference clock equal to external reference clock	0x0

Table 61. DFECRU_ERRIMODE (0*n*_9F)

Bit	Name	Access	Description	Default
15:10	RESERVED	RW	Must be set to its default	0x00
9:8	DFE_ADAPT_MODE_SEL	RW	DFE adaptation mode select. 0x0: Normal operation. 0x1: DFE tap 2 = DFE tap 1 divided by 4. Recommended setting for data rates above 11.5 Gbps.	0x0
7:1	RESERVED	RW	Must be set to its default.	0x00

Table 61. DFECRU_ERRIMODE (0*n*_9F) *(continued)*

Bit	Name	Access	Description	Default
0	ERRIMODE	RW	Clear error counter. 0: No action. 1: Clear both internal error counter and clock counter (not self-clearing).	0x0

Table 62. DFECRU_STAT_CGVF (0*n*_CE)

Bit	Name	Access	Description	Default
15	LOL	RO	Loss of lock output state 0: CRU is locked to incoming data 1: CRU is not locked to data	X
14:13	RESERVED	RO	Reserved	X
12	CKCRU128	RO	CRU clock divided by 128 output	X
11:8	RESERVED	RO	Reserved	X
7:0	CGVF_READ	RO	DFE input amplitude coefficient 0x00: Minimum 0x7F: Maximum	X

Table 63. DFECRU_CGAP_CGBT (0*n*_CF)

Bit	Name	Access	Description	Default
15:8	CGAP_READ	RO	DFE target amplitude coefficient	X
7:0	CGBT_READ	RO	DFE tap 0 (following a 1) coefficient	X

Table 64. DFECRU_CGBF (0*n*_D0)

Bit	Name	Access	Description	Default
15:8	CGBF_READ	RO	DFE tap 0 (following a 0) coefficient	X
7:0	RESERVED	RO	Reserved	X

Table 65. DFECRU_CGD1_CGD2 (0*n*_D1)

Bit	Name	Access	Description	Default
15:8	CGD1_READ	RO	DFE tap 1 coefficient. Sign magnitude.	X
7:0	CGD2_READ	RO	DFE tap 2 coefficient. Sign magnitude.	X

Table 66. DFECRU_CGD3_CGDC (0*n*_D2)

Bit	Name	Access	Description	Default
15:8	CGD3_READ	RO	DFE tap 3 coefficient. Sign magnitude.	X

Table 66. DFECRU_CGD3_CGDC (0*n*_D2) *(continued)*

Bit	Name	Access	Description	Default
7:0	CGDC_READ	RO	DFE DC offset correction output.	X

Table 67. DFECRU_ERRC0 (0*n*_D3)

Bit	Name	Access	Description	Default
15:0	ERRCNT0	RO	Bits 15:0 of the PRBS error counter. Updated upon assertion of LATCH_CNT. Number of bit errors = delta (ERRCNT0, ERRCNT1, ERRCNT2)/3).	X

Table 68. DFECRU_ERRC2 (0*n*_E8)

Bit	Name	Access	Description	Default
15	PRBS_NOSYNC	RO	Error checker out of synchronization. 0: Synchronized. 1: Out of synchronization.	X
14	ERRICNTOFLOW	RO	Error counter overflow status. 0: Not full. 1: Counter overflowed.	X
13:0	ERRCNT2	RO	Bits 45:31 of the PRBS error counter. Updated upon assertion of LATCH_CNT. Number of bit errors = delta (ERRCNT0, ERRCNT1, ERRCNT2)/3).	X

Table 69. DFECRU_ERRC1 (0*n*_E9)

Bit	Name	Access	Description	Default
15:0	ERRCNT1	RO	Bits 30:16 of PRBS error counter. Updated upon assertion of LATCH_CNT. Number of bit errors = delta (ERRCNT0, ERRCNT1, ERRCNT2)/3).	X

Table 70. DFECRU_CLKCNT1 (0*n*_FC)

Bit	Name	Access	Description	Default
15:0	CLKCNT1	RO	Bits 31:16 of internal clock counter. Updated upon assertion of LATCH_CNT.	X

Table 71. DFECRU_CLKCNT0 (0*n*_FD)

Bit	Name	Access	Description	Default
15:0	CLKCNT0	RO	Bits 15:0 of internal clock counter. Updated upon assertion of LATCH_CNT. To calculate the actual number of bits received, multiply CLKCNT by 16384.	X

3.1.3 Adaptation Timer Registers

This section provides information about the adaptation timer registers for all 12 channels. These registers can be accessed by programming page select register (0x7F) from 0x00 through 0x0B. These registers can also be written to all channels (broadcast) by setting the page select register to 0x50.

Table 72. ADAPT_TIMER_MAX (0*n*_AF)

Bit	Name	Access	Description	Default
15:0	TIMERMAX	RW	Adaptation timeout counter 0x0000: Minimum 0xFFFF: Maximum	0x0000

Table 73. ADAPT_TIMER_EN (0*n*_B0)

Bit	Name	Access	Description	Default
15	TIMEREN	RW	Adaptation timer enable 0: Disabled 1: Enabled Both TIMEREN and INEQ_ADAPT_DIS_ENABLE bits need to be set to the same value	0x0
14	INEQ_ADAPT_DIS_ENABLE	RW	Adaptation timer enable 0: Disabled 1: Enabled Both TIMEREN and INEQ_ADAPT_DIS_ENABLE bits need to be set to the same value	0x0
13:2	RESERVED	RW	Must be set to its default	0x000
1	TIMEOUT_DFELMS_DIS	RW	Adaptation timeout DFELMS disable 0: DFELMS stops adapting upon timeout 1: DFELMS continues adapting following timeout	0x0
0	TIMEOUT_INEQ_DIS	RW	Adaptation timeout INEQ disable 0: INEQ stops adapting upon timeout 1: INEQ continues adapting following timeout	0x0

Table 74. ADAPT_TIMEOUT (0*n*_E5)

Bit	Name	Access	Description	Default
15	ADAPT_TIMEOUT	RO	Adaptation timeout status 0: Adaptation still active 1: Adaptation timed out	X
14:0	RESERVED	RO	Reserved	X

Table 75. TIMEOUT_RST_CTRL (0*n*_E6)

Bit	Name	Access	Description	Default
15	TIMEOUT_FREEZE	RO	Adaptation freeze status 0: Adaptation still active 1: Adaptation stopped	X
14	TIMEOUT_PDADAPT	RO	Adaptation power down status 0: Adaptation still powered up 1: Adaptation powered down	X
13:0	RESERVED	RO	Reserved	X

3.1.4 Output Driver Registers

This section provides information about the output driver registers for all 12 channels. These registers can be accessed by programming page select register (0x7F) from 0x00 through 0x0B. These registers can also be written to all channels (broadcast) by setting the page select register to 0x50.

Table 76. OUTDRVCTRL (0*n*_A0)

Bit	Name	Access	Description	Default
15	CH_CP	RW	Adjacent channel crossover enable 0: Normal operation 1: Output adjacent channel	0x0
14	OD_SQ_HLN	RW	Transmitter output squelch polarity select 0: OUTPx/OUTNx = low/high 1: OUTPx/OUTNx = high/low	0x0
13	PRETAP_DIS	RW	KR output driver pre-tap disable 0: Enable 1: Disable	0x0
12	MAINTAP_DIS	RW	KR output driver main-tap disable 0: Enable 1: Disable	0x0
11	POSTTAP_DIS	RW	KR output driver post-tap disable 0: Enable 1: Disable	0x0
10	PD_OD	RW	Output driver power down control 0: Normal operation 1: Power down	0x0

Table 76. OUTDRVCTRL (0*n*_A0) *(continued)*

Bit	Name	Access	Description	Default
9:0	RESERVED	RW	Must be set to its default	0x000

Table 77. KR_T0TM1SET (0*n*_A1)

Bit	Name	Access	Description	Default
15:11	RESERVED	RW	Must be set to its default	0x0
10:5	MAINTAP	RW	KR output driver main-tap tail current setting 0x00: 0.5 mA 0x01: 1 mA 0x27: 20 mA	0x1E
4:0	PRETAP	RW	KR output driver pre-tap tail current setting 0x00: –3.75 mA 0x01: –3.5 mA 0x0F: 0 mA 0x1F: 4 mA	0x0B

Table 78. KR_TP1SET (0*n*_A2)

Bit	Name	Access	Description	Default
15:6	RESERVED	RW	Must be set to its default	0x000
5:0	POSTTAP	RW	KR output driver post-tap tail current setting 0x00: –0.25 mA 0x01: –0.5 mA 0x3F: –16 mA	0x10

Table 79. OUTDRV_TXINV (0*n*_A3)

Bit	Name	Access	Description	Default
15:4	RESERVED	RW	Must be set to its default	0x000
3	TX_INV	RW	Transmitter output polarity select 0: Normal 1: Inverted	0x0
2	PRETAP_INV	RW	Pre-tap inversion 0: Non-inverted 1: Inverted	0x0
1	MAINTAP_INV	RW	Main-tap inversion 0: Non-inverted 1: Inverted	0x0
0	POSTTAP_INV	RW	Post-tap inversion 0: Non-inverted 1: Inverted	0x0

Table 80. OUTDRV_SLEW (0*n*_A4)

Bit	Name	Access	Description	Default
15:6	RESERVED	RW	Must be set to its default	0x000
5:2	OD_IND_BYP	RW	Output peaking inductor bypass select 0x0: Minimum bypass 0xF: Maximum bypass	0x0
1:0	OD_SLEW	RW	Output slew rate select 0x0: V_{OUT} rise/fall ~25 ps 0x1: V_{OUT} rise/fall ~35 ps 0x2: V_{OUT} rise/fall ~45 ps 0x3: V_{OUT} rise/fall ~60 ps	0x0

Table 81. KRCTRL (0*n*_D4)

Bit	Name	Access	Description	Default
15	PRETAP_SIGN	RO	Pre-tap KR output driver sign indicator 0: Inverted 1: Not inverted	X
14	POSTTAP_DISQ	RO	Post-tap KR output driver disable indicator 0: Enabled 1: Disabled	X
13	MAINTAP_DISQ	RO	Main-tap KR output driver disable indicator 0: Enabled 1: Disabled	X
12	PRETAP_DISQ	RO	Pre-tap KR output driver disable indicator 0: Enabled 1: Disabled	X
11:0	RESERVED	RO	Reserved	X

Note Registers 0*n*_D5 through 0*n*_DD are reserved and read-only.

3.1.5 Loss of Signal and Squelch Registers

This section provides information about the LOS and squelch registers for all 12 channels. These registers can be accessed by programming page select register (0x7F) from 0x00 through 0x0B. These registers can also be written to all channels (broadcast) by setting the page select register to 0x50.

Table 82. LOSASSRT (0*n*_A5)

Bit	Name	Access	Description	Default
15:12	RESERVED	RW	Must be set to its default	0x0

Table 82. LOSASSRT (0*n*_A5) *(continued)*

Bit	Name	Access	Description	Default
11:0	LOS_ASSERT	RW	Sets the LOS assert threshold 0x000: Invalid 0x001 – 0xFFF: Hexadecimal value of the threshold in tenths of millivolts peak to peak (For example: 0x64 = 10 mVpp and 0xFFF = 409 mVpp)	0x3E8

Table 83. LOSDASSRT (0*n*_A6)

Bit	Name	Access	Description	Default
15:12	RESERVED	RW	Must be set to its default.	0x0
11:0	LOS_DASSRT	RW	Sets the LOS de-assert threshold. 0x000: Invalid 0x001 - 0xFFF: Hexadecimal value of the threshold in tenths of millivolts peak to peak (For example: 0x64 = 10 mVpp and 0xFFF = 409 mVpp) For proper hysteresis, it is recommended that LOS_DASSRT be 25 percent or more than LOS_ASSERT.	0x4EA

Table 84. LOSCTRL (0*n*_A7)

Bit	Name	Access	Description	Default
15:12	RESERVED	RW	Must be set to its default	0x0
11	PD_LOS	RW	Loss of signal power down control 0: Normal operation 1: Power down	0x0
10:0	RESERVED	RW	Must be set to its default	0x000

Note Register 0*n*_A8 is reserved read-write and must be set to its default (0x0000).

Table 85. SQCTRL (0*n*_A9)

Bit	Name	Access	Description	Default
15	LOS_INV	RW	Loss of signal polarity select 0: Normal 1: Inverted	0x0
14	LOS_SRC	RW	Loss of signal source select 0: LOS circuitry 1: State of LOS_FRC bit	0x0
13	LOS_FRC	RW	Loss of signal force 0: If LOS_SRC = 1, LOS output = 0 1: If LOS_SRC = 1, LOS output = 1	0x0

Table 85. SQCTRL (0*n*_A9) *(continued)*

Bit	Name	Access	Description	Default
12	EQSQ_INV	RW	Input equalizer squelch polarity select 0: Normal 1: Inverted The input equalizer freezes the tap settings for each stage when squelch is asserted	0x0
11	EQSQ_SRC	RW	Input equalizer squelch source select 0: Squelch signal selected by setting SQ_SEL bits 1: State of EQSQ_FRC bit	0x0
10	EQSQ_FRC	RW	Input equalizer squelch force 0: If EQSQ_SRC = 1, Normal operation 1: If EQSQ_SRC = 1, Input equalizer freezes the tap settings	0x0
9:8	SQ_SEL	RW	Selects whether the equalizer, DFE, and output driver squelches on LOS or LOL 0x0: Squelch on LOS condition 0x1: Squelch on LOL condition 0x2: Squelch on LOS or LOL condition 0x3: Squelch on LOS or LOL condition	0x0
7	DFESQ_INV	RW	DFE squelch polarity select 0: Normal 1: Inverted The DFE taps freezes all tap settings when squelch is asserted	0x0
6	DFESQ_SRC	RW	DFE squelch source select 0: Squelch signal selected by setting SQ_SEL bits 1: State of DFESQ_FRC bit	0x0
5	DFESQ_FRC	RW	DFE squelch force 0: If DFESQ_SRC = 1, Normal operation 1: If DFESQ_SRC = 1, DFE freezes the tap settings	0x0
4	ODSQ_INV	RW	Output driver squelch polarity select 0: Normal 1: Inverted The output driver sets the output pads to be steady high or low	0x0
3	ODSQ_SRC	RW	Output driver squelch source select 0: Squelch signal selected by setting SQ_SEL bits 1: State of ODSQ_FRC bit	0x0
2	ODSQ_FRC	RW	Output driver squelch force 0: If ODSQ_SRC = 1, Normal operation 1: If ODSQ_SRC = 1, output driver squelches the output signals to be high or low	0x0
1	SQ_DIS	RW	Squelch disable control 0: Normal operation 1: Disable squelch and freeze functions unless forced	0x0
0	RESERVED	RW	Must always be set to 1.	0x0

Table 86. CHPD_FCOVR (0*n*_AA)

Bit	Name	Access	Description	Default
15	PD_CH	RW	Channel power down control 0: Normal operation 1: Power down	0x0
14:13	CRUDIVSQSEL	RW	CKDIV2048 squelch select 0x0: Ignore LOS and LOL 0x1: Squelch on LOS or LOL 0x2: Squelch on LOL 0x3: Squelch on LOS	0x0
12:0	RESERVED	RW	Must be set to its default	0x000

Table 87. LOSAMPPP (0*n*_DE)

Bit	Name	Access	Description	Default
15:12	RESERVED	RO	Reserved	X
11:0	LOS_AMP_PP	RO	Input signal differential amplitude digital output 0x000: Input = 0 mVpp 0x01F: Input = 3.1 mVpp 0x800: Input = 204.8 mVpp 0xFFF: Input = 409.5 mVpp	X

Table 88. LOSRD1 (0*n*_DF)

Bit	Name	Access	Description	Default
15	EQ_SQ	RO	Input equalizer squelch signal output 0: Normal operation 1: Input equalizer is squelched to freeze its tap settings	X
14	DFE_SQ	RO	DFE squelch signal output 0: Normal operation 1: DFE is squelched to freeze its tap settings	X
13	OD_SQ	RO	Output driver squelch signal output 0: Normal operation 1: Output driver has squelched the outputs to high or low	X
12:0	RESERVED	RO	Reserved	X

3.1.6 Data Rate Detect Registers

This section provides information about the data rate detection registers for all 12 channels. These registers can be accessed by programming page select register (0x7F)

from 0x00 through 0x0B. These registers can also be written to all channels (broadcast) by setting the page select register to 0x50.

Table 89. DRDA (0*n*_AB)

Bit	Name	Access	Description	Default
15:0	DRD_THRESHOLDA	RW	Data edge count for threshold A	0x0000

Table 90. DRDB (0*n*_AC)

Bit	Name	Access	Description	Default
15:0	DRD_THRESHOLDB	RW	Data edge count for threshold B	0x0000

Table 91. DRDC (0*n*_AD)

Bit	Name	Access	Description	Default
15:0	DRD_THRESHOLDC	RW	Data edge count for threshold C	0x0000

Table 92. DRD_CTRL (0*n*_AE)

Bit	Name	Access	Description	Default
15:13	RESERVED	RW	Must be set to its default	0x0
12	DRD_DIGAVG	RW	Average data edge count 0: Normal operation 1: Data edge count averaging enabled	0x0
11	DRD_ENABLE	RW	Data rate detect enable 0: Disabled 1: Enabled	0x0
10:0	DRD_COUNTMAX	RW	Data rate detect integration time 0x000: Minimum 0x7FF: Maximum	0x000

Table 93. DRDCOUNT (0*n*_E3)

Bit	Name	Access	Description	Default
15:0	DCT	RO	Data rate detect data edge count	X

Table 94. DRDSEL (0*n*_E4)

Bit	Name	Access	Description	Default
15:14	DSEL	RO	Data Rate Detect mode 0x0: Data rate < Threshold A 0x1: Threshold A < Data rate < Threshold B 0x2: Threshold B < Data rate < Threshold C 0x3: Threshold C < Data rate	X
13:0	RESERVED	RO	Reserved	X

Table 95. LUTB1 (0*n*_B4)

Bit	Name	Access	Description	Default
15	EQ_ADAP_LUT	RW	LUT B: Adaptive input equalization algorithm control. 0: EQ Manual mode 1: EQ Adaptive mode	0x0
14	RESERVED	RW	Must be set to its default.	0x0
13:0	EQ_DIFF_LUT	RW	LUT B: Sets the difference between target high-pass and low-pass filter values when in Adaptive mode. These values are two's complement, and each LSB is 0.15 mV. These settings are valid only when EQ_ADAP_LUT = 1 or if LD_EQ_TABLE = 1.	0x0000

Table 96. LUTB2 (0*n*_B5)

Bit	Name	Access	Description	Default
15:7	RESERVED	RW	Must be set to its default	0x000
6:0	EQ_TABLE_LUT	RW	LUT B: Input equalizer on-chip look-up table for equalization settings 0x00: Minimum 0x7F: Maximum These settings are valid only when EQ_ADAP_LUT = 0 or if LD_EQ_TABLE = 1	0x00

Table 97. LUTB3 (0*n*_B6)

Bit	Name	Access	Description	Default
15:6	RESERVED	RW	Must be set to its default	0x000
5:4	DFE_AVG_LUT	RW	DFE adaptation rate 0x0: Fastest 0x3: Slowest (recommended)	0x0
3:2	RESERVED	RW	Must be set to its default	0x0

Table 97. LUTB3 (0*n*_B6) *(continued)*

Bit	Name	Access	Description	Default
1:0	DFEMODE_LUT	RW	LUT B: DFE adaptation mode 0x0: Freeze DFE tap settings 0x1: DFE auto adaptation enabled 0x2: DFE taps set through registers 0x3: Reset all DFE taps	0x0

Table 98. LUTB4 (0*n*_B7)

Bit	Name	Access	Description	Default
15:8	DFE_DELAY_LUT	RW	LUT B: DFE function internal delay adjust 0x55: Data rates higher than 10.50 Gbps 0x57: Data rates between 9.33 Gbps and 10.50 Gbps 0x56: Data rates between 8.25 Gbps and 9.33 Gbps 0x5E: Data rates between 7.75 Gbps and 8.25 Gbps 0x5A: Data rates between 7.20 Gbps and 7.75 Gbps 0xDA: Data rates between 6.25 Gbps and 7.20 Gbps 0x9A: Data rates below 6.25 Gbps	0x00
7:6	VCOSEL_LUT	RW	LUT B: Selects one of the three on-chip VCOs 0x0: 11.2 Gbps to 14.5 Gbps 0x1: 8.8 Gbps to 13.5 Gbps 0x2: 7.2 Gbps to 11 Gbps 0x3: 7.2 Gbps to 11 Gbps	0x0
5:4	VCODIVSEL_LUT	RW	LUT B: Selects VCO clock divider ratio 0x0: Divide by 1 0x1: Divide by 2 0x2: Divide by 4 0x3: Divide by 8	0x0
3:2	RESERVED	RW	Must be set to its default	0x0
1:0	RCKSEL_LUT	RW	LUT B: Channel reference clock select 0x0: Internal reference clock from FSYN0 0x1: Internal reference clock equal to external reference clock 0x2: Internal reference clock from FSYN1 0x3: Internal reference clock equal to external reference clock	0x0

Table 99. LUTB5 (0*n*_B8)

Bit	Name	Access	Description	Default
15:6	RESERVED	RW	Must be set to its default	0x000
5:2	OD_IND_BYP_LUT	RW	LUT B: Output peaking inductor bypass select 0x0: Minimum bypass 0xF: Maximum bypass	0x0
1:0	OD_SLEW_LUT	RW	LUT B: Output slew rate select 0x0: V_{OUT} rise/fall ~25 ps 0x1: V_{OUT} rise/fall ~35 ps 0x2: V_{OUT} rise/fall ~45 ps 0x3: V_{OUT} rise/fall ~60 ps	0x0

Table 100. LUTC1 (0*n*_BE)

Bit	Name	Access	Description	Default
15	EQ_ADAP_LUT	RW	LUT C: Adaptive input equalization algorithm control. 0: EQ Manual mode 1: EQ Adaptive mode	0x0
14	RESERVED	RW	Must be set to its default.	0x0
13:0	EQ_DIFF_LUT	RW	LUT C: Sets the difference between target high-pass and low-pass filter values when in Adaptive mode. These values are two's complement, and each LSB is 0.15 mV. These settings are valid only when EQ_ADAP_LUT = 1 or if LD_EQ_TABLE = 1.	0x0000

Table 101. LUTC2 (0*n*_BF)

Bit	Name	Access	Description	Default
15:7	RESERVED	RW	Must be set to its default	0x000
6:0	EQ_TABLE_LUT	RW	LUT C: Input equalizer on-chip look-up table for equalization settings 0x00: Minimum 0x7F: Maximum These settings are valid only when EQ_ADAP_LUT = 0 or if LD_EQ_TABLE = 1	0x00

Note Registers 0*n*_E0 through 0*n*_E2 are reserved and read-only.

Table 102. LUTC3 (0*n*_EA)

Bit	Name	Access	Description	Default
15:6	RESERVED	RW	Must be set to its default	0x0000
5:4	DFE_AVG_LUT	RW	DFE adaptation rate 0x0: Fastest 0x3: Slowest (recommended)	0x0
3:2	RESERVED	RW	Must be set to its default	0x0000
1:0	DFEMODE_LUT	RW	LUT C: DFE adaptation mode 0x0: Freeze DFE tap settings 0x1: DFE auto adaptation enabled 0x2: DFE taps set through registers 0x3: Reset all DFE taps	0x0

Table 103. LUTC4 (0*n*_EB)

Bit	Name	Access	Description	Default
15:8	DFE_DELAY_LUT	RW	LUT C: DFE function internal delay adjust 0x55: Data rates higher than 10.50 Gbps 0x57: Data rates between 9.33 Gbps and 10.50 Gbps 0x56: Data rates between 8.25 Gbps and 9.33 Gbps 0x5E: Data rates between 7.75 Gbps and 8.25 Gbps 0x5A: Data rates between 7.20 Gbps and 7.75 Gbps 0xDA: Data rates between 6.25 Gbps and 7.20 Gbps 0x9A: Data rates below 6.25 Gbps	0x00
7:6	VCOSEL_LUT	RW	LUT C: Selects one of the three on-chip VCOs 0x0: 11.2 Gbps to 14.5 Gbps 0x1: 8.8 Gbps to 13.5 Gbps 0x2: 7.2 Gbps to 11 Gbps 0x3: 7.2 Gbps to 11 Gbps	0x0
5:4	VCODIVSEL_LUT	RW	LUT C: Selects VCO clock divider ratio 0x0: Divide by 1 0x1: Divide by 2 0x2: Divide by 4 0x3: Divide by 8	0x0
3:2	RESERVED	RW	Must be set to its default.	0x0
1:0	RCKSEL_LUT	RW	LUT C: Channel reference clock select 0x0: Internal reference clock from FSYN0 0x1: Internal reference clock equal to external reference clock 0x2: Internal reference clock from FSYN1 0x3: Internal reference clock equal to external reference clock	0x0

Table 104. LUTC5 (0*n*_EC)

Bit	Name	Access	Description	Default
15:6	RESERVED	RW	Must be set to its default	0x000
5:2	OD_IND_BYP_LUT	RW	LUT C: Output peaking inductor bypass select 0x0: Minimum bypass 0xF: Maximum bypass	0x000
1:0	OD_SLEW_LUT	RW	LUT C: Output slew rate select 0x0: V_{OUT} rise/fall ~25 ps 0x1: V_{OUT} rise/fall ~35 ps 0x2: V_{OUT} rise/fall ~45 ps 0x3: V_{OUT} rise/fall ~60 ps	0x0

Table 105. LUTD1 (0*n*_F2)

Bit	Name	Access	Description	Default
15	EQ_ADAP_LUT	RW	LUT D: Adaptive input equalization algorithm control. 0: EQ Manual mode 1: EQ Adaptive mode	0x0

Table 105. LUTD1 (0*n*_F2) *(continued)*

Bit	Name	Access	Description	Default
14	RESERVED	RW	Must be set to its default.	0x0
13:0	EQ_DIFF_LUT	RW	LUT D: Sets the difference between target high-pass and low-pass filter values when in Adaptive mode. These values are two's complement, and each LSB is 0.15 mV. These settings are valid only when EQ_ADAP_LUT = 1 or if LD_EQ_TABLE = 1.	0x000

Table 106. LUTD2 (0*n*_F3)

Bit	Name	Access	Description	Default
15:7	RESERVED	RW	Must be set to its default	0x000
6:0	EQ_TABLE_LUT	RW	LUT D: Input equalizer on-chip look-up table for equalization settings 0x00: Minimum 0x7F: Maximum These settings are valid only when EQ_ADAP_LUT = 1 or if LD_EQ_TABLE = 1	0x00

Table 107. LUTD3 (0*n*_F4)

Bit	Name	Access	Description	Default
15:6	RESERVED	RW	Must be set to its default	0x0000
5:4	DFE_AVG_LUT	RW	DFE adaptation rate 0x0: Fastest 0x3: Slowest (recommended)	0x0
3:2	RESERVED	RW	Must be set to its default	0x0000
1:0	DFEMODE_LUT	RW	LUT D: DFE adaptation mode 0x0: Freeze DFE tap settings 0x1: DFE auto adaptation enabled 0x2: DFE taps set through registers 0x3: Reset all DFE taps	0x0

Table 108. LUTD4 (0*n*_F5)

Bit	Name	Access	Description	Default
15:8	DFE_DELAY_LUT	RW	LUT D: DFE function internal delay adjust 0x55: Data rates higher than 10.50 Gbps 0x57: Data rates between 9.33 Gbps and 10.50 Gbps 0x56: Data rates between 8.25 Gbps and 9.33 Gbps 0x5E: Data rates between 7.75 Gbps and 8.25 Gbps 0x5A: Data rates between 7.20 Gbps and 7.75 Gbps 0xDA: Data rates between 6.25 Gbps and 7.20 Gbps 0x9A: Data rates below 6.25 Gbps	0x000
7:6	VCOSEL_LUT	RW	LUT D: Selects one of the three on-chip VCOs 0x0: 11.2 Gbps to 14.5 Gbps 0x1: 8.8 Gbps to 13.5 Gbps 0x2: 7.2 Gbps to 11 Gbps 0x3: 7.2 Gbps to 11 Gbps	0x0
5:4	VCODIVSEL_LUT	RW	LUT D: Selects VCO clock divider ratio 0x0: Divide by 1 0x1: Divide by 2 0x2: Divide by 4 0x3: Divide by 8	0x0
3:2	RESERVED	RW	Must be set to its default	0x0
1:0	RCKSEL_LUT	RW	LUT D: Channel reference clock select 0x0: Internal reference clock from FSYN0 0x1: Internal reference clock equal to external reference clock 0x2: Internal reference clock from FSYN1 0x3: Internal reference clock equal to external reference clock	0x0

Table 109. LUTD5 (0*n*_F6)

Bit	Name	Access	Description	Default
15:6	RESERVED	RW	Must be set to its default	0x0000
5:2	OD_IND_BYP_LUT	RW	LUT D: Output peaking inductor bypass select 0x0: Minimum bypass 0xF: Maximum bypass	0x000
1:0	OD_SLEW_LUT	RW	LUT D: Output slew rate select 0x0: V_{OUT} rise/fall ~25 ps 0x1: V_{OUT} rise/fall ~35 ps 0x2: V_{OUT} rise/fall ~45 ps 0x3: V_{OUT} rise/fall ~60 ps	0x0

3.2 VScope Registers

This section provides information about the registers for the 12 identical VScope input signal monitoring integrated circuit blocks. These registers can be accessed by programming page select register (0x7F) with a value of 2*n,* where *n* goes from 0x0 through 0xB (for example, from 0x20 through 0x2B). These registers can also be written to all 12 VScope input signal monitoring integrated circuit blocks globally (broadcast) by setting the page select register to 0x60.

Table 110. VSCOPEV (2*n*_80)

Bit	Name	Access	Description	Default
15	VSCOPEV1SIGN	RW	Sets the voltage slicing level for the main path Values are sign magnitude 0: Positive sign 1: Negative sign	0x0
14:8	VSCOPEV1MAG	RW	Sets the voltage slicing level for the main path Values are sign magnitude 0x00: Minimum 0x7F: Maximum	0x00
7	VSCOPEV2SIGN	RW	Sets the voltage slicing level for the auxiliary path Values are sign magnitude 0: Positive sign 1: Negative sign	0x0
6:0	VSCOPEV2MAG	RW	Sets the voltage slicing level for the auxiliary path Values are sign magnitude 0x00: Minimum 0x7F: Maximum	0x00

Table 111. VSCOPETIME (2*n*_81)

Bit	Name	Access	Description	Default
15:8	RESERVED	RW	Must be set to its default	0x00
7:0	VSCOPETIME	RW	Sets the phase sampling point 0x00: Minimum 0xFF: Maximum Data rates between 7 Gbps and 14.5 Gbps use steps of 1/64 UI Data rates between 3.5 Gbps and 7 Gbps use steps of 1/128 UI Data rates between 2 Gbps and 3.5 Gbps use steps of 1/256 UI	0x00

Table 112. VSCOPECTRL (2*n*_82)

Bit	Name	Access	Description	Default
15:14	ERRDETFUNC	RW	Error detect function. 0x0: No interrupt. Counter output is error counter value. Both counters are stopped if clock counter limit is reached. 0x1: Interrupt if clock counter limit is reached. Counter output is error counter value and both counters are stopped. 0x2: Interrupt if error counter limit is reached. Counter output is clock counter value. Both counters are stopped. 0x3: No interrupt. Counter output is error counter value. Clock counter is stopped.	0x0
13:9	COUNTER_PER	RW	Preload value of the clock counter. After preload. Clock counter = 2(COUNT_PER + 1) – 1.	0x00
8	TRIGGER	RW	Error counting enable. 0: Error counting disabled 1: Error counting enable; if CNT_ENA = 1 and TRIGENA = 1	0x0
7	TRIGEN	RW	Trigger enable. 0: Error counting not dependant on the state of TRIGGER 1: Error counting is dependant on the state on TRIGGER	0x0
6:2	PRELOAD_VAL	RW	Preload value of the error counter. After preload. Error counter = 2(PRELOAD_VAL + 1) – 1.	0x00
1	CNT_EN	RW	Counter enable. 0: Counters load in the preload values 1: Counters continue counting	0x0
0	VSCOPE_INSEL	RW	VScope input select. 0: Input to VScope is the output of the DFE summing node 1: Input to VScope is the output of the input equalizer	0x0

Table 113. VSCOPEPD (2*n*_83)

Bit	Name	Access	Description	Default
15	HALFCLK	RW	Divide VCO clock by 2 0: Normal operation 1: Divide VCO clock by 2 (recommended setting)	0x0
14:9	RESERVED	RW	Must be set to its default	0x00
8	VSCOPE_TEST		VSCOPE_MODE 0: Debut mode 1: Normal operation	0x0
7:2	RESERVED		Must be set to its default	0x00
1	VSCOPE_RSTN	RW	VScope counter reset signal 0: VScope counter is reset 1: Normal operation	0x0

Table 113. VSCOPEPD (2*n*_83) *(continued)*

Bit	Name	Access	Description	Default
0	PD_VSCOPE	RW	VScope down control 0: Normal operation 1: Power down	0x1

Note Registers 2*n*_84 through 2*n*_8A are reserved and read-only.

Table 114. VSCOPECNT_MSB (2*n*_C0)

Bit	Name	Access	Description	Default
15	RESERVED	RO	Reserved	X
14:0	COUNTER	RO	Upper VScope counter Upper 15 bits of the 31 bit clock or error counter output depending on the state of ERRDETFUNC bits	X

Table 115. VSCOPECNT_LSB (2*n*_C1)

Bit	Name	Access	Description	Default
15:0	COUNTER	RO	Lower VScope counter Lower 16 bits of the 31 bit clock or error counter output depending on the state of ERRDETFUNC bits	X

Table 116. VSCOPETST0_FLAGS (2*n*_C3)

Bit	Name	Access	Description	Default
15	INTR_DONE	RO	Output of the count interrupt set through ERRDETFUNC	X
14	DONE_STICKY	RO	Counter saturation detect 0: Counter did not saturate 1: Counter saturated	X
13:0	RESERVED	RO	Reserved	X

Note Registers 2*n*_C4 through 2*n*_C8 are reserved and read-only.

3.3 Frequency Synthesizer Registers

This section provides information about the registers for the two frequency synthesizers. These registers can be accessed by programming page select register (0x7F) to 0x30 for frequency synthesizer 0 (*f* = 0), and 0x31 for frequency synthesizer

1 (*f* = 1). These registers can also be written to both frequency synthesizers (broadcast) by setting the page select register to 0x70.

Table 117. FSYNM_NVAL (3*f*_80)

Bit	Name	Access	Description	Default
15:8	MVAL	RW	M coefficient of the frequency synthesizer transfer function. For more information, see "Frequency Synthesizers," page 24.	0x28
7:0	NVAL	RW	N coefficient of the frequency synthesizer transfer function. For more information, see "Frequency Synthesizers," page 24.	0x41

Table 118. FSYNFVAL_MSB (3*f*_81)

Bit	Name	Access	Description	Default
15:8	RESERVED	RW	Must be set to its default.	0x00
7:0	FVAL_MSB	RW	Upper 8 bits of the 24-bit F coefficient of the frequency synthesizer transfer function.For more information, see "Frequency Synthesizers," page 24. FVAL is two's complement.	0x08

Table 119. FSYNFVAL_LSB (3*f*_82)

Bit	Name	Access	Description	Default
15:0	FVAL_LSB	RW	Lower 16 bits of the 24-bit F coefficient of the frequency synthesizer transfer function. For more information, see "Frequency Synthesizers," page 24. FVAL is two's complement.	0x7A00

Table 120. FSYNRVAL_MSB (3*f*_83)

Bit	Name	Access	Description	Default
15:8	RESERVED	RW	Must be set to its default.	0x00
7:0	RVAL_MSB	RW	Upper 8 bits of the 24 bit R coefficient of the frequency synthesizer transfer function. For more information, see "Frequency Synthesizers," page 24. RVAL is two's complement.	0x0F

Table 121. FSYNRVAL_LSB (3*f*_84)

Bit	Name	Access	Description	Default
15:0	RVAL_LSB	RW	Lower 16 bits of the 24 bit R coefficient of the frequency synthesizer transfer function. For more information, see "Frequency Synthesizers," page 24. RVAL is two's complement.	0x9C18

Table 122. FSYNTST (3*f*_85)

Bit	Name	Access	Description	Default
15:4	RESERVED	RW	Must be set to its default	0x000
3	PD	RW	Frequency synthesizer power down control 0: Normal operation 1: Power down	0x0 for 30_85 0x1 for 31_85
2:0	RESERVED	RW	Must be set to its default	0x0

3.4 Digital Core Registers

This section provides information about the digital core registers.

Table 123. ANMUXSEL (40_80)

Bit	Name	Access	Description	Default
15:12	ANMUX_COREBLK_SEL	RW	Core analog multiplexer select 0xC: VTEMP = Temperature monitor output 0xE: VDDDIV2 = VDD divide-by-2 output Others: Reserved	0xC
11	ANMUX_COREBLK_EN	RW	Core analog multiplexer output enable 0: Output disabled 1: Output enabled	0x1
10	ANMUX_ADCIN_EN	RW	Core analog multiplexer ADC input enable 0: Input to ADC from amux is disabled 1: Input to ADC from amux is enabled	0x1
9:0	RESERVED	RW	Must be set to its default	0x000

Table 124. DGMUXCTRL (40_81)

Bit	Name	Access	Description	Default
15:12	DGMUX_SEL	RW	Digital multiplexer channel select 0x0: Channel 0 0x1: Channel 1 0x2: Channel 2 0x3: Channel 3 0x4: Channel 4 0x5: Channel 5 0x6: Channel 6 0x7: Channel 7 0x8: Channel 8 0x9: Channel 9 0xA: Channel 10 0xB: Channel 11 0xC: DGMUXCORE 0xD - 0xF: Reserved	0x4000

Table 124. DGMUXCTRL (40_81) *(continued)*

Bit	Name	Access	Description	Default
11:8	DGMUX_CORE_SEL	RW	Digital multiplexer select When DGMUX_SEL is between 0x0 and 0xB: 0x0: LOS 0x1: LOL 0x2: CKCRU128 0x3: VGA_DONE 0x4: EQ_DONE 0x5: INB_OFB_SMX 0x6: LOS_LAT_OUT 0x7: OCK_VSCOPE 0x8: DRD_DSEL[0] 0x9: DRD_DSEL[1] 0xA - 0xF: Reserved When DGMUX_SEL is set to 0xC: 0x0: LOS_OR 0x1: LOL_OR 0x2 - 0xF: Reserved	0x0
7	DGMUX_LTCH	RW	Digital multiplexer latch control 0: Latch disabled 1: Latch enabled	0x0
6	DGMUX_RST	RW	Digital multiplexer latch reset 0: Latch is not reset 1: Latch is reset	0x0
5:0	RESERVED	RW	Do not modify	0x0

Table 125. RCKINCTRL (40_82)

Bit	Name	Access	Description	Default
15	PD_XTAL	RW	Crystal oscillator input power down control 0: Normal operation 1: Power down	0x0
14	PD_RCKI	RW	Reference clock input buffer power down control 0: Normal operation 1: Power down	0x1
13	RCKI_ENBIASP	RW	Reference clock true input internal bias enable 0: Internal bias disabled 1: Internal bias enabled	0x1
12	RCKI_ENBIASN	RW	Reference clock complement input internal bias enable 0: Internal bias disabled 1: Internal bias enabled	0x1
11	OSC_SEL	RW	Reference clock input select 0: Input from reference clock input buffer is selected 1: Input from crystal oscillator is selected	0x1
10:0	RESERVED	RW	Must be set to its default	0x000

Table 126. RCK0CTRL (40_83)

Bit	Name	Access	Description	Default
15	RCKO_DIS	RW	Reference clock output buffer disable 0: Output buffer enabled 1: Output buffer disabled	0x0
14	RCKO_ODMD	RW	Reference clock output buffer Open Drain mode 0: Normal operation 1: Open drain output configuration enabled	0x0
13	RCKO_SLWMD	RW	Reference clock output buffer slew rate 0: Normal operation 1: Slew rate enabled	0x0
12	RCKO_PULUP_EN	RW	Reference clock output buffer internal pull-up 0: Normal operation 1: Internal pull-up enabled	0x0
11	RCKO_INV	RW	Reference clock output buffer polarity select 0: Normal 1: Inverted	0x0
10:0	RESERVED	RW	Must be set to its default	0x000

Table 127. ANMUXCHEN (40_84)

Bit	Name	Access	Description	Default
15:12	RESERVED	RW	Must be set to its default	0x0
11	ANMUX_CH_EN11	RW	Channel 11 analog multiplexer enable 0: Disabled 1: Enabled	0x0
10	ANMUX_CH_EN10	RW	Channel 10 analog multiplexer enable 0: Disabled 1: Enabled	0x0
9	ANMUX_CH_EN9	RW	Channel 9 analog multiplexer enable 0: Disabled 1: Enabled	0x0
8	ANMUX_CH_EN8	RW	Channel 8 analog multiplexer enable 0: Disabled 1: Enabled	0x0
7	ANMUX_CH_EN7	RW	Channel 7 analog multiplexer enable 0: Disabled 1: Enabled	0x0
6	ANMUX_CH_EN6	RW	Channel 6 analog multiplexer enable 0: Disabled 1: Enabled	0x0
5	ANMUX_CH_EN5	RW	Channel 5 analog multiplexer enable 0: Disabled 1: Enabled	0x0

Table 127. ANMUXCHEN (40_84) *(continued)*

Bit	Name	Access	Description	Default
4	ANMUX_CH_EN4	RW	Channel 4 analog multiplexer enable 0: Disabled 1: Enabled	0x0
3	ANMUX_CH_EN3	RW	Channel 3 analog multiplexer enable 0: Disabled 1: Enabled	0x0
2	ANMUX_CH_EN2	RW	Channel 2 analog multiplexer enable 0: Disabled 1: Enabled	0x0
1	ANMUX_CH_EN1	RW	Channel 1 analog multiplexer enable 0: Disabled 1: Enabled	0x0
0	ANMUX_CH_EN0	RW	Channel 0 analog multiplexer enable 0: Disabled 1: Enabled	0x0

Note Registers 40_85 and 40_86 are reserved read-write and must be set to their default (0x0000).

Table 128. RCKMUXOVR (40_87)

Bit	Name	Access	Description	Default
15:4	RESERVED	RW	Must be set to its default	0x000
3	RCK_MUXSEL_SRC	RW	Reference clock output source select 0: Output reference clock is set per register RCK_MUXSEL 1: Output reference clock is equal to input reference clock	0x1
2:0	RESERVED	RW	Must be set to its default	0x0

Table 129. RCKMUXSEL (40_88)

Bit	Name	Access	Description	Default
15:6	RESERVED	RW	Must be set to its default	0x000
5:4	DGMUX_LAT_SEL	RW	Digital multiplexer latch select 0x0: Non-latched output 0x1: Latch low output 0x2: Latch high output 0x3: Non-latched output	0x0
3:0	RCK_MUXSEL	RW	Reference clock output select 0x0-0xB: Selects which channel's internal reference clock to output 0xC-0xF: Selects channel 11's internal reference clock to output	0x0

Note Registers 40_89 and 40_8A are reserved read-write and must be set to their default (0x0).

Table 130. DGMUXRD (40_C0)

Bit	Name	Access	Description	Default
15	RESERVED	RO	Reserved	X
14	MUXLTCHLO	RO	Digital multiplexer latch low output	X
13	MUXLTCHHI	RO	Digital multiplexer latch high output	X
12	DGMUXO	RO	Digital multiplexer output	X
11:0	RESERVED	RO	Reserved	X

Table 131. ADCOUT (40_C1)

Bit	Name	Access	Description	Default
15:13	RESERVED	RO	Reserved	X
12:0	ADC_DOUT	RO	On-die ADC output	X

Table 132. CHIPID (40_C2)

Bit	Name	Access	Description	Default
15:4	CHIPID	RO	Device identifier Lowest 12 bits of the Vitesse part number	0x227
3:0	REVID	RO	Device version identifier Latest revision of the device	0xB

Table 133. LOSSTAT (40_C3)

Bit	Name	Access	Description	Default
15:13	RESERVED	RO	Reserved	X
12	LOS_OR	RO	Logical OR of all channel LOS signals	X
11	LOS11	RO	Channel 11 LOS signal	X
10	LOS10	RO	Channel 10 LOS signal	X
9	LOS9	RO	Channel 9 LOS signal	X
8	LOS8	RO	Channel 8 LOS signal	X
7	LOS7	RO	Channel 7 LOS signal	X
6	LOS6	RO	Channel 6 LOS signal	X
5	LOS5	RO	Channel 5 LOS signal	X
4	LOS4	RO	Channel 4 LOS signal	X
3	LOS3	RO	Channel 3 LOS signal	X
2	LOS2	RO	Channel 2 LOS signal	X
1	LOS1	RO	Channel 1 LOS signal	X
0	LOS0	RO	Channel 0 LOS signal	X

Table 134. LOLSTAT (40_C4)

Bit	Name	Access	Description	Default
15:13	RESERVED	RO	Reserved	X
12	LOL_OR	RO	Logical OR of all channel LOL signals	X
11	LOL11	RO	Channel 11 LOL signal	X
10	LOL10	RO	Channel 10 LOL signal	X
9	LOL9	RO	Channel 9 LOL signal	X
8	LOL8	RO	Channel 8 LOL signal	X
7	LOL7	RO	Channel 7 LOL signal	X
6	LOL6	RO	Channel 6 LOL signal	X
5	LOL5	RO	Channel 5 LOL signal	X
4	LOL4	RO	Channel 4 LOL signal	X
3	LOL3	RO	Channel 3 LOL signal	X
2	LOL2	RO	Channel 2 LOL signal	X
1	LOL1	RO	Channel 1 LOL signal	X
0	LOL0	RO	Channel 0 LOL signal	X

Note Registers 40_C5 through 40_C7 are reserved and read-only.

4 Electrical Specifications

This section provides the DC characteristics, AC characteristics, recommended operating conditions, and stress ratings for the VSC7227 device.

4.1 DC Characteristics

The following table lists the DC specifications for the VSC7227 device.

Table 135. DC Specifications

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Condition
Power supply voltage	V_{CC}	1.14	1.2	1.26	V	
Power supply current, retimer mode	I_{CC}		2160		mA	$DOUT_{DAMP}$ = 400 mV peak-to-peak differential
Power supply current, retimer mode	I_{CCTSTO}		2300		mA	$DOUT_{DAMP}$ = 1000 mV peak-to-peak differential TSTO mode
Power supply current, full adaptation and adaptation timeout			2250		mA	INEQ, DFE full adaptive all channels, DOUT = 800 mV peak-to-peak differential
Power dissipation, retimer mode	P_{DN}		2600		mW	$DOUT_{DAMP}$ = 400 mV peak-to-peak differential
Power dissipation, full adaptation and adaptation timeout			2700		mW	INEQ, DFE full adaptive all channels, DOUT = 800 mV peak-to-peak differential
Differential input resistance	R_{INDIFF}		110		Ω	Differential
Single-ended output resistance	$VOUT_{ROUT}$		55		Ω	
Temperature monitor coefficient	K_T		–0.568		°C/mV	
Accuracy of temperature monitor	A_T		±2		°C	Over 100 °C range after a one point calibration

4.1.1 Open-Drain Outputs

The following table lists the DC specifications for the open-drain outputs of the VSC7227 device. These specifications apply to the LOS0/SDA and LOS pins.

Table 136. Open-Drain Outputs

Parameter	Symbol	Minimum	Maximum	Unit	Condition
Output low voltage	V_{OL}	0	0.3	V	I_{OL} = 2 mA
Output high voltage	V_{OH}	V_{CC} – 0.3	3.6	V	Termination resistor nominal 4.7 kΩ to V_{CC}

4.1.2 Tri-Level Static Pin Inputs

The following table lists the DC specifications for the tri-level static pin inputs of the VSC7227 device. These specifications apply to the MODE0, MODE1, EQ0/DADDR0, EQ1/DADDR1, LOS0/SDA, LOS1/SCK, RSEL0, RSEL1, TX0/RST, and TX1 pins.

Table 137. Tri-Level Static Pin Inputs

Parameter	Symbol	Minimum	Maximum	Unit	Condition
Input low voltage	V_{IL}	–0.3	0.15 V_{CC}	V	
Input float voltage	V_{FL}	0.35 V_{CC}	0.65 V_{CC}	V	Input floating
Input high voltage	V_{IH}	0.8 V_{CC}	3.6	V	
Input current	I_{IL}, I_{IH}	–200	200	µA	V_{IN} between GND and V_{CC}

4.1.3 CMOS Inputs and Outputs

The following table lists the DC specifications for the CMOS inputs and outputs of the VSC7227 device. These specifications apply to the LOS0/SDA, LOS1/SCK, RSEL0, RSEL1, TX0/RST, and TX1 pins.

Table 138. CMOS Inputs and Outputs

Parameter	Symbol	Minimum	Maximum	Unit	Condition
Output low voltage	V_{OL}		0.3	V	I_{OL} = 2 mA
Output high voltage	V_{OH}	V_{CC} – 0.3	V_{CC}	V	Termination resistor nominal 4.7 kΩ to V_{CC}
Input low voltage	V_{IL}	–0.3	0.6	V	
Input high voltage	V_{IH}	1.0	3.6	V	
Input current	I_{IL}, I_{IH}	–200	200	µA	V_{IN} between GND and V_{CC}

The following table lists the DC specifications for the CMOS inputs that apply to the FCSEL*x* pins.

Table 139. CMOS Inputs for Fibre Channel Mode Rate Select

Parameter	Symbol	Minimum	Maximum	Unit	Condition
Input low voltage	V_{IL}	–0.3	0.6	V	
Input high voltage	V_{IH}	1.0	3.6	V	
Input current	I_{IL}, I_{IH}	–200	200	µA	V_{IN} between GND and V_{CC}

4.1.4 Reference Clock/Crystal Driver Inputs

The following table lists the DC specifications for the XTALA/CKINP and XTALB/CKINN pins of the VSC7227 device.

Table 140. Reference Clock/Crystal Driver Inputs

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Condition
Input low voltage	V_{ILCP}	–0.3		0.6	V	CKINP pin input

Table 140. Reference Clock/Crystal Driver Inputs *(continued)*

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Condition
Input high voltage	V_{IHCP}	1.0		3.3	V	CKINP pin input
Input low voltage	V_{ILCN}	–0.3		0.6	V	CKINN pin input
Input high voltage	V_{IHCN}	1.0		V_{CC} + 0.3	V	CKINN pin input
Output low voltage	V_{OLCN}		0.2		V	XTAL mode CKINN pin
Output high voltage	V_{OHCN}		V_{CC} – 0.3		V	XTAL mode CKINN pin

4.1.5 Reference Clock Output

The following table lists the DC specifications for the push-pull CMOS output REFCLKOUT of the VSC7227 device.

Table 141. Reference Clock Outputs

Parameter	Symbol	Minimum	Maximum	Unit	Condition
Output low voltage	V_{OLREF}		0.33	V	I_{OL} = 2 mA
Output high voltage	V_{OHREF}	V_{CC} – 0.3	V_{CC}	V	I_{OH} = 2 mA

4.2 AC Characteristics

This section provides the AC specifications for the VSC7227 device. All AC specifications are at V_{CC} = 1.2 V and $T_{JUNCTION}$ = 25 °C, unless otherwise noted.

4.2.1 Input Characteristics

The following table lists the AC specifications, input characteristics.

Table 142. Input Characteristics

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Condition
Input bit rate	f_{IN}	1.0		14.5	Gbps	
Differential input swing	VIN_{MAX}			1200	mV	
Differential input sensitivity	VIN_{SEN}		50		mV	Clean eye input
Differential input return loss	VIN_{S11}		10		dB	100 MHz to 8 GHz
Input line equalization capability	VIN_{EQ}		28		dB	

4.2.2 Clock Recovery Unit

The following table lists the AC specifications for the clock recovery unit.

Table 143. Clock Recovery Unit

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Condition
Input frequency lock range	f_{DATA}	1.0		14.5	Gbps	
Reference clock frequency tolerance	f_{TOL}			±100	ppm	
Acquisition lock time	f_{LOCK}		1		µs	Valid reference clock and device powered up
Jitter transfer function peaking	J_{TFP}			0.1	dB	

4.2.3 Output Characteristics

The following table lists the AC specifications, output characteristics, with AC-coupled 100 Ω differential load

Table 144. Output Characteristics

Parameter	Symbol	Typical	Unit	Condition
Differential output swing	$VOUT_{DAMP}$	927	mV	Peak-to-peak
Output transition rise time	$VOUT_{RISE}$	25	ps	
Output transition fall time	$VOUT_{FALL}$	25	ps	
Output return loss	$VOUT_{S22}$	10	dB	100 MHz to 5 GHz
Output de-emphasis	$VOUT_{DE}$	20	dB	
Output driver pre-tap tail current	I_{PRETAP}	4	mA	Maximum setting
Output driver main-tap tail current	$I_{MAINTAP}$	20	mA	Maximum setting
Output driver post-tap tail current	$I_{POSTTAP}$	16	mA	Maximum setting
Output squelch amplitude	$VOUT_{SQUELCH}$	20	mV RMS	Output squelched
Random jitter	R_J	1	ps RMS	
Deterministic jitter	D_J	4	ps	Peak-to-peak
Total jitter	T_J	20	ps	Peak-to-peak, BER=$10e^{-12}$

4.2.4 LOS Characteristics

The following table lists the AC specifications for the LOS characteristics of the VSC7227 device.

Table 145. LOS Characteristics

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Condition
LOS assert sensitivity	LOS_{SEN}		3		mV	Differential
LOS assert maximum amplitude	LOS_{max}		400		mV	Differential
LOS assert threshold stability	LOS_{STA}		1		dB	LOSASSERT=0x1F LOSDASSRT=0x27
LOS response time	LOS_{TIME}			54	µs	Signal loss to LOS assert time
LOS hysteresis(1)	LOS_{HYS}	2		42	dB	
LOS assert resolution	LOS_{RES}		0.1		mV	12-bit value

1. LOS hysteresis = $20*\log[(LOSDASSERT_{10}*0.1\ mV)/(LOSASSERT_{10}*0.1\ mV)]$.

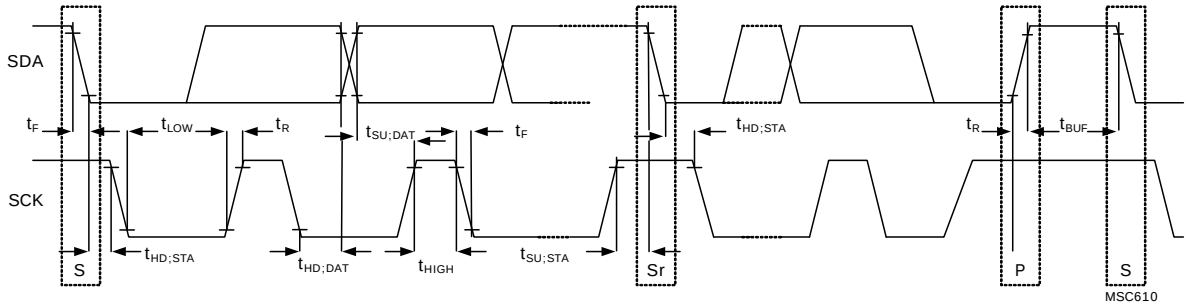
4.3 Two-Wire Serial Interface

This section provides information about the recommended interface characteristics for the two-wire serial port timing of the VSC7227 device.

Table 146. Two-Wire Serial Interface

		Standard Mode		Fast Mode		
Parameter	**Symbol**	**Minimum**	**Maximum**	**Minimum**	**Maximum**	**Unit**
Serial clock frequency	f_{SCK}		100		400	kHz
Hold time START condition (first CLL pulse is generated after this period)	$t_{HD;STA}$	4		0.6		µs
Low period of SCK	t_{LOW}	4.7		1.3		µs
High period of SCK	t_{HIGH}	4		0.6		µs
Data hold time	$t_{HD;DAT}$	0.00001	3.45	0.00001	0.9	µs
Data setup time	$t_{SU;DAT}$	250		100		ns
Rise time for SDA and SCK	t_R		1000		300	ns
Fall time for SDA and SCK	t_F		300		300	ns
Setup time for STOP condition	$t_{SU;STO}$	4		0.6		µs
Bus free time between a STOP and START	t_{BUE}	4.7		1.3		µs
Capacitive load for SCK and SDA bus line	C_B		400		400	pF
External pull-up resistor	R_P	900		900		Ω

Figure 9. Two-Wire Serial Timing Diagram



4.4 Operating Conditions

The following table lists the recommended operating conditions for the VSC7227 device.

Table 147. Recommended Operating Conditions

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Power supply	V_{CC}	1.14	1.2	1.26	V
Operating temperature(1)	T	–40		110	°C

1. Minimum specification is ambient temperature, and the maximum is junction temperature.

4.5 Stress Ratings

This section contains the stress ratings for the VSC7227 device.

Warning Stresses listed in the following table can be applied to devices one at a time without causing permanent damage. Functionality at or exceeding the values listed is not implied. Exposure to these values for extended periods may affect device reliability.

Table 148. Stress Ratings

Parameter	Symbol	Minimum	Maximum	Unit
Power supply voltage	V_{DD}	–0.3	1.32	V
Storage temperature	T_S	–40	125	°C
Electrostatic discharge voltage, charged device model	V_{ESD_CDM}	–250	250	V
Electrostatic discharge voltage, human body model	V_{ESD_HBM}	See note(1)		V

1. This device has completed all required testing as specified in the JEDEC standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*, and complies with a Class 2 rating. The definition of Class 2 is any part that passes an ESD pulse of 2000 V, but fails an ESD pulse of 4000 V.

Warning This device can be damaged by electrostatic discharge (ESD) voltage. Vitesse recommends that all integrated circuits be handled with appropriate

precautions. Failure to observe proper handling and installation procedures may adversely affect reliability of the device.

5 Pin Descriptions

The VSC7227 device has 144 pins, which are described in this section.

The pin information is also provided as an attached Microsoft Excel file, so that you can copy it electronically. In Adobe Reader, double-click the attachment icon.

5.1 Pin Diagram

The following illustration shows the pin diagram for the VSC7227 device, as seen from the top view.

Figure 10. Pin Diagram

	1	2	3	4	5	6	7	8	9	10	11	12
A	GND	INP0	GND	INP1	TD_ANODE	CKINP	CKINN	MODE0	OUTP1	GND	OUTP0	GND
B	GND	INN0	GND	INN1	TD_CATHODE	LOS	RESET	MODE1	OUTN1	GND	OUTN0	GND
C	INP2	GND	INP3	GND	VDD	EQ0_DADDR0	EQ1_DADDR1	VDD	GND	OUTP3	GND	OUTP2
D	INN2	GND	INN3	GND	VDD	FCSEL0	FCSEL1	VDD	GND	OUTN3	GND	OUTN2
E	GND	INP4	GND	INP5	VDD	FCSEL2	FCSEL3	VDD	OUTP5	GND	OUTP4	GND
F	GND	INN4	GND	INN5	VDD	FCSEL4	FCSEL5	VDD	OUTN5	GND	OUTN4	GND
G	INP6	GND	INP7	GND	VDD	FCSEL6	FCSEL7	VDD	GND	OUTP7	GND	OUTP6
H	INN6	GND	INN7	GND	VDD	FCSEL8	FCSEL9	VDD	GND	OUTN7	GND	OUTN6
J	GND	INP8	GND	INP9	VDD	FCSEL10	FCSEL11	VDD	OUTP9	GND	OUTP8	GND
K	GND	INN8	GND	INN9	VDD	LOS0_SDA	RSEL0	VDD	OUTN9	GND	OUTN8	GND
L	INP10	GND	INP11	GND	VDDR	LOS1_SCK	RSEL1	TX1	GND	OUTP11	GND	OUTP10
M	INN10	GND	INN11	GND	VDDR	REFCLKOUT	TX0	AOUT	GND	OUTN11	GND	OUTN10

5.2 Pins by Function

This section contains the functional pin descriptions for the VSC7227 device.

5.2.1 Analog

The following table shows the analog pins for the VSC7227 device.

Table 149. Analog Pins

Name	Number	Type	Description
AOUT	M8	Analog	Analog multiplexer output pin. For internal test purposes only.
TD_ANODE	A5	Analog	On-die temperature diode anode.
TD_CATHODE	B5	Analog	On-die temperature diode cathode.
VDDR	L5	Analog	Internal linear regulator capacitor. Connect a 4.7 µF capacitor to ground and a 0.1 µF capacitor to VDD to the VDDR pins.
VDDR	M5	Analog	Short L5 and M5 on the board.

5.2.2 Open-Drain Outputs

The following table shows the open-drain output pin for the VSC7227 device.

Table 150. Open-Drain Output Pins

Name	Number	Type	Description
LOS	B6	Open drain output	Loss of signal. Terminate with nominal external load resistor of 4.7 kΩ to V_{CC} (1.2 V to 3.3 V).

5.2.3 CMOS Inputs and Outputs

The following table shows the CMOS input and output pins for the VSC7227 device.

Table 151. CMOS Input and Output Pins

Name	Number	Type	Description
FCSEL0	D6	CMOS input	Fibre Channel and Infiniband rate select pin 0.
FCSEL1	D7	CMOS input	Fibre Channel and Infiniband rate select pin 1.
FCSEL2	E6	CMOS input	Fibre Channel and Infiniband rate select pin 2.
FCSEL3	E7	CMOS input	Fibre Channel and Infiniband rate select pin 3.
FCSEL4	F6	CMOS input	Fibre Channel and Infiniband rate select pin 4.
FCSEL5	F7	CMOS input	Fibre Channel and Infiniband rate select pin 5.
FCSEL6	G6	CMOS input	Fibre Channel and Infiniband rate select pin 6.
FCSEL7	G7	CMOS input	Fibre Channel and Infiniband rate select pin 7.
FCSEL8	H6	CMOS input	Fibre Channel and Infiniband rate select pin 8.
FCSEL9	H7	CMOS input	Fibre Channel and Infiniband rate select pin 9.

Table 151. CMOS Input and Output Pins *(continued)*

Name	Number	Type	Description
FCSEL10	J6	CMOS input	Fibre Channel and Infiniband rate select pin 10.
FCSEL11	J7	CMOS input	Fibre Channel and Infiniband rate select pin 11.
RESET	B7	CMOS input	Digital reset signal input. Reset is active high.
REFCLKOUT	M6	CMOS output	Internal reference clock output, 1.2 V rail-to-rail.

5.2.4 Crystal Driver Inputs and CMOS

The following table shows the crystal driver inputs and CMOS pins for the VSC7227 device.

Table 152. Crystal Driver Input and CMOS Pins

Name	Number	Description
CKINP	A6	Crystal driver input A in reference-less CRU operation. True reference clock input otherwise. AC-couple to this input.
CKINN	A7	Crystal driver input B in reference-less CRU operation. Complement reference clock input otherwise. AC-couple to this input.

5.2.5 Differential Pair Inputs

The following table shows the differential pair input pins for the VSC7227 device.

Table 153. Differential Pair Input Pins

Name	Number	Description
INN0	B2	Inverted input. AC-coupled input100 nF capacitor in the package. On-chip 100 Ω differential impedance.
INN1	B4	Inverted input. AC-coupled input100 nF capacitor in the package. On-chip 100 Ω differential impedance.
INN2	D1	Inverted input. AC-coupled input100 nF capacitor in the package. On-chip 100 Ω differential impedance.
INN3	D3	Inverted input. AC-coupled input100 nF capacitor in the package. On-chip 100 Ω differential impedance.
INN4	F2	Inverted input. AC-coupled 100 nF capacitor in the package. On-chip 100 Ω differential impedance.
INN5	F4	Inverted input. AC-coupled 100 nF capacitor in the package. On-chip 100 Ω differential impedance.
INN6	H1	Inverted input. AC-coupled 100 nF capacitor in the package. On-chip 100 Ω differential impedance.
INN7	H3	Inverted input. AC-coupled 100 nF capacitor in the package. On-chip 100 Ω differential impedance.
INN8	K2	Inverted input. AC-coupled 100 nF capacitor in the package. On-chip 100 Ω differential impedance.
INN9	K4	Inverted input. AC-coupled 100 nF capacitor in the package. On-chip 100 Ω differential impedance.

Table 153. Differential Pair Input Pins *(continued)*

Name	Number	Description
INN10	M1	Inverted input. AC-coupled 100 nF capacitor in the package. On-chip 100 Ω differential impedance.
INN11	M3	Inverted input. AC-coupled 100 nF capacitor in the package. On-chip 100 Ω differential impedance.
INP0	A2	Non-inverted input. AC-coupled 100 nF capacitor in the package. On-chip 100 Ω differential impedance.
INP1	A4	Non-inverted input. AC-coupled 100 nF capacitor in the package. On-chip 100 Ω differential impedance.
INP2	C1	Non-inverted input. AC-coupled 100 nF capacitor in the package. On-chip 100 Ω differential impedance.
INP3	C3	Non-inverted input. AC-coupled 100 nF capacitor in the package. On-chip 100 Ω differential impedance.
INP4	E2	Non-inverted input. AC-coupled 100 nF capacitor in the package. On-chip 100 Ω differential impedance.
INP5	E4	Non-inverted input. AC-coupled 100 nF capacitor in the package. On-chip 100 Ω differential impedance.
INP6	G1	Non-inverted input. AC-coupled 100 nF capacitor in the package. On-chip 100 Ω differential impedance.
INP7	G3	Non-inverted input. AC-coupled 100 nF capacitor in the package. On-chip 100 Ω differential impedance.
INP8	J2	Non-inverted input. AC-coupled 100 nF capacitor in the package. On-chip 100 Ω differential impedance.
INP9	J4	Non-inverted input. AC-coupled 100 nF capacitor in the package. On-chip 100 Ω differential impedance.
INP10	L1	Non-inverted input. AC-coupled 100 nF capacitor in the package. On-chip 100 Ω differential impedance.
INP11	L3	Non-inverted input. AC-coupled 100 nF capacitor in the package. On-chip 100 Ω differential impedance.

5.2.6 Differential Pair Outputs

The following table shows the differential pair output pins for the VSC7227 device.

Table 154. Differential Pair Output Pins

Name	Number	Description
OUTN0	B11	External AC-coupled inverted output. On-chip 100 Ω differential impedance.
OUTN1	B9	External AC-coupled inverted output. On-chip 100 Ω differential impedance.
OUTN2	D12	External AC-coupled inverted output. On-chip 100 Ω differential impedance.
OUTN3	D10	External AC-coupled inverted output. On-chip 100 Ω differential impedance.
OUTN4	F11	External AC-coupled inverted output. On-chip 100 Ω differential impedance.

Table 154. Differential Pair Output Pins *(continued)*

Name	Number	Description
OUTN5	F9	External AC-coupled inverted output. On-chip 100 Ω differential impedance.
OUTN6	H12	External AC-coupled inverted output. On-chip 100 Ω differential impedance.
OUTN7	H10	External AC-coupled inverted output. On-chip 100 Ω differential impedance.
OUTN8	K11	External AC-coupled inverted output. On-chip 100 Ω differential impedance.
OUTN9	K9	External AC-coupled inverted output. On-chip 100 Ω differential impedance.
OUTN10	M12	External AC-coupled inverted output. On-chip 100 Ω differential impedance.
OUTN11	M10	External AC-coupled inverted output. On-chip 100 Ω differential impedance.
OUTP0	A11	External AC-coupled non-inverted output. On-chip 100 Ω differential impedance.
OUTP1	A9	External AC-coupled non-inverted output. On-chip 100 Ω differential impedance.
OUTP2	C12	External AC-coupled non-inverted output. On-chip 100 Ω differential impedance.
OUTP3	C10	External AC-coupled non-inverted output. On-chip 100 Ω differential impedance.
OUTP4	E11	External AC-coupled non-inverted output. On-chip 100 Ω differential impedance.
OUTP5	E9	External AC-coupled non-inverted output. On-chip 100 Ω differential impedance.
OUTP6	G12	External AC-coupled non-inverted output. On-chip 100 Ω differential impedance.
OUTP7	G10	External AC-coupled non-inverted output. On-chip 100 Ω differential impedance.
OUTP8	J11	External AC-coupled non-inverted output. On-chip 100 Ω differential impedance.
OUTP9	J9	External AC-coupled non-inverted output. On-chip 100 Ω differential impedance.
OUTP10	L12	External AC-coupled non-inverted output. On-chip 100 Ω differential impedance.
OUTP11	L10	External AC-coupled non-inverted output. On-chip 100 Ω differential impedance.

5.2.7 Ground and Power Supplies

The following table shows the ground and power supply pins for the VSC7227 device.

Table 155. Ground and Power Supply Pins

Name	Number	Description
GND	A1, A3, A10, A12, B1, B3, B10, B12, C2, C4, C9, C11, D2, D4, D9, D11, E1, E3, E10, E12, F1, F3, F10, F12, G2, G4, G9, G11, H2, H4, H9, H11, J1, J3, J10, J12, K1, K3, K10, K12, L2, L4, L9, L11, M2, M4, M9, M11	Ground
VDD	C5, C8, D5, D8, E5, E8, F5, F8, G5, G8, H5, H8, J5, J8, K5, K8	1.2 V power supply

5.2.8 Tri-Level Inputs

The following table shows the tri-level input and output pins for the VSC7227 device

Table 156. Tri-Level Input Pins

Name	Number	Description
EQ0DADDR0	C6	Two-wire serial mode: device address pin 0. Pin strap mode: equalizer setting pin 0. Input has a nominal termination of 50 kΩ to VDD/2.
EQ1DADDR1	C7	Two-wire serial mode: device address pin 1. Pin strap mode: equalizer setting pin 1. Input has a nominal termination of 50 kΩ to VDD/2.
MODE0	A8	Mode setting pin 0. Input has a nominal termination of 50 kΩ to VDD/2.
MODE1	B8	Mode setting pin 1. Input has a nominal termination of 50 kΩ to VDD/2.
RSEL0	K7	Pin strap mode: rate select pin 0. Input has a nominal termination of 50 kΩ to VDD/2.
RSEL1	L7	Pin strap mode: rate select pin 1. Input has a nominal termination of 50 kΩ to VDD/2.
TX0	M7	Pin strap mode: output de-emphasis setting pin 0. Input has a nominal termination of 50 kΩ to VDD/2.
TX1	L8	Pin strap mode: output de-emphasis setting pin 1. Input has a nominal termination of 50 kΩ to VDD/2.

5.2.9 Tri-Level and CMOS Inputs and Outputs

The following table shows the tri-level and CMOS input pins for the VSC7227 device

Table 157. Tri-Level/CMOS Input and Output Pins

Name	Number	Description
LOS0_SDA	K6	Two-wire serial mode: input/output for two-wire serial slave data. Pin strap mode: loss of signal setting pin 0. Input has a nominal termination of 50 kΩ to VDD/2. Terminate with nominal external load resistor of 4.7 kΩ to microcontroller V_{CC} (1.2 V to 3.3 V) in two-wire serial mode.
LOS1/SCK	L6	Two-wire serial mode: input/output for two-wire serial slave clock. Pin strap mode: loss of signal setting pin 1. Input has a nominal termination of 50 kΩ to VDD/2. Terminate with nominal external load resistor of 4.7 kΩ to microcontroller V_{CC} (1.2 V to 3.3 V) in two-wire serial mode.

5.3 Pins by Number

This section provides a numeric list of the VSC7227 pins.

A1	GND	D3	INN3	G5	VDD
A2	INP0	D4	GND	G6	FCSEL6
A3	GND	D5	VDD	G7	FCSEL7
A4	INP1	D6	FCSEL0	G8	VDD
A5	TD_ANODE	D7	FCSEL1	G9	GND
A6	CKINP	D8	VDD	G10	OUTP7
A7	CKINN	D9	GND	G11	GND
A8	MODE0	D10	OUTN3	G12	OUTP6
A9	OUTP1	D11	GND	H1	INN6
A10	GND	D12	OUTN2	H2	GND
A11	OUTP0	E1	GND	H3	INN7
A12	GND	E2	INP4	H4	GND
B1	GND	E3	GND	H5	VDD
B2	INN0	E4	INP5	H6	FCSEL8
B3	GND	E5	VDD	H7	FCSEL9
B4	INN1	E6	FCSEL2	H8	VDD
B5	TD_CATHODE	E7	FCSEL3	H9	GND
B6	LOS	E8	VDD	H10	OUTN7
B7	RESET	E9	OUTP5	H11	GND
B8	MODE1	E10	GND	H12	OUTN6
B9	OUTN1	E11	OUTP4	J1	GND
B10	GND	E12	GND	J2	INP8
B11	OUTN0	F1	GND	J3	GND
B12	GND	F2	INN4	J4	INP9
C1	INP2	F3	GND	J5	VDD
C2	GND	F4	INN5	J6	FCSEL10
C3	INP3	F5	VDD	J7	FCSEL11
C4	GND	F6	FCSEL4	J8	VDD
C5	VDD	F7	FCSEL5	J9	OUTP9
C6	EQ0_DADDR0	F8	VDD	J10	GND
C7	EQ1_DADDR1	F9	OUTN5	J11	OUTP8
C8	VDD	F10	GND	J12	GND
C9	GND	F11	OUTN4	K1	GND
C10	OUTP3	F12	GND	K2	INN8
C11	GND	G1	INP6	K3	GND
C12	OUTP2	G2	GND	K4	INN9
D1	INN2	G3	INP7	K5	VDD
D2	GND	G4	GND	K6	LOS0_SDA

Pins by name *(continued)*

K7	RSEL0
K8	VDD
K9	OUTN9
K10	GND
K11	OUTN8
K12	GND
L1	INP10
L2	GND
L3	INP11
L4	GND
L5	VDDR
L6	LOS1_SCK
L7	RSEL1
L8	TX1
L9	GND
L10	OUTP11
L11	GND
L12	OUTP10
M1	INN10
M2	GND
M3	INN11
M4	GND
M5	VDDR
M6	REFCLKOUT
M7	TX0
M8	AOUT
M9	GND
M10	OUTN11
M11	GND
M12	OUTN10

5.4 Pins by Name

This section provides an alphabetical list of the VSC7227 pins.

AOUT	M8	GND	F3	INN11	M3
CKINN	A7	GND	F10	INP0	A2
CKINP	A6	GND	F12	INP1	A4
EQ0_DADDR0	C6	GND	G2	INP2	C1
EQ1_DADDR1	C7	GND	G4	INP3	C3
FCSEL0	D6	GND	G9	INP4	E2
FCSEL1	D7	GND	G11	INP5	E4
FCSEL2	E6	GND	H2	INP6	G1
FCSEL3	E7	GND	H4	INP7	G3
FCSEL4	F6	GND	H9	INP8	J2
FCSEL5	F7	GND	H11	INP9	J4
FCSEL6	G6	GND	J1	INP10	L1
FCSEL7	G7	GND	J3	INP11	L3
FCSEL8	H6	GND	J10	LOS	B6
FCSEL9	H7	GND	J12	LOS0_SDA	K6
FCSEL10	J6	GND	K1	LOS1_SCK	L6
FCSEL11	J7	GND	K3	MODE0	A8
GND	A1	GND	K10	MODE1	B8
GND	A3	GND	K12	OUTN0	B11
GND	A10	GND	L2	OUTN1	B9
GND	A12	GND	L4	OUTN2	D12
GND	B1	GND	L9	OUTN3	D10
GND	B3	GND	L11	OUTN4	F11
GND	B10	GND	M2	OUTN5	F9
GND	B12	GND	M4	OUTN6	H12
GND	C2	GND	M9	OUTN7	H10
GND	C4	GND	M11	OUTN8	K11
GND	C9	INN0	B2	OUTN9	K9
GND	C11	INN1	B4	OUTN10	M12
GND	D2	INN2	D1	OUTN11	M10
GND	D4	INN3	D3	OUTP0	A11
GND	D9	INN4	F2	OUTP1	A9
GND	D11	INN5	F4	OUTP2	C12
GND	E1	INN6	H1	OUTP3	C10
GND	E3	INN7	H3	OUTP4	E11
GND	E10	INN8	K2	OUTP5	E9
GND	E12	INN9	K4	OUTP6	G12
GND	F1	INN10	M1	OUTP7	G10

Pins by name *(continued)*

OUTP8	J11
OUTP9	J9
OUTP10	L12
OUTP11	L10
REFCLKOUT	M6
RESET	B7
RSEL0	K7
RSEL1	L7
TD_ANODE	A5
TD_CATHODE	B5
TX0	M7
TX1	L8
VDD	C5
VDD	C8
VDD	D5
VDD	D8
VDD	E5
VDD	E8
VDD	F5
VDD	F8
VDD	G5
VDD	G8
VDD	H5
VDD	H8
VDD	J5
VDD	J8
VDD	K5
VDD	K8
VDDR	L5
VDDR	M5

6 Package Information

The VSC7227YKV package is a lead-free (Pb-free), 144-pin, flip chip ball grid array (FCBGA) with a 13 mm × 13 mm body size, 1 mm pin pitch, and 1.6 mm maximum height.

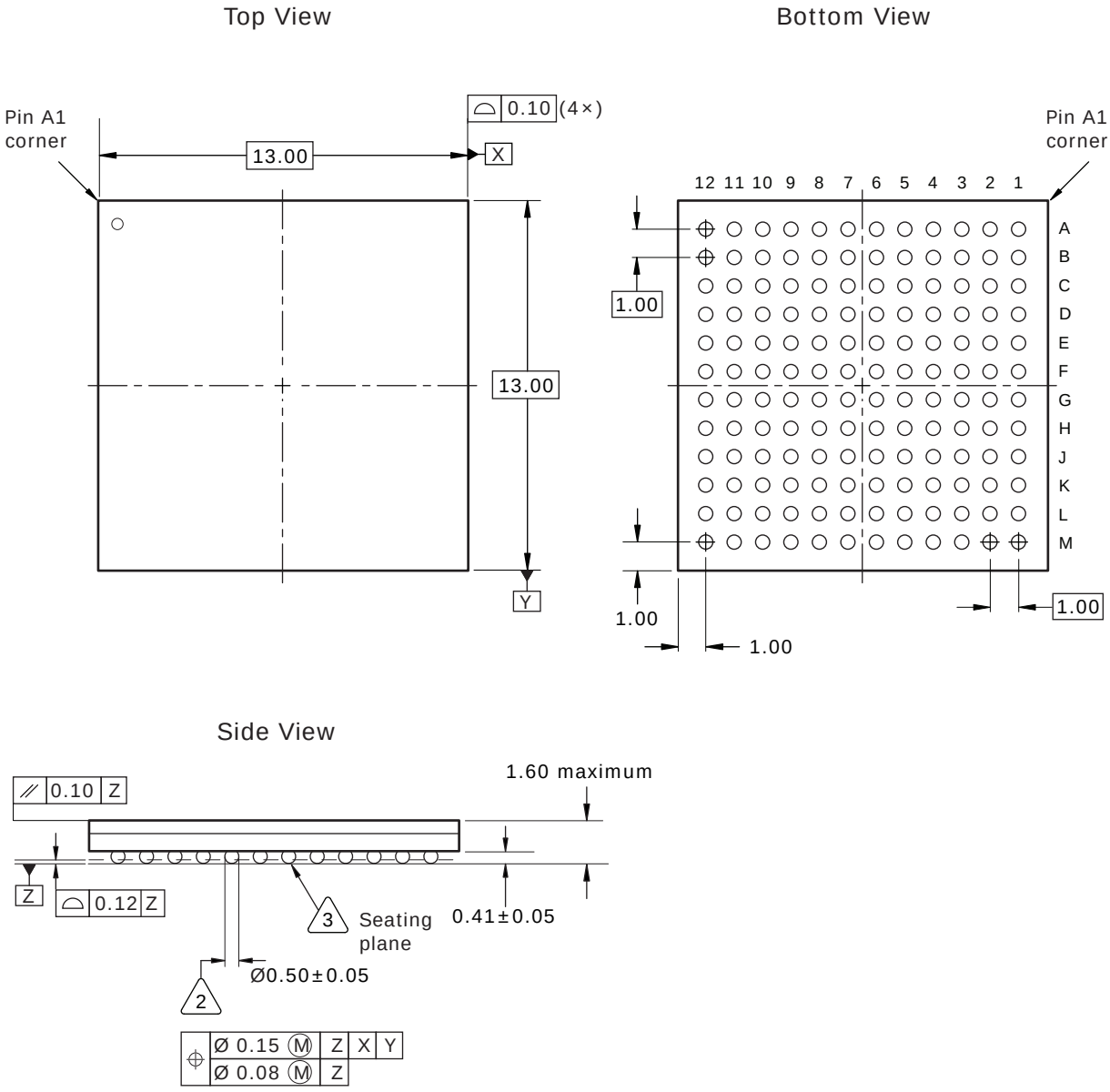
Lead-free products from Vitesse comply with the temperatures and profiles defined in the joint IPC and JEDEC standard IPC/JEDEC J-STD-020. For more information, see the IPC and JEDEC standard.

This section provides the package drawing, thermal specifications, and moisture sensitivity rating for the VSC7227 device.

6.1 Package Drawing

The following illustration shows the package drawing for the VSC7227 device. The drawing contains the top view, bottom view, side view, dimensions, tolerances, and notes.

Figure 11. Package Drawing



Notes

1. All dimensions and tolerances are in millimeters (mm).
2. Dimension is measured at the maximum solder ball diameter, parallel to primary datum Z.
3. Primary datum Z and seating plane are defined by the spherical crowns of the solder balls.
4. Radial true position is represented by typical values.

6.2 Thermal Specifications

Thermal specifications for this device are based on the JEDEC JESD51 family of documents. These documents are available on the JEDEC Web site at www.jedec.org. The thermal specifications are modeled using a four-layer test board with two signal layers, a power plane, and a ground plane (2s2p PCB). For more information about the thermal measurement method used for this device, see the JESD51-1 standard.

Table 158. Thermal Resistances

Symbol	°C/W	Parameter
θ_{JCtop}	3.4	Die junction to package case top
θ_{JB}	14.4	Die junction to printed circuit board
θ_{JA}	24.7	Die junction to ambient
θ_{JMA} at 1 m/s	20.8	Die junction to moving air measured at an air speed of 1 m/s
θ_{JMA} at 2 m/s	18.5	Die junction to moving air measured at an air speed of 2 m/s

To achieve results similar to the modeled thermal measurements, the guidelines for board design described in the JESD51 family of publications must be applied. For information about applications using FCBGA packages, see the following:

- JESD51-2A, *Integrated Circuits Thermal Test Method Environmental Conditions, Natural Convection (Still Air)*
- JESD51-6, *Integrated Circuit Thermal Test Method Environmental Conditions, Forced Convection (Moving Air)*
- JESD51-8, *Integrated Circuit Thermal Test Method Environmental Conditions, Junction-to-Board*
- JESD51-9, *Test Boards for Area Array Surface Mount Package Thermal Measurements*

6.3 Moisture Sensitivity

This device is rated moisture sensitivity level 4 as specified in the joint IPC and JEDEC standard IPC/JEDEC J-STD-020. For more information, see the IPC and JEDEC standard.

7 Ordering Information

The VSC7227YKV package is a lead-free (Pb-free), 144-pin, flip chip ball grid array (FCBGA) with a 13 mm × 13 mm body size, 1 mm pin pitch, and 1.6 mm maximum height.

Lead-free products from Vitesse comply with the temperatures and profiles defined in the joint IPC and JEDEC standard IPC/JEDEC J-STD-020. For more information, see the IPC and JEDEC standard.

The following table lists the ordering information for the VSC7227 device.

Table 159. Ordering Information

Part Order Number	Description
VSC7227YKV	Lead-free, 144-pin FCBGA with a 13 mm × 13 mm body size, 1 mm pin pitch, and 1.6 mm maximum height