TN2640

N-Channel Enhancement-Mode Vertical DMOS FET

Features

- 2V Maximum Low Threshold
- High Input Impedance
- Low Input Capacitance
- Fast Switching Speeds
- Low On-Resistance
- Free from Secondary Breakdown
- Low Input and Output Leakage

Applications

- Logic-Level Interfaces (Ideal for TTL and CMOS)
- Solid-State Relays
- Battery-Operated Systems
- Photovoltaic Drives
- Analog Switches
- General Purpose Line Drivers
- Telecommunication Switches

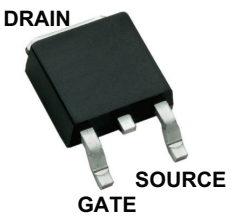
General Description

The TN2640 low-threshold Enhancement-mode (normally-off) transistor uses a vertical DMOS structure and a well-proven silicon-gate manufacturing process. This combination produces a device with the power handling capabilities of bipolar transistors and the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, this device is free from thermal runaway and thermally induced secondary breakdown.

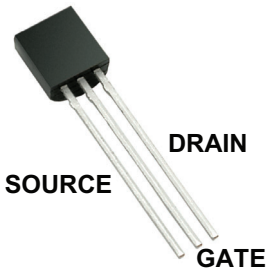
Microchip's vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where very low threshold voltage, high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Package Types

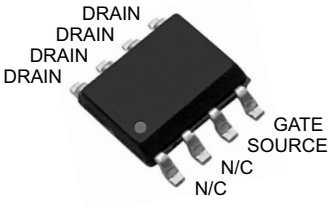
3-lead TO-252 (D-PAK)
(Top view)



3-lead TO-92
(Top view)



8-lead SOIC
(Top view)



See Table 3-1, Table 3-2, and Table 3-3 for pin information.

1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings†

Drain-to-Source Voltage ..... BV_{DSS}
Drain-to-Gate Voltage ..... BV_{DGS}
Gate-to-Source Voltage..... ±20V
Operating Ambient Temperature, T_A ..... -55°C to +150°C
Storage Temperature, T_S ..... -55°C to +150°C

† Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

Electrical Specifications: T_A = 25°C unless otherwise specified. All DC parameters are 100% tested at 25°C unless otherwise stated. (Pulse test: 300 µs pulse, 2% duty cycle)

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Drain-to-Source Breakdown Voltage	BV_{DSS}	400	—	—	V	V_{GS} = 0V, I_D = 1 mA
Gate Threshold Voltage	$V_{GS(th)}$	0.8	—	2	V	V_{GS} = V_{DS}, I_D = 2 mA
Change in $V_{GS(th)}$ with Temperature	$\Delta V_{GS(th)}$	—	-2.5	-4	mV/°C	V_{GS} = V_{DS}, I_D = 2 mA (**Note 1**)
Gate Body Leakage Current	I_{GSS}	—	—	100	nA	V_{GS} = ±20V, V_{DS} = 0V
Zero-Gate Voltage Drain Current	I_{DSS}	—	—	10	µA	V_{GS} = 0V, V_{DS} = Maximum rating
		—	—	1	mA	V_{DS} = 0.8 Maximum rating, V_{GS} = 0V, T_A = 125°C (**Note 1**)
On-State Drain Current	$I_{D(ON)}$	1.5	3.5	—	A	V_{GS} = 5V, V_{DS} = 25V
		2	4	—	A	V_{GS} = 10V, V_{DS} = 25V
Static Drain-to-Source On-State Resistance	$R_{DS(ON)}$	—	3.2	5	Ω	V_{GS} = 4.5V, I_D = 500 mA
		—	3	5	Ω	V_{GS} = 10V, I_D = 500 mA
Change in $R_{DS(ON)}$ with Temperature	$\Delta R_{DS(ON)}$	—	—	0.75	%/°C	V_{GS} = 10V, I_D = 500 mA (**Note 1**)

Note 1: Specification is obtained by characterization and is not 100% tested.

AC ELECTRICAL CHARACTERISTICS

Electrical Specifications: T_A = 25°C unless otherwise specified. All AC parameters are not 100% sample tested.

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Forward Transconductance	G_{FS}	200	330	—	mmho	V_{DS} = 25V, I_D = 100 mA
Input Capacitance	C_{ISS}	—	210	225	pF	V_{GS} = 0V, V_{DS} = 25V, f = 1 MHz
Common-Source Output Capacitance	C_{OSS}	—	30	50	pF	
Reverse Transfer Capacitance	C_{RSS}	—	8	15	pF	
Turn-On Delay Time	$t_{d(ON)}$	—	4	15	ns	V_{DD} = 25V, I_D = 2A, R_{GEN} = 25Ω
Rise Time	t_r	—	15	20	ns	
Turn-Off Delay Time	$t_{d(OFF)}$	—	20	25	ns	
Fall Time	t_f	—	22	27	ns	
DIODE PARAMETER						
Diode Forward Voltage Drop	V_{SD}	—	—	0.9	V	V_{GS} = 0V, I_{SD} = 200 mA (**Note 1**)
Reverse Recovery Time	t_{rr}	—	300	—	ns	V_{GS} = 0V, I_{SD} = 1A

Note 1: All DC parameters are 100% tested at 25°C unless otherwise stated. (Pulse test: 300 µs pulse, 2% duty cycle)

TEMPERATURE SPECIFICATIONS

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
TEMPERATURE RANGE						
Operating Ambient Temperature	T_A	-55	—	+150	°C	
Storage Temperature	T_S	-55	—	+150	°C	
PACKAGE THERMAL RESISTANCE						
3-lead TO-252 (D-PAK)	θ_{JA}	—	81	—	°C/W	
8-lead SOIC	θ_{JA}	—	101	—	°C/W	
3-lead TO-92	θ_{JA}	—	132	—	°C/W	

THERMAL CHARACTERISTICS

Package	I_D (Note 1) (Continuous) (mA)	I_D (Pulsed) (A)	Power Dissipation at T_A = 25°C (W)	I_{DR} (Note 1) (mA)	I_{DRM} (A)
3-lead TO-252 (D-PAK)	500	3	2.5 (Note 2)	500	3
8-lead SOIC	260	2	1.3 (Note 2)	260	2
3-lead TO-92	220	2	0.74	220	2

Note 1: I_D (continuous) is limited by maximum T_J.

2: Mounted on an FR4 board, 25 mm x 25 mm x 1.57 mm

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g. outside specified power supply range) and therefore outside the warranted range.

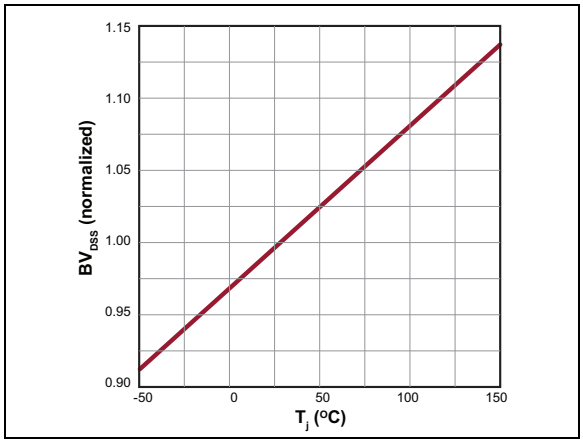


FIGURE 2-1: *BV_{DSS} Variation with Temperature.*

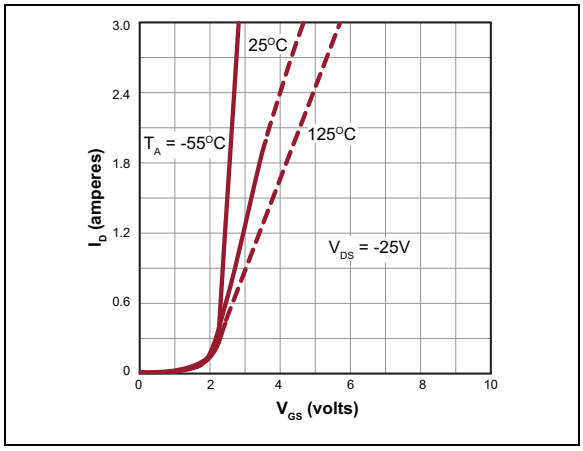


FIGURE 2-2: *Transfer Characteristics.*

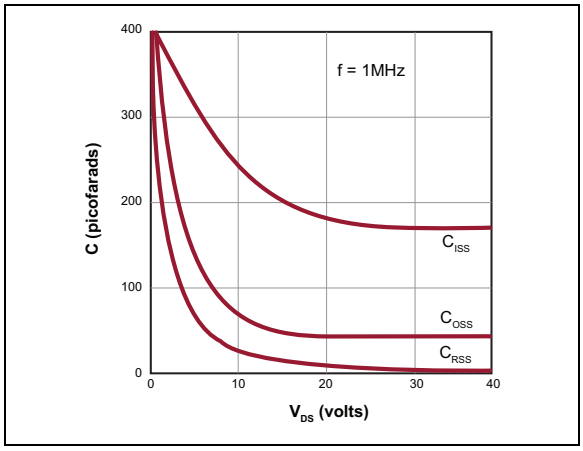


FIGURE 2-3: *Capacitance vs. Drain-to-Source Voltage.*

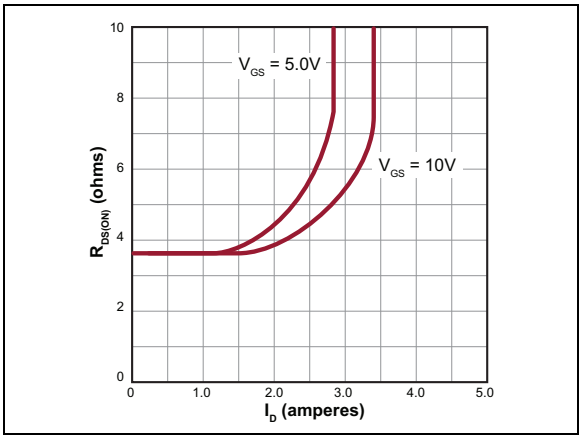


FIGURE 2-4: *On-Resistance vs. Drain Current.*

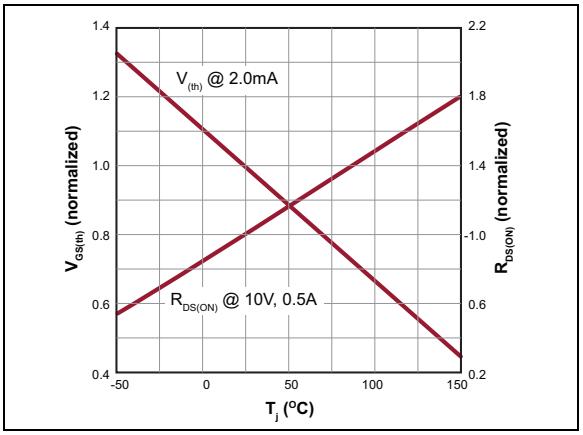


FIGURE 2-5: *$V_{GS(th)}$ and $R_{DS(ON)}$ Variation with Temperature.*

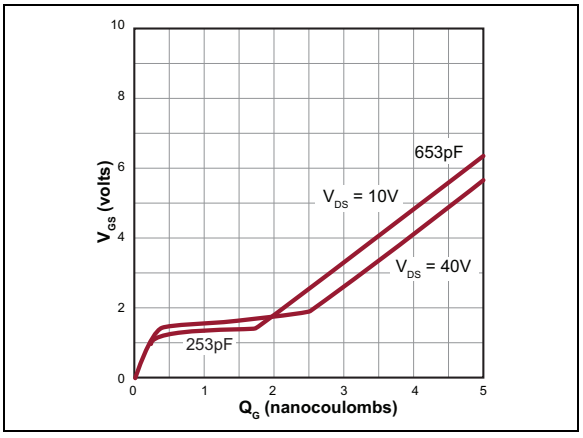


FIGURE 2-6: *$V_{GS(th)}$ and $R_{DS(ON)}$ Variation with Temperature.*

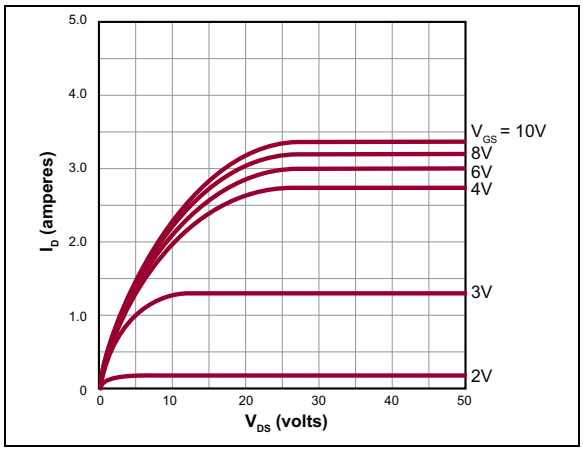


FIGURE 2-7: *Output Characteristics.*

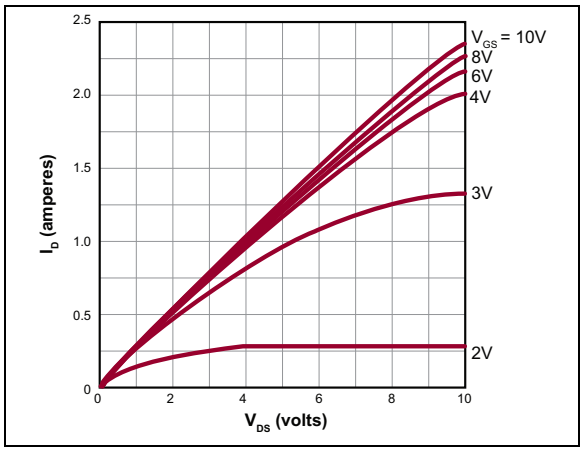


FIGURE 2-10: *Saturation Characteristics.*

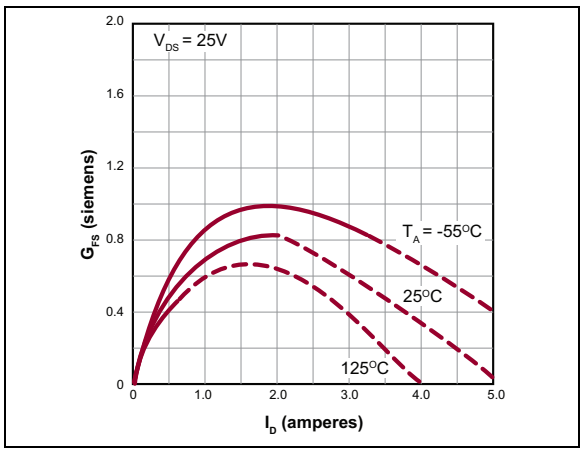


FIGURE 2-8: *Transconductance vs. Drain Current.*

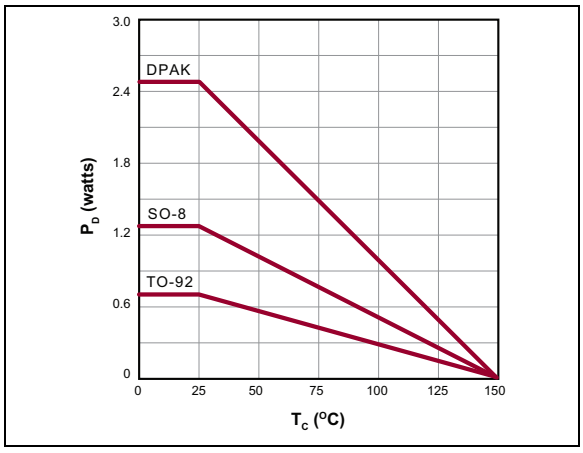


FIGURE 2-11: *Power Dissipation vs. Temperature.*

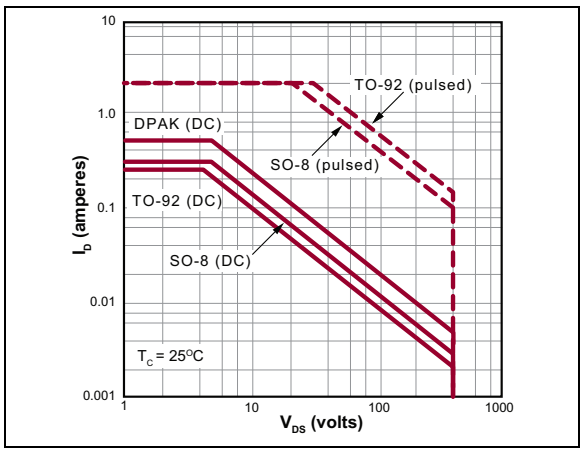


FIGURE 2-9: *Maximum Rated Safe Operating Area.*

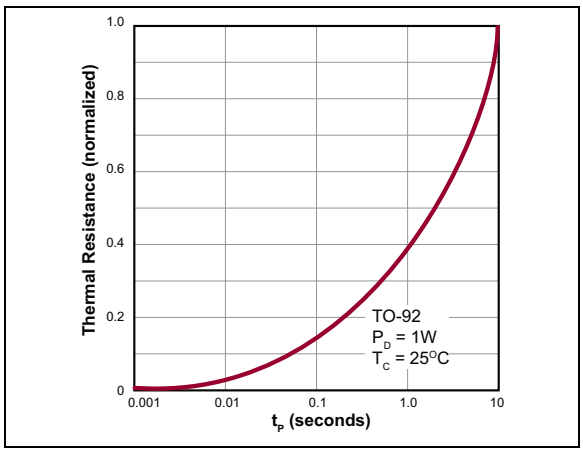


FIGURE 2-12: *Thermal Characteristics.*

3.0 PIN DESCRIPTION

Table 3-1, Table 3-2, and Table 3-3 show the description of pins in TN2640. Refer to **Package Types** for the location of the pins.

TABLE 3-1: 3-LEAD TO-252 (DPAK) PIN FUNCTION TABLE

Pin Number	Pin Name	Description
1	Gate	Gate
3	Source	Source
4	Drain	Drain

TABLE 3-2: 8-LEAD SOIC PIN FUNCTION TABLE

Pin Number	Pin Name	Description
1	N/C	No connect
2	N/C	No connect
3	Source	Source
4	Gate	Gate
5	Drain	Drain
6	Drain	Drain
7	Drain	Drain
8	Drain	Drain

TABLE 3-3: 3-LEAD TO-92 PIN FUNCTION TABLE

Pin Number	Pin Name	Description
1	Source	Source
2	Gate	Gate
3	Drain	Drain

4.0 FUNCTIONAL DESCRIPTION

Figure 4-1 illustrates the switching waveforms and test circuit for TN2640.

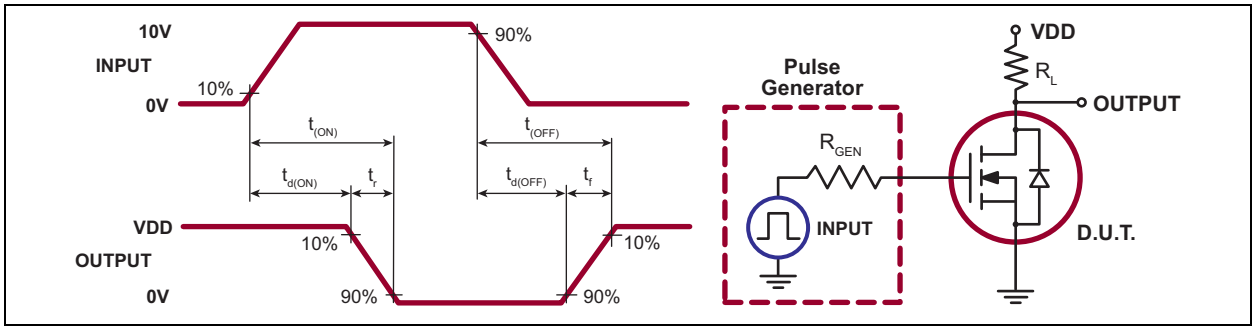


FIGURE 4-1: *Switching Waveforms and Test Circuit.*

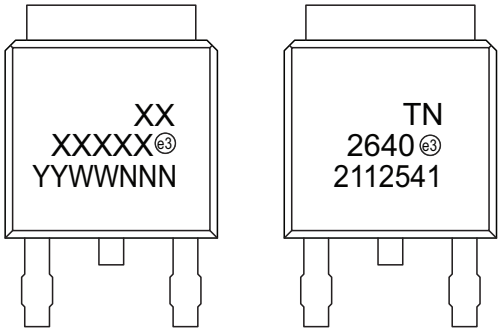
TABLE 4-1: PRODUCT SUMMARY

BV_{DSS}/BV_{DGS} (V)	$R_{DS(ON)}$ (Maximum) (Ω)	$I_{D(ON)}$ (Minimum) (A)	$V_{GS(th)}$ (Maximum) (V)
400	5	2	2

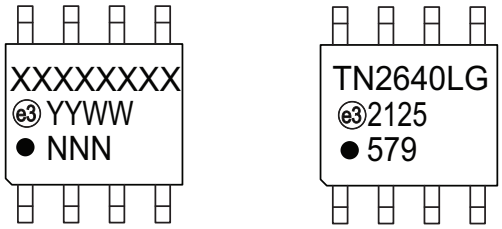
5.0 PACKAGING INFORMATION

5.1 Package Marking Information

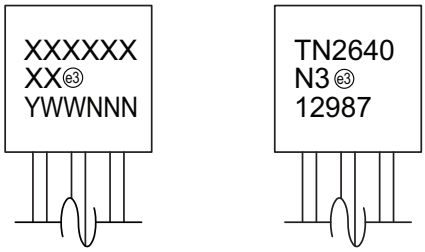
TO-252 (D-PAK) Example



8-lead SOIC Example



3-lead TO-92 Example

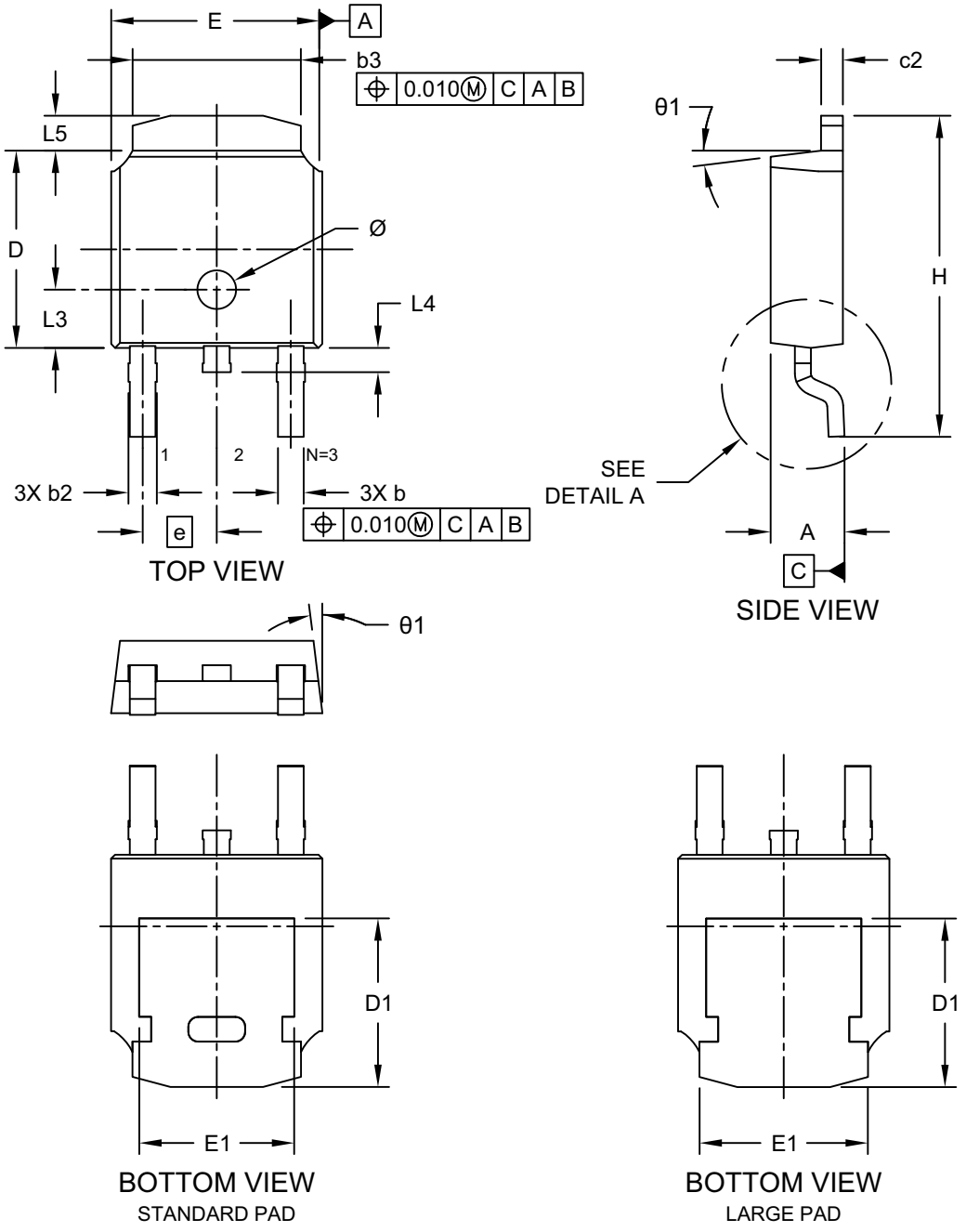


Legend:	XX...X	Product Code or Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for product code or customer-specific information. Package may or not include the corporate logo.

3-Lead Deca-Watt Package, TO-252 (EA) - [DPAK]; Supertex Legacy Package Code K4

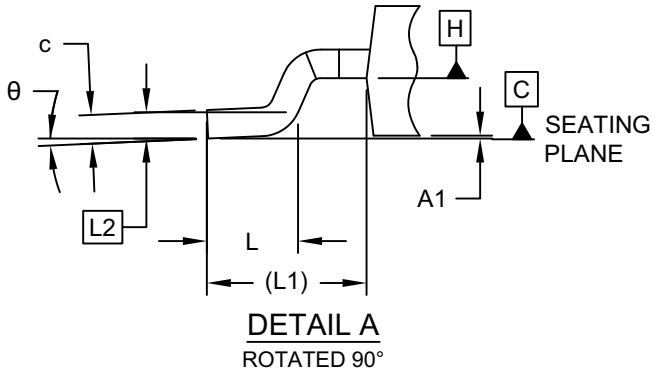
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

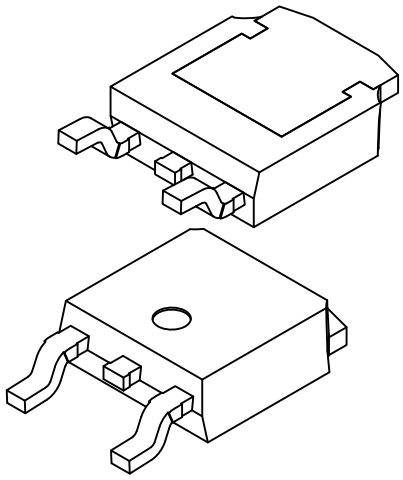


Microchip Technology Drawing C04-189 Rev C Sheet 1 of 2

3-Lead Deca-Watt Package, TO-252 (EA) - [DPAK]; Supertex Legacy Package Code K4

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging





Units	INCHES		
	MIN	NOM	MAX
N (Leads)		3	
e		.090 BSC	
A	.086	-	.094
A1	.000	-	.005
b	.028	-	.035
b2	.030	-	.045
c	.018	-	.024
c2	.018	-	.035
D	.235	.240	.245
D1	.205	-	-
E	.250	-	.265
E1	.170	-	-
H	.370	-	.410
L	.055	.060	.070
L1		.108 REF	
L2		.020 BSC	
L3	.065	-	.077
L4	.024	-	.035
L5	.035	-	.050
θ	1°	-	5°
θ1		7° REF	

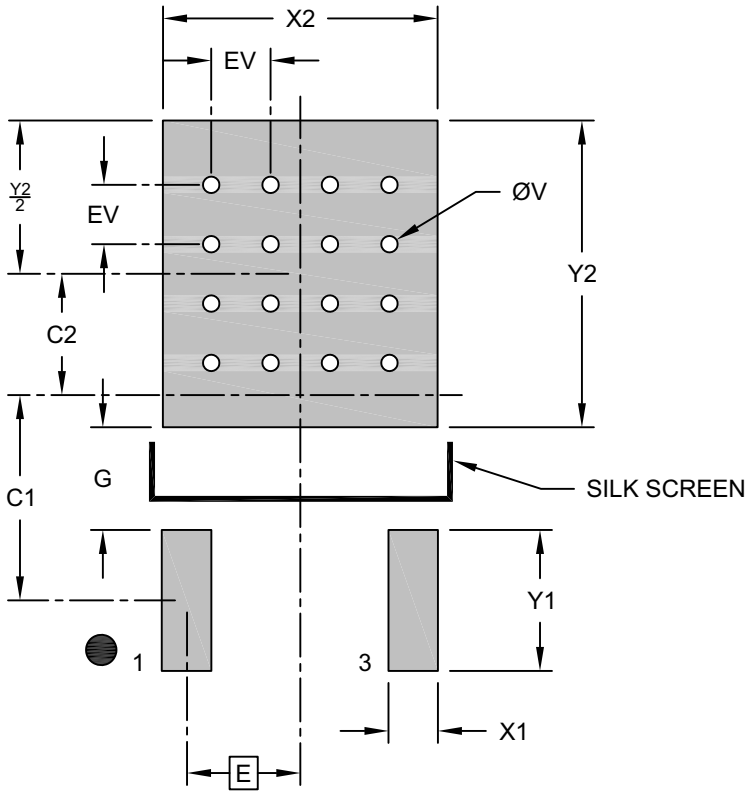
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-189 Rev C Sheet 1 of 2

3-Lead Deca-Watt Package, TO-252 (EA) - [DPAK]; Supertex Legacy Package Code K4

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		INCHES		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	.090 BSC		
Center Pad Width	X2			.219
Center Pad Length	Y2			.244
Contact Pad Spacing	C1		.163	
Contact Pad Spacing	C2		.096	
Contact Pad Width (Xnn)	X1			.039
Contact Pad Length (Xnn)	Y1			.112
Contact Pad to Contact Pad (Xnn)	G	.412		
Thermal Via Diameter	V		.013	
Thermal Via Pitch	EV		.047	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

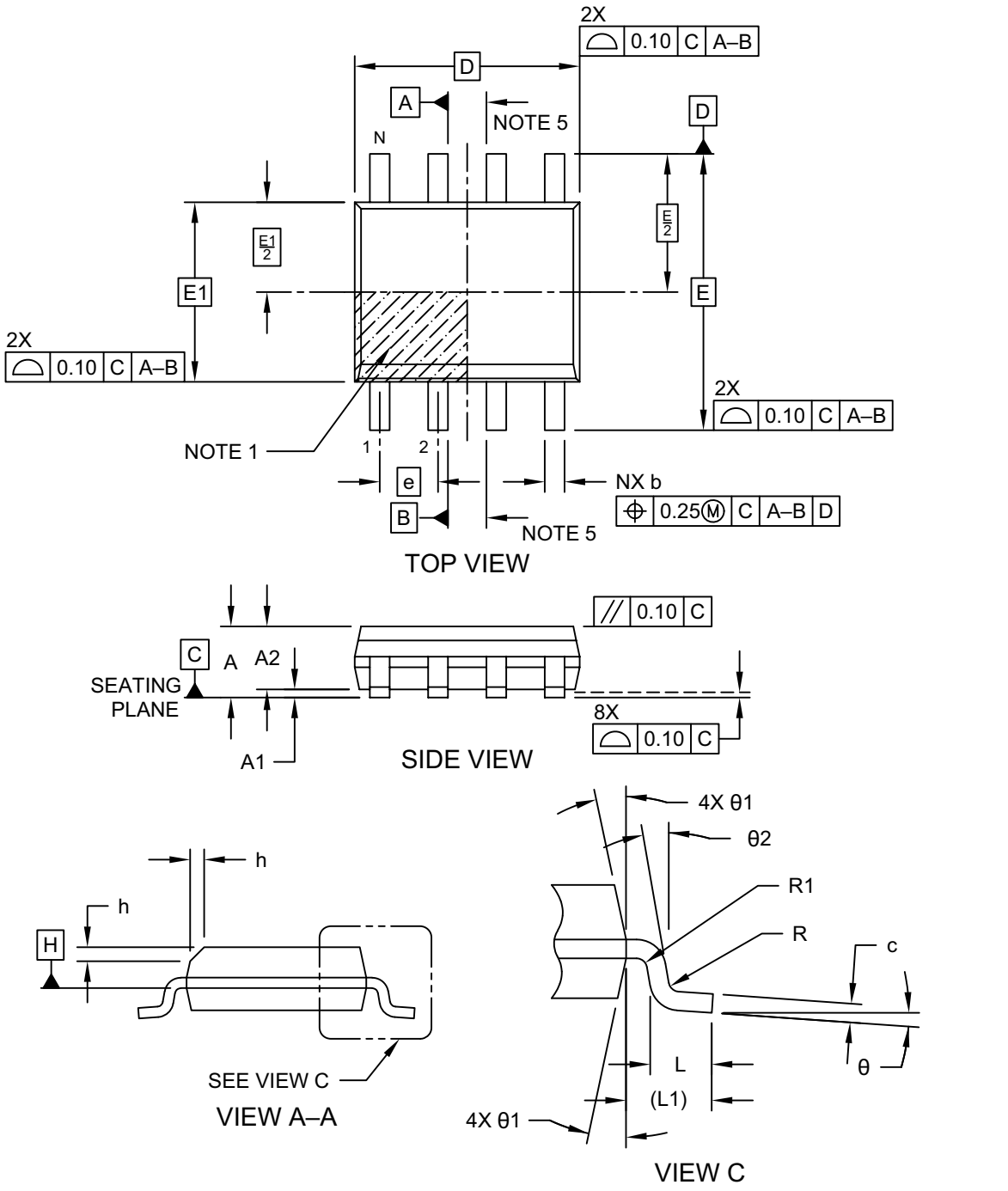
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-2189 Rev C

8-Lead Plastic Small Outline (C2X) - Narrow, 3.90 mm (.150 In.) Body [SOIC]
Atmel Legacy Global Package Code SWB

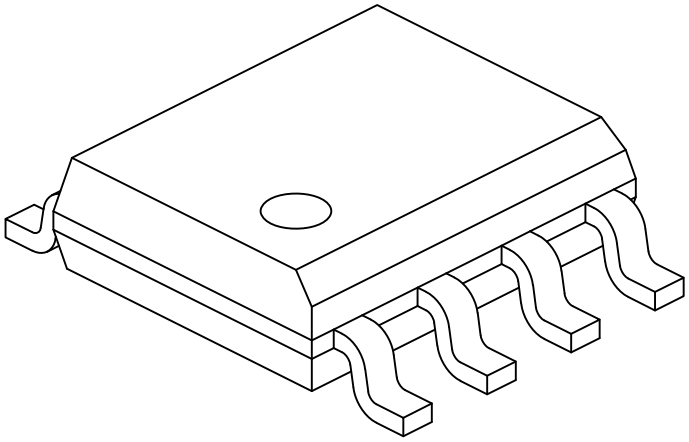
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing No. C04-057-C2X Rev K Sheet 1 of 2

8-Lead Plastic Small Outline (C2X) - Narrow, 3.90 mm (.150 In.) Body [SOIC]
Atmel Legacy Global Package Code SWB

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		1.27 BSC	
Overall Height	A	–	–	1.75
Molded Package Thickness	A2	1.25	–	-
Standoff §	A1	0.10	–	0.25
Overall Width	E		6.00 BSC	
Molded Package Width	E1		3.90 BSC	
Overall Length	D		4.90 BSC	
Chamfer (Optional)	h	0.25	–	0.50
Foot Length	L	0.40	–	1.27
Footprint	L1		1.04 REF	
Lead Thickness	c	0.17	–	0.25
Lead Width	b	0.31	–	0.51
Lead Bend Radius	R	0.07	–	–
Lead Bend Radius	R1	0.07	–	–
Foot Angle	θ	0°	–	8°
Mold Draft Angle	θ1	5°	–	15°
Lead Angle	θ2	0°	–	–

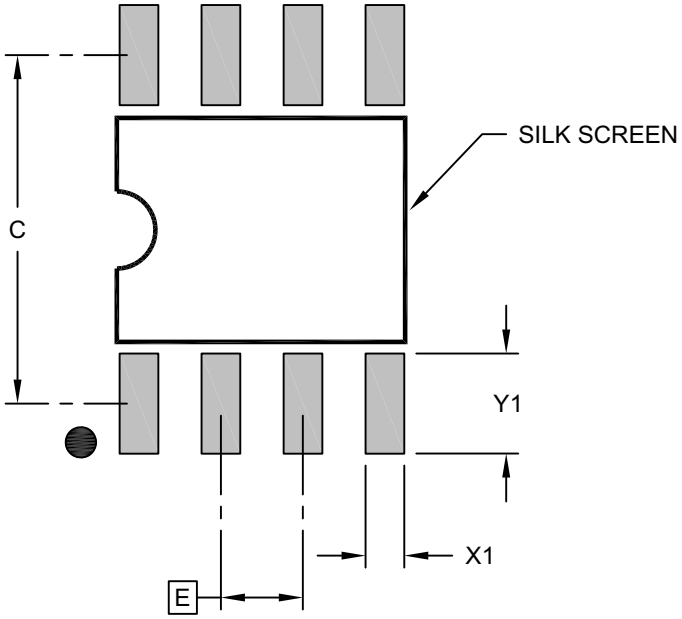
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.
5. Datums A & B to be determined at Datum H.

Microchip Technology Drawing No. C04-057-C2X Rev K Sheet 2 of 2

8-Lead Plastic Small Outline (C2X) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		1.27 BSC	
Contact Pad Spacing	C		5.40	
Contact Pad Width (X8)	X1			0.60
Contact Pad Length (X8)	Y1			1.55

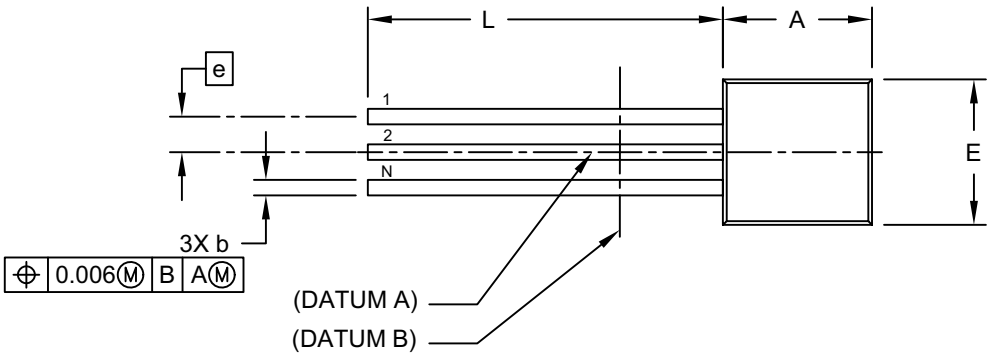
Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2057-C2X Rev K

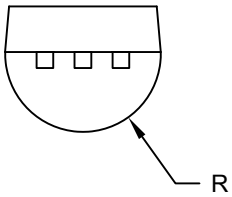
3-Lead Plastic Transistor Outline (TO) [TO-92]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW

SIDE VIEW

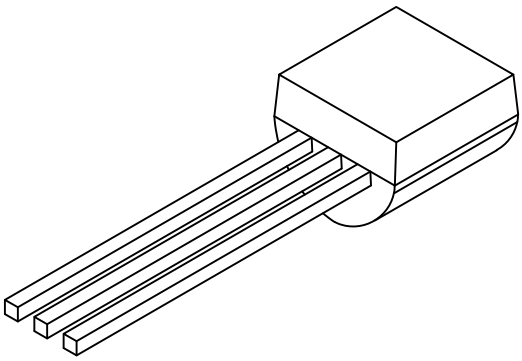


VIEW A-A

Microchip Technology Drawing C04-101-TO Rev D Sheet 1 of 2

3-Lead Plastic Transistor Outline (TO) [TO-92]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		INCHES		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		3	
Pitch	e		.050 BSC	
Bottom to Package Flat	D	.125	-	.165
Overall Width	E	.175	-	.205
Overall Length	A	.170	-	.210
Molded Package Radius	R	.080	-	.105
Tip to Seating Plane	L	.500	-	-
Lead Thickness	c	.014	-	.021
Lead Width	b	.014	-	.022

Notes:

1. Dimensions D and E do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .005" per side.
2. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-101-TO Rev D Sheet 2 of 2

APPENDIX A: REVISION HISTORY

Revision B (February 2024)

- Updated Figure 2-9 in **Section 2.0 "Typical Performance Curves"**.
- Updated package drawings in **Section 5.0 "Packaging Information"**.

Revision A (February 2021)

- Converted Supertex Doc# DSFP-TN2640 to Microchip DS20005795A.
- Changed the package marking format.
- Updated the quantity of the 8-lead SOIC from 2500/Reel to 3300/Reel to align it with the actual BQM.
- Removed the TO-92 N3 P002, P003, P005, P013, and P015 media types to align package specifications with the actual BQM.
- Made minor text changes throughout the document.

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART NO.	XX	-	X	-	X
Device	Package Options		Environmental		Media Type

Device:	TN2640	=	N-Channel Enhancement-Mode Vertical DMOS FET
Packages:	K4	=	3-lead TO-252 (D-PAK)
	LG	=	8-lead SOIC
	N3	=	3-lead TO-92
Environmental:	G	=	Lead (Pb)-free/RoHS-compliant Package
Media Types:	(blank)	=	2000/Reel for a K4 Package
		=	3300/Reel for an LG Package
		=	1000/Bag for an N3 Package

Examples:

a) TN2640K4-G: N-Channel Enhancement-Mode Vertical DMOS FET, 3-lead TO-252 (D-PAK), 2000/Reel

b) TN2640LG-G: N-Channel Enhancement-Mode Vertical DMOS FET, 8-lead SOIC, 3300/Reel

c) TN2640N3-G: N-Channel Enhancement-Mode Vertical DMOS FET, 3-lead TO-92, 1000/Bag

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