

## Introduction [\(Ask a Question\)](#)

The RT PolarFire® Development Kit is an RoHS-compliant, cost-optimized kit with general purpose interfaces that enables you to evaluate features of the RT PolarFire family of FPGAs.

The RT PolarFire Development Kit supports the following interfaces:

- DDR3 x72 Dual Inline Memory Module (DIMM) connector
- High-pin Count (HPC) FMC1, HPC FMC2
- QSPI Flash
- Reduced Gigabit Media-Independent Interface (RGMII)
- USB – UART
- I<sup>2</sup>C-PowerMonitor
- SPI Flash
- DIP Switches
- Push buttons
- User defined LEDs
- JTAG Programming through external header
- Programming using an on-board programmer
- Programming through JTAG external header

The RT PolarFire device available on the RT PolarFire Development Kit is programmed using the on-board programmer. The on-board FlashPro6 programmer is used to develop and debug embedded applications using SoftConsole, Identify, or SmartDebug.

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## 1. Getting Started [\(Ask a Question\)](#)

This section provides information about kit contents, board components, and other high-level information about the kit.

### 1.1 Kit Contents [\(Ask a Question\)](#)

The following table lists the RT PolarFire kit contents.

**Table 1-1.** Kit Contents

| Item                                                                                                                | Quantity |
|---------------------------------------------------------------------------------------------------------------------|----------|
| RT PolarFire® Development Kit (PROTO). For more information about the kit variants, see <a href="#">Table 1-2</a> . | 1        |
| 12V, 5A AC adapter                                                                                                  | 1        |
| 6.00' Power Cord                                                                                                    | 1        |
| Ethernet cable                                                                                                      | 1        |
| USB 2.0 micro A to Mini-B connector for UART interface to PC                                                        | 1        |
| Quickstart card                                                                                                     | 1        |

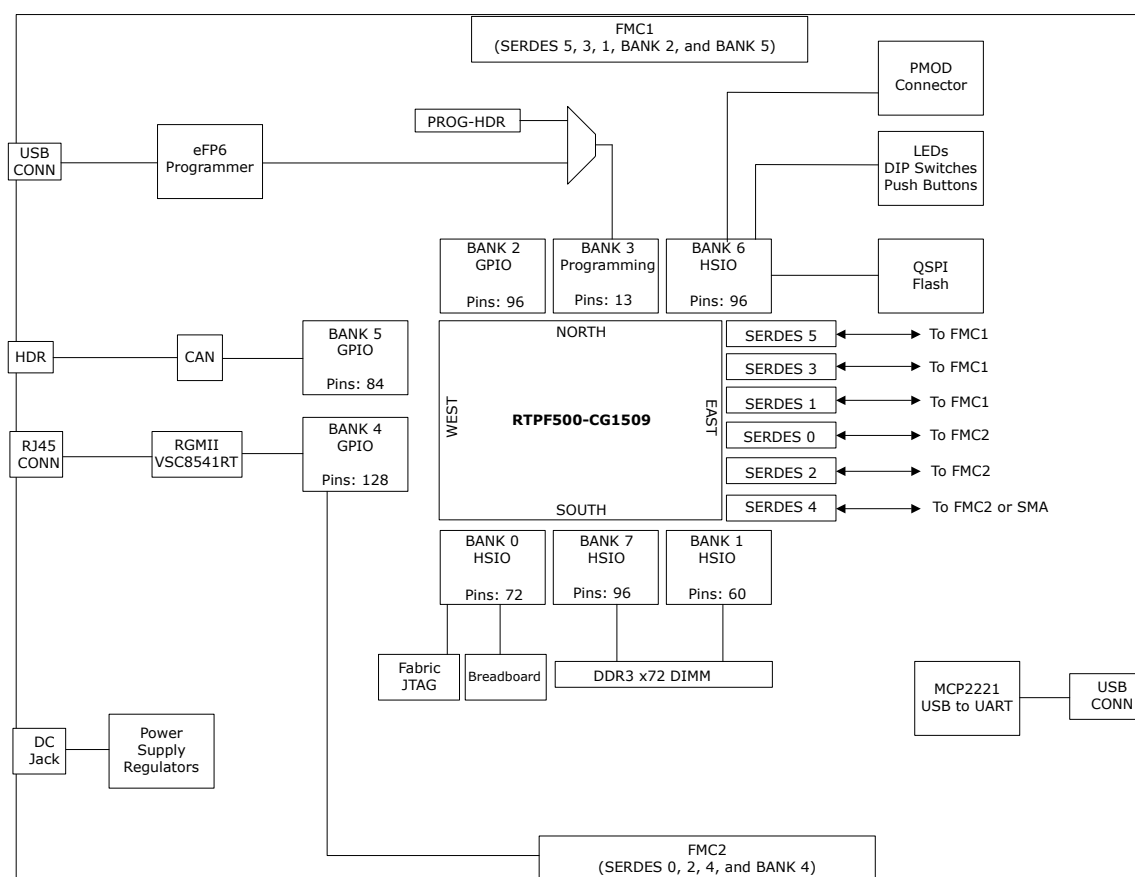
**Table 1-2.** Kit Variants

| Kit Name          | Silicon Part Number   |
|-------------------|-----------------------|
| RTPF-DEV-KIT-CB   | RTPF500T-CB1509PROTO  |
| RTPF-DEV-KIT-CB-1 | RTPF500T-1CB1509PROTO |

You can order any of the preceding variants of the RT PolarFire development kit.

### 1.2 Block Diagram [\(Ask a Question\)](#)

The following block diagram shows the key components of the RT PolarFire Development kit.

**Figure 1-1. Block Diagram**

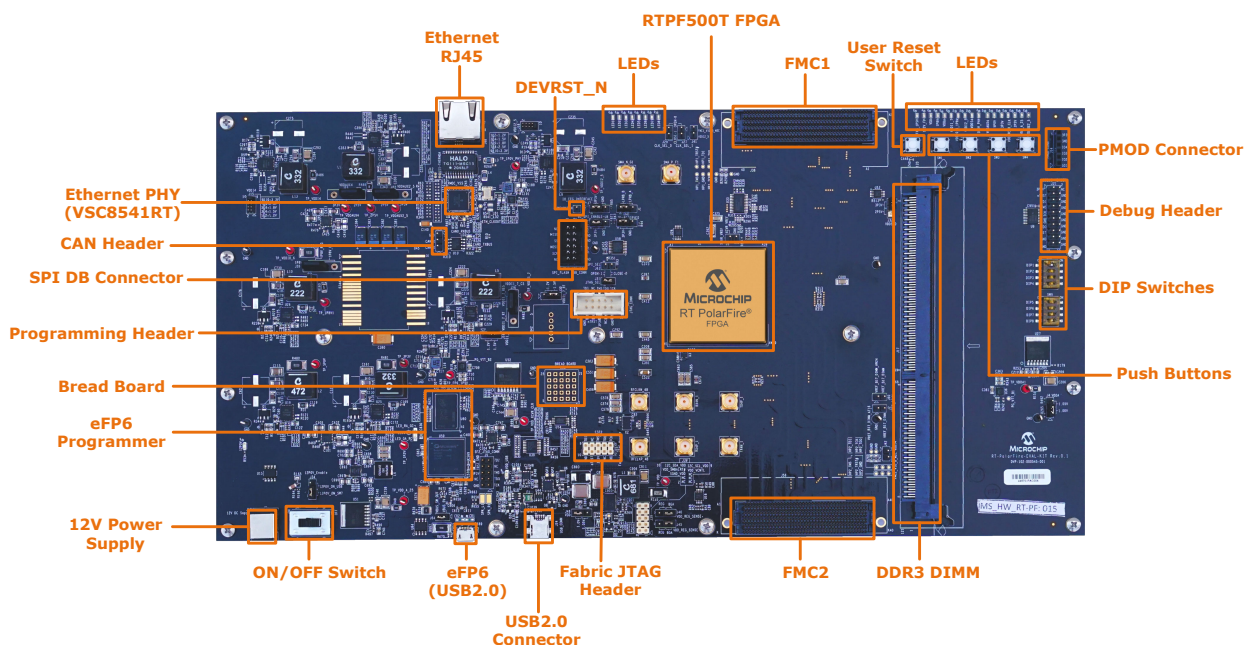
### 1.3 Board Overview [\(Ask a Question\)](#)

The RT PolarFire Development kit features the RTPF500T device with the following capabilities.

- VSC8541RT with an RJ45 connector for 10/100/1000 Mbps Ethernet
- DDR3 x 72 DIMM connector
- Power monitor module
- QSPI Flash device
- USB-UART device
- Bread board
- Fabric JTAG Header
- Push buttons/LEDs/DIP switches
- Debug header
- PMOD Type 1 connector
- FMC1 (HPC) and FMC2 connectors
- On-board programmer
- External JTAG header
- 50 MHz clock oscillator

The following illustration highlights various components of the RT PolarFire Development Kit.

**Figure 1-2. Board Callout**



### 1.3.1 Form Factor [\(Ask a Question\)](#)

The RT PolarFire Development Kit has the following dimensions:

- Form factor (X-Y axis):
  - X-axis (14 inch)
  - Y-axis (6.95 inch)
- The maximum height of the component at the top side is 835 mils
- The maximum height of the component at the bottom side is 413.39 mils

### 1.3.2 Assignment of FPGA I/O Banks [\(Ask a Question\)](#)

The following table lists the assignment of FPGA I/O Banks to on-board interfaces.

**Table 1-3. FPGA I/O Bank Assignments**

| On-Board Interface            | Assigned FPGA I/O BANK |
|-------------------------------|------------------------|
| DDR3 DIMM                     | BANK 1, BANK 7         |
| FMC1 connector                | BANK 2, BANK 5         |
| CAN                           | BANK 5                 |
| FMC2 connector                | BANK 4                 |
| RGMI interface                | BANK 4                 |
| QSPI Flash                    | BANK 6                 |
| User defined LEDs             | BANK 6                 |
| DIP Switches and Push buttons | BANK 6                 |
| Debug header                  | BANK 6                 |
| PMOD (Type 1) connector       | BANK 6                 |

.....continued

| On-Board Interface          | Assigned FPGA I/O BANK |
|-----------------------------|------------------------|
| Bread board                 | BANK 0                 |
| Fabric JTAG Header          | BANK 0                 |
| USB-UART                    | BANK 0                 |
| External Programming header | BANK 3                 |
| External SPI Flash          | BANK 3                 |

## 1.4 Board Components [\(Ask a Question\)](#)

The following table lists the important components of the RT PolarFire Development Kit.

| Component                                           | Label on Board | Description                                                                                                                                                                                                                                                                       |
|-----------------------------------------------------|----------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>Featured Device</b>                              |                |                                                                                                                                                                                                                                                                                   |
| RT PolarFire® FPGA                                  | U1             | For silicon part number, see <a href="#">Table 1-2</a> .                                                                                                                                                                                                                          |
| <b>Power Supply and Monitoring</b>                  |                |                                                                                                                                                                                                                                                                                   |
| 12V power supply input                              | J19            | The board is powered by a 12V power source using an external +12V/5 A DC jack.                                                                                                                                                                                                    |
| ON/OFF switch                                       | SW7            | Power ON/OFF switch from +12V external DC jack                                                                                                                                                                                                                                    |
| <b>Clocks</b>                                       |                |                                                                                                                                                                                                                                                                                   |
| On-board 50 MHz clock oscillator                    | X3             | 50 MHz clock oscillator with single-ended output                                                                                                                                                                                                                                  |
| <b>FPGA Programming and Debugging</b>               |                |                                                                                                                                                                                                                                                                                   |
| SPI Flash                                           | U55            | 1 Gb Micron MT25QU01GBBB8ESF-0SIT QSPI Flash memory device connected to SPI pins on BANK 3 of the RT PolarFire device.                                                                                                                                                            |
| QSPI Flash                                          | U38            | 1 Gb Micron MT25QL01GBBB8ESF-0SIT SPI Flash memory device connected to HSIO pins on BANK 6 of the RT PolarFire device.                                                                                                                                                            |
| JTAG programming MUX                                | U56            | MUX to select the programmer for RT PolarFire device<br>It is used to select on-board programmer or external programmer                                                                                                                                                           |
| SPI programming MUX                                 | U58            | MUX to select SPI<br>Programming MUX to select SPI Flash device or SPI DB                                                                                                                                                                                                         |
| External programming header                         | J3             | External programming header to program and debug the RT PolarFire device using FlashPro. The appropriate programmer must be selected in the FlashPro software.<br><b>Note:</b> For PROTOTYPE kits, the device can be programmed using an external FlashPro 4, 5, or 6 programmer. |
| On board programmer                                 | U59            | On-board programming                                                                                                                                                                                                                                                              |
| <b>Expansion Interfaces</b>                         |                |                                                                                                                                                                                                                                                                                   |
| PMOD                                                | J14            | PMOD Type 1 connector                                                                                                                                                                                                                                                             |
| Bread board                                         | J33            | Bread board connector                                                                                                                                                                                                                                                             |
| <b>Communication Interfaces</b>                     |                |                                                                                                                                                                                                                                                                                   |
| Ethernet PHY                                        | U12            | VSC8541XMVRT                                                                                                                                                                                                                                                                      |
| 1000Base-X Gigabit Ethernet Transceiver RJ45 conn-1 | J68            | Ethernet (RJ45) jack with external magnetics interfacing with VSC8541RT in RGMII mode                                                                                                                                                                                             |
| USB-UART                                            | U7             | MCP2221                                                                                                                                                                                                                                                                           |
| USB connector                                       | J24            | USB Micro A to B connector                                                                                                                                                                                                                                                        |
| CAN                                                 | J20            | CAN Header                                                                                                                                                                                                                                                                        |
| <b>Memory Chips</b>                                 |                |                                                                                                                                                                                                                                                                                   |
| DDR3 DIMM                                           | J17            | DDR3 DIMM connector x72 for North NE anchor point (HSIO BANK 1 and 7)                                                                                                                                                                                                             |
| <b>General Purpose I/O</b>                          |                |                                                                                                                                                                                                                                                                                   |
| Debug Switches                                      | SW1 to SW4     | For debug                                                                                                                                                                                                                                                                         |

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| Component                    | Label on Board | Description                                                              |
|------------------------------|----------------|--------------------------------------------------------------------------|
| Light-emitting diodes (LEDs) | LED1 to LED8   | Eight Active-High LEDs connected to some of the user I/Os for debugging. |
| DIP Switches                 | DIP1 to DIP8   | Eight DIP switches connected to some of the user I/Os for debugging.     |

## 1.5 Handling the Board [\(Ask a Question\)](#)

Handle the board with electrostatic discharge (ESD) precautions to avoid any possible damage or malfunction. For more information about using the board with ESD precautions, see [Understanding Product Handling and ESD Precautions \(for Hybrid Devices\)](#).

## 1.6 Operating Temperature [\(Ask a Question\)](#)

The extended commercial operating temperature range is 0 °C to 100 °C.

## 1.7 Powering Up the Board [\(Ask a Question\)](#)

To Power-Up the board, perform the following steps:

1. Connect 12V, 5A power supply brick to J19.
2. Connect the USB mini cable to J24 and another end to the test PC.
3. Slide Switch SW7 to the **ON** position.
4. Power status LEDs 12P0V, 5P0V, 3P3V, VDDAUX4, VDD\_A\_25, VDD\_XCVR\_CLK, 2P5V, VDDAUX2\_5, VDD, 1P8V, VDDA, VDDI1\_7, VDDI0\_6\_1P8V, VDDI2\_5, VDDI4, 1P0V\_PHY\_VSC8541, FP6\_DDR3\_1P5V, 1P2V\_FP.
5. Install the software required for developing designs and set the jumpers for the pre-programmed design. See [2. Installation and Settings](#).

The following table provides the probe points for power rails.

**Table 1-4.** Power Measurements

| Serial Number | Power Rail    | Probe point | Allowed Tolerance | Expected Voltage (Volts) |
|---------------|---------------|-------------|-------------------|--------------------------|
| 1             | 12P0V         | C61         | ±5%               | 12V                      |
| 2             | VDD           | C522        | ±5%               | 1V                       |
| 3             | 5P0V          | C114        | ±5%               | 5V                       |
| 4             | 3P3V          | C397        | ±5%               | 3.3V                     |
| 5             | 1P8V          | C325        | ±5%               | 1.8V                     |
| 6             | 2P5V          | C341        | ±5%               | 2.5V                     |
| 7             | VDDI1_7       | C309        | ±5%               | 1.5V                     |
| 8             | VDDI2_5       | C373        | ±5%               | 3.3V                     |
| 9             | VDDI4         | C412        | ±5%               | 3.3V                     |
| 10            | VDDA          | C609        | ±5%               | 1V                       |
| 11            | VDDA25        | C663        | ±5%               | 2.5V                     |
| 12            | VDD_XCVR_CLK  | C673        | ±5%               | 2.5V                     |
| 13            | 1P2_FP6       | C691        | ±5%               | 1.2V                     |
| 14            | FP6_DDR3_1P5V | C719        | ±5%               | 1.5V                     |
| 15            | 1P0V_VSC8541  | C194        | ±5%               | 1V                       |
| 16            | VTT_B17_DIMM  | C363        | ±5%               | 0.75V                    |
| 17            | VREF_B17_DIMM | C364        | ±5%               | 0.75V                    |
| 18            | VTT_FP6_DDR3  | C711        | ±5%               | 0.75V                    |
| 19            | VREF_FP6_DDR3 | C712        | ±5%               | 0.75V                    |
| 19            | 1P8V_RT       | C384        | ±5%               | 1.8V                     |
| 20            | VDDI1_7_RT    | C379        | ±5%               | 1.5V                     |

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| Serial Number | Power Rail | Probe point | Allowed Tolerance | Expected Voltage (Volts) |
|---------------|------------|-------------|-------------------|--------------------------|
| 21            | VDDAUX_2_5 | C392        | ±5%               | 2.5V                     |
| 22            | VDDAUX4    | C445        | ±5%               | 2.5V                     |
| 23            | VDD18      | C578        | ±5%               | 1.8V                     |

## 2. Installation and Settings [\(Ask a Question\)](#)

This section provides information about the software and hardware settings required to run the pre-programmed demo design on the RT PolarFire Development Kit.

### 2.1 Software Settings [\(Ask a Question\)](#)

For setting the software, visit the [Libero® Soc Software Download](#) web page, and download and install the latest release of Libero SoC software.



**Important:** A [Platinum license](#) is required to use the RTPF500T device which must be purchased and is not included with the kit.

For further information regarding the Libero SoC installation process, refer to the following:

- For instructions about installing Libero SoC, see [Libero Software Installation and License Installation Guide](#).
- For instructions about purchasing, downloading, and installing Platinum license on the PC where Libero SoC is installed, see [Purchasing Licenses through microchipDirect](#).

### 2.2 Hardware Settings [\(Ask a Question\)](#)

This section provides information about jumper settings, switches, and LEDs on the RT PolarFire Development Kit.

#### 2.2.1 Jumper Settings [\(Ask a Question\)](#)

The following table lists the default jumper settings on the RT PolarFire Development Kit.

**Table 2-1.** Jumper Settings

| Jumper | Description                                                  | Pin     | Default Setting |
|--------|--------------------------------------------------------------|---------|-----------------|
| J60    | BANK 1 VREF for DIMM connector                               | —       | Open            |
| J2     | BANK 7 VREF for DIMM connector                               | —       | Open            |
| J41    | FMC1 connector HB BANK voltage                               | —       | Open            |
| J42    | FMC2 connector HB BANK voltage                               | —       | Open            |
| J27    | CLK_SEL1 pin for SerDes Mux                                  | —       | Open            |
| J29    | CLK_SEL0 pin for SerDes Mux                                  | —       | Open            |
| J31    | Mux select pin for RTPF silicon programming                  | —       | Open            |
| J62    | Mux select pin for SPI Flash or SPI DB                       | —       | Open            |
| J5     | XCVR_Vref pin                                                | —       | Open            |
| J48    | Jumper to select VDD voltage to 1.0V and 1.05V               | 2 and 3 | —               |
| J45    | Jumper to select VDD_REG_SENSE-                              | 2 and 3 | —               |
| J46    | Jumper to select VDD_REG_SENSE+                              | 2 and 3 | —               |
| J30    | Jumper to select VDDI1_7 voltage for MHP8565ASC RT regulator | 2 and 3 | —               |
| J16    | VDDI1_7 voltage select jumper                                | 2 and 3 | —               |
| J32    | VDDSPD voltage select jumper for DDR3 or DDR4                | 1 and 2 | —               |
| J1     | LPRB_A or LPRB_B select jumper                               | 1 and 2 | —               |
| J6     | Reserved pin for BANK3 pullup/pull down option               | 1 and 2 | —               |
| J7     | IO_CFG_INTF select jumper                                    | 1 and 2 | —               |
| J8     | SPI_Enable select jumper                                     | 1 and 2 | —               |
| J64    | USB3320_VBUS                                                 | 1 and 2 | —               |
| J34    | 12PV enable select jumper                                    | 1 and 2 | —               |

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| Jumper | Description                                                                | Pin      | Default Setting |
|--------|----------------------------------------------------------------------------|----------|-----------------|
| J28    | Jumper to select MHP50601A (RT regulator) or MIC2690 for VDD18 and VDDI0_6 | 1 and 2  | —               |
| J26    | Jumper to select MHP8565ASC (RT regulator) or MIC2690 for VDD11_7          | 1 and 2  | —               |
| J4     | Jumper to select VDDA voltage                                              | 1 and 2  | —               |
| J22    | Jumper to select VDDAUX2_5 voltage                                         | 1 and 2  | —               |
| J23    | Jumper to select VDDAUX4 voltage                                           | 1 and 2  | —               |
| J18    | Jumper to select VDDI2_5_Vadj_FMC1 voltage                                 | 9 and 10 | —               |
| J15    | Jumper to select VDDI4_Vadj_FMC2 voltage                                   | 9 and 10 | —               |

### 2.2.2 Power Supply LEDs [\(Ask a Question\)](#)

The following table lists the power supply LEDs on the RT PolarFire Development Kit.

**Table 2-2.** Power Supply LEDs

| LED          | Description                        |
|--------------|------------------------------------|
| 12P0V        | 12V power supply                   |
| 5P0V         | 5V power supply                    |
| 3P3V         | 3.3V power supply                  |
| VDD_A_25     | VDDA25 voltage                     |
| 1P8V         | 1.8V power supply                  |
| VDD          | Core voltage                       |
| VDDI1_7      | BANK 1 and 7 voltage               |
| 1P0V_PHY     | VSC8541_Phy_1V                     |
| VDDI4        | BANK 4 voltage                     |
| VDDI2_5      | BANK 2, 5 voltage                  |
| VDDI0_6_1P8V | BANK 0, 6 voltage                  |
| FP6_1P5V     | FlashPro6 1.5V voltage             |
| 1P2V_FP      | FlashPro6 1.2V voltage             |
| VDDAUX4      | BANK 4 auxiliary voltage           |
| VDD_XCVR_CLK | Transceiver reference clock supply |
| 2P5V         | 2.5V                               |
| VDDAUX2_5    | BANK 2, 5 auxiliary voltages       |

### 2.2.3 Test Points [\(Ask a Question\)](#)

The following table lists all the test points available on the RT PolarFire Development Kit.

| Test Point                | Description                                 |
|---------------------------|---------------------------------------------|
| GND1TP_BLK to GND18TP_BLK | Test point for Ground                       |
| ETH_CLKOUT                | Test point for VSC8541_CLK out              |
| 8541_MDC                  | Test point for VSC8541_MDC                  |
| 8541_MDIO                 | Test point for VSC8541_MDIO                 |
| TP_5P0V                   | Test point for 5V supply                    |
| TP_3P3V                   | Test point for 3.3V supply                  |
| TP_1P8V1                  | Test point for 1.8V supply                  |
| TP_VDDI0_6                | Test point for BANK voltage 0 and 6         |
| TP_2P5V                   | Test point for 2.5V supply                  |
| TP_VDD                    | Test point for VDD core supply              |
| PG_VDD                    | Test point for power good for VDD regulator |

.....continued

| Test Point      | Description                                |
|-----------------|--------------------------------------------|
| TP_VDDI1_7      | Test point for BANK voltage 1 and 7        |
| TP_VDDI2_5      | Test point for BANK voltage 2 and 5        |
| TP_VDDI4        | Test point for BANK 4 voltage              |
| TP_VDDAUX2_5    | Test point for BANK 2 and 5 Aux voltage    |
| TP_VDDAUX4      | Test point for SD_CLK_FB/eMMC_DATA4 at Mux |
| TP_VDDA1        | Test point for VDDA                        |
| TP_VDD_A_25     | Test point for VDDA25 and VDD25            |
| TP_VDD_XCVR_CLK | Test point for VDD_XCVR_CLK                |
| TP_1P2V         | Test point for VDD core voltage for FP6    |
| TP_FP6_1P5V     | Test point for 1.5V_eFP6 DDR3              |
| TP_1P0V_PHY     | Test point for PHY 1V voltage              |

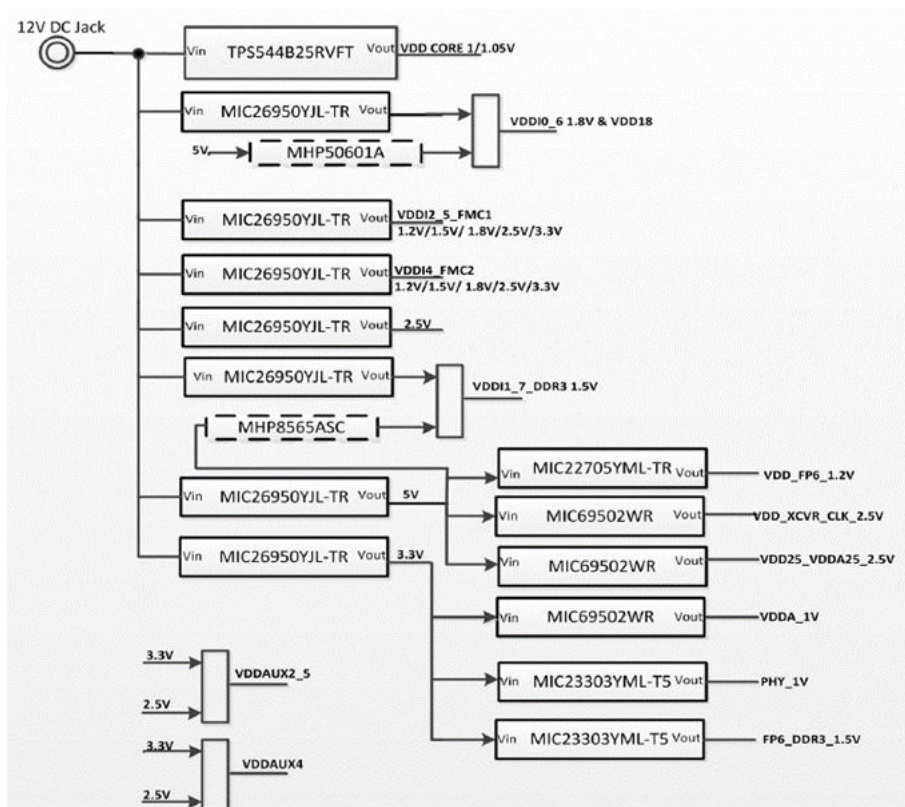
## 2.3 Power Sources [\(Ask a Question\)](#)

RT PolarFire Development Kit uses Microchip power regulators. For more information about these power supply devices, see [Power Management](#). RT PolarFire devices have multiple I/O banks that require power supplies. The following table lists these key power supplies required for normal operation of the RT PolarFire Development Kit.

**Table 2-3.** I/O Voltage Rails

| Name                           | Description                                                                                                                                                                                                                                                                                                              | Operating Voltage                                                                                                                                                                                  | Unused Condition                                                                                                                                                                     |
|--------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| V <sub>DDI<sub>x</sub></sub>   | Supply for I/O circuits in a bank                                                                                                                                                                                                                                                                                        | For JTAG bank—1.8V/2.5V/3.3V For GPIO bank—1.2V/1.5V/ 1.8V/2.5V/3.3V For HSIO bank—1.2V/1.5V/1.8V                                                                                                  | The bank supply is not allowed to be left floating for any unused bank. It must be powered down to ground by direct connection.                                                      |
| V <sub>DD25</sub>              | Power for corner PLLs and PNVM                                                                                                                                                                                                                                                                                           | 2.5V                                                                                                                                                                                               | Must connect to 2.5V                                                                                                                                                                 |
| V <sub>DD18</sub>              | Power for programming and HSIO receiver                                                                                                                                                                                                                                                                                  | 1.8V                                                                                                                                                                                               | Must connect to 1.8V                                                                                                                                                                 |
| V <sub>D<sub>DAUXx</sub></sub> | Auxiliary supply for I/O circuitsAuxiliary supply voltage must be set to 2.5V or 3.3V and must always be equal to or higher than V <sub>DDI<sub>x</sub></sub> . For information about legal V <sub>DDI</sub> and V <sub>D<sub>DAUX</sub></sub> combinations, see <a href="#">RT PolarFire FPGA User I/O User Guide</a> . | Greater than or equal to V <sub>DDI</sub> In cases where V <sub>DDI</sub> and V <sub>D<sub>DAUX</sub></sub> in a given GPIO bank are both 2.5V or 3.3V, they must be tied together to same supply. | Must connect to greater than or equal to V <sub>DDI</sub>                                                                                                                            |
| V <sub>REF</sub>               | Supply reference voltage for reference receiversEach bank can have only one V <sub>REF</sub> value. V <sub>REF</sub> can be externally supplied or internally generated. For more information, see <a href="#">RT PolarFire FPGA User I/O User Guide</a> .                                                               | Depends on the I/O standards                                                                                                                                                                       | The regular I/Os are used as V <sub>REF</sub> supply. Libero® SoC configures unused user I/Os as the input buffer is disabled and the output buffer is tri-stated with weak pull-up. |

The following figure shows the power scheme of the RT PolarFire Development kit.

**Figure 2-1.** RT PolarFire Power Scheme

The following table lists the power regulators used on the RT PolarFire Development kit.

**Table 2-4.** Power Regulators

| Voltage Rail                 | Part Number    | Description                      | Current |
|------------------------------|----------------|----------------------------------|---------|
| 5V                           | MIC26950JL-TR  | IC REG BUCK ADJUSTABLE           | 12A     |
| VDD (1.2V) 1P2_FP6, VDD (1V) | MIC22705YML    | IC REG BUCK ADJUSTABLE           | 7A      |
| VSC_PHY(1.2V)                | MIC23303YML-T5 | IC REG BUCK ADJUSTABLE           | 3A      |
| 1.1V_LPDDR4                  | MIC23303YML-T5 | IC REG BUCK ADJUSTABLE           | 3A      |
| 1P8V                         | MIC23303YML-T5 | IC REG BUCK ADJUSTABLE           | 3A      |
| VDD_XCVR_CLK (2P5V)          | MIC69502WR     | IC REG LINEAR POS ADJUSTABLE     | 5A      |
| 3P3V                         | MIC26950JL-TR  | IC REG BUCK ADJUSTABLE           | 12A     |
| VDDA                         | MIC69502WR     | IC REG LINEAR POS ADJUSTABLE     | 5A      |
| 1P5V_DDR3                    | MIC23303YML-T5 | IC REG BUCK ADJUSTABLE           | 3A      |
| VTT and VREF                 | MIC5166YML-TR  | IC PWR SUP 3 A HS DDR TERM 10MLF | 3A      |
| VDD18 and VDDI0_6            | MIC26950YJL-TR | IC REG BUCK ADJUSTABLE           | 12A     |
| VDD (1V/1.05V)               | TPS544B25RVFT  | IC REG BUCK ADJUSTABLE           | 20A     |
| VDDI1_7                      | MIC26950YJL-TR | IC REG BUCK ADJUSTABLE           | 12A     |
| VDDI2_5                      | MIC26950YJL-TR | IC REG BUCK ADJUSTABLE           | 12A     |
| VDDI4                        | MIC26950YJL-TR | IC REG BUCK ADJUSTABLE           | 12A     |
| VDDA25                       | MIC69502WR     | IC REG LINEAR POS ADJUSTABLE     | 5A      |

### 3. Board Components and Operation [\(Ask a Question\)](#)

This section describes the key components of the RT PolarFire Development Kit and provides information about the important board operations. For more information, see the board level schematics.

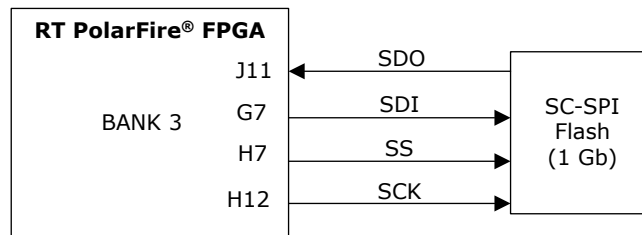
#### 3.1 SPI Serial Flash [\(Ask a Question\)](#)

RT PolarFire Development Kit has a 1 Gb SPI Flash and SPI Flash daughter board connector. The SPI Flash is connected to BANK 3 SC-SPI pins to support IAP programming.

**Part number:** MT25QL01GBBB8ESF-0SIT  
**Manufacturer:** Micron  
**Flash Type:** NOR

The following figure shows the SPI Flash interface on the RT PolarFire® Development kit.

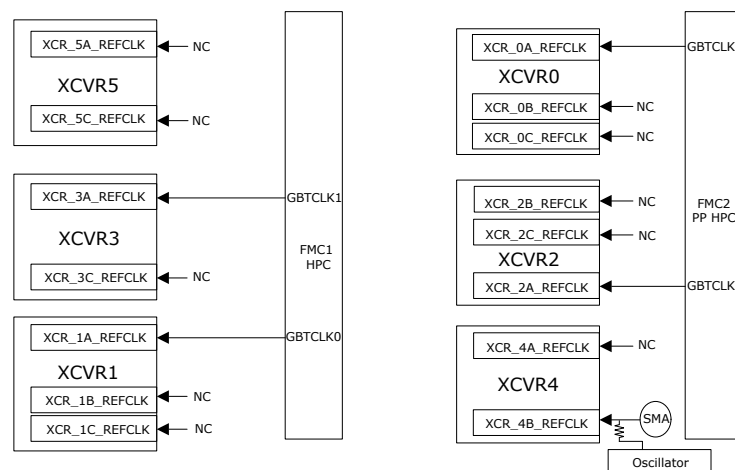
**Figure 3-1.** SPI Flash Interface



#### 3.2 High-Speed Transceivers Configuration [\(Ask a Question\)](#)

The RTPF500T device includes six XCVR blocks and 24 SerDes lanes. The XCVR clocking scheme for driving the FMC connectors is shown in the following figure.

**Figure 3-2.** XCVR Clocking Scheme



As shown in the preceding figure, SerDes1 and SerDes3 lanes provide clocks to FMC1. SerDes0 and SerDes2 lanes provide clocks to FMC2.

### 3.3 Communication Interfaces [\(Ask a Question\)](#)

This section describes the communication interfaces available on the kit.

#### 3.3.1 Ethernet (RGMII Interface) [\(Ask a Question\)](#)

The RT PolarFire Development Kit includes Microchip's VSC8541RT device for Ethernet connectivity. The VSC8541RT device is a radiation tolerant single port Fast Ethernet copper PHY targeting space-constrained 10/ 100/1000BASE-T applications. The on-board VSC8541RT (GMII) is connected to I/O BANK 4 (GPIO) of the RT PolarFire FPGA.

#### 3.3.2 CAN Interface [\(Ask a Question\)](#)

The RT PolarFire Development Kit does not support Controller Area Network (CAN) interface.

### 3.4 Memory Interface [\(Ask a Question\)](#)

The kit supports a standard DDR3 Dual Inline Memory Module (DIMM) socket for plugging in any standard DDR3 DIMM with variable density.

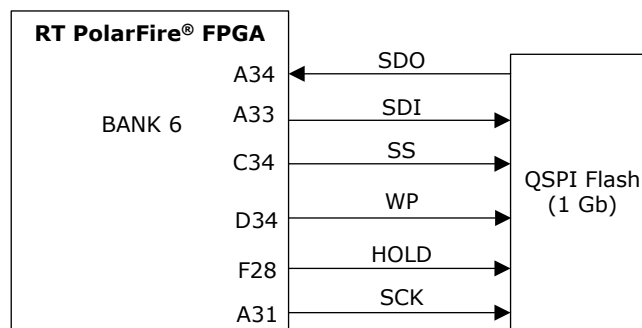
### 3.5 QSPI Serial Flash [\(Ask a Question\)](#)

RT PolarFire Development Kit has a 1 Gb QSPI Flash. The QSPI Flash is connected to BANK 6 to support application execution.

**Part Number:** MT25QU01GBBB8ESF-0SIT  
**Manufacturer:** Micron  
**Flash Type:** NOR

The following figure shows the QSPI Flash interface on the RT PolarFire Development kit.

**Figure 3-3.** QSPI Flash Interface



### 3.6 Expansion Capabilities [\(Ask a Question\)](#)

The following sections explain the expansion connectors for the RT PolarFire Development Kit.

#### 3.6.1 Pmod Type 1 Connector [\(Ask a Question\)](#)

The kit supports a Pmod (peripheral module interface) Type 1 connector (part number: PPPC061LFBN-RC). The I/O BANK 6 (HSIO) supports Pmod Type1 connections through a voltage-level translator.

#### 3.6.2 Debug Header [\(Ask a Question\)](#)

The kit supports a debug header connected to I/O BANK 6 (HSIO). This header supports debug header connections through a voltage-level translator.

### 3.6.3 Bread Board [\(Ask a Question\)](#)

The kit supports a bread board. 20 pins of the I/O BANK 0 (HSIO) are connected to bread board connections.

### 3.6.4 Fabric JTAG Header [\(Ask a Question\)](#)

The kit supports a fabric JTAG header connected to I/O BANK 0 (HSIO) supports JTAG header through voltage-level translator.

## 3.7 Voltage and Current Monitoring [\(Ask a Question\)](#)

The kit has provision to measure current for the following power rails:

- VDD
- VDDIO\_6\_1P8V ( 1.8V for BANK 0 and 6)
- VDDA
- VDD\_XCVR\_CLK
- 3P3V
- 5P0V
- VDD\_A\_25
- VDDI1\_7
- 2P5V
- VDDI4
- VDDI2\_5
- 1P8V

Current sensing is done by PAC1934T-I/JQ. The I<sup>2</sup>C interface is available on digital values to read back values. Sensor's I<sup>2</sup>C interface is connected to the MCP2221 I<sup>2</sup>C interface.

### 3.8 User I/Os [\(Ask a Question\)](#)

The kit includes four push-buttons, eight DIP switches, and eight LED indicators connected to I/O BANK 6 (HSIO).

### 3.9 USB to UART Interface [\(Ask a Question\)](#)

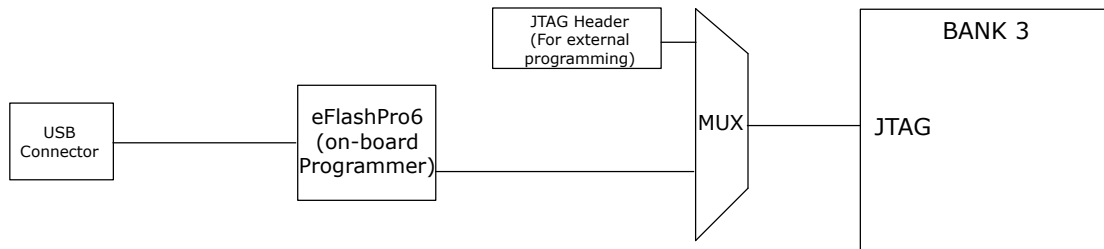
The kit includes Microchip's MCP2221 device that is a USB to UART bridge controller to support UART interface on the board. UART I/Os are connected to the I/O BANK 0 (HSIO) of the RT PolarFire FPGA. I<sup>2</sup>C interface signals are connected to current measurement IC PCA9516APW,118.

## 3.10 Programming Scheme [\(Ask a Question\)](#)

The on-board RT PolarFire FPGA can be programmed using [3.10.1. JTAG Programming Scheme](#) or [3.10.2. SPI Programming Scheme](#).

### 3.10.1 JTAG Programming Scheme [\(Ask a Question\)](#)

The on-board RT PolarFire device can be programmed using the on-board JTAG programmer or an external JTAG programmer as shown in the following figure.

**Figure 3-4. JTAG Programming Scheme**

The kit includes a multiplexer (U56) for selecting either the external programming JTAG header or the on-board programmer. The following are the multiplexer details:

**Part Number** 74CBTLV3257BQ,115  
**Manufacturer** NXP

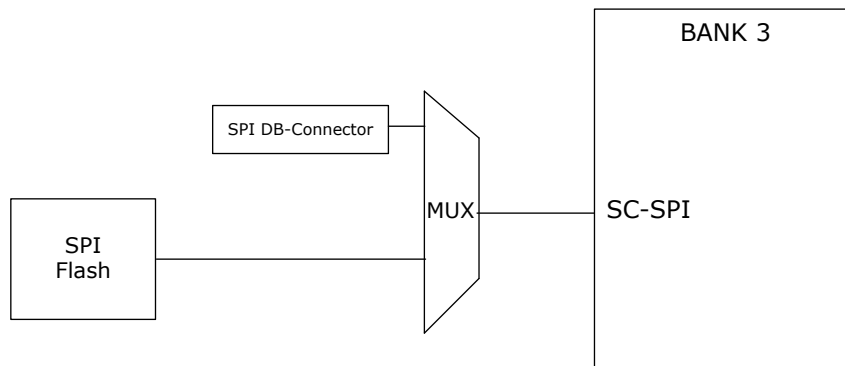
The following table lists the J31 jumper setting for selecting the required JTAG programmer.

**Table 3-1. J31 Jumper Setting**

| Jumper (J31) | JTAG Selection              |
|--------------|-----------------------------|
| Open         | External Programming header |
| Close        | On-board Programmer         |

### 3.10.2 SPI Programming Scheme [\(Ask a Question\)](#)

The on-board RT PolarFire device can be programmed using the on-board SPI interface or an external SPI interface as shown in the following figure.

**Figure 3-5. SPI Programming Scheme**

The kit includes a multiplexer (U58) for selecting either the external SPI DB-Connector header or the on-board SPI Flash. The following are the multiplexer details:

**Part number** 74CBTLV3257PW,118  
**Manufacturer** NXP

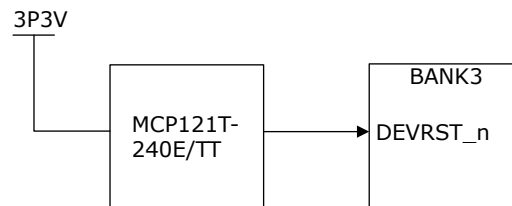
The following table lists the J62 jumper setting for selecting the required SPI programming.

**Table 3-2.** J62 Jumper Setting

| Jumper (J62) | SPI Selection    |
|--------------|------------------|
| Open         | On-board SPI     |
| Close        | SPI DB-Connector |

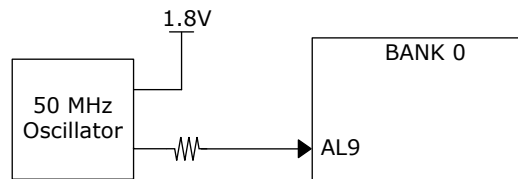
### 3.11 System Reset [\(Ask a Question\)](#)

DEVRST\_N is an input-only reset pad that asserts a full reset of the chip at any time. The following figure shows a sample reset circuit that uses a Microchip MCP121T-240E/TT device.

**Figure 3-6.** Reset Scheme

### 3.12 50 MHz Oscillator [\(Ask a Question\)](#)

A 50 MHz clock oscillator with an accuracy of  $\pm 10$  ppm is available on the board.

**Figure 3-7.** 50 MHz Clock Oscillator

The connection of this clock oscillator with the FPGA fabric is listed the following table.

**Table 3-3.** Clock Oscillator and the FPGA Fabric Connection

| RT PolarFire® Package Pin Number | RT PolarFire Device Pin Name                           |
|----------------------------------|--------------------------------------------------------|
| AL9                              | HSIO194PB0/CLKIN_N_2/CCC_NW_CLKIN_N_2/CCC_NW_PLL1_OUT0 |

For more information, refer to board-level schematics (provided separately).

### 3.13 Pin List [\(Ask a Question\)](#)

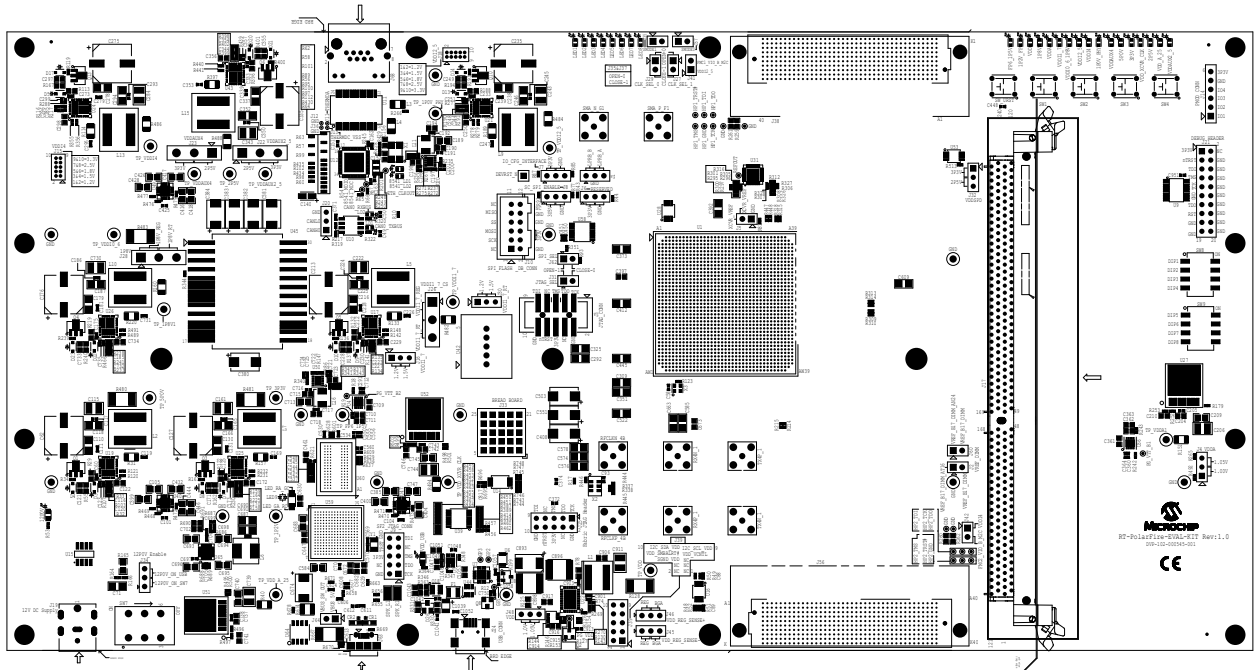
For more information about the package pins, see [PPAT](#).

### 3.14 Board Component Placement [\(Ask a Question\)](#)

This section provides PCB silkscreens to identify board components along with their reference designators.

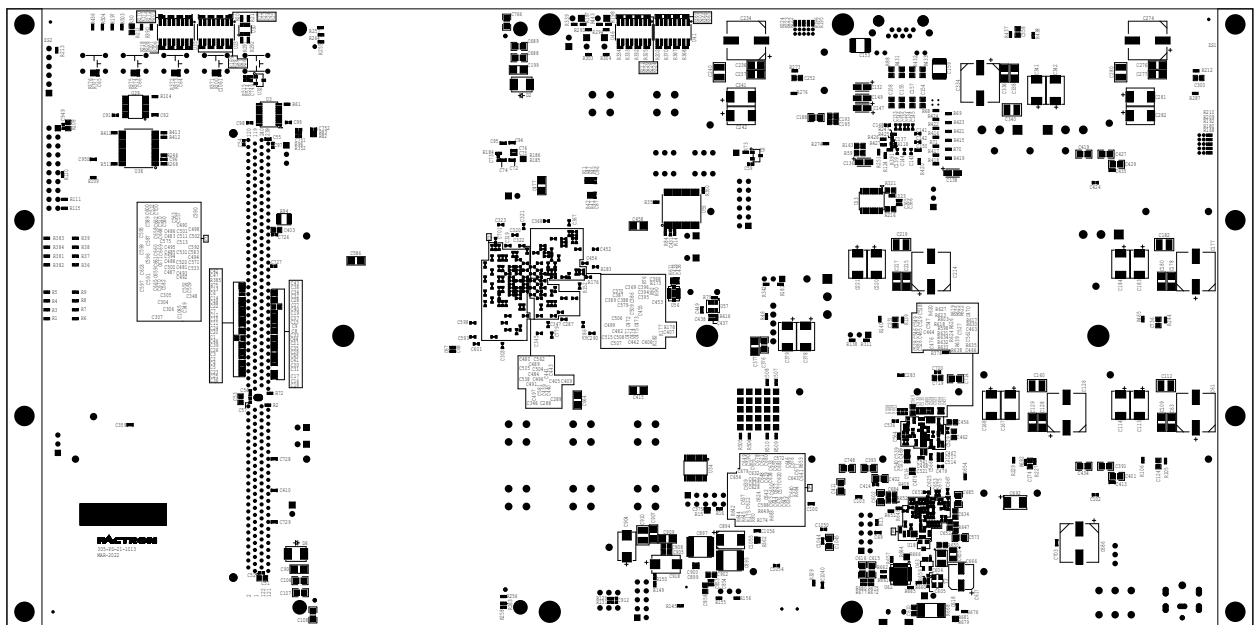
The following silkscreen shows the top view of the board.

Figure 3-8. Top View



The following silkscreen shows the bottom view of the board.

Figure 3-9. Bottom View



## 4. Appendix: Programming the RT PolarFire Device Using On-Board Programmer [\(Ask a Question\)](#)

The RT PolarFire Development Kit includes an on-board programmer. Therefore, an external programmer hardware is not required to program the RT PolarFire device. The device can be programmed using the FlashPro Express software installed on the host PC.



**Important:** The programming file will be available in a future release.

---

To program the on-board RT PolarFire device using the on-board programmer, perform the following steps:

1. Connect the power supply cable to the **J19** connector on the board.
2. Close Jumper **J31** for MUX U56.
3. Power on the board using the **SW7** slide switch.
4. When the board is successfully set up, the power LEDs start glowing.
5. Download FlashPro Express from [Programming and Debug Tools Downloads](#).
6. On the host PC, launch the FlashPro Express software.
7. Click **New Project**.
8. In the **New Project** window, do the following, and click **OK**.
  - Enter a project name
  - Select **Single device** as the programming mode
9. Click **Configure Device**.
10. Click **Program** to program the device.
11. From the **View Programmer** pane, select the on-board FlashPro6 programmer.
12. Click **Browse**, and select the `.stp` file from the **Load Programming File** window.

The **Programmer List** window in the FlashPro Express software shows the programmer name, programmer type, port, programmer status, and information about whether the programmer is enabled.

When the device is programmed successfully, the `Run Program PASSED` status is displayed.

## 5. Revision History [\(Ask a Question\)](#)

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

**Table 5-1.** Revision History

| Revision | Date    | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|----------|---------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| C        | 08/2024 | The following is a summary of the changes made in revision C of this document. <ul style="list-style-type: none"><li>• Updated <a href="#">Table 1-1</a> and <a href="#">Table 1-2</a> in <a href="#">1.1. Kit Contents</a> section.</li><li>• Updated Platinum license information in <a href="#">2.1. Software Settings</a> section.</li><li>• Updated <a href="#">Figure 3-2</a> and removed "SerDes5" in <a href="#">3.2. High-Speed Transceivers Configuration</a> section.</li></ul> |
| B        | 04/2023 | <ul style="list-style-type: none"><li>• Made the silkscreen figures searchable, see <a href="#">Figure 3-8</a> and <a href="#">Figure 3-9</a>.</li><li>• Updated <a href="#">Table 2-2</a>.</li></ul>                                                                                                                                                                                                                                                                                      |
| A        | 09/2022 | Initial revision                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |

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