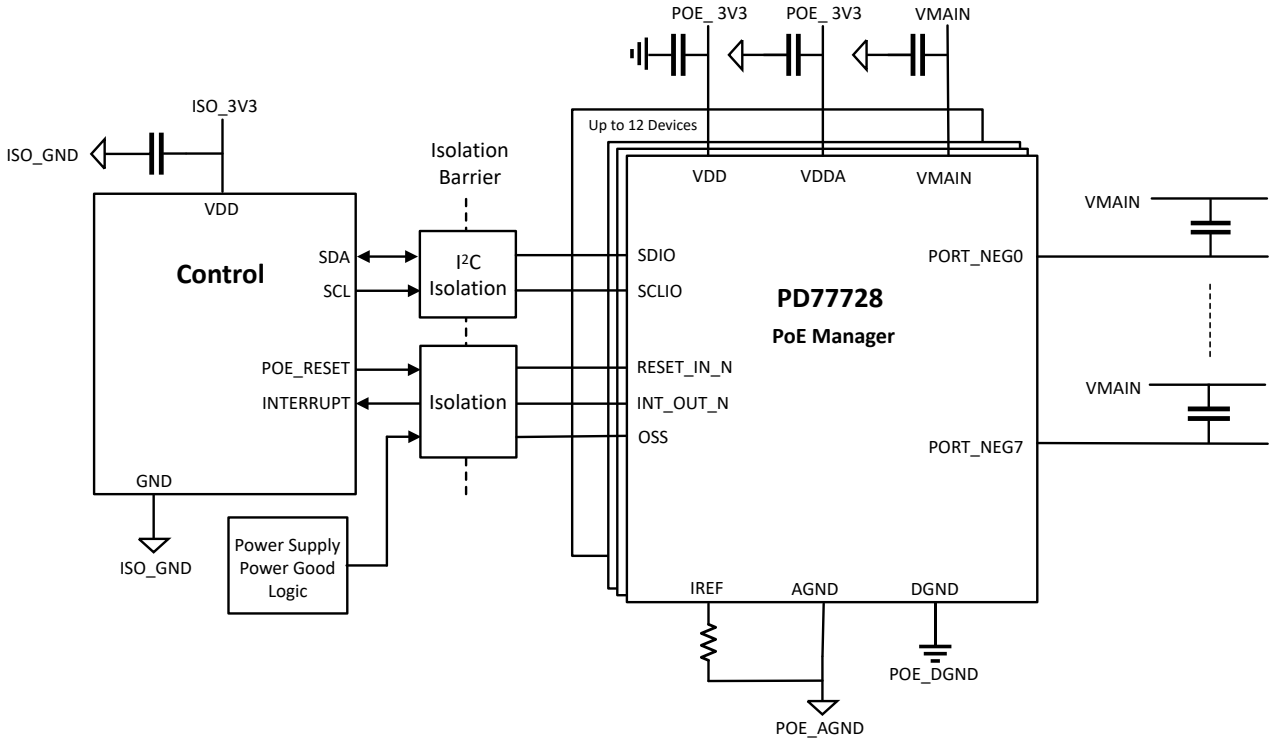
Introduction

The PD77728 device is a part of Microchip's seventh generation IEEE® 802.3bt compliant Power over Ethernet (PoE) Power Sourcing Equipment (PSE) family. This device is a fully integrated 8-port PoE manager with integrated Field Effect Transistor (FET) switches and current sense resistors. Up to 12 devices can be cascaded to provide 48 4-pair ports. The device is available in a 56-pin 8 mm × 8 mm QFN package.

The following figure shows the typical PoE application of the PD77728 device.

Figure 1. Typical PoE Application



Features

The PD77728 device and PD77728 based PSE have the following key features:

- Supported Standards
  - IEEE 802.3bt
- Supported PD Types
  - Type 1 (802.3af) , Type 2 PDs, (802.3at)
  - Single-Signature PDs
  - Dual-Signature PDs
  - Pre-Standard (Legacy) 2-pair PDs
  - Supports non-compliant and legacy PDs
- Three Operational Modes
  - Semi-Auto mode
  - Managed Auto mode
  - Unmanaged Auto mode
- Cascade up to 12 devices to support 96 × 2-pair ports or 48 × 4-pair ports and any 4-pair/2-pair combination
- Device Features
  - Stand-Alone device supports up to 8 × 2-pair ports or 4 × 4-pair ports and any 4-pair/2-pair combination
  - Per-Port integrated FET, sense resistor, and port diode
  - Total port resistance of 160 mΩ
  - Device power dissipation ≤ 2W at full load
  - Two power rails (55V and 3.3V) for maximum power efficiency
  - Guaranteed 4-pair output power of > 90W
  - Over Supply Signal (OSS) support
  - AutoClass support
  - MarkHold function support
  - Supports Fast and Perpetual PoE
  - Host Interface through I^2C Communication
- Real-Time Protection (RTP)
- Measurements
  - Per-Port voltage and current measurement
  - Accurate main power measurement
- Surge
  - Surge up to 2 kV without additional components per IEC61000-4-5-2014
  - Surge compliance, ITU-T K.21, GR1089, IE61000-4-5-2014, EN55024
    - Up to 10 kV per IEC61000-4-5-2014
    - Up to 6 kV per ITU-T K.21
- Physical Characteristics
  - Ambient temperature range –40 °C to 85 °C
  - 56-pin 8 mm × 8 mm QFN package with thermal pad
  - MSL3, RoHS compliant

Applications

The PD77728-based PSE has the following typical applications:

- Campus switches
- Switches and routers for enterprises, small and medium businesses, Small Office Home Office (SOHO), and commercial markets
- Switches for lighting markets
- PoE injectors

Table of Contents

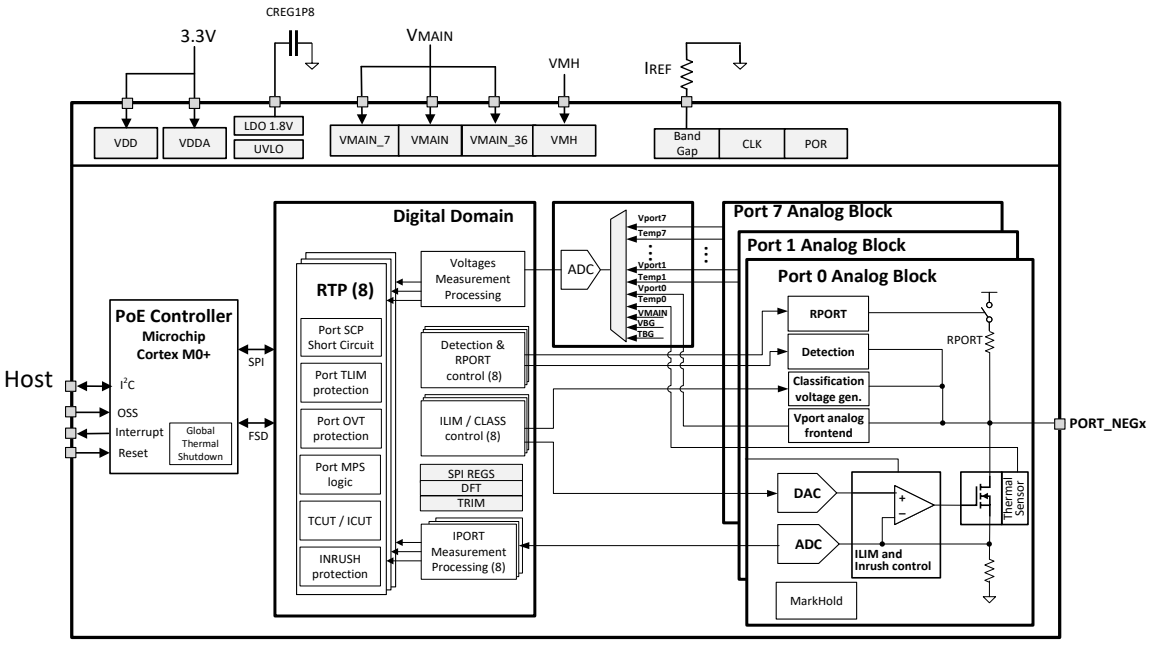
1. Functional Descriptions

This section describes the following four main blocks of the PD77728 device:

- Analog front-end block (x8)
- Voltage and temperature measurement module
- Digital processing and control block
- PoE controller (based on the Cortex® -M device)

The following figure shows a high-level block diagram of the device.

Figure 1-1. Block Diagram



1.1 Analog Front-End Block

The analog front-end block of each port contains the following components:

- Current limiting block—fast acting current limiting loop
- Classification voltage regulation
- V_{PORT} measurement analog interface
- Detection module
- Current measurement module
- Proprietary MarkHold analog block

This structure allows efficient and flexible port control. It also supports simultaneous power-up/power-on 8 ports control.

1.2 Voltage and Temperature Measurement Module

The module measures port voltages, V_{MAIN} voltage, and temperature.

1.3 Digital Processing and Control Block

The digital block communicates with the integrated PoE controller and controls the analog front-end block. It consists of the following blocks:

- Ports ON/OFF control block
- I_{LIM} and I_{CLASS} control blocks
- I_{INRUSH} control and protection block
- Detection and R_{PORT} control block
- Port voltage and temperature measurement post-processing module
- Port current post-processing module
- RTP module

1.4 Integrated PoE Controller

The integrated PoE controller controls both port-level and device-level PoE tasks. The firmware is pre-programmed into the integrated controller with field-upgradable capability through the I^2C host interface.

The integrated PoE controller provides the following features:

- Host communication interface (Fast-Mode Plus I^2C interface, INT_OUT signal)
- OSS fast shut-down control
- Device-level data processing
- Supports PoE firmware download capability from host
- Manages one device 2p and 4p ports configuration
- Device-Level power budgeting and power assignment

1.5 Power

The PD77728 device is designed for low power consumption and low power dissipation, using cutting-edge process technology and proprietary port's MOSFET design.

The following two parameters allow a total power dissipation of equal to or less than 2W at T_J = 125 °C:

- Very low channel (port) resistance (typically, 160 mΩ at 25 °C)
- Very low V_{MAIN} quiescent current

The PD77728 device supports any power rail sequencing of the V_{MAIN} and V_{DD} rails.

1.6 Real-Time Protection (RTP)

This section describes the RTP blocks included in the PD77728 device. The device supports multi-level and real-time support mechanisms. All RTP mechanisms are configured by the PoE controller, implemented in the digital domain, and directly control the port analog front-end. Each port has its own RTP protection blocks. This type of design ensures fast-acting protection under all conditions.

1.6.1 Current Overload (T_{LIM}/I_{LIM}) Protection

The configurable I_{LIM} and T_{LIM} parameters are based on the IEEE 802.3bt standard. T_{LIM} and I_{LIM} threshold levels are selected by firmware based on the assigned class. The port shuts down if it enters current limit (I_{LIM}) and maintains I_{LIM} for a period of T_{LIM}. Current overload RTP also protects against repetitive overload conditions, where the port repetitively enters current limit for a duration less than T_{LIM}, which might result in a device damage due to accumulated overheating. The PD77728 overload protection mechanism disconnects the port if the accumulated power poses danger to the Safe Operating Area (SOA) of the MOSFET.

1.6.2 Short-Circuit Protection

If the port enters the current limit and the port voltage (V_{PORT}) drops below a configurable value, the port is considered to be in a short-circuit condition. In this case, the port is turned off within 100 µs (typical) to minimize the power dissipation on the MOSFET during such a harsh condition. The voltage below which the port is considered to be in a short-circuit condition is also configurable.

1.6.3 Inrush (Power-Up) Protection

During the port inrush phase, the PD capacitor is charged with a constant current for up to 75 ms. If the PD is not limiting the current, the PSE uses its current limit to limit the capacitor inrush current (for most cases, I_{LIM} is 0.425A). Inrush current is also configurable. A failed PD capacitor, or too large a capacitor value, might result in either a true short-circuit condition on the port during inrush (leads to very high-power dissipation, equal to 0.425A × V_{MAIN}), or a very high-power dissipation due to the slow increase in the capacitor voltage. A dedicated inrush protection mechanism is provided to protect the device from such events, assuring that the port's MOSFET does not exceed its SOA under any condition.

1.6.4 Over-Temperature (OVT) Protection

OVT protection adds an additional layer of protection to the device, and protects the device from overheating and damaging in parallel to the other protection mechanisms. An example for OVT protection is a slow increase in ambient temperature (for example, a failed fan), resulting in an elevated junction temperature which exceeds the maximum operating junction temperature. In this case, the OVT real-time protection either limits the number of ports that can be turned on at such temperature, or turns off the port (s) with the highest junction temperature.

1.6.5 T_{CUT}/I_{CUT} Protection

The firmware selects T_{CUT} and I_{CUT} threshold levels based on the assigned class. The port is turned off if the port current exceeds I_{CUT} for a cumulative time of T_{CUT} (typical 65 ms). Both T_{CUT} and I_{CUT} values are configurable.

1.6.6 Maintain Power Signature (MPS)

Although this condition does not endanger the PSE device, the MPS signature is required to keep a PD powered and to disconnect its power if PD is removed. The PD77728 device incorporates MPS protection, in which the port is turned off if the PD current does not comply with the required hold current and time, as defined in the IEEE 802.3bt standard. Both the hold current (I_{HOLD}/$I_{HOLD-2P}$) and the duration (T_{MPS}, T_{MPDO}) are configurable parameters.

1.7 Over Supply Shutdown (OSS)

OSS is a control pin required to turn off ports of a certain priority due to failure in one of the power supplies. Both 1-bit signal priority and 3-bit signal priority are supported.

1.8 V_{MAIN} Under-Voltage Lockout (V_{MAIN_UVLO})

V_{MAIN} under-voltage lockout (V_{MAIN_UVLO}) turns off ports when V_{MAIN} drops below a set threshold.

1.9 Surge

The PD77728 device supports up to 2 kV per IEC-61000-4-5-2014 without external protection components.

For a higher level of surge, request *AN4813 Surge Protection for Systems Based on PD777xx 8-Port PSE PoE Manager* Application note.

1.10 PSE System Modes of Operation

The device supports the following PSE system modes of operation:

- Semi-Auto mode
- Managed Auto mode
- Unmanaged Auto mode

For more details, see Application Information.

2. Electrical Specifications

This section describes the electrical specifications of the device.

2.1 Absolute Maximum Ratings

PoE performance is not guaranteed when it exceeds the recommended rating. Exposure to any stress in the range between the recommended rating and the absolute maximum rating must be limited to a short time. Exceeding these ratings might impact long-term operating reliability. The following table lists the absolute maximum ratings.

Table 2-1. Absolute Maximum Ratings

Parameter	Minimum	Maximum	Unit
V_{DD}	–0.3	3.8	V
V_{DDA}	–0.3	3.8	V
V_{DDA} to V_{DD}	–0.3	0.3	V
V_{MAIN}	–0.3	80	V
V_{MAIN_7}, V_{MAIN_36}	V_{MAIN}	80	V
MarkHold FET is OFF	0	V_{MAIN}	V
PORT_NEGx to AGND	–0.3	Lower of V_{MAIN_x} + 0.5 or 80	V
DGND to AGND	–0.3	0.3	V
Digital I/O	–0.3	3.6	V
AUTO	–0.3	Lower of V_{DDA} + 0.3 or 3.8	V
Junction Temperature	–40	Self Protected	°C
Storage	–55	150	°C
Solder 10 Seconds	—	260	°C

2.2 Immunity

The following tables list the device immunity.

Table 2-2. ESD

Model	Pins	Minimum Rating	Test Method
Human Body Model (HBM)	All	±2000V	JS-001-2017
Charge Device Model (CDM)	All	±1000V	JESD22-C101F

Table 2-3. Surge Protection

Standard	Application	Minimum Rating
IEC61000-4-5 Ed3	Common mode	1 kV, 2 kV, 4 kV, 6 kV, and 10 kV
ITU-T K.21 2019	Common mode	2.5 kV, 4 kV, and 6 kV
	Differential mode	2.5 kV and 6 kV
EN55024 2010	Common mode	1 kV and 4 kV
GR1089 Issue 6	Common mode	1 kV and 2.5 kV
	Differential mode	1 kV

Note: Device meets 2 kV per IEC-61000-4-5 without need for additional surge protection components. Consult Microchip for recommended protection circuitry for enhanced surge capability.

2.3 Recommended Operating Conditions

The following table lists the recommended operating conditions.

Table 2-4. Recommended Operating Conditions

Parameter	Conditions	Min.	Typ.	Max.	Units
Junction temperature	—	–40	—	125	°C
Ambient temperature	—	–40	—	85	°C
V_{MAIN}	Type 1: Reference to AGND	44	—	57	V
	Type 2, 3: Reference to AGND	50	—	57	V
	Type 4: Reference to AGND	52	—	57	V
V_{MAIN_7}/V_{MAIN_36}	Reference to AGND	—	V_{MAIN}	—	V
V_{MAIN} slew rate	V_{MAIN} = 0V to 57V V_{DD} may be either present or absent	—	—	1.0	V/µs
V_{DD}	Reference to DGND	3.0	3.3	3.6	V
V_{DDA}	Reference to AGND	3.0	3.3	3.6	V
DGND–AGND voltage difference	—	–0.3	—	0.3	V

2.4 Electrical Characteristics

If not specified under conditions, the minimum and maximum ratings listed in the following table apply to the entire specified operating ratings of the device. Typical values stated are either by design or by production testing at 25 °C ambient.

The following tables list the electrical characteristics of the device.

Table 2-5. Current and Power Consumption

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
V_{MAIN} current	I_{MAIN}	Power on Reset (POR) threshold exceeded. V_{MAIN} > 12V	—	—	1.5	mA
		V_{MAIN}< POR threshold 0V < V_{MAIN} ≤ 8V V_{DD} and V_{DDA} not present IC is non-operational	—	—	100	µA
V_{DD} rail + V_{DDA} rail current	I_{VDD} + I_{VDDA}	V_{MAIN} = 55V, V_{DD} = V_{DDA} = 3.6V	—	—	30	mA

Table 2-6. Port Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Port supported continuous current	I_{PORT_CONT}	• Single-Signature PD • V_{MAIN} = 52V, port not in current limit • Class 8 with P_{CLASS_PD} = 99.7W • Maximum unbalance	1.185	—	—	A
Power dissipation	P_{DISS}	All ports 4P Class 8 power (90W) V_{MAIN} = 52V V_{DD} = V_{DDA} = 3.3V	—	—	2.0	W
Total channel resistance	R_{CH_ON}	T_A = 25 °C,	—	0.160	—	Ω
Port resistance	R_{CH_OFF}	R_{PORT} connected, T_J = 25 °C V_{PORT} < 30V	50	60	70	kΩ
		R_{PORT} disconnected, T_J = 25 °C	—	1.8	—	MΩ
V_{PORT} leakage	$I_{LEAKAGE}$	V_{PORT_NEGx} to AGND	—	—	5	µA
Port capacitance	C_{PSE}	**Required:** External X7R port capacitance (typical capacitor values)	47	100	220	nF
	C_{PD}	Supported PD capacitance for IEEE® 802.3bt compliant detection	50	—	150	nF
		Supported PD capacitance, non-compliant PD detection	0.05	—	12.8	µF
		Supported PD capacitance, inrush phase, IEEE® 802.3bt compliant	5	—	180	µF
		Supported PD capacitance, inrush phase, not IEEE® 802.3bt compliant	—	—	432	µF
Supported output power	P_{PORT4P}	2 ports power, connected to a single-signature PD, V_{MAIN} = 52V	—	—	100	W

Table 2-7. Current Limit (I_{LIM})

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Port current limit	I_{LIM}	Class 0–Class 3, 2-pair single signature	—	0.720	—	A
		Class 4, 2-pair single signature	—	0.850	—	A
		Class 4, 4-pair dual signature	—	0.850	—	A
		Class 5, 4-pair single signature	—	0.850	—	A
		Class 6, 4-pair single signature	—	0.890	—	A
		Class 7, 4-pair single signature	—	1.000	—	A
		Class 8, 4-pair single signature Class 5, 4-pair dual signature	—	1.200	—	A
Inrush current limit	I_{INRUSH_B}	I_{LIM} setting $I_{LIM\_2P\_B}$	0.400	0.425	0.450	A

Table 2-8. Power Accuracy

Parameter	Conditions	Min.	Typ.	Max.
Single port (2 pairs) power accuracy	Port power: 5W to 15W	−5.0%	—	5.0%
	Port power: 15W to 55W	−2.5%	—	2.5%
2 ports (4 pairs) power accuracy	Total 4-pair power: 5W to 30W	−5.0%	—	5.0%
	Total 4-pair power: 30W to 100W	−2.5%	—	2.5%

Table 2-9. Detection and Connection Check

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Accept signature resistance	R_{DET}	—	17	25	29	kΩ
Accept signature capacitance	C_{DET}	—	—	—	0.15	µF
Reject signature resistance (low)	R_{REJ}	—	—	—	15	kΩ
Reject signature resistance (high)	R_{REJ}	—	33	—	—	kΩ
Reject signature capacitance	C_{REJ}	—	10	—	—	µF
Detection open circuit resistance	R_{OC}	—	0.5	—	—	MΩ
Valid detection test voltage	V_{VALID}	—	2.8	—	10	V
Detection open circuit voltage	V_{OC}	—	—	—	30	V
Total detection timing	T_{DET}	—	—	—	400	ms

Table 2-10. Classification

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Measured I_{CLASS} at PSE	I_{CLASS}	Class Signature 0	0	—	5	mA
		Class Signature 1	8	—	13	mA
		Class Signature 2	16	—	21	mA
		Class Signature 3	25	—	31	mA
		Class Signature 4	35	—	45	mA

Table 2-11. Real-Time Protection

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Short Circuit Protection (SCP) disconnection time	T_{SCP}	Port in current limit, V_{PORT} < 40V, no bouncing	—	100	—	µs
Overload protection (T_{LIM})	T_{LIM_2P}	Port in current limit, V_{PORT} ≥ 40V Class 1 to Class 6	—	11	—	ms
		Port in current limit, V_{PORT} ≥ 40V Class 7 and Class 8	—	7	—	ms

Table 2-11. Real-Time Protection (continued)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Port MPS current threshold	I_{MPS}	SSPD, Class 1–4, 4P operation	2.0	3.5	5.0	mA
		SSPD, Class 1–4, 2P operation	5.0	7.0	9.0	mA
		SSPD, Class 5–8, 4P operation	2.0	4.5	7.0	mA
		DSPD	2.0	4.5	7.0	mA
MPS on time detection	T_{MPS}	—	—	—	6	ms
MPS off time	T_{MPDO}	—	340	356	372	ms
Port OVT protection	Reference temperature	Temperature above which the OVT protection is active	—	—	150	°C

Table 2-12. I_{CUT} and T_{CUT} Specifications

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
I_{CUT} threshold	I_{CUT_2P}	44V < V_{MAIN} < 57V Class 0–3	—	0.375	—	A
		50V < V_{MAIN} < 57V Class 4 SSPD 2P operation	—	0.644	—	A
		50V < V_{MAIN} < 57V Class 5 SSPD 4P operation	—	0.700	—	A
		52V < V_{MAIN} < 57V Class 6 SSPD 4P operation	—	0.800	—	A
		52V < V_{MAIN} < 57V Class 7 SSPD 4P operation	—	0.900	—	A
		52V < V_{MAIN} < 57V Class 8 SSPD 4P operation Class 5 DSPD 4P operation	—	1.090	—	A
T_{CUT} disconnect time	T_{CUT_2P}	—	—	65	—	ms
P_{CUT} disconnect time	P_{CUT_2P}	$I_{PORT} \geq P_{CUT}/V_{MAIN}$	—	132	—	ms

Table 2-13. Inrush (Power-Up) Phase

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Inrush time	T_{INRUSH}	Per port V_{MAIN} = 57V I_{INRUSH_2P} = 0.425A	—	65	—	ms
Number ports for simultaneous power-up	N_{PORT}	Power-up to maximum capacitor of 360 µF + 20%	—	—	8	Ports

Table 2-14. UVLO

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
VMAIN_UVLO Threshold voltage	$V_{MAIN\_UVLO\_F}$	Threshold level below which ports are turned off. V_{MAIN} falling.	29.5	30	30.5	V
	$V_{MAIN\_UVLO\_R}$	Threshold level above which ports are operational. V_{MAIN} rising.	39.4	40	40.6	V
VMAIN_UVLO ports off response time	$t_{VMAIN\_UVLO\_F}$	Time between V_{MAIN} falling below VMAIN_UVLO_F and ports turned off. V_{MAIN} falling.	8	—	24	ms

Table 2-15. External Current Reference Resistor I_{REF}

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
I_{REF} resistor value	I_{REF}	External 0402 reference resistor value	—	10	—	kΩ
	$I_{REF\%}$	External 0402 reference resistor accuracy	–0.1	—	0.1	%
	I_{REF_TEMPCO}	Resistor temperature coefficient	—	25	50	ppm/°C

Table 2-16. I/O Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
R_{PULL}	Internal Pull-up/Pull-down resistance	—	20	40	60	kΩ
V_{IL}	Input low-level voltage	V_{DD} = 3.0V–3.6V	—	—	0.3 × V_{DD}	V
V_{IH}	Input high-level voltage	V_{DD} = 3.0V–3.6V	0.55 × V_{DD}	—	—	
V_{OL}	Output low-level voltage	V_{DD} > 3.0V, I_{OL} maxI	—	0.1 × V_{DD}	0.2 × V_{DD}	
V_{OH}	Output high-level voltage	V_{DD} > 3.0V, I_{OH} maxII	0.8 × V_{DD}	0.9 × V_{DD}	—	
I_{OL}	Output low-level current	V_{DD} = 3V–3.63V	—	—	10	mA
I_{OH}	Output high-level current	V_{DD} = 3V–3.63V	—	—	7	mA
t_{RISE}	Rise time[1]	load = 20 pF, V_{DD} = 3.3V	—	—	15	ns
t_{FALL}	Fall time[1]	load = 20 pF, V_{DD} = 3.3V	—	—	15	ns
I_{LEAK}	Input leakage current	Pull-up resistors disabled	–1	±0.015	1	µA

Note:

1. These values are based on simulation. These values are not covered by test limits in production or characterization.

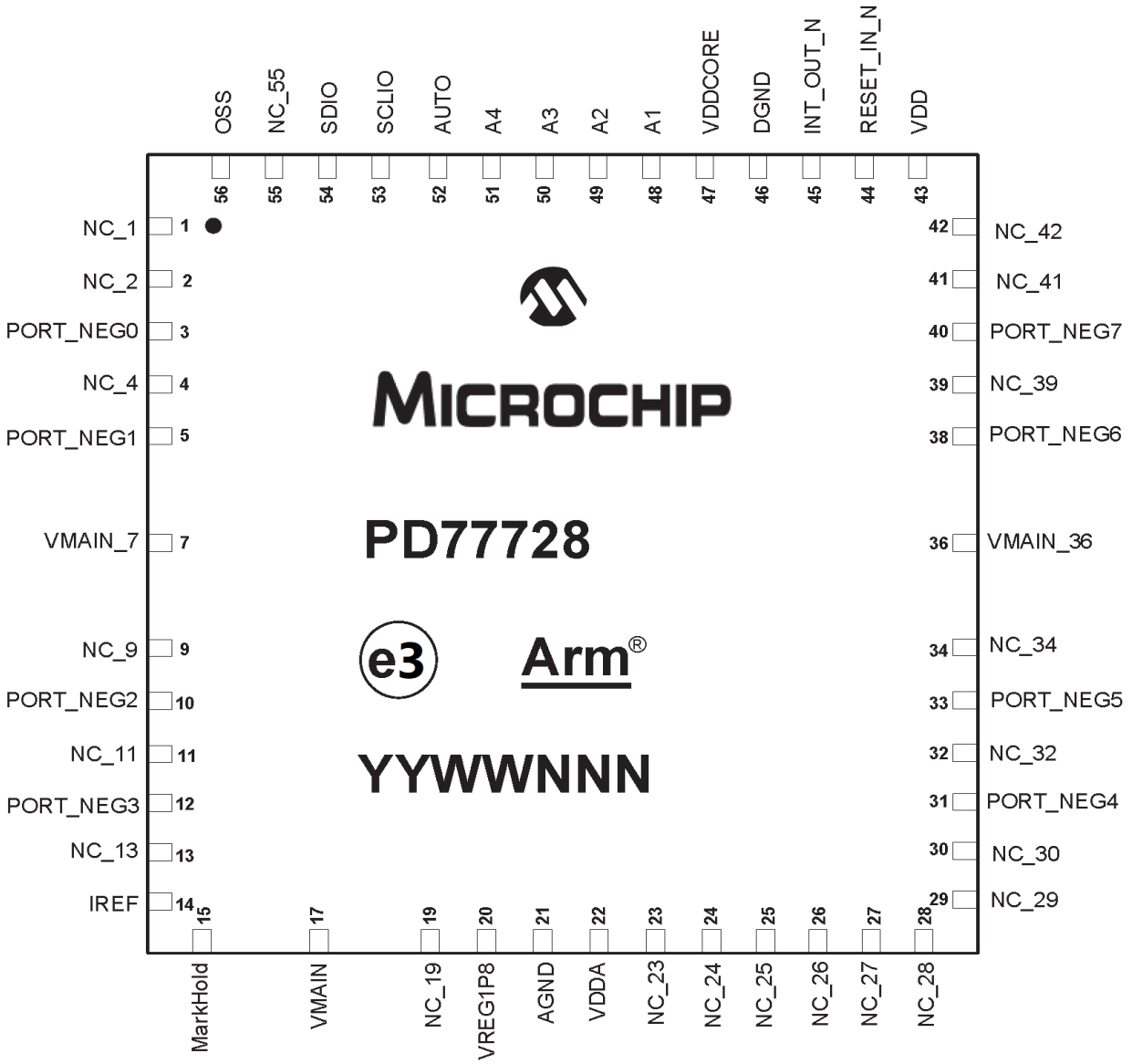
Table 2-17. I^2C Pins Characteristics in I^2C Configuration

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
V_{IL}	Input low-level voltage	V_{DD} = 3.0V–3.6V	—	—	0.3 × V_{DD}	V
V_{IH}	Input high-level voltage	V_{DD} = 3.0V–3.6V	0.55 × V_{DD}	—	—	
V_{HYS}	Hysteresis of Schmitt trigger inputs		0.08 × V_{DD}	—	—	
V_{OL}	Output low-level voltage	V_{DD} > 3.0V, I_{OL} = 3 mA	—	—	0.4	
I_{OL}	Output low-level current	V_{OL} = 0.4V Fast Mode Plus	20	—	—	mA
f_{SCL}	SCL clock frequency		—	—	400	KHz

3. Pin Descriptions

The following figure shows the device pinout.

Figure 3-1. Pinout



Top View
8x8 QFN

The following table lists the pin descriptions of the PD77728 device.

Table 3-1. Pin Descriptions

Pin	Designator	Type	Description
1, 2, 4, 9, 11, 13, 19, 23, 24, 25, 26, 27, 28, 29, 30, 32, 34, 39, 41, 42, 55	Not Connected (NC)	N/A	NC. Leave floating.
3	PORT_NEG0	Power	Negative port 0 output
5	PORT_NEG1	Power	Negative port 1 output
6, 8, 16, 18, 35, 37	N/A	N/A	Pin removed
7	VMAIN_7	Power	Connect to V_{MAIN} through PCB trace or 0Ω resistor for basic level protection. Leave unconnected for enhanced surge protection. See *PD77728 Surge Protection Application Note* for more details.
10	PORT_NEG2	Power	Negative port 2 output
12	PORT_NEG3	Power	Negative port 3 output
14	IREF	Analog Input	Current reference resistor. Connect through 10K 0.1% to AGND.
15	MarkHold	Analog Input	MarkHold input. Leave unconnected when not used.
17	VMAIN	Power	Connect to V_{MAIN}. Connect a 1 µF, 100V, X7R capacitor near each device's V_{MAIN} pin.
20	VREG1P8	Power	Internal 1.8V regulator output capacitor connection. Connect a low-ESR, 1 µF capacitor to DGND.
21	AGND	GND	Analog Ground. Connect to DGND through a single point connection.
22	VDDA	Power	Analog 3.3V supply. Connect a capacitor to AGND. Connected to main 3.3V supply on the board.
31	PORT_NEG4	Power	Negative port 4 output
33	PORT_NEG5	Power	Negative port 5 output
36	VMAIN_36	Power	Connect to V_{MAIN} through PCB trace or 0Ω resistor for basic level protection. Leave unconnected for enhanced surge protection. See *PD77728 Surge Protection Application Note* for more details.
38	PORT_NEG6	Power	Negative port 6 output
40	PORT_NEG7	Power	Negative port 7 output
43	VDD	Power	Digital 3.3V supply. Connect a capacitor to DGND. Connected to main 3.3V supply on the board.
44	RESET_IN_N	Input	Device Reset. Connect a pull-up resistor to V_{DD}.
45	INT_OUT_N	Output	Interrupt output pin (open drain). Leave open if not used.
46	DGND	GND	Digital Ground. Connect to AGND through a single point connection.
47	VDDCORE	Power	Internal 1.2V regulator output capacitor pin. Connect 1.0 µF low ESR capacitor to DGND.
48	A1	Input	I^2C device address. Connect to V_{DD} or DGND.
49	A2	Input	I^2C device address. Connect to V_{DD} or DGND.
50	A3	Input	I^2C device address. Connect to V_{DD} or DGND.
51	A4	Input	I^2C device address. Connect to V_{DD} or DGND.
52	AUTO	Input	Connect a resistor divider comprised of a 10 kΩ resistor from V_{DD} to AUTO pin, and a resistor from AUTO pin to DGND to select the AUTO mode configuration. See Table 4-1 for resistor selection and AUTO mode configurations.

Table 3-1. Pin Descriptions (continued)

Pin	Designator	Type	Description
53	SCLIO	Bidirectional	I^2C clock
54	SDIO	Bidirectional	I^2C data input/output
56	OSS	Input	OSS is used to shut down ports based on priority settings. Connect to AGND through 10K, if unused.
EPAD	EPAD	Analog	Exposed Pad. Connect to AGND through short trace on PCB underneath device. AGND must have enough copper mask to ensure adequate thermal performance.

4. Application Information

This section provides practical operation information for the PD77728 device with Firmware 1.xx.

4.1 Operational Modes

This section provides a high level description of the three available operational modes:

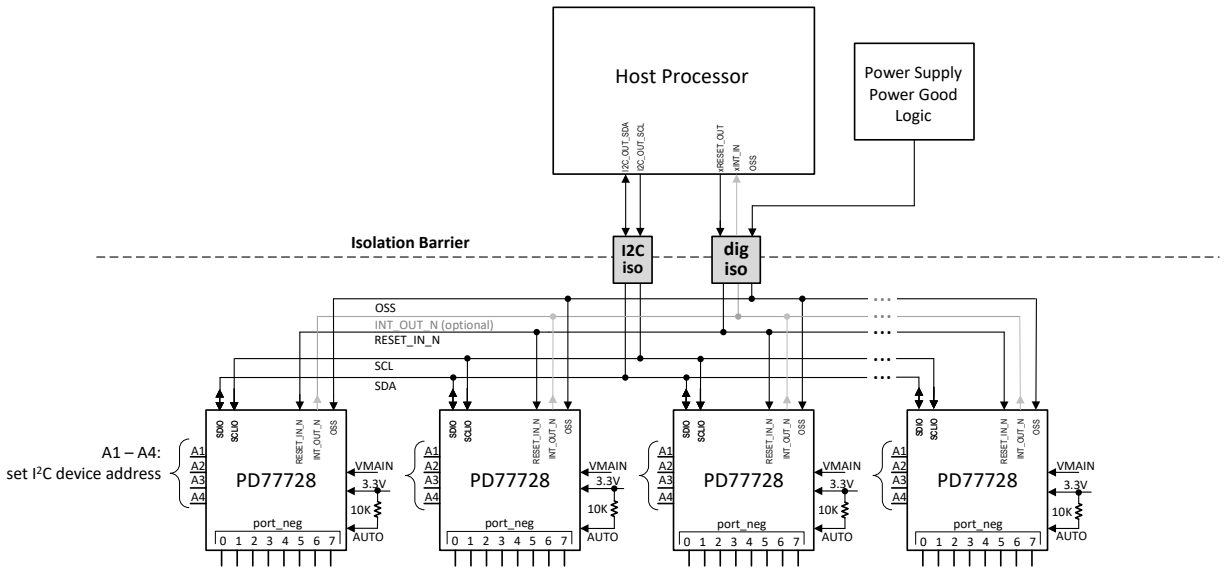
- Semi-Auto mode
- Managed Auto mode
- Unmanaged Auto mode

4.1.1 Semi-Auto Mode

In the Semi-Auto mode, the device performs periodic connection check, detection, and classification, but does not power-up the ports without a host command. Each device has initial PSE configuration containing the Port Matrix (2P/4P configuration) and stores the port investigation results in the memory for host control. The host can override these settings. In this mode, the PoE controller is responsible for the periodic or cyclic detection and classification of the ports.

The following figure shows the Semi-Auto mode application.

Figure 4-1. Semi-Auto Mode Application



4.1.2 Auto Mode

The Auto mode is an operational mode where PSE can perform the required functionality with predetermined configuration values. In this mode, the device performs connection check, detection, classification, and power-up autonomously following POR, and turning valid PoE ports ON without host intervention. A device supporting the Auto mode might either be connected to a host (Managed Auto mode) or be used as a stand-alone system without any control interface (Unmanaged Auto mode).

The following tasks are supported in the Auto mode:

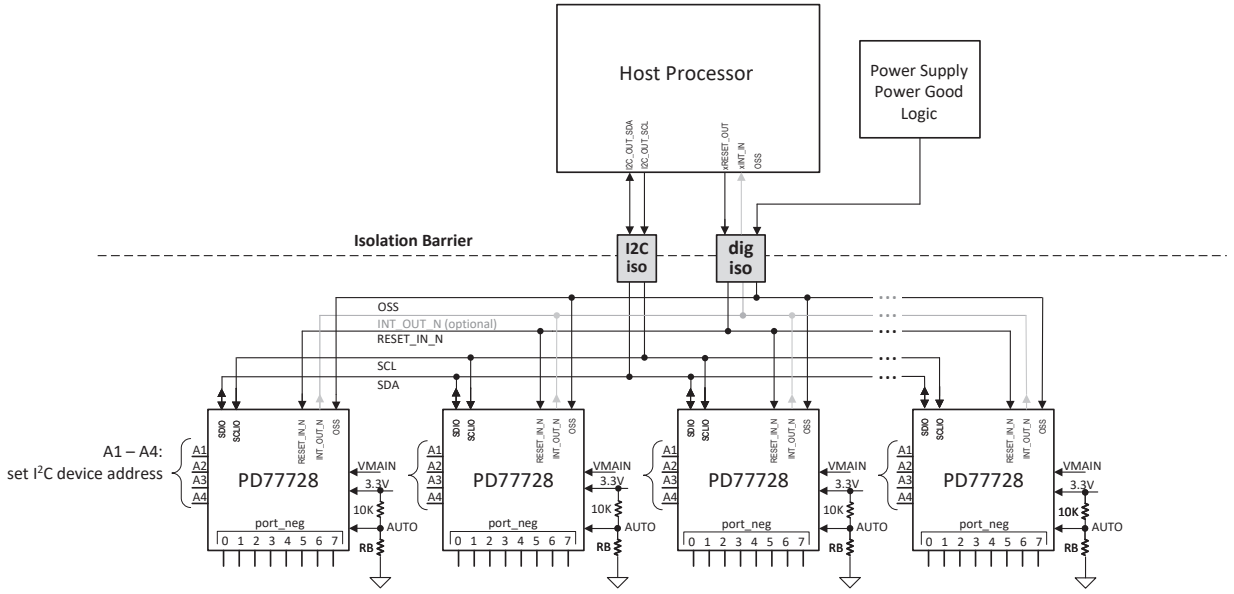
- Autonomous detection, classification, power-up, and power-on ports based on configuration pins
- Device-Level matrix configuration (Managed Auto Mode only)

4.1.2.1 Managed Auto Mode

In the Managed Auto mode, the device has initial PSE configuration with which the system can be operated without the need for host communication. However, host communication allows subsequent changes to the PSE configuration.

The following figure shows the host-controlled Managed Auto mode application.

Figure 4-2. Host-Controlled Managed Auto Mode Application

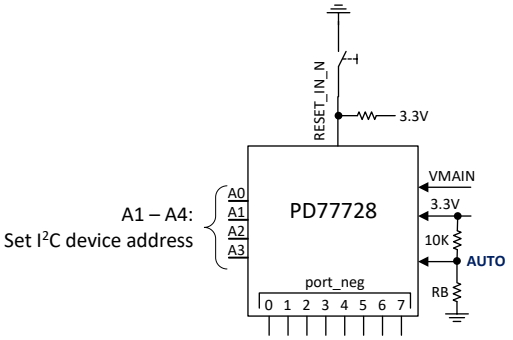


4.1.2.2 Unmanaged Auto Mode

In the Unmanaged Auto mode, the device is a stand-alone system. There is no host I^2C communication to the device. All PSE configurations are stored within the system and are available to the device (s) without host communication. This is the typical application of a single device system. More than one device may be employed in this type of system, but each device operates interdependently of other devices.

The following figure shows the unmanaged Auto mode application.

Figure 4-3. Unmanaged Auto Mode Application



The following table lists the values of the resistor RB that are used to set the PSE type.

Table 4-1. AUTO Pin Configuration

Level	Level Range (V)	Mode	RB (kΩ)	Set Value (V)
0	0–0.278	Class8	0.442	0.140
1	0.279–0.557	Class7	1.47	0.423
2	0.558–0.847	Class6	2.67	0.695
3	0.847–1.115	Class5	4.22	0.979
4	1.115–1.393	Class4–4P	6.19	1.262
5	1.394–1.693	Class4–2P	8.87	1.551
6	1.694–1.951	Class3–2P	12.4	1.827
7	1.951–2.23	AUTO mode disabled	> 17.4 or open	2.096

Note: A 10KΩ resistor from 3.3V to AUTO pin is the top resistor value, RTOP, which along with RB creates the required voltage level at AUTO pin input.

4.2 I²C

The port I²C address is programmed through pins A1, A2, A3, and A4 (pins 48–51). Tie each pin to V_{DD} or DGND to set the I²C address, as listed in the following table.

Note: The I²C address is a 7-bit address.

Table 4-2. I²C Address Select

A4	A3	A2	A1	Ports	I²C Address
0	0	0	0	0–3	0x20
				4–7	0x21
0	0	0	1	0–3	0x22
				4–7	0x23
0	0	1	0	0–3	0x24
				4–7	0x25
0	0	1	1	0–3	0x26
				4–7	0x27
0	1	0	0	0–3	0x28
				4–7	0x29
0	1	0	1	0–3	0x2A
				4–7	0x2B
0	1	1	0	0–3	0x2C
				4–7	0x2D
0	1	1	1	0–3	0x2E
				4–7	0x2F
1	0	0	0	0–3	0x30
				4–7	0x31
1	0	0	1	0–3	0x32
				4–7	0x33
1	0	1	0	0–3	0x34
				4–7	0x35
1	0	1	1	0–3	0x36
				4–7	0x37
1	1	0	0	0–3	0x38
				4–7	0x39
1	1	0	1	0–3	0x3A
				4–7	0x3B
1	1	1	0	0–3	0x3C
				4–7	0x3D
1	1	1	1	0–3	0x3E
				4–7	0x3F

4.3 2-Pair and 4-Pair (2P/4P) Operation

The IEEE 802.3bt standard introduces the ability to drive a PD (that supports this mode) by using four pairs and allowing higher PD power support. The IEEE 802.3bt standard discusses the 4P definition from a logical port point of view. That is, a port in the IEEE 802.3bt standard can operate either in 2P mode or in 4P mode. A PD that can accept power on both ALT-A and ALT-B at the same time is regarded as a single 4P-capable PD.

4.3.1 2P Operation

PSE port can operate over two pairs, that is, only two pairs are used to actively deliver power to the PD, either on ALT-A or ALT- B, but not both. This is allowed when the assigned class is 0 to 4. A 2P operation uses a single physical port that is considered as a logical port.

4.3.2 4P Operation

When the assigned class is 5 to 8, the PSE port must deliver the power over four pairs. When operating in 4P, powered is delivered to the PD on both pairsets (ALT-A and ALT-B), that is, two physical ports are combined to create a single logical 4P port required for the 4P operation.

When operating in the 4P mode, the two physical ports that create the one logical four pair port must be chosen from the same physical PD77728 IC. In addition, the logical 4P port must be created from the same physical port group (0, 1, 2, and 3) or (4, 5, 6, and 7). For example, a logical 4P port from physical ports 0 and 3 is allowed, but a logical 4P port from physical ports 0 and 4 is not allowed.

4.4 PD77728 Communication Interface

In Controller Mode, the I^2C interface is the communication interface between the PD77728 and the PD77020 PoE Controller. In Semi-Auto and the Managed Auto modes, communication between PD77728 and the host processor is also through I^2C. For more detailed information, see *PD77728 Register Map*.

4.5 OSS Pin Behavior

The OSS pin can be used to turn off groups of ports based on the signal type received on the pin.

The OSS pin has two modes of operation:

- Single-Bit Priority Shutdown mode
- Multi-Bit Priority Shutdown mode

The OSS pin mode of operation is set in register **MISC** (0x17) bit [4]. The default value of the OSS pin is Single-Bit Priority Shutdown mode.

4.5.1 Single-Bit Priority Shutdown Mode

To enable the Single-Bit Priority Shutdown, bit [4] in register **MISC** (0x17) must be set to 0 (Default).

In this mode of operation, a rising edge of the OSS hardware pin shuts down low priority ports:

- Powered ports are turned off
- Unpowered ports stop detection
- If the OSS bit is asserted, then the low priority ports do not perform detection
- Once OSS is back to low level, all low priority ports resume detection

Low-priority ports are defined by writing to register **PWRPR** (0x15) bits [7:4] (Port Power Priority). This register sets the ports to be turned off if OSS is asserted.

In the Auto mode, the low priority ports that are turned off are automatically re-enabled after OSS has cleared.

In the Controller mode, the low priority ports that are turned off are automatically re-enabled based on the value written in register **Detect/Class Enable** (0x14) bits [3:0].

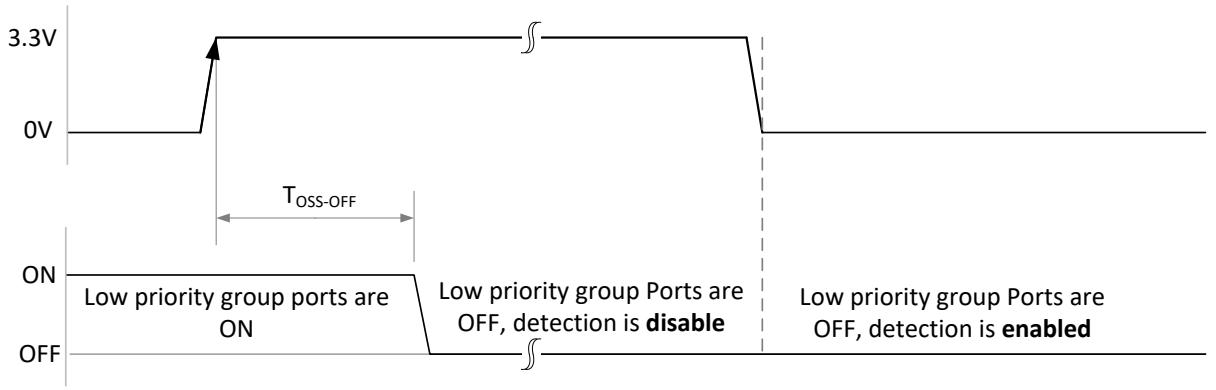
In the Semi-Auto mode, the host must re-enable Detection and Classification.

Note: Do not clear bits [3:0] of register **Detect/Class Enable** (0x14) during the assertion of OSS.

The following events occur when the OSS pin is set:

- **OSS event** (bit [1]) in register **SUPPLY** (registers 0x0A, 0x0B) and **Supply Event** (bit [7]) in **Interrupt** register (0x00) are set.
- Ports that are on and assigned as low-priority ports, are turned off.
- Ports that were turned off, set the corresponding Power Good and Power Enable bits in **Power** register (0x10).
- Ports that are not on, but perform detection and class and are assigned as low priority ports, stop detection and classification without reporting any bit.

Figure 4-4. OSS Pin Single-Bit Priority Shutdown Mode Timing



4.5.2 Multi-Bit Priority Shutdown Mode

The Multi-Bit Priority Shutdown mode has the following characteristics:

- 3-bit priority for every port
- Each bit has a length of $T_{BIT-OSS}$
- Idle state of OSS pin is low level (0)
- A start-bit comprising of transition from 0 (IDLE) to 1 back to 0 precedes the data
- 000 is the highest priority (reducing as the bit value increases)

The OSS mode is set to the Multi-Bit Priority mode by setting **Multi Bit Priority** (bit [4]) in the **MISC** register (0x17).

Multi-bit power priority code is set in **Multi-bit Power Priority** registers (0x27, 0x28). `Port power priority` field in register **PWRPR** (register 0x15 bits [7:4]) are ignored. If the host selects certain priority ports to be turned off, then it sends the relevant shutdown code on the OSS, based on the timing diagram shown in Figure 4-5.

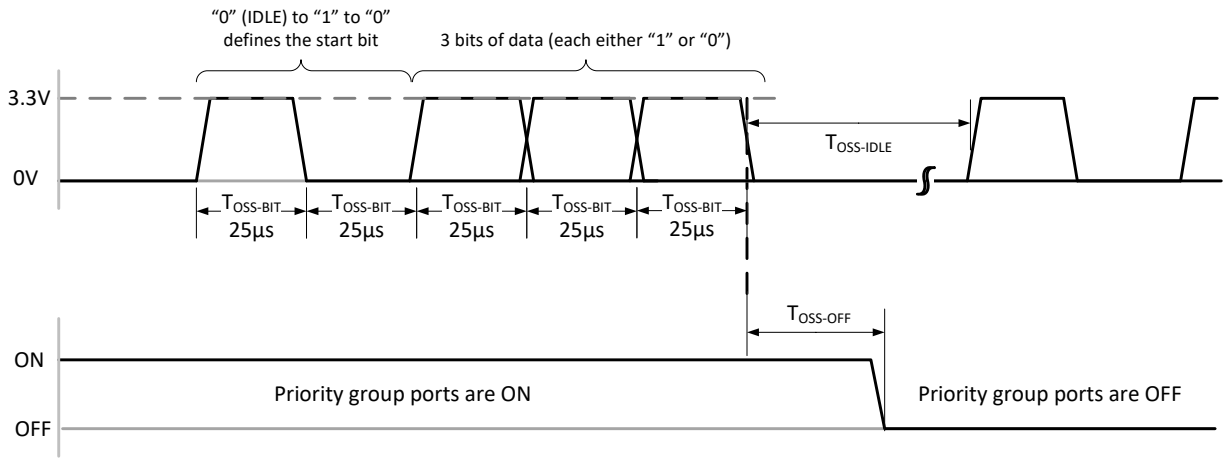
The PD77728 device compares the code received on OSS with the power priority of each port (as defined by registers 0x27 and 0x28) and shuts down the ports which are less than or equal to the received priority. Then, the PD77728 device returns to normal operation, that is, ports that were turned off due to OSS shut-down event immediately restart detection. These ports are re-enabled for detection. Ports that are not on, but perform detection/classification, and are assigned to the priority code, are not interrupted.

The following events occur when the OSS code is received:

- **OSS event** (bit [1]) in register **SUPPLY** (registers 0x0A, 0x0B) and **Supply Event** (bit [7]) in the **Interrupt** register (0x00) are set.
- Ports that are on and assigned as corresponding OSS code, are turned off
- Ports that are turned off, set the corresponding Power Good and Power Enable bits in the **Power** register (0x10).
- Ports that are not on and assigned with the corresponding OSS code, continue to perform uninterrupted detection and classification.

The following figure shows the OSS pin Multi-Bit Priority Shutdown mode timing.

Figure 4-5. OSS Pin Multi-Bit Priority Shutdown Mode Timing



The following table lists the OSS Pin Multi-Bit Priority Shutdown mode parameters.

Table 4-3. OSS Pin Multi-Bit Priority Shutdown Mode Parameters

Parameter	Description	Min.	Typ.	Max.	Unit
$T_{BIT-OSS}$	OSS bit period	24	25	26	µs
$T_{OSS-OFF}$	Time between receiving shutdown code and shutting down of ports.	1	—	50	µs
$T_{OSS-IDLE}$	Idle time between consecutive shutdown code transmission in the Multi-Bit mode.	—	50	—	µs

Notes:

- If only one of the IC's addresses is configured to multi-bit, then the configuration is applied on both sub-chips.
- There is no support for single bit and multi bit on the same IC.
- In the Multi-Bit Priority mode, if OSS I/O has changed but a valid start-bit is not detected, then the OSS event is discarded.
- OSS priority table is rebuilt every 3 ms. Therefore, it might take up to 3 ms for a new configuration to take place.
- The OSS priority table is locked against changes during an OSS event.

4.6 Compliance to Limited Power Source Requirements

The Microchip PD77728 PoE manager fulfills Limited Power Source (LPS) requirements per IEC/UL/EN62368-1. In other words, the PD77728 device is an IC current limiter that is used for current limiting the output of the power source in accordance with the requirements of an LPS.

As per IEC62368-1 Ed.2, if the system power supply exceeds 250 VA, then the PD77728 device is shorted during compliance testing. Therefore, an external current limiter or per-port fuse is required. If the total system power is less than 250 VA, then the PD77728 device is not shorted during compliance testing and LPS requirements are met by virtue of the PD77728 device being an IC current limiter.

As per IEC62368-1 Ed.3, the IC current limiters used for current limiting in power sources are not shorted from input to output if they comply with all of the following:

- The IC current limiters limit the current to manufacturer's defined value which must be less than 5A under normal operating conditions with any specified drift accounted for.
- The IC current limiters are entirely electronic and have no means of manual operation or reset.
- The IC current limiters output current is limited to 5A or less (specified maximum load).

This implies that per port fuses might not be required to meet IEC62368-1 Ed3. The compliance requirements are as follows:

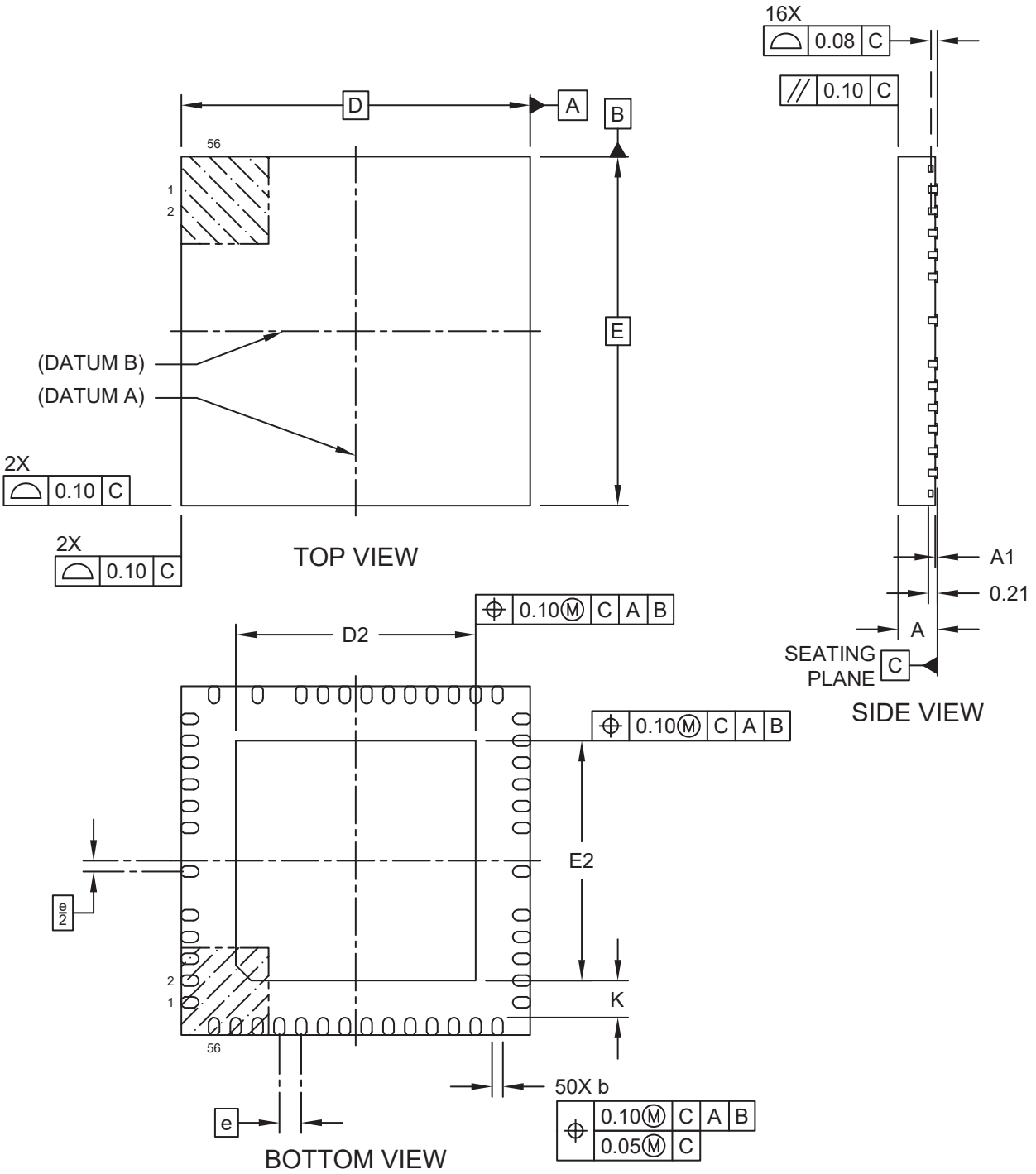
- If a system is intended to meet IEC62368-1Ed2: Per port fuse is required if the total system power > 250 VA.
- If a system is intended to meet IEC62368-1Ed2: Per port fuse is not required if the total system power is < 250 VA.
- If a system is intended to meet IEC62368-1Ed3: Per port fuse may not be required.

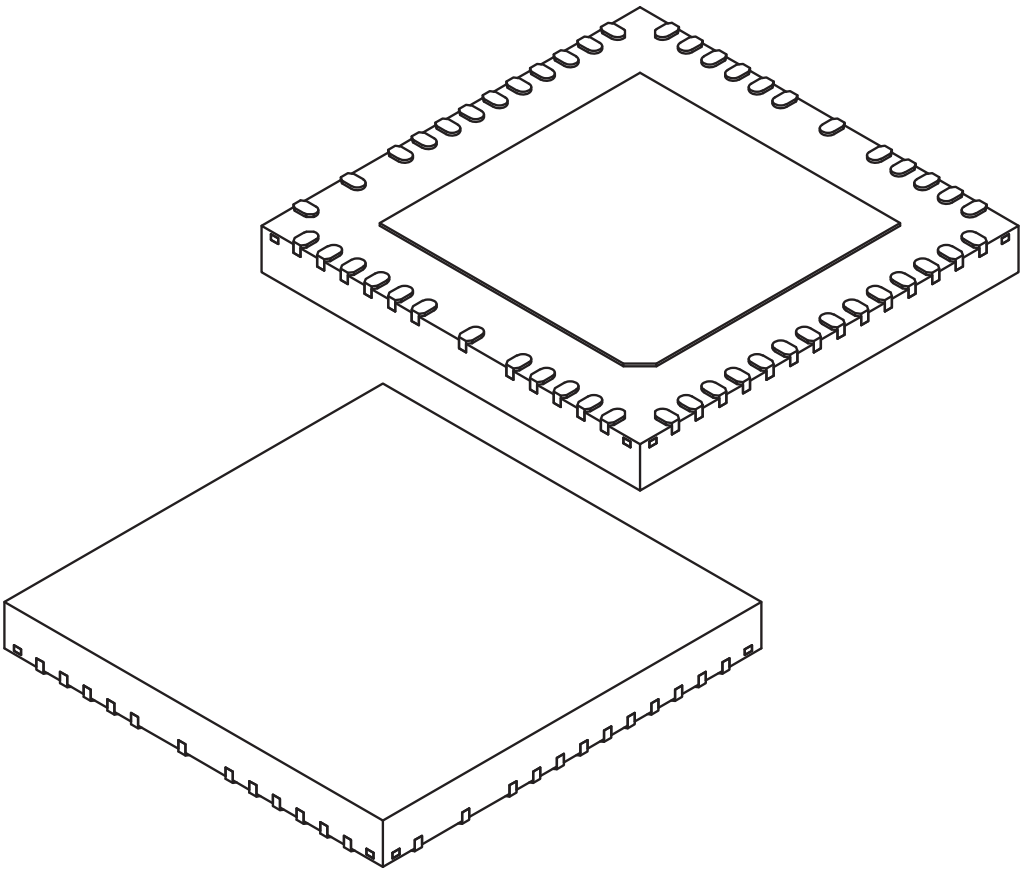
For additional details, request for Microchip *AN3527 Compliance to Limited Power Source Requirements*. These statements are Microchip's good faith interpretation of the IED62368-1 standard. Consult IEC or equivalent agency and the IEC62368-1 Ed2/Ed3 standards for official positions with respect to this topic.

5. Package Specifications

This device is a 56-lead very thin plastic quad flat, no lead package (KDC), 8 mm x 8 mm x 0.9 mm body [VQFN] with depopulated terminals and 5.5 mm^2 exposed pad. For latest package drawings, see Microchip Package Drawings.

Figure 5-1. Package Outline Drawing (POD)





Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		56	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.85	0.90
Standoff	A1	0.00	0.035	0.05
Terminal Thickness	A3		0.203 REF	
Overall Length	D		8.00 BSC	
Exposed Pad Length	D2	5.40	5.50	5.60
Overall Width	E		8.00 BSC	
Exposed Pad Width	E2	5.40	5.50	5.60
Terminal Width	b	0.20	0.25	0.30
Terminal Length	L	0.30	0.40	0.50
Terminal-to-Exposed-Pad	K	0.70	–	–

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

5.1 Recommended PCB Layout

The following figures show the recommended PCB layout of the PD77728 device.

Note: All figure dimensions are in mm.

Figure 5-2. Solder Mask (Component Side)

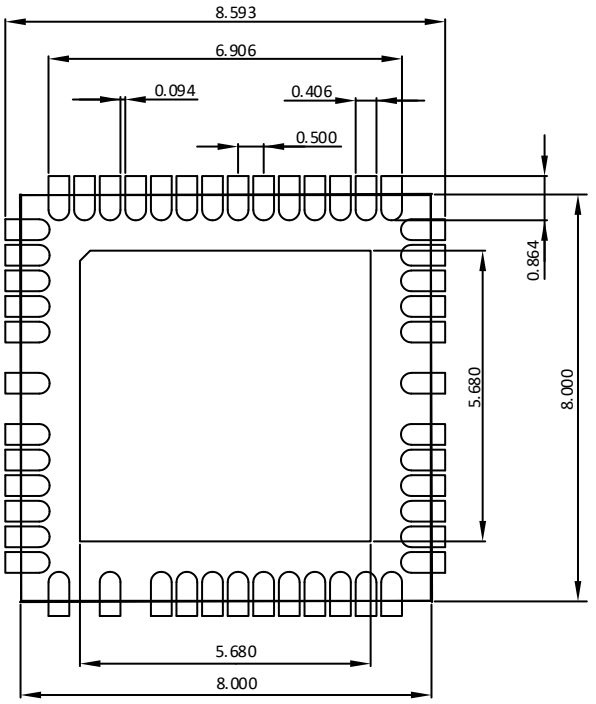


Figure 5-3. Solder Mask (Print Side)

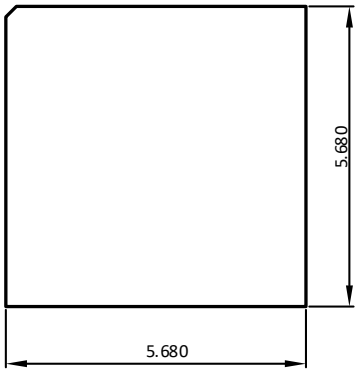


Figure 5-4. Copper Layer (Component Side)

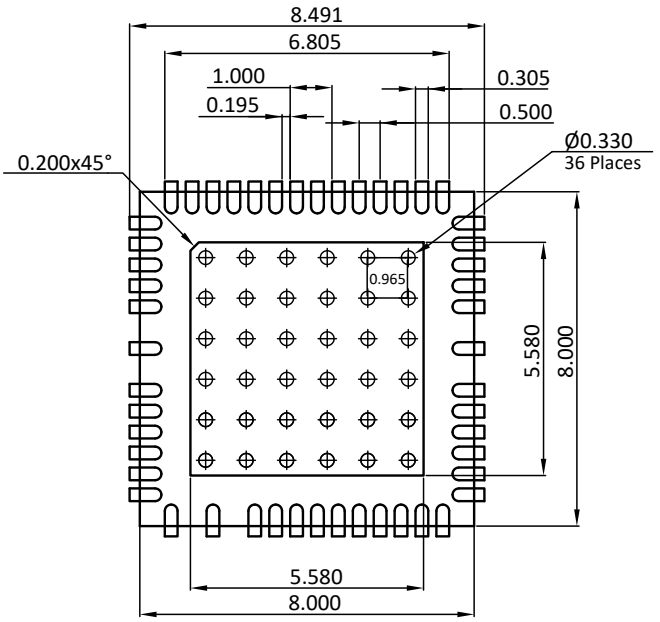
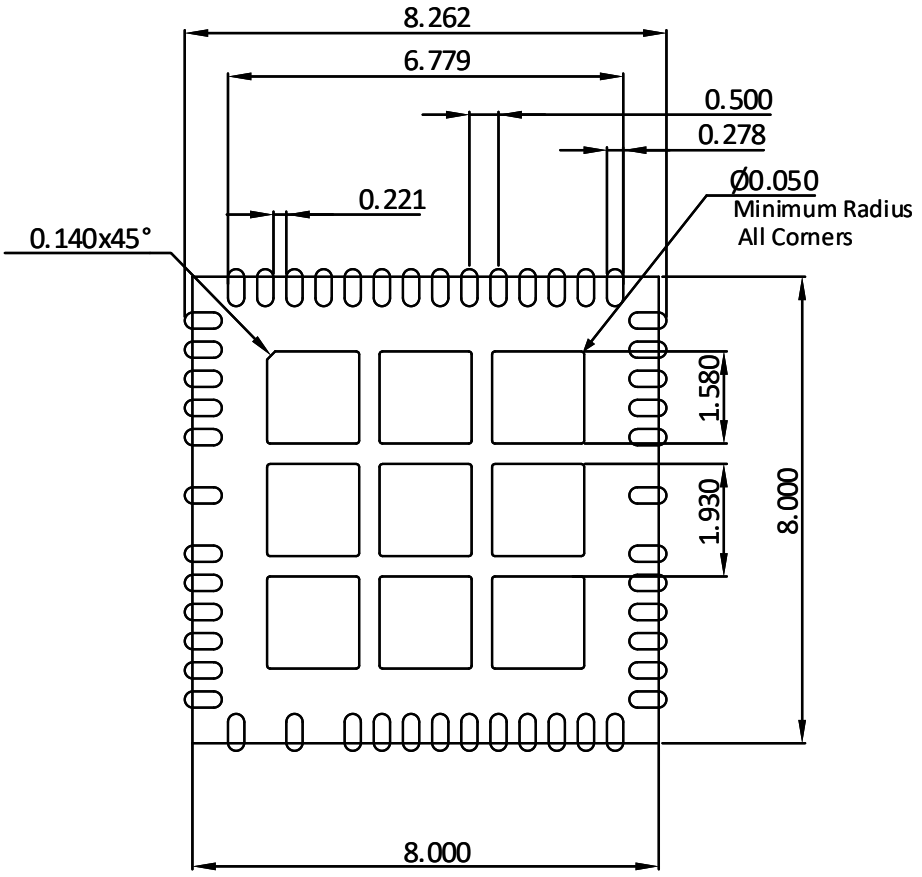
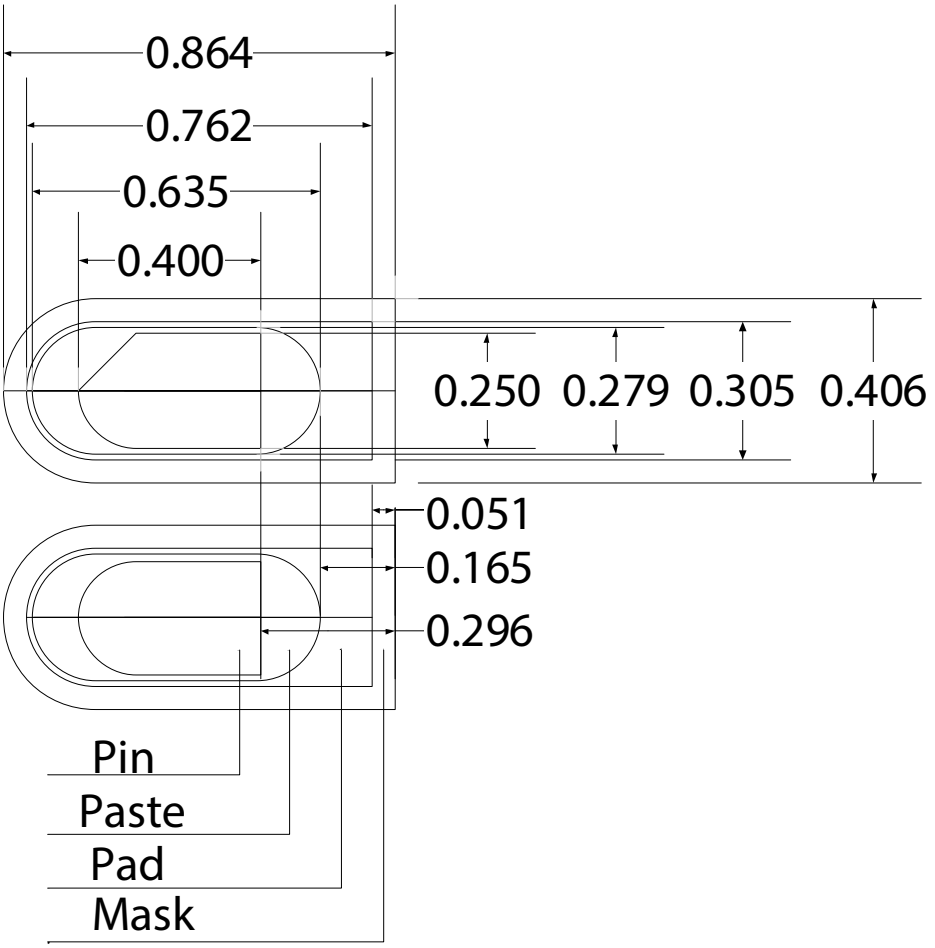


Figure 5-5. Paste Mask (Component Side)



Note: Use a 5 mil stencil.

Figure 5-6. Pin Geometry (Component Side)



5.2 Thermal Properties

The following table lists the thermal properties of the device.

Table 5-1. Thermal Properties[1]

Parameter	Symbol	Typical	Unit
Junction-to-ambient thermal resistance	Θ_{JA}	21.03	°C/W
Junction-to-case (top) thermal resistance	$\Theta_{JC(TOP)}$	10.04	°C/W
Junction-to-board thermal resistance	Θ_{JB}	4.12	°C/W
Junction-to-top characterization parameter	ψ_{JT}	0.334	°C/W

Note:

1. Using the JESD51-7 test board.

5.3 Recommended Solder Reflow Information

The following list shows the solder reflow information:

- RoHS 6/6
- Pb-free 100% Matte Tin Finish
- Package Peak Temperature for Solder Reflow (40s maximum exposure)—260 °C (0 °C, –5 °C)

The following tables list the classification reflow profile and Pb-Free Process—package classification reflow temperature details.

Table 5-2. Classification Reflow Profile

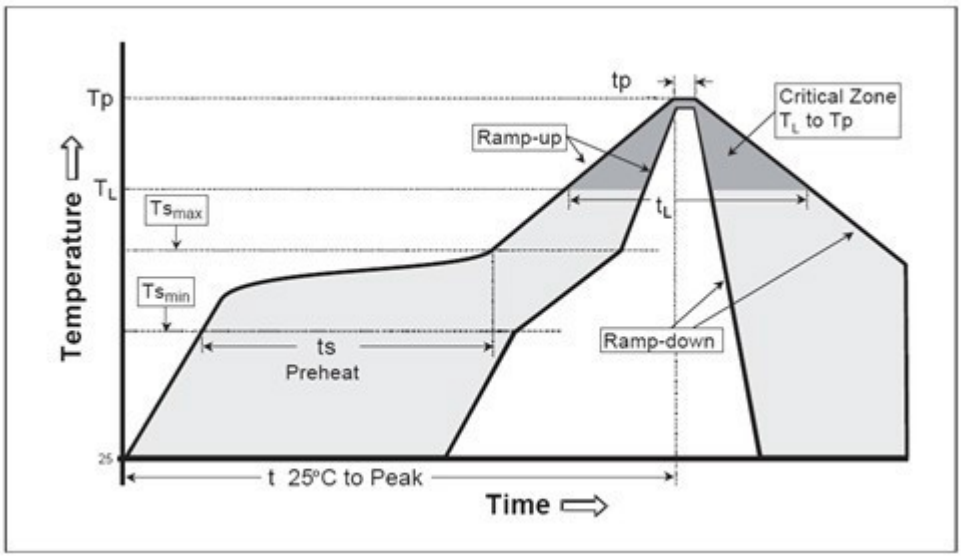
Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Average ramp-up rate (TS_{MAX} to T_P)	3 °C/s maximum	3 °C/s maximum
Preheat		
Temperature min (TS_{MIN})	100 °C	150 °C
Temperature max (TS_{MAX})	150 °C	200 °C
Time (ts_{MIN} to ts_{MAX})	60s to 120s	60s to 180s
Time Maintained		
Temperature (T_L)	183 °C	217 °C
Time (t_L)	60s to 150s	60s to 150s
Peak classification temperature (T_P)	210 °C to 235 °C	240 ℃ to 255 °C
Time within 5 °C of actual peak temperature (t_P)	10s to 30s	20s to 40s
Ramp-down rate	6 °C/s maximum	6 °C/s maximum
Time 25 °C to peak temperature	6 minutes maximum	8 minutes maximum

Table 5-3. Pb-Free Process—Package Classification Reflow Temperatures

Package Thickness	Volume < 350 mm^3	Volume 350–2000 mm^3	Volume > 2000 mm^3
Less than 1.6 mm	260 + 0 °C	260 + 0 °C	260 + 0 °C
1.6 mm to 2.5 mm	260 + 0 °C	250 + 0 °C	245 + 0 °C

The following figure shows the classification reflow profile.

Figure 5-7. Classification Reflow Profile



6. Tape and Reel Specifications

This section provides the tape and reel specifications.

The following figures show the tape and reel pin 1 orientation and tape specifications of the PD77728 device.

Figure 6-1. Tape and Reel Pin 1 Orientation

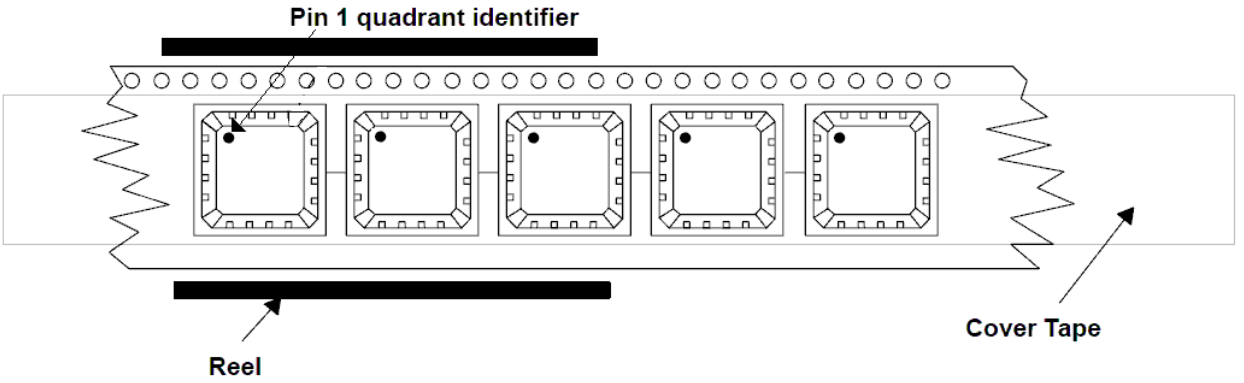
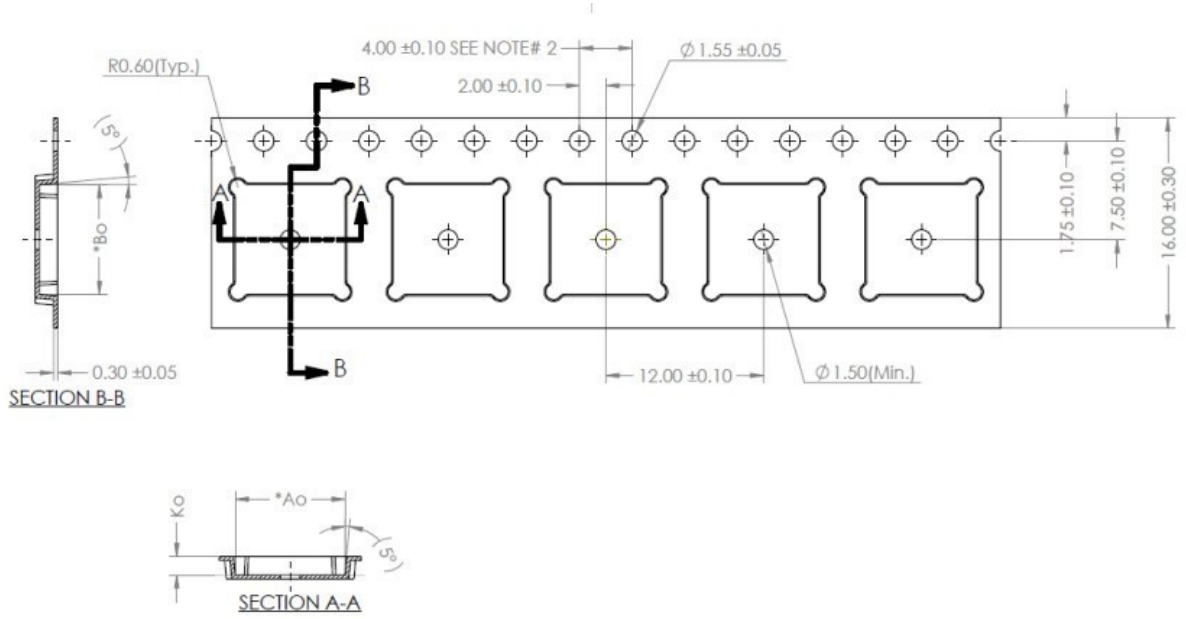


Figure 6-2. Tape Specifications



The following table lists the tape mechanical data details of the PD77728 device.

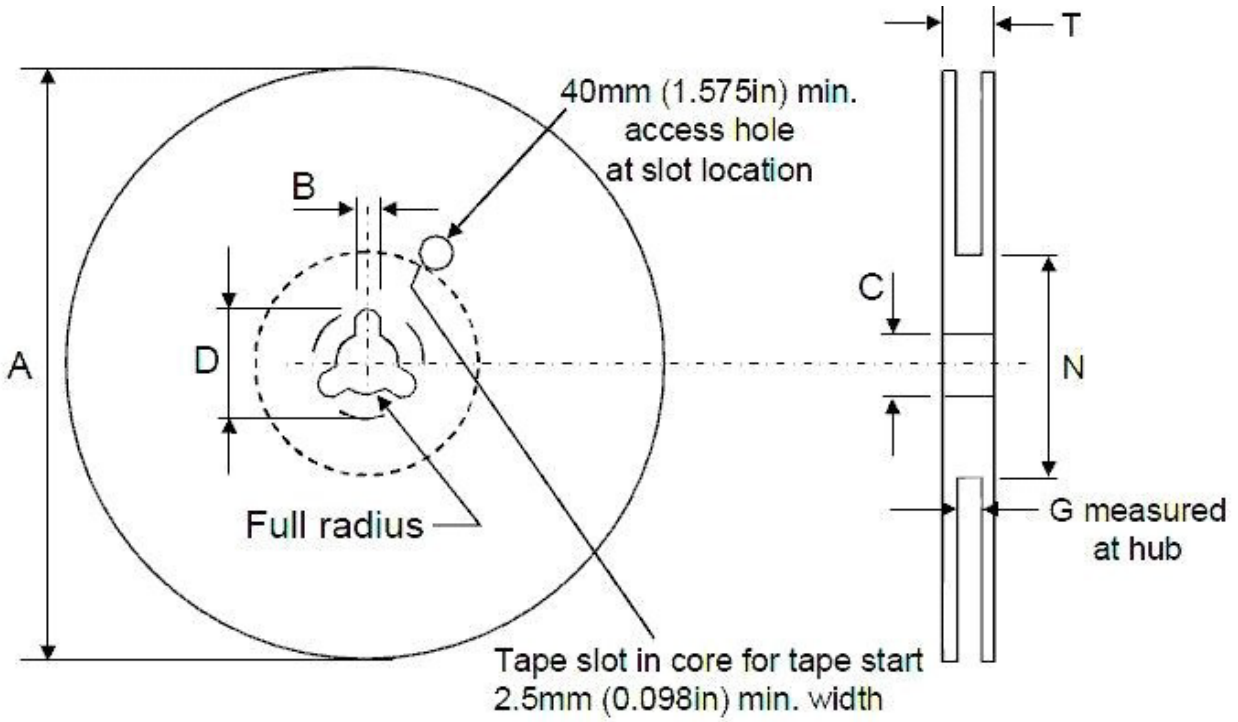
Table 6-1. Tape Mechanical Data

Dimension	Value (mm)
A0	8.35 ±0.10
B0	8.35 ±0.10
K0	1.40 ±0.10
K1	N/A
Pitch	12.00 ±0.10

Table 6-1. Tape Mechanical Data (continued)	
Dimension	**Value (mm)**
Width	16.00 ±0.30

The following figure shows the reel specifications of the PD77728 device.

Figure 6-3. Reel Specification



The following table lists the reel mechanical data details of the PD77728 device.

Table 6-2. Reel Mechanical Data

Dimensions	Value (mm)	Value (inch)
Tape size	16.00 ±0.3	0.630 ±0.012
A maximum	330	13
B maximum	1.5	0.059
C	13.0 ±0.20	0.512 ±0.008
D minimum	20.2	0.795
N minimum	50	1.968
G	16.4 +2.0/−0.0	0.724 to 0.645
T maximum	29	1.142

Note: Base quantity: 2000 pieces

7. Ordering Information

The following table lists the part ordering information of the device.

Table 7-1. Ordering Information

Part Number	Package	Packaging Type	Temperature	Part Marking
PD77728ILQ-01VV[1]-TR	Plastic QFN 8 mm × 8 mm (56 lead)	Tape and Reel	−40 °C to 85 °C	Microchip Logo PD77728 e3 Arm® YYWWNNN[2]

Notes:

1. 01VV = Firmware version
2. YY = Year, WW = Week, and NNN = Trace code.

8. Reference Documents

This document has the following reference documents:

- *AN4896 Designing an IEEE® 802.3bt/at/af PoE System Based on PD77728*
- *AN4813 Surge Protection for Systems Based on PD777xx 8-Port PSE PoE Manager*
- *PD77728 Auto Mode Register Map*
- *AN4952 PD777xx PSE Firmware Download and Replace Flow*
- *PD77728 Auto Mode Evaluation Board User Guide*

9. Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

Table 9-1. Revision History

Revision	Date	Description
F	02/2025	The following is the summary of changes made in this revision: • Updated the following: – Figure 1 – Figure 4-1 – Table 4-1 Pin Descriptions – Table 8-1. Ordering Information • Deleted the following sections: – PD77020 PSE Power Management Controller – Controller Mode
E	07/2024	The following is the summary of changes made in this revision: • Updated the following tables: – Table 2-5 – Table 2-6 – Table 2-11 • Added the following tables: – Table 2-16 – Table 2-17 • Updated the Controller Mode Application diagram
D	05/2023	The following is the summary of the changes made in this revision: • Updated the following figures: – Controller Mode Application – Figure 4-1 – Host-Controlled Managed Auto Mode Application, – Unmanaged Auto Mode Application • Edited Ordering Information • Edited Table 2-5
C	03/2023	The following is the summary of the changes made in this revision: • Re-defined Operational Modes • Added OSS Pin Behavior • Updated descriptions of Over voltage and T_{CUT}/I_{CUT} Protection in Over-Temperature (OVT) Protection and TCUT/ICUT Protection respectively. • Added additional Surge Protection information in Surge • Incorporated minor editorial changes throughout the document.
B	08/2022	Added and revised all the sections, and updated information regarding functional descriptions, electrical specifications, and pin descriptions throughout the document to align with device performance.
A	05/2021	This is a preliminary version of the data sheet.

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