MIC24097

20V, 20A High Performance Switching Buck Regulators

Features

- Input Voltage Range: 4.5V to 20V (Optimized for 12V Bus)
- Adjustable Output from 0.6V to 12V (also Limited by Duty Cycle)
- High Current Capability of 20A
- Adaptive Constant on Time Control
- Output Sense for Tight Voltage Regulation
- 0.6V Internal Reference with ±1% Accuracy (±0.5% Over -40°C to +105°C)
- Up to 800 kHz Switching Frequency
- High-Voltage Internal LDO for Single Supply Operation
- Supports Start-Up into Pre-Bias Output
- Internal Compensator
- Precision Enable Function
- Programmable HLL/CCM Operation Using Mode Pin
- Programmable Soft Start Time
- Droop Feature to Support Adaptive Voltage Positioning (AVP) for Improved Load Transient Response
- Hiccup Short Circuit Protection and Programmable Current Limit
- Thermal Shut Down with Hysteresis
- Compact Size: 6 mm x 7 mm 39-Pin QFN
- -40°C to +125°C Junction Temperature Range

Applications

- Servers, Workstations and Cloud Computing
- Routers, Switches and Telecom Equipment
- Base Stations, Data Center Power Solutions
- High-Power Density Point-of-Load Conversion

General Description

The MIC24097 is a wide input range (4.5V-20V) integrated FET switching regulator that supports a 20A load.

This device integrates an enhanced Adaptive Constant On-Time (ACOT) controller with a pair of N-channel MOSFETs. The output voltage is adjustable down to 0.6V with +/-0.5% accuracy.

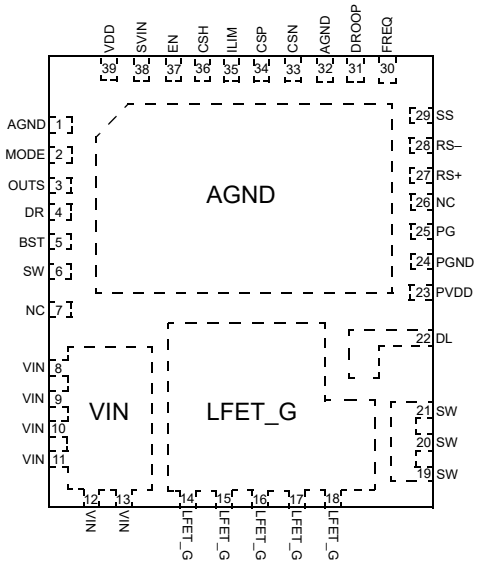
The proprietary Hyper Speed Control architecture has ultra-fast transient response, enabling a reduction in the output capacitance.

The MIC24097 utilizes Ripple Injection from the SW node to derive the necessary ripple required for controller operation.

It features a programmable switching frequency from 270 kHz to 800 kHz and has an optional droop function, which allows positioning of the output voltage in the middle of the regulation window. This adaptive positioning reduces the output filter size for a given transient response requirement.

Package Type

MIC24097
39-Pin 6 x 7 mm QFN*
(Top View)



*Includes Exposed Thermal Pads (AGND, VIN & SW); see Table 3-1.

Typical Application Circuits

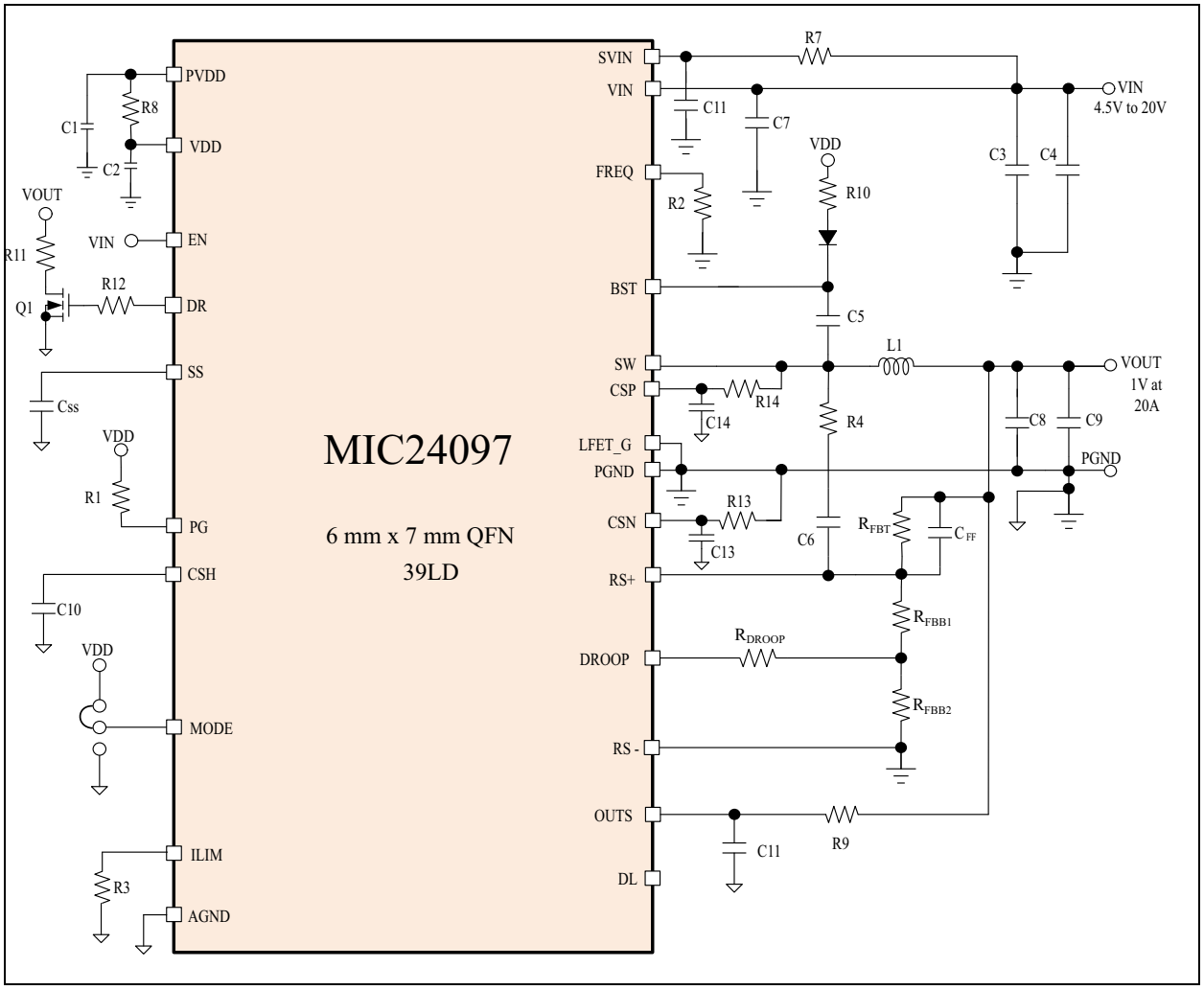


FIGURE 1: *Low Side FET R_{SDON} Sensing.*

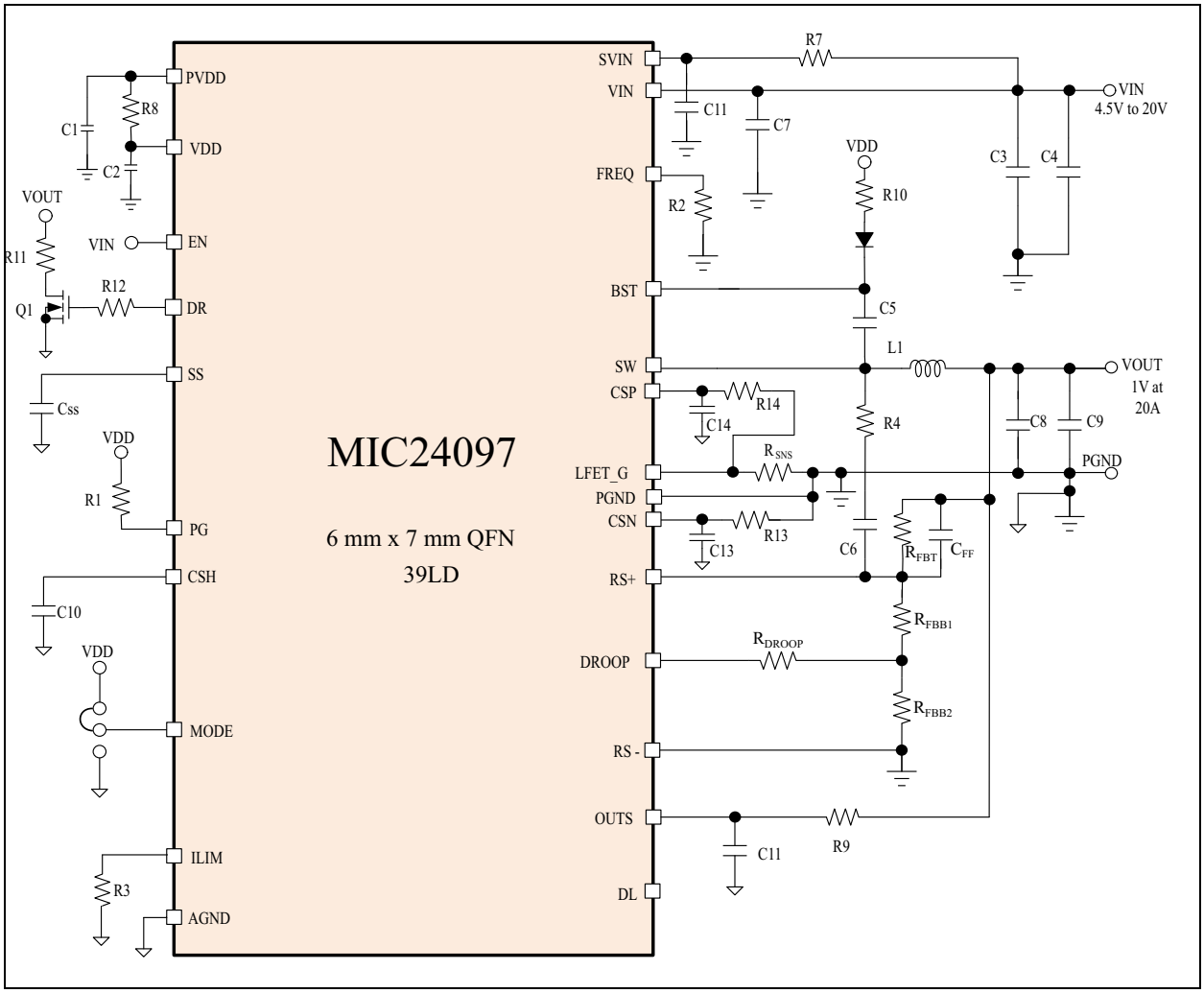
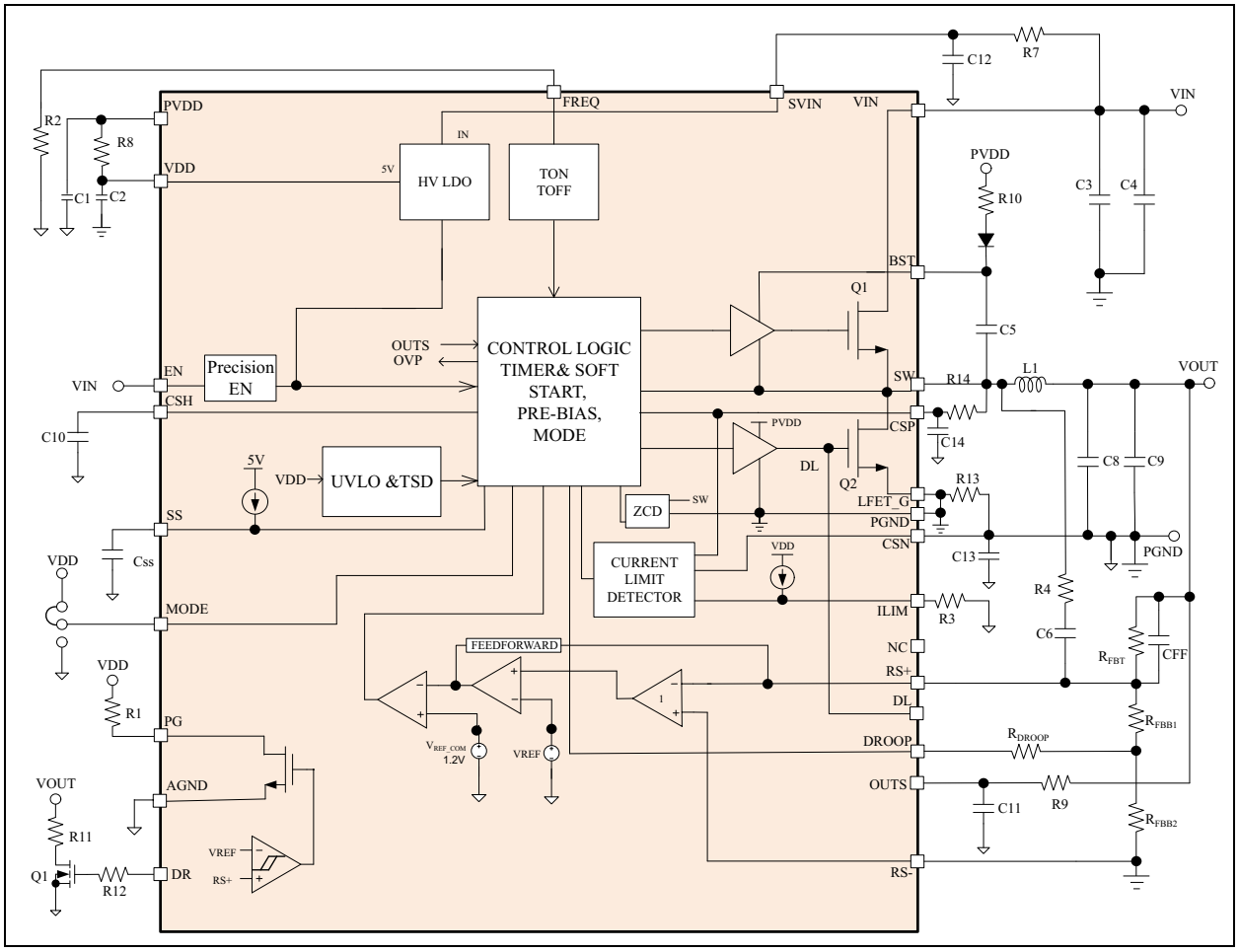


FIGURE 2: *Resistive Sensing.*

RECOMMENDED CONFIGURATION TABLE (REFER TO THE FIGURES ABOVE)

V_{OUT}	R4	C6	V_{RIP_INJ}	R_{FBT}	R_{FBB1}	R_{DROOP}	R_{FBB2}	C_{FF}	L1	R_{FREQ}(R2)	Freq.
0.8V	5.1 kΩ	10 nF	180 mV	8.2 kΩ	24 kΩ	Open	100 Ω	2.2 nF	400 nH	49.9 kΩ	400 kHz
1V	5.1 kΩ	10 nF	200 mV	8.2 kΩ	12 kΩ	Open	100 Ω	2.2 nF	450 nH	49.9 kΩ	400 kHz
1.8V	10 kΩ	10 nF	200 mV	8.2 kΩ	4.22 kΩ	Open	100 Ω	2.2 nF	1 µH	49.9 kΩ	400 kHz
3.3V	15 kΩ	10 nF	200 mV	8.2 kΩ	1.8 kΩ	Open	100 Ω	2.2 nF	2 µH	49.9 kΩ	400 kHz
5V	24 kΩ	10 nF	140 mV	8.2 kΩ	1.13 kΩ	Open	100 Ω	2.2 nF	2 µH	49.9 kΩ	400 kHz

Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings†

VIN, SVIN to PGND, LFET_G ..... -0.3V to +25V
VDD to PGND ..... -0.3V to +6V
PVDD to PGND ..... -0.3V to +6V
EN, CSP, CSN to PGND ..... -0.3V to (VIN + 0.3V)
SW to PGND, LFET_G ..... -0.3V to (VIN + 0.3V)
BST to SW ..... -0.3V to 6V
FREQ, ILIM, MODE, PG, OUTS, SS to PGND, LFET_G ..... -0.3V to (VDD + 0.3V)
DR, DROOP, RS+, RS-, RIP_INJ to PGND, LFET_G ..... -0.3V to (VDD + 0.3V)
PGND to AGND ..... -0.3V to +0.3V
Maximum Junction Temperature (T_J) ..... +150°C
Storage Temperature (T_S) ..... -65°C to +150°C
Lead Soldering Temperature (30s, reflow) ..... +260°C
ESD Rating(1):
HBM 500V
CDM ..... 1 kV

Operating Ratings‡

Supply Voltage (VIN, SVIN) ..... 4.5V to 20V
PVDD, VDD Pin Voltage ..... 4.5V to 5.5V
BST to SW Pin Voltage ..... 0V to VDD
FREQ, ILIM, MODE, PG, OUTS, SS to PGND, LFET_G ..... 0V to VDD
DR, DROOP, RS+, RS–, RIP_INJ to PGND, LFET_G ..... 0V to VDD
SW, EN, CSP, CSN ..... 0V to VIN
Junction Temperature (T_J)‡ ..... -40°C to +125°C

† **Notice:** Stresses above those listed under “Maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

‡ **Notice:** The device is not guaranteed to function outside its operating ratings.

Note 1: Devices are ESD sensitive. Handling precautions recommended. Human body model, 1.5 kΩ in series with 100 pF.

ELECTRICAL CHARACTERISTICS

VIN = SVIN = 12V, V_{OUT} = 1.2V, $V_{BST} - V_{SW}$ = 5V; T_A = 25°C, unless noted.
Bold values indicate –40°C ≤ T_J ≤ +125°C.

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
Power Supply Input						
VIN, SVIN Voltage Range	V_{IN}	**4.5**	—	**20**	V	
Quiescent Supply Current	I_Q	—	5	—	mA	V_{FBS} = +1.5V, MODE = 0V
Shut Down Current	I_{SD}	—	25	**50**	µA	V_{IN} = 20V, V_{EN} = 0V
VDD						
VDD Output Voltage	VDD	**4.7**	5.1	**5.4**	V	SVIN = 7V to 20V, IV_{DD} = 20 mA
VDD Undervoltage Lockout Upper Threshold	VDD_{UV}	**3.7**	4.2	**4.5**	V	VDD Rising
VDD UVLO Hysteresis	VDD_{UV_HYS}	—	600	—	mV	Hysteresis
VDD Regulator Dropout Voltage	V_{DROP_VDD}	—	0.8	1.05	V	SVIN = 5.5V, I_{PVDD} = 25 mA
Soft Start						
Soft Start Period	t_{SS}	—	5	—	ms	C_{SS} = 10 nF
Soft Start Source Current	I_{SS}	0.9	1.2	1.7	µA	
DC-DC Regulator						
Output Voltage Adjustable Range	V_{OUT_ADJ}	0.6	—	12	V	**Note 1**
Reference and Error Amplifier						
Feedback Regulation Voltage (RS+ – RS-)	V_{FB}	**0.597**	0.6	**0.603**	V	-40ºC ≤ T_J ≤ +105ºC
		0.593	0.6	**0.606**	V	-40ºC ≤ T_J ≤ +125ºC
RS+ Bias Current	I_{FBS}	—	2	—	nA	V_{FBS} = +0.6V, **Note 1**
RS- Bias Current	I_{GFB}	—	12	—	µA	
Error Amplifier Gain	AV_{RS}	—	1	—	V/V	V_{FBS} = +0.6V
Enable						
Enable Threshold Voltage High	V_{EN_THH}	**1.05**	1.2	**1.36**	V	Enable rising
Enable Hysteresis	V_{EN_HYS}	—	65	—	mV	
Enable Bias Current	I_{EN}	—	100	**200**	nA	V_{EN} = 12V
MODE						
MODE Logic Level High	V_{MODE_THH}	**2.8**	—	—	V	MODE rising

Note 1: Ensured by design and characterization. Not production tested.

2: Measured in test mode.

3: The maximum duty-cycle is limited by the fixed mandatory off-time of typically 360 ns.

4: Ensured by design and characterization. Not production tested.

ELECTRICAL CHARACTERISTICS (CONTINUED)

VIN = SVIN = 12V, V_{OUT} = 1.2V, $V_{BST} - V_{SW}$ = 5V; T_A = 25°C, unless noted.
Bold values indicate –40°C ≤ T_J ≤ +125°C.

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
MODE Logic Level Low	V_{MODE_THL}	—	—	**0.2**	V	MODE falling
On Timer						
Nominal Switching Frequency	$f_{SW\_Nominal}$	**400**	500	**600**	kHz	V_{IN} = 12V, OUTS = 5V, R_{FREQ} = 40.2K
Minimum Switching Frequency	f_{SW_MIN}	—	100	—	kHz	V_{IN} = 12V, OUTS = 5V, R_{FREQ} = 200K
Maximum Switching Frequency	f_{SW_max}	—	800	—	kHz	V_{IN} = 12V, OUTS = 5V, R_{FREQ} = 25.5K
Minimum ON-Time	T_{ONMIN}	—	60	—	ns	Measured in application, **Note 1**
Minimum OFF-Time	T_{OFFMIN}	—	360	—	ns	V_{FBS} = 0V
Maximum Duty Cycle	D_{MAX}	—	85	—	%	f_{SW} = 400 kHz, **Note 3**
Minimum Duty Cycle	D_{MIN}	—	0	—	%	V_{FBS} = +1V, **Note 4**
Current Limit						
ILIM Source Current	I_{CL}	**8.64**	9.6	**10.56**	µA	Trimmed
ILIM Source Current Tempco	TC_{ICL}	—	0	—	ppm/°C	
Nominal Current Limit Threshold Voltage	I_{LIM_TH}	61	71.28	79.5	mV	R_{ILIM} = 95.3 kΩ
Negative Current Limit Threshold Voltage	I_{LIM_NTH}	—	35.64	—	mV	R_{ILIM} = 95.3 kΩ
Zero Crossing Offset		**-10**	-6	**-0.6**	mV	
Current Sense Amplifier						
Current Sense Amplifier Input Offset	V_{CSA_Offset}	**-5**	0	**6**	mV	V_{CSN} = 0V, V_{FBS} = 0.59V, **Note 2**
Operating Point		**1.154**	1.19	**1.226**	V	$V_{CSN} = V_{CSP}$ = 0V
Current Sense Amplifier Gain	V_{CSA_Gain}	—	4	—	V/V	After Reflected on CSH Pin and DROOP Pin
Current Sense Input Voltage Range	$V_{CSA\_\Delta VI}$	**-120**	—	**120**	mV	-40ºC ≤ T_J ≤ +125ºC, $V_{CSP} - V_{CSN}$ = 150 mV

Note 1: Ensured by design and characterization. Not production tested.

2: Measured in test mode.

3: The maximum duty-cycle is limited by the fixed mandatory off-time of typically 360 ns.

4: Ensured by design and characterization. Not production tested.

ELECTRICAL CHARACTERISTICS (CONTINUED)

VIN = SVIN = 12V, V_{OUT} = 1.2V, $V_{BST} - V_{SW}$ = 5V; T_A = 25°C, unless noted.
Bold values indicate –40°C ≤ T_J ≤ +125°C.

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
Adaptive Voltage Positioning (AVP), i.e., DROOP						
V_{DROOP}	V_{DRP_NLOAD}	—	10	—	mV	Measure DROOP voltage ~ 0V when $V_{CSP1} - V_{CSN1}$ = 0V
	$V_{DRP\_FullLOAD}$	—	0.48	—	V	Measure DROOP voltage ~1.2V when $V_{CSP1} - V_{CSN1}$ = –120 mV
Internal MOSFET Drivers						
DH ON-Resistance, High State	DH_{RON_Hi}	—	2.5	4.5	Ω	I_{SOURCE} = 0.1A
DH ON-Resistance, Low State	DH_{RON_LOW}	—	1.2	2.2	Ω	I_{SINK} = 0.1A
DL ON-Resistance, High State	DL_{RON_Hi}	—	2.5	4.5	Ω	I_{SOURCE} = 0.1A
DL ON-Resistance, Low State	DL_{RON_LOW}	—	0.8	1.5	Ω	I_{SINK} = 0.1A
Internal MOSFET Parameters						
High Side MOSFET ON-Resistance	R_{DSON_HS}	—	7	—	mΩ	I_{SOURCE} = 0.8A
Low Side MOSFET ON-Resistance	R_{DSON_LS}	—	2.3	—	mΩ	I_{SOURCE} = 0.8A
SW, VIN and BST Leakage						
BST Leakage	$I_{LEAK(BST)}$	—	—	10	µA	V_{IN} = 20V
VIN Leakage	$I_{LEAK(VIN)}$	—	—	60	µA	V_{IN} = 20V
SW Leakage	$I_{LEAK(SW)}$	—	—	20	µA	V_{IN} = 20V
Power Good (PG)						
PG Threshold Low to High	V_{PG_TH}	**83**	90	**95**	$\%V_{OUT}$	V_{FB} rising
PG Threshold Hysteresis	V_{PG_HYS}	—	7	—	$\%V_{OUT}$	V_{FB} falling
PG Delay	t_{D_PG}	—	100	—	µs	V_{FB} rising, **Note 1**
PG Low State Voltage	V_{PG_L}	—	70	**200**	mV	V_{FBS} < (V_{PG_TH} – 7%), I_{PG} = 1 mA
PG Leakage Current	$I_{LEAK(PG)}$	—	—	**100**	nA	V_{PG} = 5.5V
Output Overvoltage Protection (DR)						
OVP Threshold	V_{OVP_TH}	**0.64**	0.67	**0.7**	V	OVP is activated after UVLO goes high and soft start

Note 1: Ensured by design and characterization. Not production tested.

2: Measured in test mode.

3: The maximum duty-cycle is limited by the fixed mandatory off-time of typically 360 ns.

4: Ensured by design and characterization. Not production tested.

ELECTRICAL CHARACTERISTICS (CONTINUED)

VIN = SVIN = 12V, V_{OUT} = 1.2V, $V_{BST} - V_{SW}$ = 5V; T_A = 25°C, unless noted.
Bold values indicate –40°C ≤ T_J ≤ +125°C.

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
OVP De-glitch Timer	$t_{DEGLITCH}$	—	12	—	µs	**Note 4**
DR Output High R_{DSON}	R_{ON_DRH}	—	30	—	Ω	I_{DR} = 10 mA
DR Output Low R_{DSON}	R_{ON_DRL}	—	25	—	Ω	I_{DR} = -10 mA
DR Rise Time	t_{R_DR}	—	160	—	ns	C_{LOAD} = 1 nF (**Note 1**)
Thermal Shutdown						
Thermal Shutdown Threshold	T_{SD}	—	160	—	°C	T_J Rising
Thermal Shutdown Hysteresis	T_{SD_HYS}	—	20	—	°C	**Note 1**

Note 1: Ensured by design and characterization. Not production tested.

2: Measured in test mode.

3: The maximum duty-cycle is limited by the fixed mandatory off-time of typically 360 ns.

4: Ensured by design and characterization. Not production tested.

TEMPERATURE SPECIFICATIONS

Parameters	Symbol	Min.	Typ.	Max.	Units	Conditions
Temperature Ranges						
Operating Junction Temperature Range	T_J	–40	—	125	°C	Note 1
Maximum Junction Temperature	$T_{J(ABSMAX)}$	—	—	150	°C	—
Storage Temperature Range	T_S	–65	—	150	°C	—
Lead Temperature	T_{LEAD}	—	—	260	°C	Reflow Soldering, 30s
Package Thermal Resistance						
39-Lead VQFN, 6 mm x 7 mm (Note 2)	Ψ_{JT}	—	0.41	—	°C/W	Junction to Surface
	θ_{JC}	—	14.9	—	°C/W	Junction to Case
	θ_{JA}	—	21.5	—	°C/W	Junction to Ambient

Note 1: The maximum allowable power dissipation is a function of ambient temperature, the maximum allowable junction temperature and the thermal resistance from junction to air (i.e., T_A, T_J, θ_{JA}). Exceeding the maximum allowable power dissipation will cause the device operating junction temperature to exceed the maximum +125°C rating. Sustained junction temperatures above +125°C can impact the device reliability.

2: Measured on MCHP MIC24097 EVB (EV28T12A) in still air.

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables shown following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, V_{IN} = 12V; V_{OUT} = 1V; f_{SW} = 400 kHz; $V_{BST} - V_{SW}$ = 5V; T_A = +25°C.

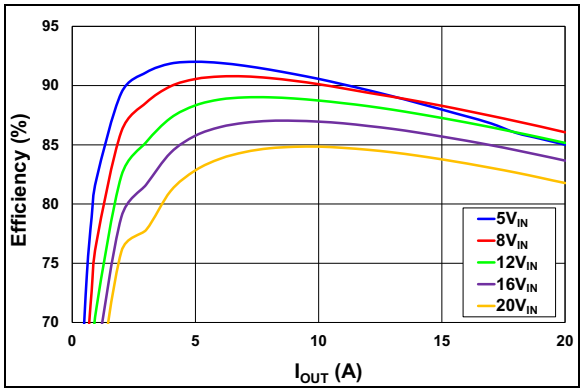


FIGURE 2-1: *Efficiency (V_{OUT} = 1.04V) vs. Load (Mode = HLL, f_{SW} ≈ 400 kHz).*

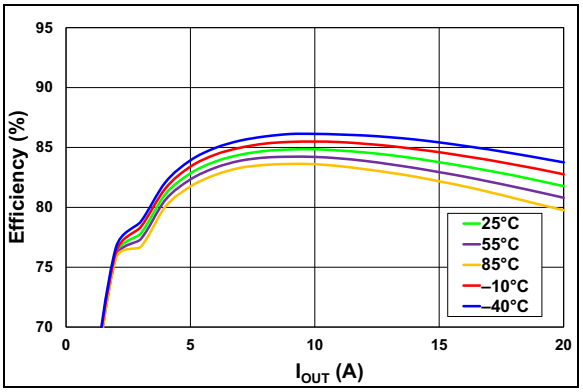


FIGURE 2-4: *Efficiency (V_{OUT} = 1.04V) vs. Temperature (V_{IN} = 20V, f_{SW} ≈ 400 kHz).*

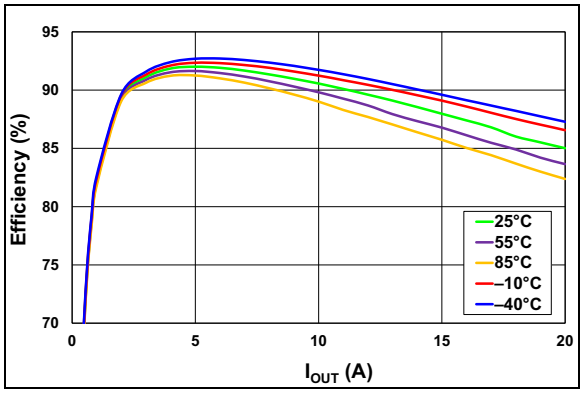


FIGURE 2-2: *Efficiency (V_{OUT} = 1.04V) vs. Temperature (V_{IN} = 5V, f_{SW} ≈ 400 kHz).*

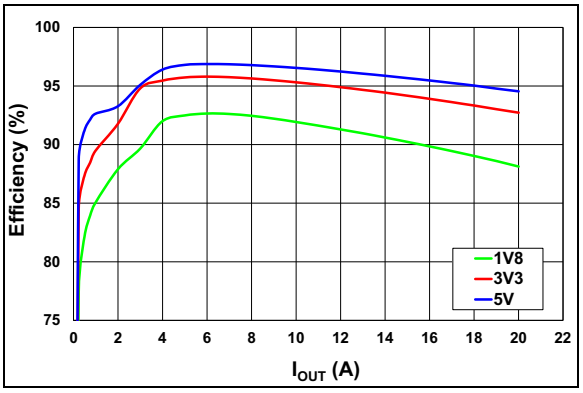


FIGURE 2-5: *Efficiency V_{OUT} vs. Output Current (f_{SW} ≈ 400 kHz).*

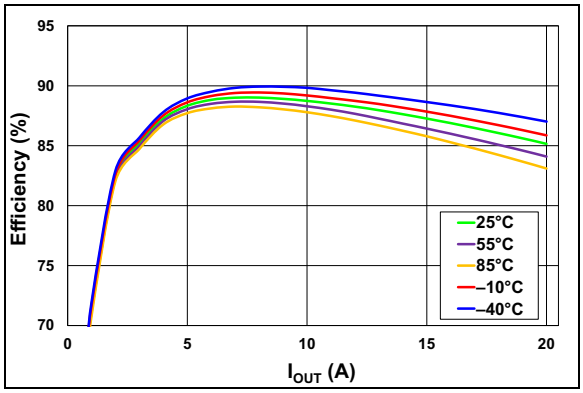


FIGURE 2-3: *Efficiency (V_{OUT} = 1.04V) vs. Temperature (V_{IN} = 12V, f_{SW} ≈ 400 kHz).*

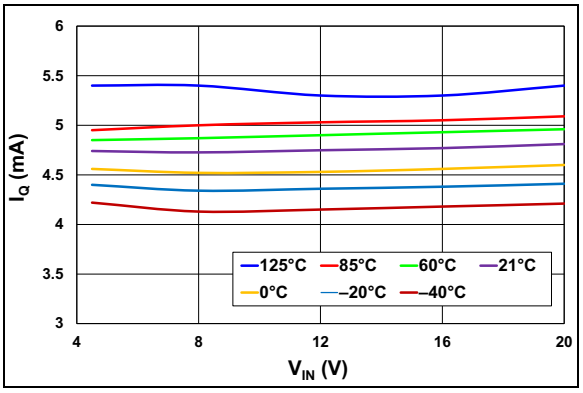


FIGURE 2-6: *V_{IN} Quiescent Current vs. Input Voltage.*

Note: Unless otherwise indicated, V_{IN} = 12V; V_{OUT} = 1V; f_{SW} = 400 kHz; $V_{BST} – V_{SW}$ = 5V; T_A = +25°C.

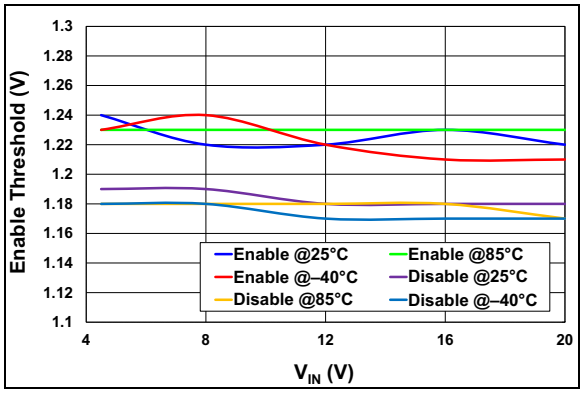


FIGURE 2-7: *Enable Threshold vs. Input Voltage over Temperature.*

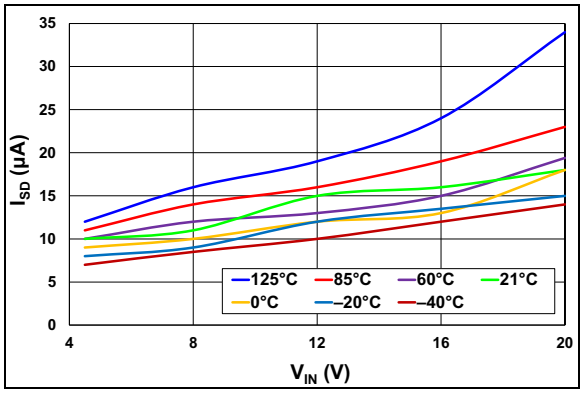


FIGURE 2-10: *Shutdown Current vs. Input Voltage.*

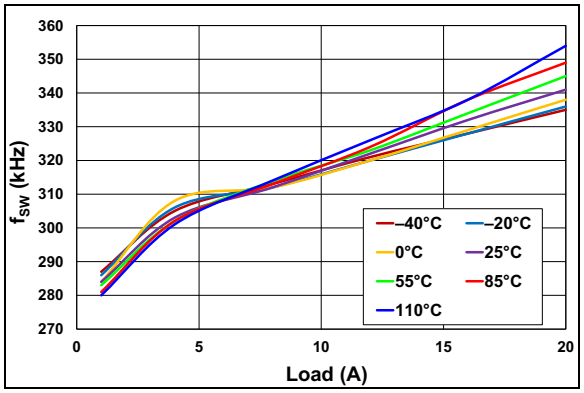


FIGURE 2-8: *Frequency vs. Load Current Over the Temperature (R_{FREQ} = 68 kΩ).*

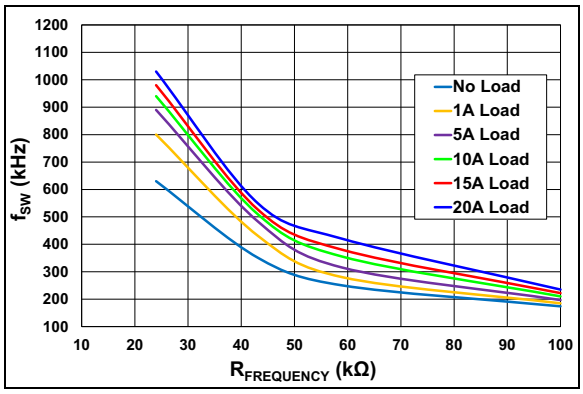


FIGURE 2-11: *Frequency vs. $R_{FREQUENCY}$.*

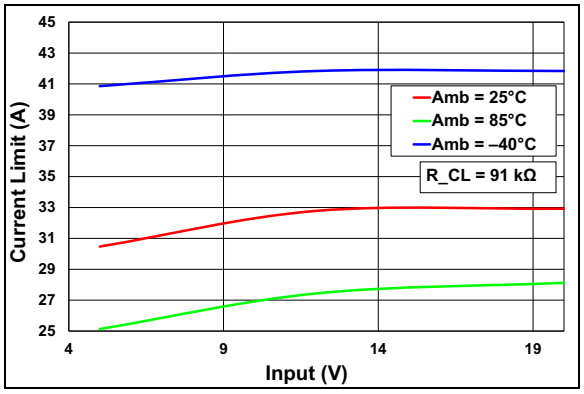


FIGURE 2-9: *Current Limit vs. Input Voltage.*

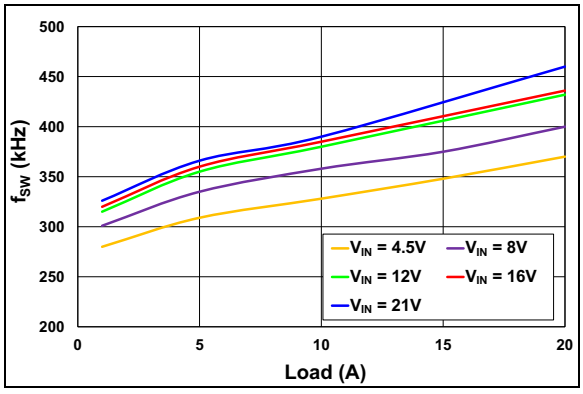


FIGURE 2-12: *Frequency vs. Load over Input Voltage (R_{FREQ} = 68 kΩ).*

Note: Unless otherwise indicated, V_{IN} = 12V; V_{OUT} = 1V; f_{SW} = 400 kHz; $V_{BST} - V_{SW}$ = 5V; T_A = +25°C.

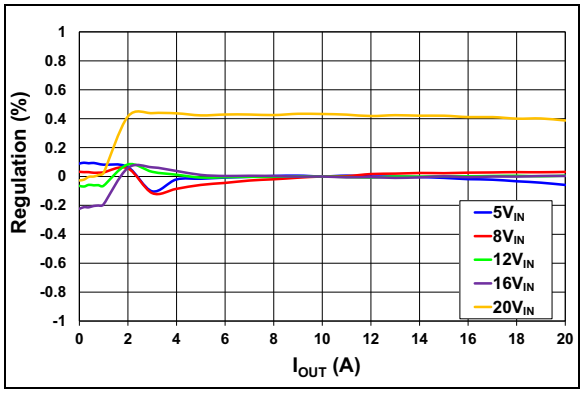


FIGURE 2-13: *Output Load Regulation (V_{OUT} = 1.0V, f_{SW} ≈ 400 kHz).*

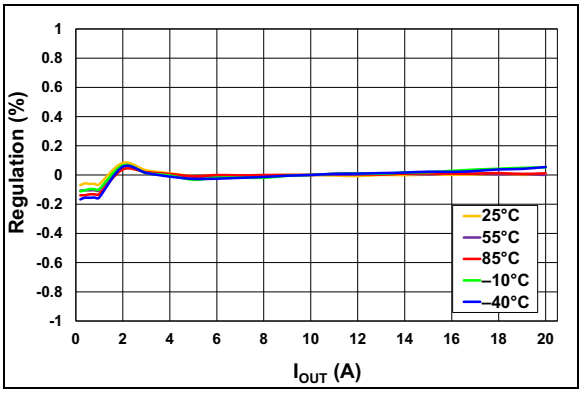


FIGURE 2-16: *Load Regulation (V_{IN} = 12V) vs. Temperature (V_{OUT} = 1.0V, f_{SW} ≈ 400 kHz).*

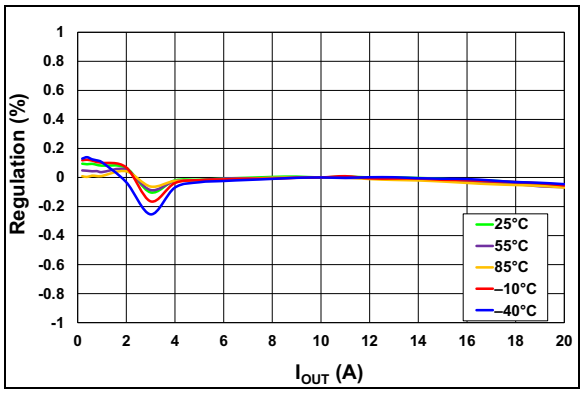


FIGURE 2-14: *Load Regulation (V_{IN} = 5V) vs. Temperature (V_{OUT} = 1.0V, f_{SW} ≈ 400 kHz).*

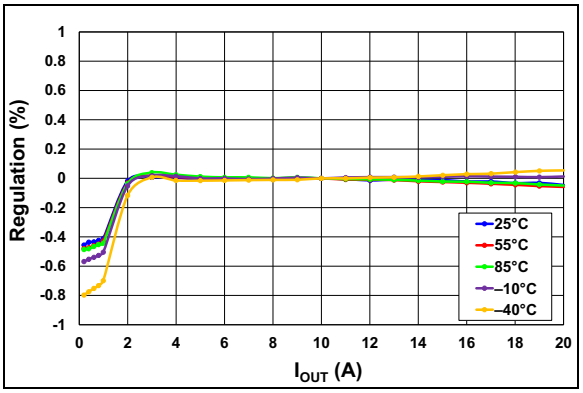


FIGURE 2-17: *Load Regulation (V_{IN} = 20V) vs. Temperature (V_{OUT} = 1.0V, f_{SW} ≈ 400 kHz).*

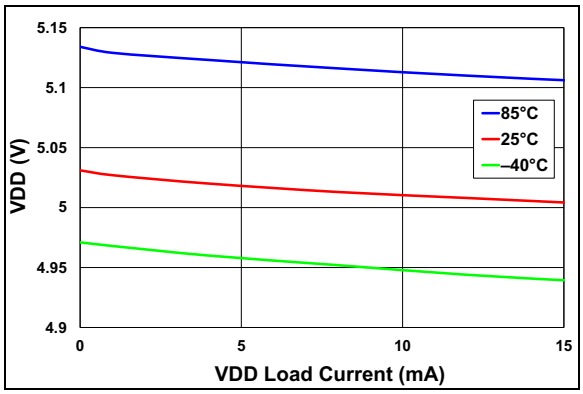


FIGURE 2-15: *VDD vs. Load over Temperature.*

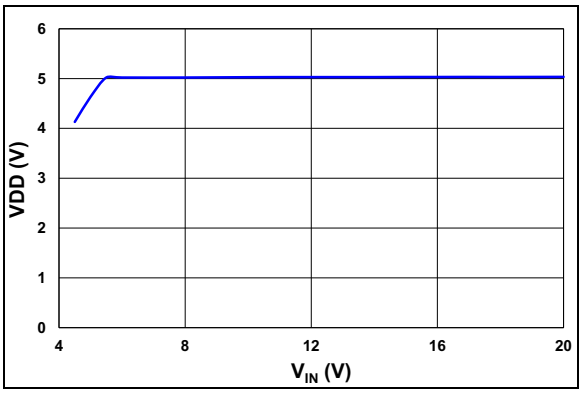


FIGURE 2-18: *VDD vs. V_{IN}.*

Note: Unless otherwise indicated, V_{IN} = 12V; V_{OUT} = 1V; f_{SW} = 400 kHz; $V_{BST} – V_{SW}$ = 5V; T_A = +25°C.

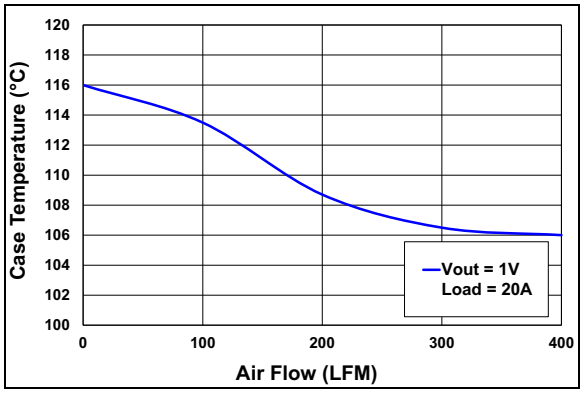


FIGURE 2-19: *Case Temperature vs. LFM @ 85°C.*

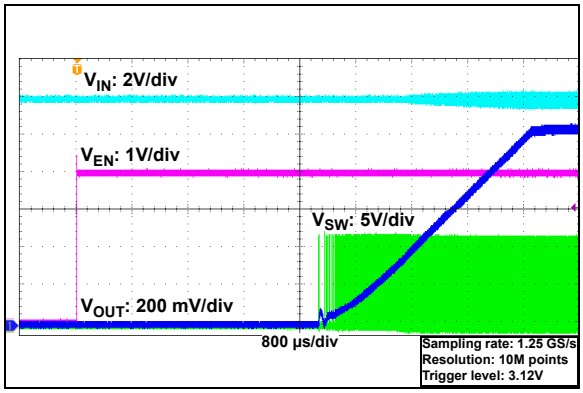


FIGURE 2-22: *Enable Turn-on and Rise Time Switching Waveform (I_{OUT} = 20A).*

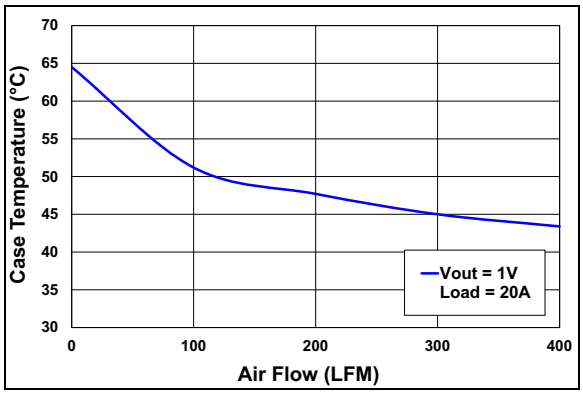


FIGURE 2-20: *Case Temperature vs. LFM @ 25°C.*

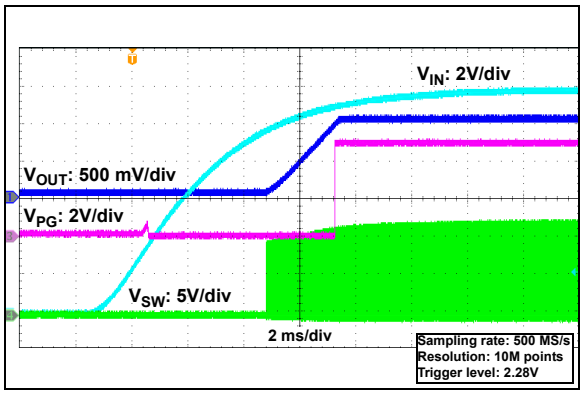


FIGURE 2-23: *Input Turn-on and Rise Time Switching Waveform (I_{OUT} = 0A).*

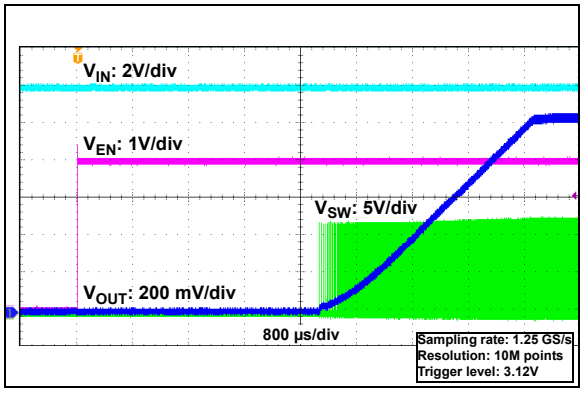


FIGURE 2-21: *Enable Turn-on and Rise Time Switching Waveform (I_{OUT} = 0A).*

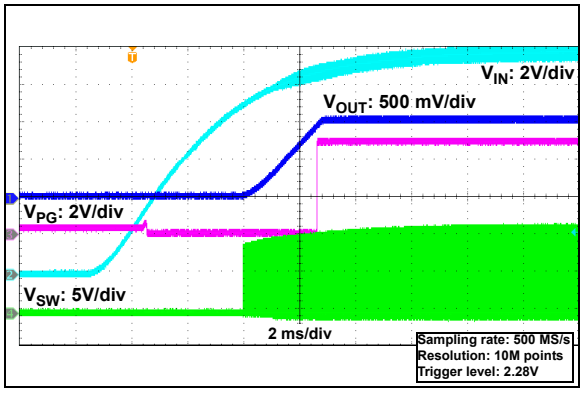


FIGURE 2-24: *VIN Start-up and Rise Time Switching Waveform (I_{OUT} = 20A).*

Note: Unless otherwise indicated, V_{IN} = 12V; V_{OUT} = 1V; f_{SW} = 400 kHz; $V_{BST} - V_{SW}$ = 5V; T_A = +25°C.

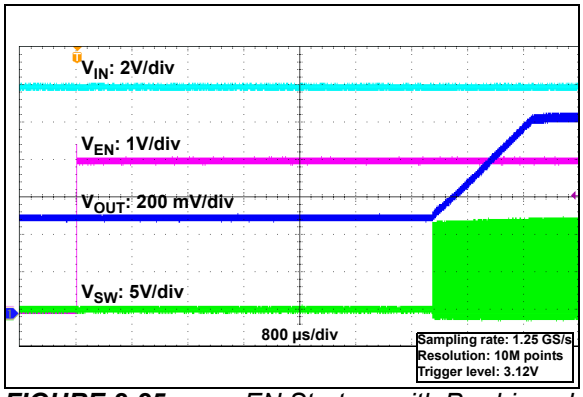


FIGURE 2-25: *EN Start-up with Pre-biased Output.*

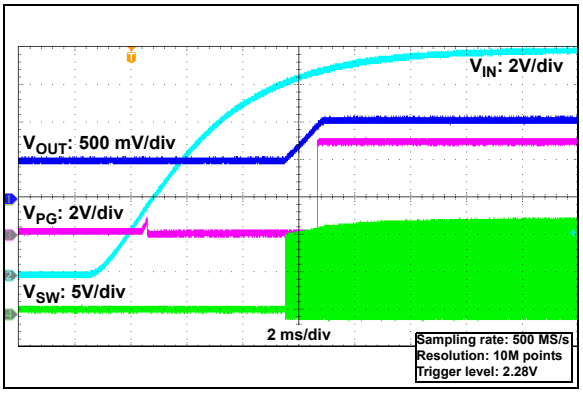


FIGURE 2-28: *VIN Start-up with Pre-biased Output.*

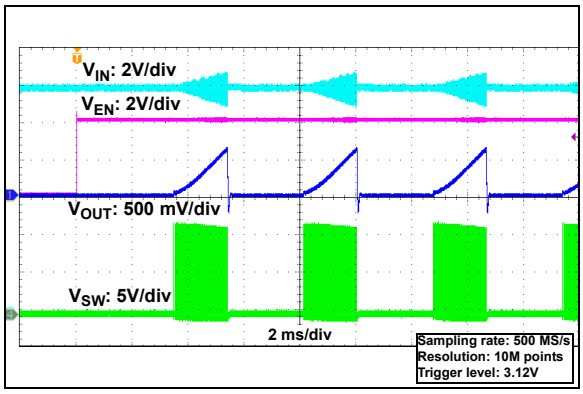


FIGURE 2-26: *Enable Startup into Short Circuit.*

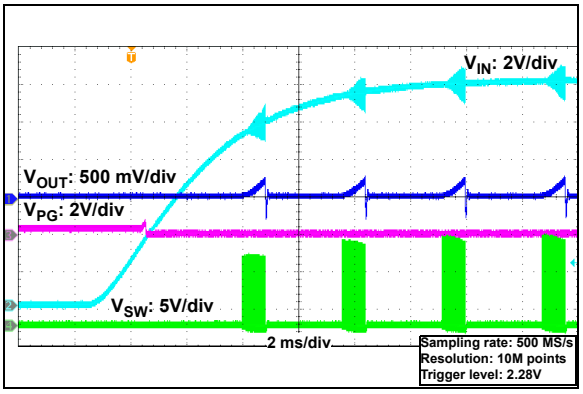


FIGURE 2-29: *VIN Startup into Short Circuit.*

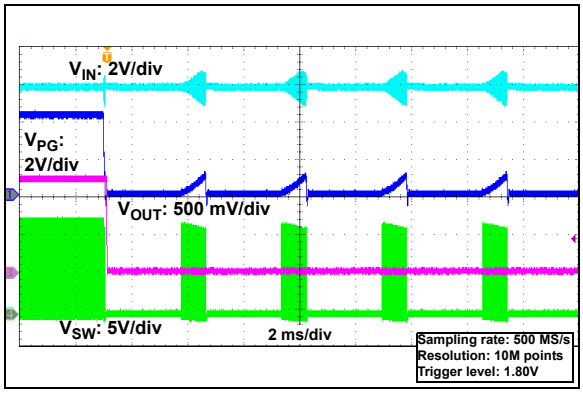


FIGURE 2-27: *Response to Short Circuit.*

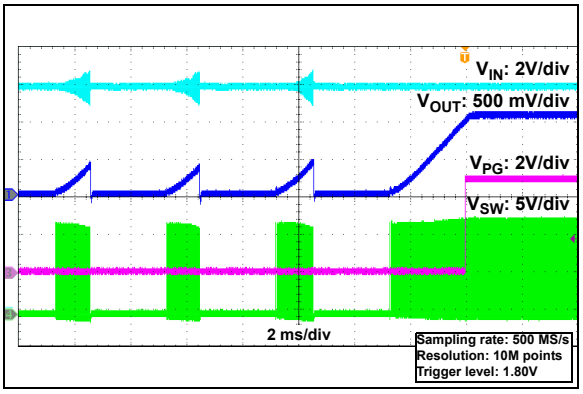


FIGURE 2-30: *Recovery from Short Circuit.*

Note: Unless otherwise indicated, V_{IN} = 12V; V_{OUT} = 1V; f_{SW} = 400 kHz; $V_{BST} – V_{SW}$ = 5V; T_A = +25°C.

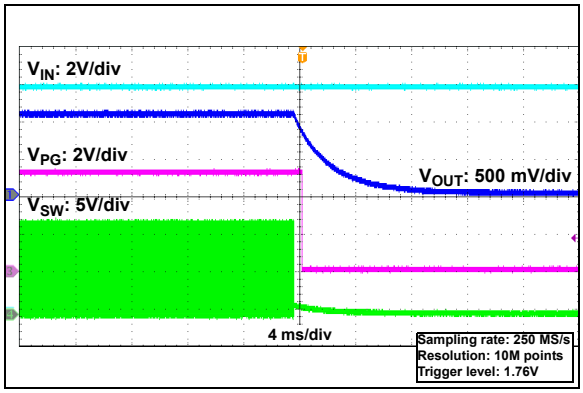


FIGURE 2-31: *Thermal Shutdown Response.*

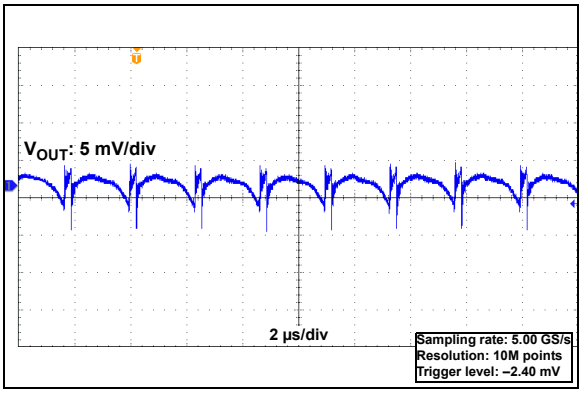


FIGURE 2-34: *Output Ripple Voltage (Load = 20A).*

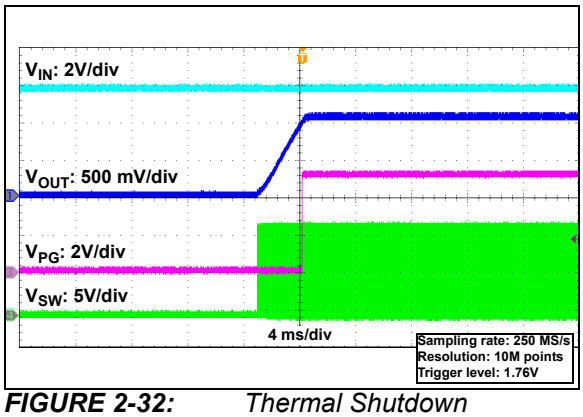


FIGURE 2-32: *Thermal Shutdown Recovery.*

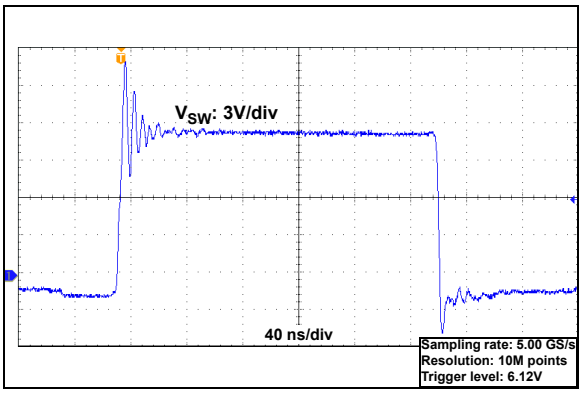


FIGURE 2-35: *Switching Waveform, 1 Cycle (Load = 20A).*

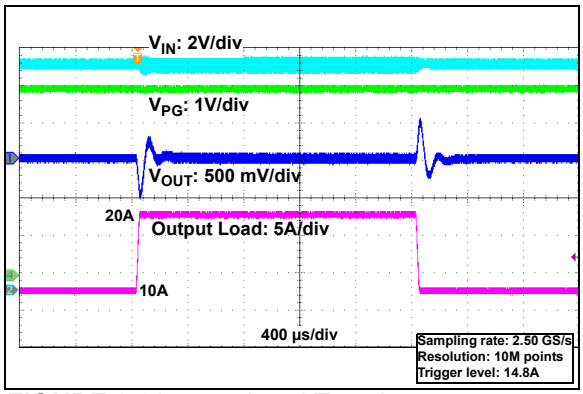


FIGURE 2-33: *Load Transient.*

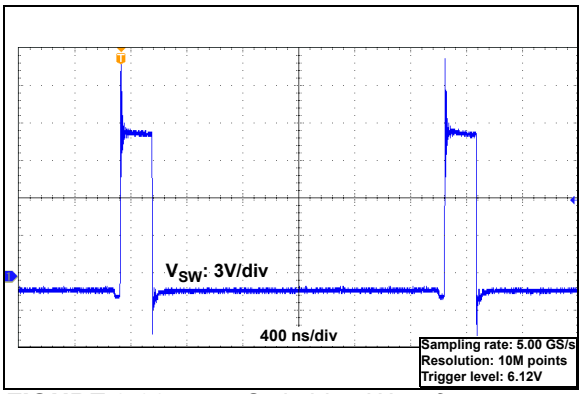


FIGURE 2-36: *Switching Waveform, 2 Cycles (Load = 20A)*

3.0 PIN CONFIGURATION

TABLE 3-1: PIN CONFIGURATION TABLE

Pin	Name	Description
1, 32	AGND	Analog ground. Reference node for all the control logic circuits inside the MIC24097. Connect AGND and EP to PGND at one star point.
2	MODE	MODE selection pin. Connect MODE to GND for Hyper Light Load operation. Connect MODE to VDD for CCM operation.
3	OUTS	Output voltage sense. It is required to connect the OUTS pin to the output through a 10k resistor for VOUT ≤ 5V. For VOUT > 5V, it is required to connect the OUTS pin through a resistive divider from VOUT to AGND in order to bring OUTS to 5V. The OUTS pin will help maintain the correct switching frequency adaptive to the output voltage.
4	DR	Gate driver output for output OVP discharge MOSFET. One single event for a duration longer than 12 µs sets DR = High. The MIC24097 must be restarted by EN or by power cycling to reset DR low.
5	BST	Bootstrap Capacitor connection. BST pin is the supply voltage for the high-side MOSFET driver. Connect a 0.1 µF low ESR ceramic capacitor between the BST pin and the SW pin.
6	SW	Switch Node Output. Connect all the SW pins together. Connect one terminal of the inductor to the SW node. SW also needs to be connected to the CSP pin for low-side MOSFET RDSON current sensing.
7	NC	Not connected.
8, 9, 10, 11, 12, 13	VIN	Input voltage supply to the drain of the internal high-side power MOSFET.
14, 15, 16, 17, 18	LFET_G	LFET_G is the return path for the low-side MOSFET current. Connect all the LFET_G pins together and connect to the RSENSE resistor or power ground plane.
19, 20, 21	SW	Switch Node Output. Connect all the SW pins together. Connect one terminal of the inductor to the SW node. SW is also connected to the CSP pin for low-side MOSFET RDSON current sensing.
22	DL	Low-Side Switch Gate Driver Output. DL is internally connected to the gate of the low-side MOSFET. Leave this pin unconnected.
23	PVDD	PVDD is the supply for the low-side MOSFET driver. Connect to VDD through a series resistor in the range of 1-5Ω. Connect a minimum 4.7 µF low ESR ceramic capacitor from PVDD to PGND.
24	PGND	Power ground connection for the low-side MOSFET driver in the controller circuit. Connect to the PGND plane on the PCB.
25	PG	Open drain Power Good Output. PG is pulled to ground when the output voltage is below 10% of the target voltage. Pull-up to VDD through a 10 kΩ resistor to set logic high level when the output voltage is above 90% of the target voltage.
26	NC	Not connected.
27	RS+	Feedback Input. Connect RS+ to the midpoint of a resistor divider from the output voltage to RS– to set the desired output voltage.
28	RS-	Ground feedback sense pin. Connect directly across output capacitor ground through low-side FB resistor ground connection.
29	SS	Soft start adjustment pin. Connect a capacitor from SS pin to AGND to adjust soft start time. See more details in Section 5.0, Application Information.
30	FREQ	Frequency Programming Input. Connect to ground through a resistor to set the switching frequency.
31	DROOP	Analog Output DROOP pin for implementing “Adaptive voltage positioning” feature. Connect a resistor from DROOP pin to RS+. The DROOP voltage is proportional with inductor current.

TABLE 3-1: PIN CONFIGURATION TABLE (CONTINUED)

Pin	Name	Description
33	CSN	Current sense return pin. Connect kelvin connection from LFET_G pins (for LFET R_{DSON} sensing) or from bottom of sense resistor to CSN via R-C filter (for resistor sensing) to avoid switching noise affecting current sensing. Please refer to Typical Application Circuits.
34	CSP	Current sense positive pin. Connect kelvin connection from SW pins 19, 20, 21 (for LFET R_{DSON} sensing) or LFET_G pins to CSP via R-C filter (for resistor sensing) to avoid switching noise affecting current sensing. Please refer to Typical Application Circuits.
35	ILIM	Current Limit Adjust Input. Connect a resistor from ILIM to the AGND to set current limit. Refer Section 4.5.2, Current Limit for more details.
36	CSH	Current sense output. This is a bidirectional pin. This can be used for analog current sense output or be left floating.
37	EN	Enable Logic Input. Connect to VIN or drive from an external logic signal to enable/disable the MIC24097. When EN = Logic High, the MIC24097 is enabled when EN = Logic Low, the MIC24097 is disabled.
38	SVIN	Input voltage to controller. Connect to VIN through 1-5Ω resistor to filter noise and ripple on the VIN rail. Connect a 1 µF capacitor from this pin to PGND.
39	VDD	5V LDO output. Bias supply for the control logic circuitry. Connect a minimum 2.2 µF low ESR ceramic capacitor from VDD to AGND.

4.0 FUNCTIONAL DESCRIPTION

4.1 Control Architecture

The MIC24097 is an adaptive ON-time synchronous step-down DC/DC regulator. It is designed to operate over a wide input voltage range from 4.5V to 20V and provides a regulated output voltage with up to 20A of load current. An adaptive ON-time control scheme is employed in order to obtain a constant-switching frequency and to simplify the control compensation. Over-current protection could be implemented without the use of an external sense resistor. The device includes a programmable soft-start function which reduces the power supply input surge current at start-up by controlling the output voltage rise time.

The output voltage is sensed by the feedback pin (RS+) and ground sense pin (RS-) via the voltage divider R1 and R2, and is compared to a 1.2V reference voltage V_{REF_COM} at the error comparator through a low-gain transconductance (gm) amplifier. If the feedback voltage decreases and the output of the gm amplifier fall below 1.2V, then the error comparator will trigger the control logic and generate an ON–time period. The ON–time period length is predetermined by the “FIXED t_{ON} ESTIMATION” circuitry:

EQUATION 4-1:

$$T_{ON(EST)} = \frac{V_{OUT}}{V_{IN} \times f_{SW}}$$

Where:

V_{OUT} = Output voltage
V_{IN} = Power stage input voltage
f_{SW} = Switching frequency

At the end of the ON–time period, the internal high–side driver turns off the high–side MOSFET and the low–side driver turns on the low–side MOSFET. The OFF–time period length depends upon the feedback voltage in most cases. When the feedback voltage decreases and the output of the gm amplifier falls below 0.6V, the ON-time period is triggered and the OFF–time period ends. If the OFF–time period determined by the feedback voltage is less than the minimum OFF–time $t_{OFF(MIN)}$, which is about 360 ns then the MIC24097 control logic will apply the $t_{OFF(MIN)}$ instead. The minimum $t_{OFF(MIN)}$ period is required to maintain enough energy in the bootstrap capacitor (C_{BST}) to drive the high–side MOSFET.

The maximum duty cycle is obtained from the 360 ns $t_{OFF(MIN)}$:

EQUATION 4-2:

$$D_{MAX} = \frac{T_S - T_{OFF(MIN)}}{T_S} = 1 - \frac{360\ ns}{T_S}$$

Where:

$T_S = 1/f_{SW}$

It is not recommended to use MIC24097 with an OFF-time close to $t_{OFF(MIN)}$ during steady-state operation.

The actual ON–time and resulting switching frequency will vary with the part-to-part variation in the rise and fall times of the internal MOSFETs, the output load current, and variations in the VDD voltage. Also, the minimum t_{ON} results in a lower switching frequency in high V_{IN} to V_{OUT} applications, such as 20V input to 1.0V output.

Figure 4-1 shows the control loop timing during steady-state operation. During steady-state, the gm amplifier senses the feedback voltage ripple, which is proportional to the output voltage ripple and the inductor current ripple, to trigger the ON–time period. The ON–time is predetermined by the t_{ON} estimator. The termination of the OFF–time is controlled by the feedback voltage. At the valley of the feedback voltage ripple, which occurs when V_{GM} falls below V_{REF_COM}, the OFF period ends and the next ON–time period is triggered through the control logic circuitry.

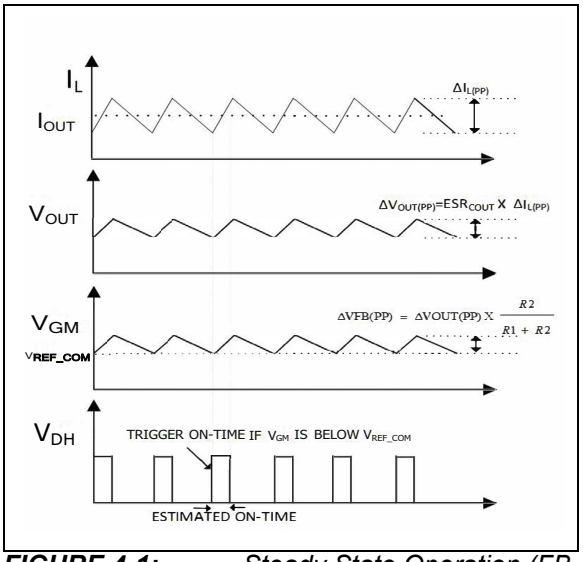


FIGURE 4-1: *Steady State Operation (FB Ripple Shows Injected and ESR Ripple Only, Reactive Impedances Neglected).*

Figure 4-2 shows the operation of the MIC24097 during load transient. The output voltage drops due to the sudden load increase, which causes the V_{GM} to be less than V_{REF_COM}. This will cause the error comparator to

trigger an ON-time pulse. At the end of the ON-time, a minimum OFF-time $t_{OFF(MIN)}$ is generated to charge C_{BST} since the feedback voltage is still below V_{REF_COM}. Then, the next ON-time pulse is triggered due to the low feedback voltage. Therefore, the switching frequency changes during the load transient, but returns to the nominal fixed frequency once the output has stabilized at the new load current level. With the varying duty cycle and switching frequency, the output recovery time is fast and the output voltage deviation is minimized.

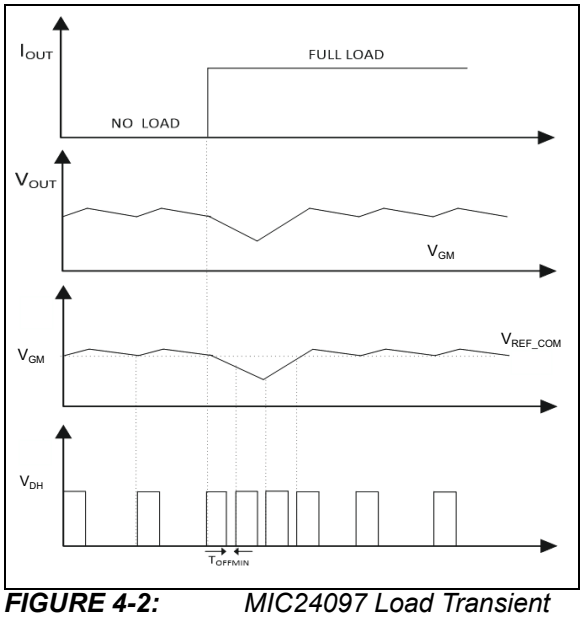


FIGURE 4-2: *MIC24097 Load Transient Response.*

Unlike true Current-mode control, the MIC24097 uses the output voltage ripple to trigger an ON-time pulse. The output voltage ripple is proportional to the inductor current ripple if the ESR of the output capacitor is large enough. To meet the stability requirements, the feedback voltage ripple should be in phase with the inductor current ripple and be large enough to be sensed by the gm amplifier and the error comparator. The recommended feedback voltage ripple is ~40-200 mV. If a low-ESR output capacitor is selected, then the feedback voltage ripple may be too small to be sensed by the gm amplifier and the error comparator. Also, the output voltage ripple and the feedback voltage ripple are not necessarily in phase with the inductor current ripple if the ESR of the output capacitor is very low. In these cases, ripple injection is required to ensure proper operation.

4.2 Stability Analysis

The MIC24097 uses a ripple-based ACOT architecture to generate switching pulses. The FB node requires in-phase ripple which resembles inductor current for regulation. The magnitude of ripple needs to be in the range of ~40-200 mV. The ripple can be extracted from ESR of the output capacitor in addition to capacitor ripple. Figure 4-3 shows the ripple at FB node with respect to the reference voltage.

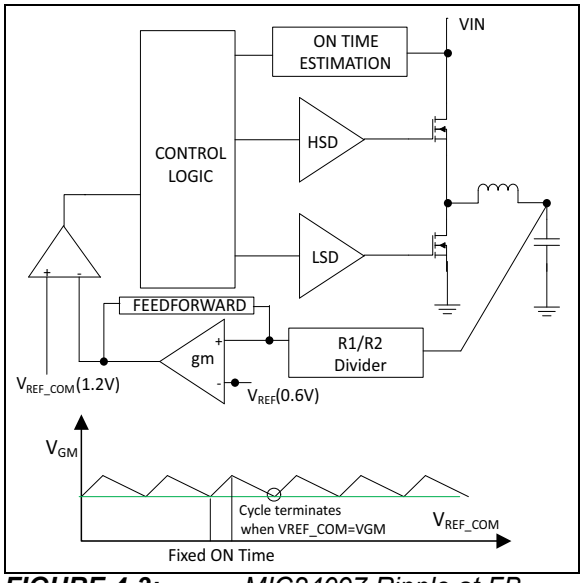


FIGURE 4-3: *MIC24097 Ripple at FB Node.*

If the ripple voltage at the FB node is not in phase with the inductor current ripple, double or multiple pulsing may occur, causing the circuit to become unstable. The output capacitors generally have three components: (1) capacitive ripple, which lags the inductor current ripple, (2) ESR ripple, which is in phase with inductor current, and (3) ESL ripple, which has very minimal impact in low-voltage capacitors. Capacitive and ESR ripple are depicted in Figure 4-4. Figure 4-5 shows the vector relation of effective FB ripple voltage for high ESR capacitors.

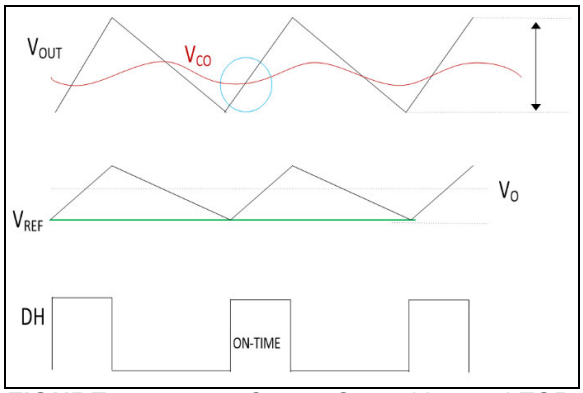


FIGURE 4-4: *Output Capacitive and ESR Ripple.*

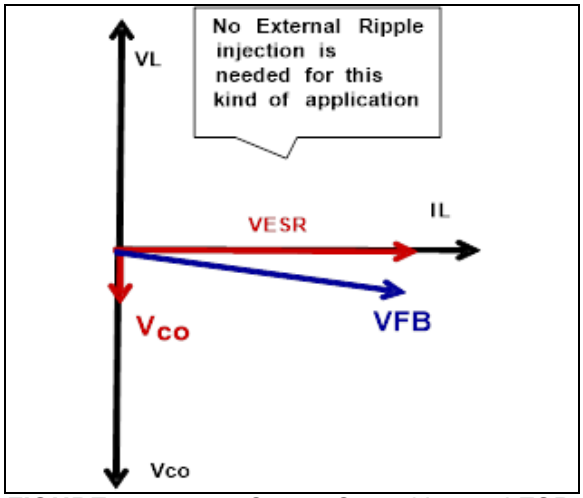


FIGURE 4-5: *Output Capacitive and ESR Ripple Vector Relation.*

External injected ripple is not required when ESR ripple is high as compared to capacitive ripple. Modern loads require output voltage steady-state ripple to be less than 1% of regulation voltage. For output voltages in the range of 1V, output steady-state ripple voltage requirement is on the order of 10 mV. Customers generally use ceramic capacitors or low-ESR tantalum capacitors to meet steady-state requirements for their loads, and the MIC24097 control loop will require external ripple injection to the FB node for these situations.

4.3 Ripple Injection for Low ESR Capacitors

When customers use low ESR electrolytic capacitors or tantalum capacitors, external ripple can be injected by connecting a feed forward capacitor (CFF) from the output to the FB node as shown in Figure 4-6.

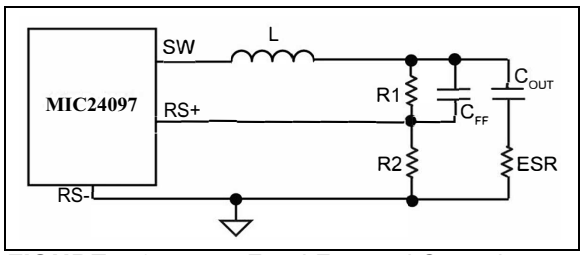


FIGURE 4-6: *Feed Forward Capacitor.*

EQUATION 4-3:

$$\frac{V_{FB}}{V_{OUT}}(s) = \frac{R2}{R1+R2} \times \frac{1 + s \times C_{FF} \times R1}{1 + s \times C_{FF} \times \frac{R1 \times R2}{R1+R2}}$$

As detailed by Equation 4-3 and shown in Figure 4-7, a feed-forward capacitor bypasses high-frequency ripple to the FB pin and provides phase boost at mid frequency.

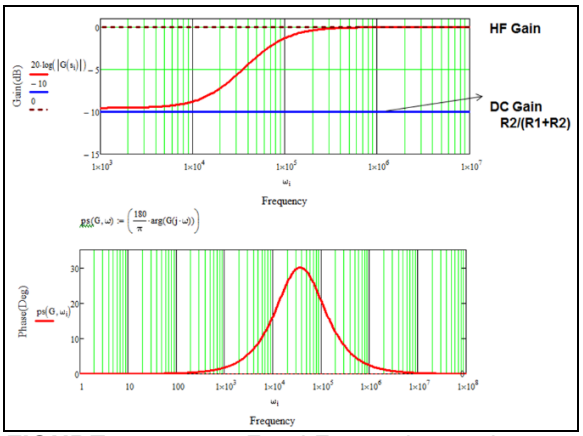


FIGURE 4-7: *Feed Forward capacitor Gain and Phase Plots.*

4.4 Ripple Injection for Ceramic Capacitors

Customers use ceramic capacitors in the output filter for many high-performance ASIC applications. Ceramic capacitors have very low ESR and ESL; in this case, the MIC24097 needs extra ripple injected from the switch node. In these applications, external ripple can be injected by connecting series RC network from the switch node to the FB node, as shown in Figure 4-7.

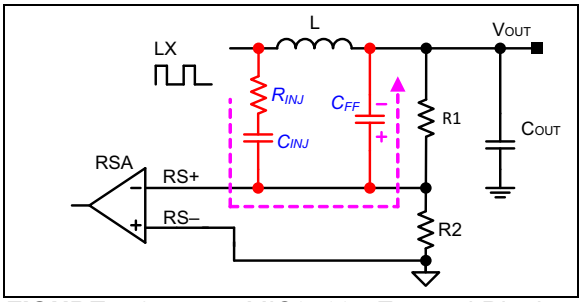


FIGURE 4-8: *MIC24097 External Ripple Injection Circuit.*

The purpose of CINJ is to block the DC component and forward high-frequency content from the switch node. It is required to select CINJ value very much higher than CFF value.

Follow the steps below for selecting ripple injection circuit components if low ESR output capacitors are used. Note that the assumption used for the below guidelines is that the crossover frequency is well over the output filter LC resonant frequency.

1. Calculate the product of R_{INJ} and C_{FF} for a given injected Feedback Ripple Voltage, ΔV_{FB}, using Equation 4-4. Choose ΔV_{FB} in the range from 40-200 mV. A good starting point for ΔV_{FB} is 100 mV.

EQUATION 4-4:

$$R_{INJ} = \frac{1}{C_{FF}} \times \frac{V_{OUT}}{\Delta V_{FB(MIN)}} \times (1 - D) \times T_{SW}$$

Where:

V_{OUT} = Output voltage
ΔV_{FB} = Feedback ripple voltage
D = Duty cycle
T_{SW} = Switching period

2. Choose C_{FF} in the range of 0.47-10 nF.
3. Calculate R_{INJ} using Equation 4-4.
4. Calculate $R_{FB(TOP)}$ using Equation 4-5 below:

EQUATION 4-5:

$$R_{FB(TOP)} \geq \frac{1}{2\pi \times C_{FF} \times 0.8 f_{LC}}$$

Where:

f_{LC} = Is the LC resonant frequency
L = Inductor

C_{OUT} output capacitor $f_{LC} = \frac{1}{2\pi\sqrt{LC_{OUT}}}$

5. Calculate $R_{FB(BOT)}$ using Equation 4-6 below:

EQUATION 4-6:

$$R_{FB(BOT)} = \frac{R_{FB(TOP)}}{\frac{V_{OUT}}{V_{REF}} - 1}$$

Where:

V_{OUT} = The target output voltage
V_{REF} = The reference voltage (which is 0.6V for MIC24097)

6. Estimate the crossover frequency using Equation 4-7 below:

EQUATION 4-7:

$$f_{CO(EST)} = \frac{R_{INJ} \times C_{FF}}{2 \times \pi \times L \times C_{OUT}}$$

7. Select C_{INJ} using Equation 4-8 below to get phase margin > 60 degrees.

Using a lower C_{INJ} gives better load transient performance in DCM and CCM mode, but it affects the phase margin. The optimal value should be selected using an iterative approach.

EQUATION 4-8:

$$C_{INJ} \geq \frac{1}{2\pi \times R_{INJ} \times 1.25 f_{CO(EST)}}$$

8. Check if:

EQUATION 4-9:

$$C_{INJ} \leq C_{FF} \times \frac{R_{RFB(TOP)}}{R_{RFB(BOT)}}$$

This criterion ensures that there is no overshot at the end of the soft start. If this criterion is not met, add a resistor in parallel to the SS capacitor. The following criteria in Equation 4-10 can be used to select the parallel resistor.

EQUATION 4-10:

$$R_{SS} \geq \frac{0.8V}{I_{SS}}$$

Where:

I_{SS} = Soft start current source (which is 1.2 µA)

Follow the below steps for selecting ripple injection circuit components when f_{CO}(EST) (refer to the step #6 above) is below f_{SW}/10 (i.e. when the f_{CO} is limited by the minimum FB ripple required). Customers may need to follow this method mainly in lower V_{OUT} applications where the FB ripple limits the f_{CO}.

1. Steps 1-5 are the same as the above.
2. Assume $f_{CO} = f_{SW}/10$
3. Ensure that the output capacitor ESR meets the following criteria:

EQUATION 4-11:

$$ESR_{COUT} \leq \frac{\Delta V_{OUT(TRANS)}}{\Delta I_{LOAD(STEP)}}$$

Where:

I_{SS} = Soft start current source (which is 1.2 µA)

4. Calculate minimum C_{OUT} using Equation 4-12 below.

EQUATION 4-12:

$$C_{OUT} \geq \frac{1}{\pi \times f_{CO} \times ESR_{COUT}}$$

4.5 Detailed Device Description

The MIC24097 has a soft start feature, which is adjustable with an external capacitor. MIC24097 has a MODE selector for CCM/DCM and has a fixed internal soft start.

4.5.1 HYPER LIGHT LOAD (HLL) MODE

In Continuous Conduction Mode (CCM), the inductor current can go negative at light loads. However, at light loads the MIC24097 is able to force the inductor current to operate in Discontinuous Conduction Mode (DCM) when the MIC24097 is set to HLL Mode. In HLL mode, the light-load efficiency is optimized by shutting down all the non-essential circuits and minimizing the supply current. The MIC24097 wakes up and turns on the high-side MOSFET when the feedback voltage VFB drops below 0.6V.

The MIC24097 has a zero-crossing comparator (ZC Detection) that monitors the inductor current by sensing the voltage drop across the low-side MOSFET during its ON-time. If V_{FB} > 0.6V and the inductor current goes slightly negative, then the MIC24097 automatically powers down most of the IC circuitry and goes into a low-power mode.

In DCM both the high-side and low-side MOSFETs are disabled, the load current is supplied by the output capacitors and V_{OUT} drops. If the drop of V_{OUT} causes V_{FB} to go below V_{REF}, then all the circuits will wake up into normal continuous mode. Figure 4-9 shows the control loop timing in discontinuous mode.

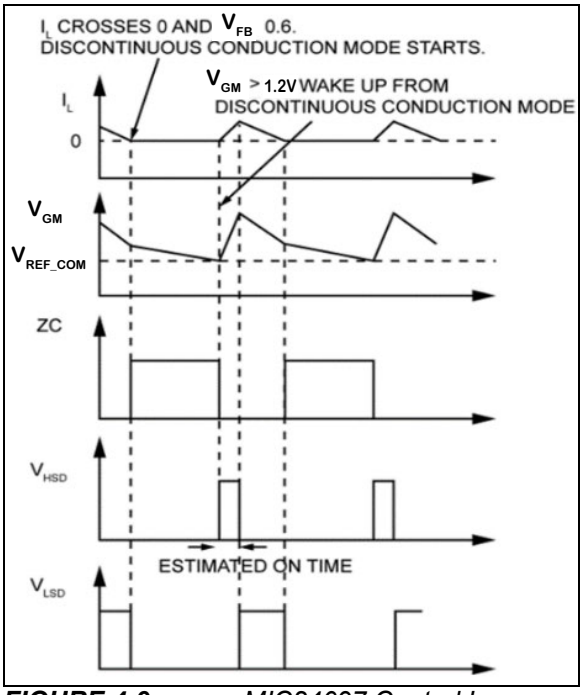


FIGURE 4-9: *MIC24097 Control Loop Timing (HLL Mode).*

In DCM, the bias current of most circuits is reduced. As a result, the total power supply current in DCM allows the MIC24097 to achieve high efficiency in light load applications.

4.5.2 CURRENT LIMIT

The MIC24097 uses the $R_{DS(ON)}$ of the low-side power MOSFET, or an additional sense resistor in series with the source of the low-side FET, to sense overcurrent conditions. The low-side power MOSFET $R_{DS(ON)}$ method will avoid the additional cost, board space and power losses incurred by a discrete current sense resistor. As shown in Figure 4-10, the current limit threshold can be programmed by connecting a resistor from the ILIM pin to AGND.

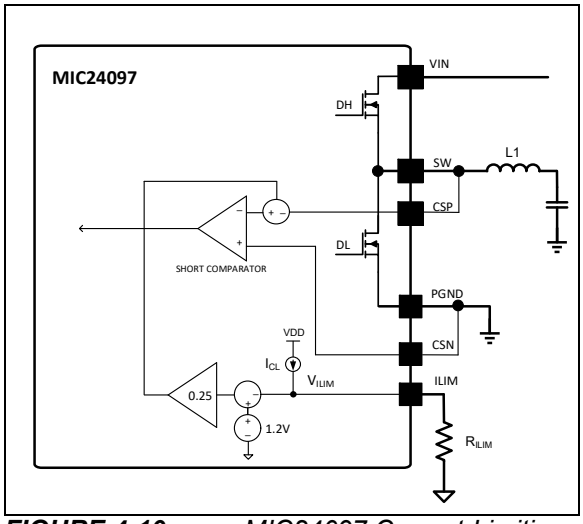


FIGURE 4-10: *MIC24097 Current-Limiting Circuit.*

The MIC24097 forces a constant current ICL of typically 9.6 µA through the ILIM pin to the resistor tied from the ILIM pin to ground to program V_{ILIM}. In each switching cycle of the MIC24097 converter, the inductor current is sensed by monitoring the low-side MOSFET during the OFF period. There is a 150 ns (typical) blanking period after which the current sense signal is considered for protection. The blanking period improves noise immunity. If the low-side MOSFET current is greater than the target ILIM threshold for 7 consecutive cycles, then the MIC24097 turns off the high-side MOSFET and a soft-start sequence is triggered. This mode of operation is called “hiccup mode” and its purpose is to protect the downstream load in case of a hard short.

The clock frequency during the current limit depends on the output voltage. If the output voltage is below the target level, which is true in most cases, the clock frequency is very high and is decided by the steady-state duty cycle. The time period is approximately 1/(steady state ON time + Minimum off time). If the output voltage is the same as the target voltage, the clock frequency is the same as the steady-state switching frequency.

Figure 4-11 illustrates the MIC24097 operation during overload conditions. When the load current is increased gradually, the inductor current also increases. When the load current is around the current limit threshold, the high-side and the low-side MOSFET currents can be higher than the current limit, as highlighted in Figure 4-11 as case #1. In case #1, even though the low-side MOSFET instantaneous current exceeds the current limit threshold for some duration, the low-side MOSFET current is lower than the current limit at the end of the blanking time of 150 ns. This causes the MIC24097 to not enter the current limit protection, and the next high-side MOSFET turn-on cycle is initiated normally. After the high-side MOSFET is turned on, the current ramps up to a value that is determined by the operating duty cycle and inductor value. When the high-side MOSFET is turned off and the low-side MOSFET is turned on, as shown in case #2 in Figure 4-11, the current through the low-side MOSFET is higher than the current limit after the blanking time of 150 ns, causing the MIC24097 to enter the current limit.

When the MIC24097 enters the current limit, both the high-side and low-side MOSFETs are turned off for a hiccup timeout of 2ms. The inductor current flows through the body diode of the low-side MOSFET until it reaches 0A. The MIC24097 initiates a soft start after the hiccup timeout, as shown in Figure 4-11.

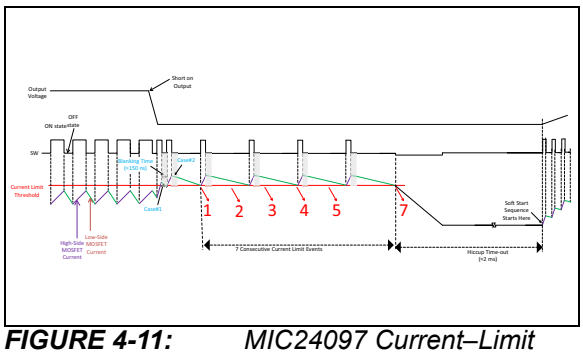


FIGURE 4-11: *MIC24097 Current–Limit Threshold Relationship to Output Current.*

The MIC24097 current limit needs to be temperature insensitive. Since MOSFET $R_{DS(ON)}$ increases by close to 50% from 25°C to 125°C, it was designed to use an external NTC resistor to program the current limit in this case. In the case where a precision sense resistor is used, no NTC resistance is needed.

To realize a positive temperature coefficient from the negative one of the NTC resistor, the current limit of the peak inductor current is internally generated using Equation 4-13 below:

EQUATION 4-13:

$$I_{LIM} = \frac{0.3V - 0.25V_{ILIM}}{R_{DS(ON)}}$$

$$I_{OUT\_CL} = I_{LIM} - \Delta I_L$$

Where:

- I_{LIM} = Inductor peak current
- ΔI_L = Inductor peak to peak ripple current
- $R_{DS(ON)}$ = On-resistance of the low-side power MOSFET

Equation 4-13 can be rearranged into Equation 4-14:

EQUATION 4-14:

$$V_{ILIM} = 1.2V - 4R_{DS(ON)} \times I_{LIM}$$

To program the target peak inductor current limit, the voltage across the current limit setting resistor RILIM is set to the VILIM value, i.e. I_{CL} x R_{ILIM} = V_{ILIM}. The R_{ILIM} resistance value can be calculated by the Equation 4-15 below:

EQUATION 4-15:

$$R_{ILIM} = \frac{1.2V - 4R_{DS(ON)} \times I_{LIM}}{I_{CL}}$$

Where:

I_{CL} = Current source for Current Limit = 9.6 µA

R_{ILIM} = CL programming resistor

Example:

Using (Equation 4-8)

$$I_{LIM} = 28A,\ R_{DS(ON)} @ 25°C = 2.3\ m\Omega$$

Using Equation 4-14 we can calculate V_{ILIM} @ 25°C

$$V_{ILIM} = 1.2V - 4 \times 28A \times 2.8\ m\Omega$$

$$V_{ILIM} = 1.2V - 257.6\ mV = 0.9424V$$

Using Equation 4-15, we calculate R_{ILIM}

$$R_{ILIM} = \frac{0.9424V}{9.6\ \mu A} = 92.33\ k\Omega$$

Choose standard value

$$R_{ILIM} = 98.16\ k\Omega @ 25°C$$

If the temperature increases to 125°C then

$$R_{DS(ON)} @ 25°C = 3.45\ m\Omega\ (50\%\ increase)$$

For the same 28A limit, we recalculate V_{ILIM} and R_{ILIM}:

$$V_{ILIM} = 0.8136V$$

$$R_{ILIM} = \frac{0.8136V}{9.6\ \mu A} = 84.75\ k\Omega$$

The current limit calculation at @ 25°C needs to be verified over temperature, to ensure Equation 4-14 and Equation 4-15 work correctly in the application.

A resistance network used in conjunction with an NTC resistor is highlighted in Figure 4-12.

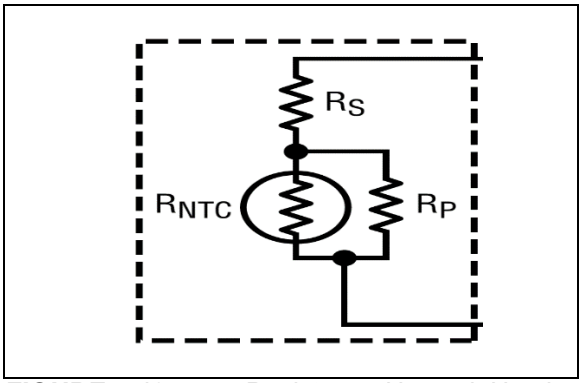


FIGURE 4-12: *Resistance Network Used with R_{NTC} Resistor to Program the Current Limit for Linearization and Fitting the Tempo of $R_{DS(ON)}$.*

4.5.3 NEGATIVE CURRENT LIMIT

MIC24097 supports cycle-by-cycle negative current limit. The absolute value of the negative current limit threshold is 50% of the programmed current limit. If the low-side MOSFET current is going to trigger negative current limit, the low-side MOSFET will be turned OFF and allow current through its body diode. During this time, the output voltage tends to rise because this protection limits current to discharge the output capacitors. To prevent overvoltage, the low-side FET is turned on after 500 ns, maintaining the negative current at the programmed level.

4.5.4 PVDD REGULATOR

The MIC24097 has an integrated high-voltage LDO that provides a 5V regulated output. The internal LDO powers VDD for the control circuitry and PVDD gate drive current. As shown in Figure 4-13, a 2Ω resistor is recommended between VDD and PVDD to filter the PVDD ripple reflecting back to VDD.

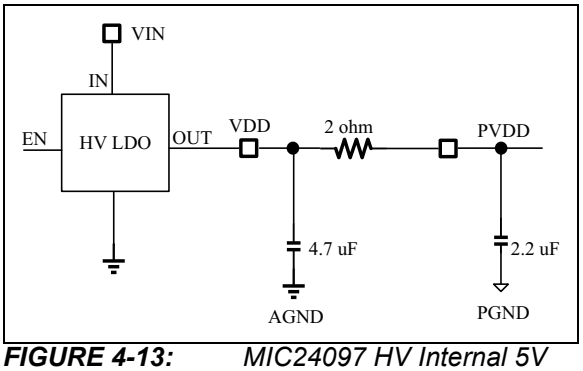


FIGURE 4-13: *MIC24097 HV Internal 5V Block.*

4.5.5 POWER GOOD (PG)

The Power Good (PG) pin is an open-drain output which indicates logic high when the output is nominally >92% of its steady state voltage. A pull-up resistor of more than 10 kΩ should be connected from PG to VDD.

4.5.6 PRECISION EN FUNCTION

The precision enable input (EN) is used to control the regulator. This feature allows simple sequencing of multiple power supplies with a resistor divider from another supply. Connecting this pin to ground or to a voltage less than 1.2V (typical) will turn off the regulator. The current drain from the input supply, in this state, is 25 µA (typical) at an input voltage of 12V. A voltage greater than 1.2 V (typical) is required to turn the regulator on. The hysteresis on this input is about 65 mV (typical) below the 1.2V (typical) threshold. When driving the enable input, the voltage must never exceed the absolute maximum specification for this pin. It is good practice to pull the EN input high when this feature is not used.

4.5.7 SEQUENCING

The MIC24097 has an EN pin, which is used to either enable/disable switching. When the EN pin threshold is higher than 1.2V, MIC24097 starts functioning. The internal regulator will power-up and start switching. Figure 4-14 shows the EN pin sequencing.

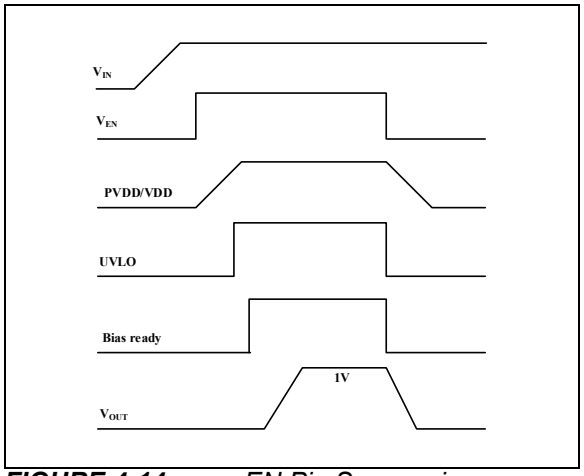


FIGURE 4-14: *EN Pin Sequencing.*

When the EN pin voltage is below 0.6V, the MIC24097 goes into shutdown mode, switching is halted and all internal control circuitry is switched OFF to reduce quiescent current. The EN pin, along with the PG pin, can be used for sequencing multiple MIC24097s. It is recommended to power-up VIN before EN signal.

4.5.8 NEGATIVE CURRENT LIMIT

MIC24097 supports a cycle-by-cycle negative current limit. The absolute value of the negative current limit threshold is 50% of the programmed current limit. If the low-side MOSFET current is going to trigger the negative current limit, the low-side MOSFET will be turned OFF and allow current to flow through its body diode. During this time, the output voltage tends to rise because this protection limits the current to discharge the output capacitors. In order to prevent overvoltage, the low-side FET is turned ON after 500 ns, maintaining the negative current at the programmed level.

EQUATION 4-16:

$$I_{NLIM} = \frac{I_{LIM}(Forward)}{2}$$

Where:

I_{NLIM} = Negative Current Limit
I_{LIM} = Forward Current Limit

4.5.9 PRE-BIAS STARTUP

In the case of pre-bias on the output, both the LSFET and HSFET are disabled from switching as the soft start (SS) ramps up. As shown in Figure 4-15, when the SS voltage reaches the FB pin pre-bias voltage level, the MOSFETs' switching is enabled. The output voltage then starts ramping up monotonically from the pre-biased voltage. This mechanism is active only during start-up; it is not active during load transients.

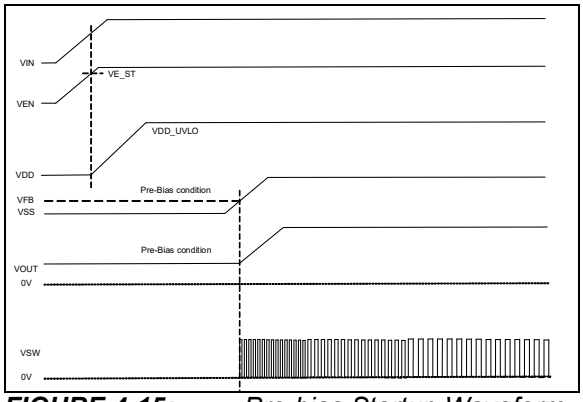


FIGURE 4-15: *Pre-bias Startup Waveform.*

4.5.10 UNDERVOLTAGE LOCKOUT (UVLO)

The MIC24097 device also incorporates an input undervoltage lock-out (UVLO) feature. This prevents the regulator from turning on when the input voltage is not high enough to properly bias the internal circuitry. The rising threshold is 4.2V (typ) while the falling threshold is 3.6V (typ). In some cases, these thresholds may be too low to provide good system performance. The solution is to use the EN input as an external UVLO to disable the part when the input voltage falls below a lower boundary. This is often used to

prevent excessive battery discharge or early turn-on during start-up. This method is also recommended to prevent abnormal device operation in applications where the input voltage falls below the minimum of 4.5 V. Figure 4-16 shows the connections to implement this method of UVLO. Equation 4-17 and Equation 4-18 can be used to determine the correct resistor values.

EQUATION 4-17:

$$R_{TOP} = R_{BOT} \times \left(\frac{V_{OFF}}{V_{EN}} - 1 \right)$$

EQUATION 4-18:

$$V_{ON} = V_{OFF} \times \left(\frac{V_{OFF} + V_{EN} HYST}{V_{EN}} \right)$$

Where:

V_{OFF} is the input voltage where the regulator shuts off.

V_{ON} is the voltage where the regulator turns on.

Due to the 6 µA pull-up, the current in the divider should be much larger than this. A value of 20 kΩ, for RBOT is a good first choice. Also, a Zener diode may be needed between the EN pin and ground in order to comply with the absolute maximum ratings on this pin.

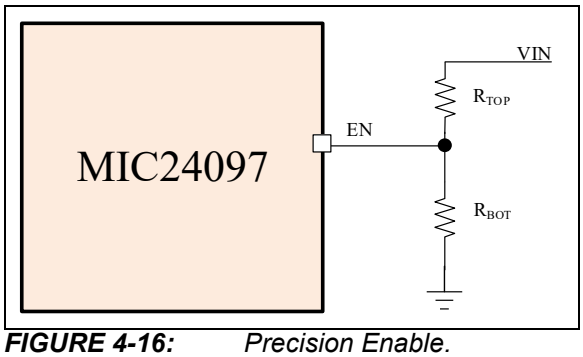


FIGURE 4-16: *Precision Enable.*

4.5.11 SWITCHING FREQUENCY

The switching frequency in CCM can be programmed by the equation below:

EQUATION 4-19:

$$R_{FREQ} = \frac{20.1 \times 10^9}{f_{SW}}$$

The switching frequency can be adjusted between 270 kHz and 800 kHz by changing the resistor between the FREQ pin and the AGND pins. The typical switching frequency vs. RFREQ curves are shown in Figure 4-17.

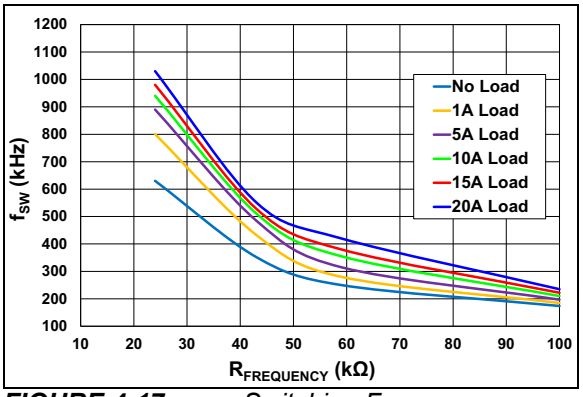


FIGURE 4-17: *Switching Frequency vs. R_{FREQ} (V_{IN} = 12V).*

4.5.12 THERMAL SHUTDOWN

When the junction temperature of the MIC24097 reaches ~160°C, the buck converter goes into thermal shutdown. When the junction temperature falls below ~140°C, the MIC24097 buck converter starts up with a soft start again.

4.5.13 ADAPTIVE VOLTAGE POSITIONING (AVP), ALSO KNOWN AS DROOP FUNCTION (CCM ONLY)

In some high-current applications, a requirement for a precisely controlled output impedance is imposed. This dependence of output voltage on load current is often termed, “droop”, “load line” regulation or Adaptive Voltage Positioning (AVP).

The basic functionality of the AVP function is to achieve a controlled output resistance for the buck regulator so that, at 0A load, the output is +Ɛ% higher than the nominal voltage and, at maximum load, the output is -Ɛ% in relation to the nominal output value, as shown in Figure 4-18.

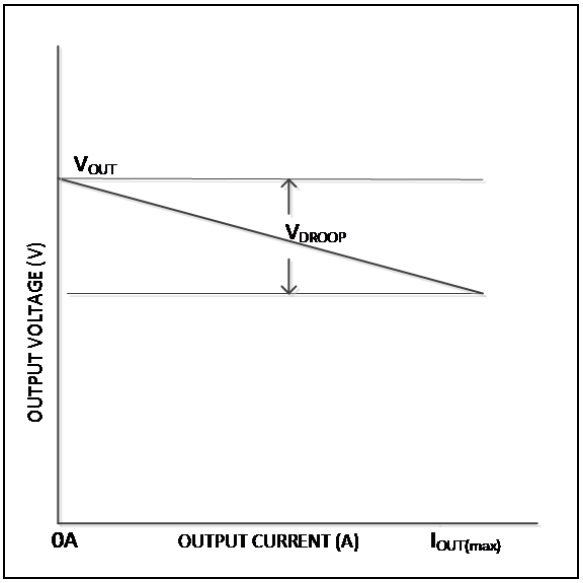


FIGURE 4-18: *AVP Ideal Output Resistive Characteristic.*

It is necessary to achieve the resistive characteristic over the full frequency range of output loads.

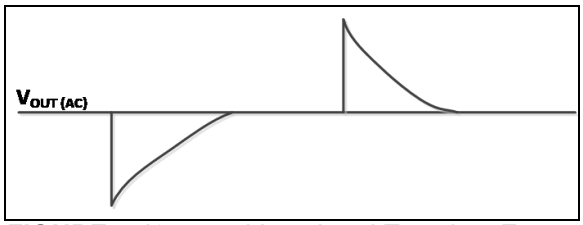


FIGURE 4-19: *V_{OUT} Load Transient Error without AVP/DROOP.*

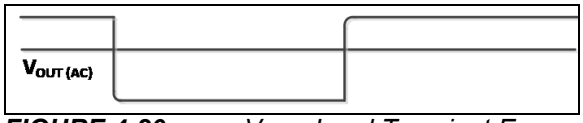


FIGURE 4-20: *V_{OUT} Load Transient Error with AVP/DROOP.*

Figure 4-19 and Figure 4-20 show how the AVP design window of ±Ɛ can be used to reduce the capacitance of the output capacitor necessary to sustain the load transient. Alternatively, the AVP can be used to improve the error of the load transient if it is decided to keep the same output capacitor.

The DROOP pin is an analog output that provides a voltage proportional to the output current in CCM, according to equation Equation 4-20.

EQUATION 4-20:

$$V_{DROOP} = V_{CSH} - 1.2V = 4R_{SENSE} \times I_L$$

Where:

V_{CSH} = Voltage at CSH Pin in CCM

R_{SENSE} = Current Sensing Resistance

I_L = Inductor Current per Phase

Because the current-sensing range is ±120 mV, the output voltage range of V_{DROOP} is 0V to 0.48V.

The schematic showing how to implement the AVP for a 5V output is found below.

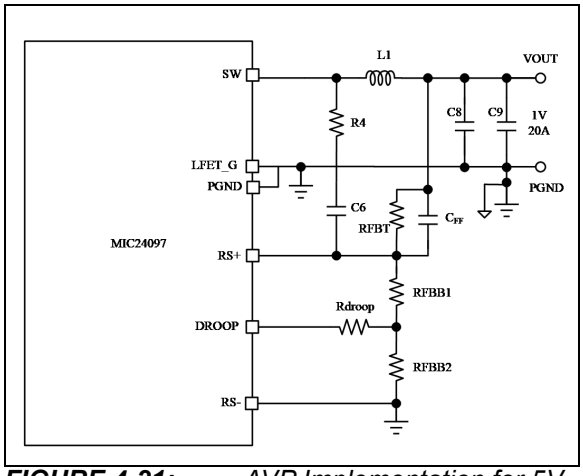


FIGURE 4-21: *AVP Implementation for 5V Output with 2% AVP Range for DROOP Pin Range 0V to 300 mV.*

The underlying assumption is that the current sense is done using sense resistors independent of temperature.

The sizing starts with the conditions: V_{DROOP} = 0V for I_{OUT} = 0A and V_{DROOP} = 300 mV for I_{OUT} = $I_{OUT(MAX)}$.

Depending on the voltage drop on the sense resistors at $I_{OUT(MAX)}$, the DROOP pin can have a value different than 300 mV, if $V_{DROOP(IOUTMAX)}$ = 300 mV.

Step 1: Size the resistors to get (1 + Ɛ) × V_{OUT} at I_{LOAD} = 0A. Due to V_{DROOP} = 0V, we have Equation 4-21.

EQUATION 4-21:

$$V_{OUT} = \left(1 + \frac{R_{FBT}}{R_{FBB1} + (R_{FBB2} \parallel R_{DROOP})}\right) \times V_{REF}$$

As a first approximation, consider choosing R_{FBB2} to be small enough so that $R_{FBB2} \parallel R_{DROOP} \approx R_{FBB2}$, and calculate R_{FBB1}, R_{FBB2} and R_{FBT} to get the correct 5.00V injection and stability.

Step 2: Size the resistors to have the trip of:

V_{OUT} × 2Ɛ from I_{OUT} = 0A to $I_{OUT} = I_{OUT(MAX)}$,

OR

from V_{DROOP} = 0V to V_{DROOP} = 300 mV.

Then,

EQUATION 4-22:

$$2\varepsilon = \frac{\Delta V_{FBS}}{V_{REF}} = \frac{V_{DROOP\_Max}}{V_{REF}} \times \frac{R_{FBB2}}{R_{FBB2} + R_{DROOP}} \times \frac{R_{FBT}}{R_{FBT} + R_{FBB1} + R_{FBB2} \parallel R_{DROOP}}$$

If $R_{DROOP} >> R_{FBB2}$, Equation 4-22 can be simplified to the following equations:

EQUATION 4-23:

$$2\varepsilon = \frac{V_{DROOP\_Max}}{V_{REF}} \times \frac{R_{FBB2}}{R_{FBB2} + R_{DROOP}} \times \frac{R_{FBT}}{R_{FBT} + R_{FBB1} + R_{FBB2}}$$

OR

EQUATION 4-24:

$$R_{DROOP} = R_{FBB2} \times \left(\frac{1}{2\varepsilon} \times \frac{V_{DROOP\_Max}}{V_{REF}} \times \frac{R_{FBT}}{R_{FBT} + R_{FBB1} + R_{FBB2}} - 1\right)$$

Step 3: The R_{FBB1} is slightly adjusted to get V_{OUT} × (1+Ɛ) for I_{OUT} = 0A. The result is shown in Figure 4-21.

Equation 4-23 and Equation 4-24 can also have an exact solution; the main difficulty is finding standard resistors of 0.1% that respect the initial positioning of +Ɛ for I_{OUT} = 0A and the 2×Ɛ move down for $I_{OUT(MAX)}$.

The example above was based on temperature independent current sensing, using sense resistors. In case the bottom FET is used, the V_{DROOP} is defined as:

EQUATION 4-25:

$$V_{DROOP} = V_{CSH} - 1.2V = 4R_{DSON(LS)} \times I_L$$

Where:

$R_{DSON(LS)}$ = Low-side MOSFET turn-on resistance

Considering the sensing current range of 120 mV, the maximum operating voltage value is:

EQUATION 4-26:

$$V_{DROOP} = 120\,mV \times 4 = 0.48V$$

$R_{DSON(LS)}$ increases to about 2x at 125°C compared to the value at 25°C; therefore, it is necessary to choose $R_{DSON} \times I_{OUT(MAX)}$ < 60 mV at 25°C to comply with the sensing range over temperature.

To desensitize the AVP to the temperature variation of RDSON, a resistance network with an NTC resistor needs to be used, as shown in the figure below.

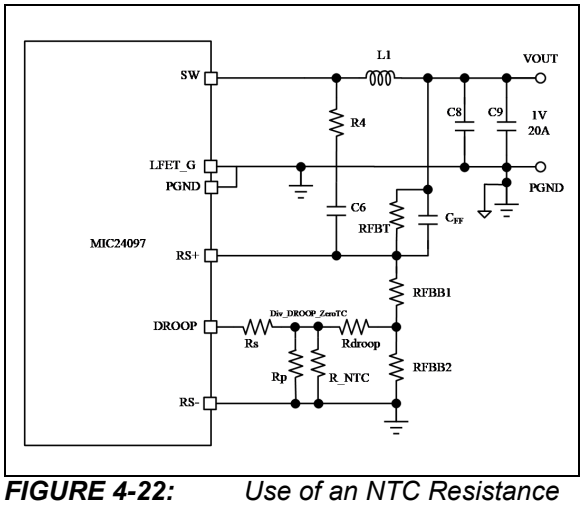


FIGURE 4-22: *Use of an NTC Resistance to Compensate the R_{DSON} Temperature Coefficient on the DROOP Pin.*

The above figure illustrates that increasing the D_{ROOP} voltage with temperature at the $I_{OUT(MAX)}$ (positive temperature coefficient) is compensated by the R_NTC (negative temperature coefficient) to keep the node of the divider, Div_DROOP_ZeroTC, constant regardless of temperature.

The rest of the calculations are similar to the aforementioned case, where the sensing current was temperature independent. If the AVP is not necessary, a 10 kΩ, 1 nF series RC filter to ground can be used to obtain a reading of the filtered output current.

5.0 APPLICATION INFORMATION

5.1 Output Voltage Setting

The output voltage can be adjusted using a resistor divider from output to AGND whose midpoint is connected to the FB pin, as shown in Figure 5-1.

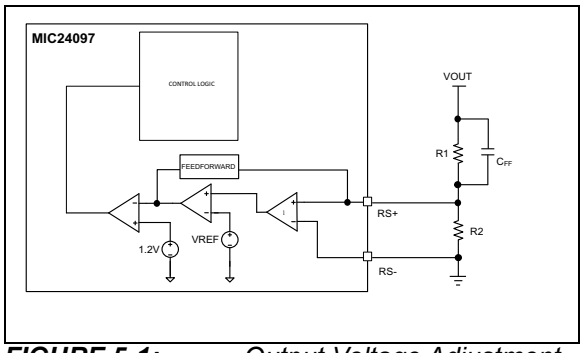


FIGURE 5-1: *Output Voltage Adjustment.*

The output voltage can be calculated using Equation 5-1.

EQUATION 5-1:

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R_1}{R_2}\right)$$

Where:

V_{REF} = 0.6V

The maximum output voltage that can be programmed using the MIC24097 is limited by the maximum duty cycle (see Equation 4-2).

A typical value of R_1 is less than 30 kΩ. If R_1 is too large, it may allow noise to be introduced into the voltage feedback loop and also increase the offset between the set output voltage and actual output voltage because of the error amplifier bias current. If R_1 is too small in value, it will decrease the efficiency of the power supply, especially at light loads. Once R_1 is selected, R_2 can be calculated using Equation 5-2.

EQUATION 5-2:

$$R_2 = \frac{R_1}{\frac{V_{OUT}}{V_{REF}} - 1}$$

5.2 Setting the Soft-start Time

The output soft-start time can be set by connecting a capacitor from SS to AGND, ranging from 2 ms to 100 ms, as shown in Figure 5-2.

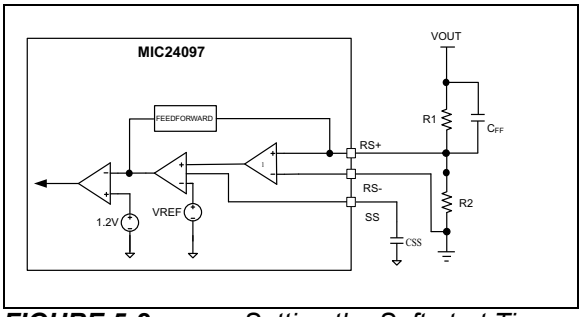


FIGURE 5-2: *Setting the Soft-start Time.*

The value of the capacitor can be calculated using Equation 5-3.

EQUATION 5-3:

$$C_{ss} = \frac{I_{ss} \times t_{ss}}{V_{REF}}$$

Where:

C_{SS} = Capacitor from SS pin to A_{GND}

I_{SS} = Internal soft start current (1.2 µA typ.)

t_{SS} = Output soft start time

V_{REF} = 0.6V

5.3 Inductor Selection

Inductance value, saturation and RMS currents are required to select the output inductor. The input and output voltages, as well as the inductance value, determine the peak-to-peak inductor ripple current.

The lower the inductance value, the higher the peak-to-peak ripple current through the inductor, which increases the core losses in the inductor. Higher inductor ripple current also requires more output capacitance to smooth out the ripple current. The greater the inductance value, the lower the peak-to-peak ripple current, which results in a larger and more expensive inductor.

A good compromise between size, loss and cost is to set the inductor ripple current to be equal to 25% of the maximum output current.

The inductance value is calculated using Equation 5-4.

EQUATION 5-4:

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times 0.25 I_{FL}}$$

Where:

V_{IN} = Input voltage
V_{OUT} = Output voltage
f_{SW} = Switching frequency
I_{FL} = Full load current

For a selected inductor, the peak-to-peak inductor ripple current can be calculated using Equation 5-5.

EQUATION 5-5:

$$\Delta I_{LPP} = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times L}$$

The peak inductor current is equal to the load current plus one-half of the peak-to-peak inductor current ripple, as shown in Equation 5-6.

EQUATION 5-6:

$$I_{LPK} = I_{LOAD} + \frac{\Delta I_{LPP}}{2}$$

The RMS and saturation current ratings of the selected inductor should be at least equal to the RMS current and saturation current calculated in the Equation 5-7.

EQUATION 5-7:

$$I_{LRMS} = \sqrt{I_{LOAD(MAX)}^2 + \frac{\Delta I_{LPP}^2}{12}}$$

Where:

$I_{LOAD(MAX)}$ = Maximum load current

Maximizing efficiency requires the proper selection of core material and minimizing the winding resistance. Use of ferrite materials is recommended in the higher switching frequency applications. Lower cost iron powder cores may be used but the increase in core loss reduces the efficiency of the power supply. This is especially noticeable at low output power. The winding resistance decreases efficiency at the higher output current levels. The winding resistance must be minimized, although this usually comes at the expense of a larger inductor. The power dissipated in the inductor is equal to the sum of the core and copper losses. At higher output loads, the core losses are usually insignificant and can be ignored. At lower output currents, the core losses can be a significant contributor. Core loss information is usually available from the vendor.

The amount of copper power loss in the inductor is calculated as shown in Equation 5-8.

EQUATION 5-8:

$$P_{INDUCTOR(CU)} = I_{LRMS}^2 \times R_{DCR}$$

5.4 Output Capacitor Selection

The main parameters for selecting the output capacitor are the capacitance value, voltage rating and RMS current rating. The type of the output capacitor is usually determined by its equivalent series resistance (ESR). Recommended capacitor types are ceramic, tantalum, low-ESR aluminum electrolytic, OS-CON and POS-CAP. The output capacitor ESR also affects the control loop from a stability point of view. The maximum value of ESR can be calculated using Equation 5-9.

EQUATION 5-9:

$$ESR \leq \frac{\Delta I_{OUTPP}}{\Delta I_{LPP}}$$

Where:

ΔI_{OUTPP} = Peak-to-peak output voltage ripple
ΔI_{LPP} = Peak-to-peak inductor current ripple

The required output capacitance to meet steady state output ripple can be calculated using Equation 5-10.

EQUATION 5-10:

$$C_{OUT} = \frac{\Delta I_{LPP}}{8 \times f_{SW} \times \Delta V_{OUTPP}}$$

Where:

C_{OUT} = Output capacitance
f_{SW} = Switching frequency

As described in Section 4.1, Control Architecture, the MIC24097 requires at least 40 mV peak-to-peak ripple at the FB pin to ensure that the GM amplifier and the comparator behave properly. Also, the output voltage ripple should be in phase with the inductor current. Therefore, the output voltage ripple caused by the output capacitor's value should be much smaller than the ripple caused by the output capacitor ESR. If low-ESR

capacitors, such as ceramic capacitors, are selected as the output capacitors, a ripple injection circuit should be used to provide the enough feedback voltage ripple. Refer to the Section 4.4, Ripple Injection for Ceramic Capacitors for details.

The voltage rating of the capacitor should be twice the output voltage for a tantalum and 20% greater for aluminum electrolytic, ceramic or OS-CON. The output capacitor RMS current is calculated in Equation 5-11.

EQUATION 5-11:

$$I_{COUT(RMS)} = \frac{\Delta I_{LPP}}{\sqrt{12}}$$

The power dissipated in the output capacitor is shown in Equation 5-12.

EQUATION 5-12:

$$P_{COUT} = I^2_{COUT(RMS)} \times ESR_{COUT}$$

5.5 Input Capacitor Selection

The input capacitor reduces peak current drawn from the power supply and reduces noise and voltage ripple on the input. The input voltage ripple depends on the input capacitance and ESR. The input capacitance and ESR values can be calculated using Equation 5-13.

EQUATION 5-13:

$$C_{IN} = \frac{I_{LOAD} \times D \times (1 - D)}{\eta \times f_{SW} \times \Delta V_{INC}}$$

$$ESR_{CIN} = \frac{\Delta V_{INESR}}{I_{LPK}}$$

Where:

I_{LOAD}	=	Load current
I_{LPK}	=	Peak inductor current
ΔV_{INC}	=	Input ripple due to input capacitance
ΔV_{INESR}	=	Input ripple on input capacitor ESR
η	=	Power conversion efficiency

The input capacitor should be rated for ripple current and voltage. The RMS value of the input capacitor current is determined by the maximum output current. The RMS current rating of the input capacitor should be greater than or equal to the input capacitor RMS current, calculated using Equation 5-14.

EQUATION 5-14:

$$I_{CIN(RMS)} = I_{LOAD(MAX)} \times \sqrt{D \times (1 - D)}$$

The power dissipated in the input capacitor is calculated using Equation 5-15.

EQUATION 5-15:

$$P_{CIN} = I^2_{CIN(RMS)} \times ESR_{CIN}$$

6.0 PCB LAYOUT GUIDELINES

Note:	To minimize EMI and output noise, follow these layout recommendations.

PCB layout is critical to achieve reliable, stable, and efficient performance. A ground plane is required to control EMI and minimize the inductance in power and signal return paths. Use star ground technique between AGND and PGND, and minimize trace length for high-current paths.

Follow these guidelines to ensure proper operation of the MIC24066/7 buck regulator.

6.1 Integrated Circuit

- The ceramic decoupling capacitor (2.2 µF minimum), connected to the VDD pin, must be located right at the IC. The VDD pin is very noise sensitive, so placement of the capacitor is critical. Use wide traces to connect to the VDD, PVDD and PGND pins.
- Connect the Analog Ground pin (AGND) directly to the ground planes. Do not route the AGND pin to the PGND pad on the top layer.
- Place the IC close to the Point of Load (POL).
- Use thick traces and minimize trace length for the input and output power lines.
- Keep the signal and power grounds separate and connected at only one location.

6.2 Input Capacitor

- Use parallel input capacitors to minimize effective ESR and ESL of the input capacitor.
- Place input capacitors next to the high-side power MOSFETs for each phase channel.
- Place the input capacitors on the same side of the board and as close to the IC as possible.
- Connect the V_{IN} supply to the VIN pin through a 1.2Ω resistor and connect a 1 µF ceramic capacitor from the VIN pin to the PGND pin. Keep both the VIN pin and GND connections short.
- Place several vias to the ground plane close to the input capacitor's ground terminal.
- Use either X7R or X5R dielectric input ceramic capacitors. Do not use Y5V or Z5U type capacitors.
- Do not replace the ceramic input capacitor with any other type of capacitor. Any additional other type of capacitor can be placed in parallel with the input capacitor.
- In "Hot-Plug" applications, use an Electrolytic bypass capacitor to limit the overvoltage spike seen on the input supply when power is suddenly applied.

6.3 Inductor

- Keep the inductor connection to the switch node (SW) short.
- Do not route any signal traces underneath or close to the inductor.
- Keep the switch node (SW) away from the feedback (FBS) pin.
- Connect the CSPx and CSNx pins directly to the drain and source of the low-side power MOSFET, respectively, and route the CSP and CSN traces together for each phase channel to accurately sense the voltage across the low-side MOSFET, achieving accurate current sensing.
- To minimize noise, place a ground plane under the inductor.
- The inductor can be placed on the opposite side of the PCB with respect to the IC. There should be sufficient vias on the power traces to conduct high current between the inductor, the IC and the output load. It does not matter whether the IC or the inductor is on the top or bottom, as long as there is enough heatsink and airflow to keep the power components within their temperature limits. Place the input and output capacitors on the same side of the board as the IC.

6.4 Output Capacitor

- Use a wide trace to connect the output capacitor ground terminal to the input capacitor ground terminal.
- The feedback trace should be separate from the power trace and connected as close as possible to the output capacitor. Sensing a long, high current load trace can degrade the DC load regulation

6.5 V_{OUT} Sense

- The sense traces must be routed close together or on adjacent layers to minimize noise pickup. The traces should be routed away from the switch node, inductors, MOSFETs and other high dv/dt or di/dt sources.

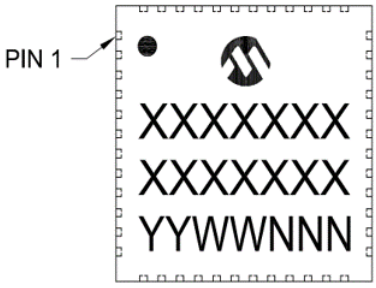
6.6 RC Snubber

- Place the RC snubber on either side of the board and as close to the SW pin as possible.

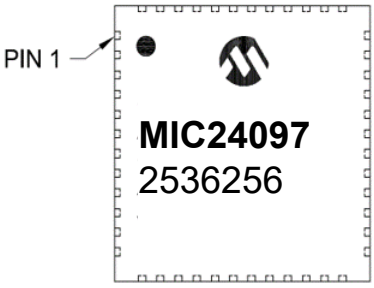
7.0 PACKAGING INFORMATION

7.1 Package Drawing

39-Pin 6 x 7 mm QFN



Example:

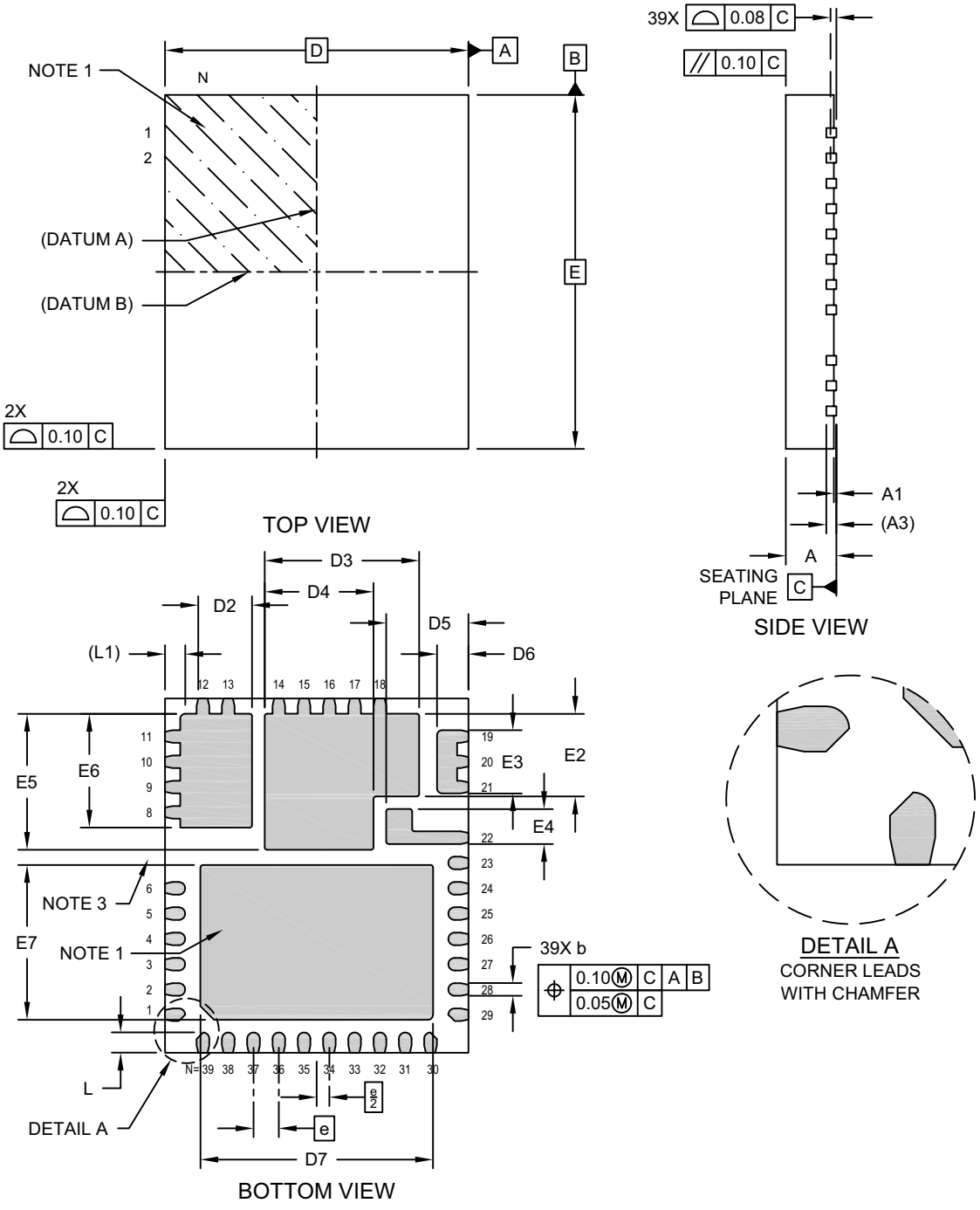


Legend:	XX...X	Product Code or Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or not include the corporate logo.

39-Lead Very Thin Quad Flat, No Lead Package (SJC) - 6x7x1.0 mm Body [VQFN] With Multiple Exposed Pads

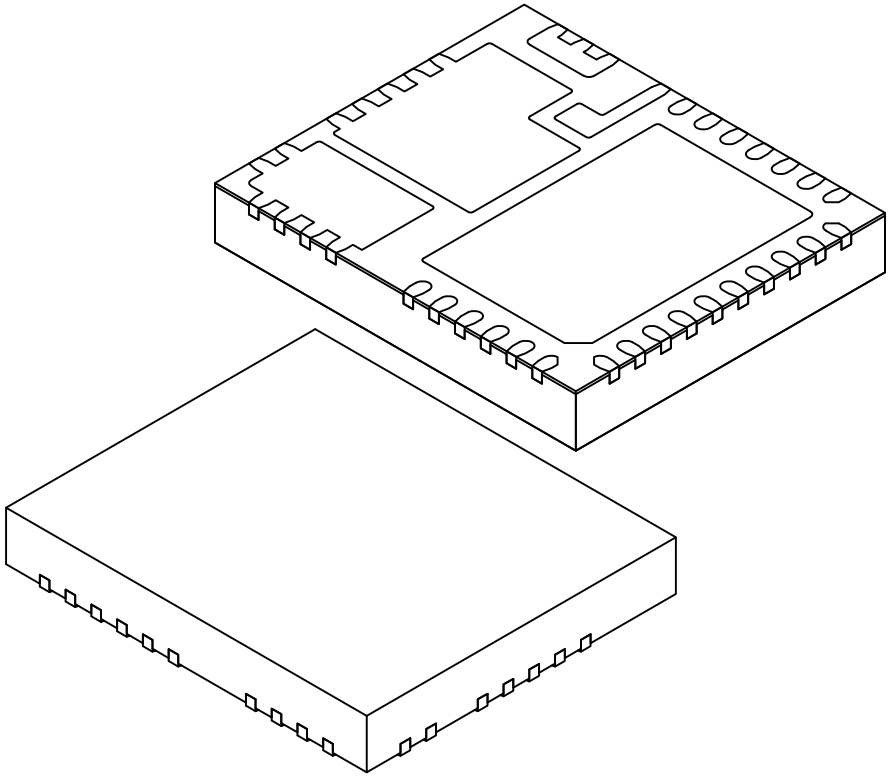
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-25645 Rev D Sheet 1 of 2

39-Lead Very Thin Quad Flat, No Lead Package (SJC) - 6x7x1.0 mm Body [VQFN] With Multiple Exposed Pads

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		39	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.20 REF	
Overall Length	D		6.00 BSC	
Exposed Pad Length	D2	1.32	1.42	1.52
Exposed Pad Length	D3	2.95	3.05	3.15
Exposed Pad Length	D4	2.05	2.15	2.25
Exposed Pad Length	D5	1.53	1.63	1.73
Exposed Pad Length	D6	0.52	0.62	0.72

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Exposed Pad Length	D7	4.50	4.60	4.70
Overall Width	E		7.00 BSC	
Exposed Pad Width	E2	1.53	1.63	1.73
Exposed Pad Width	E3	1.15	1.25	1.35
Exposed Pad Width	E4	0.59	0.69	0.79
Exposed Pad Width	E5	2.59	2.69	2.79
Exposed Pad Width	E6	2.15	2.25	2.35
Exposed Pad Width	E7	2.96	3.06	3.16
Terminal Width	b	0.18	0.25	0.30
Terminal Length	L	0.30	0.40	0.50
—	L1		0.30 REF	

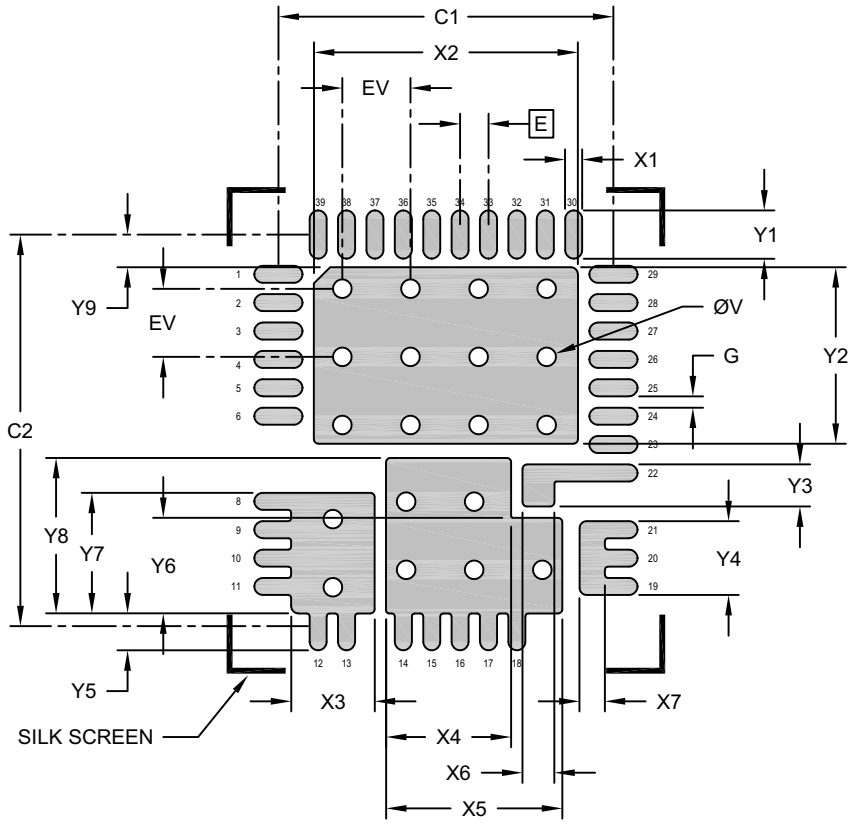
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Pin 7 is omitted.
4. Dimensioning and tolerancing per ASME Y14.5M.
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-25645 Rev D Sheet 2 of 2

39-Lead Very Thin Quad Flat, No Lead Package (SJC) - 6x7x1.0 mm Body [VQFN] With Multiple Exposed Pads

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Contact Pad Spacing	C1		5.90	
Contact Pad Spacing	C2		6.90	
Contact Pad Width	X1			0.30
Contact Pad Length	Y1			0.85
—	X2			4.65
—	X3			1.47
—	X4			2.20
—	X5			3.10
—	X6			0.56
—	X7			0.45

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
—	Y2			3.11
—	Y3			0.74
—	Y4			1.30
—	Y5			0.65
—	Y6			1.68
—	Y7			2.63
—	Y8			2.74
—	Y9			0.58
Contact Pad to Contact Pad	G	0.20		
Thermal Via Diameter	V		0.33	
Thermal Via Pitch	EV		1.20	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-27645 Rev D

APPENDIX A: REVISION HISTORY

Revision A (November 2024)

- Initial release of this document.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	[T]	-X	/XXX
Device	Tape and Reel	Temperature Range	Package

Device:	MIC24097:	20V, 20A High Performance Switching Buck Regulators
Tape and Reel Option(1):	(Blank) T	= Standard packaging (tube: 52/tube) = Tape and Reel[1] (3300/reel)
Temperature Range:	E	= -40°C to +125°C (Extended)
Package:	SJC	= Very Thin Quad Flatpack No-leads (VQFN) Package, Copper Clip, MP, EP\

Examples:

a) MIC24097-E/SJC: 20V, 20A High Performance Switching Buck Regulators, Extended Temperature Range, VQFN Package, Standard Packaging (Tube)

b) MIC24097T-E/SJC: 20V, 20A High Performance Switching Buck Regulators, Extended Temperature Range, VQFN Package, Tape and Reel

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

NOTES:

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