KSZ9131 EDS2 Daughter Card User's Guide

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Preface

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For the most up-to-date information on development tools, see the MPLAB® IDE online help. Select the Help menu, and then Topics to open a list of available online help files.

INTRODUCTION

This chapter contains general information that will be useful to know before using the KSZ9131 EDS2 Daughter Card User's Guide. Items discussed in this chapter include:

- Document Layout
- Conventions Used in this Guide
- Warranty Registration
- The Microchip Website
- Development Systems Customer Change Notification Service
- Customer Support
- Document Revision History

DOCUMENT LAYOUT

This document features the KSZ9131 EDS2 Daughter Card. The manual layout is as follows:

- **Chapter 1. "Overview"** – This chapter provides an overview of the KSZ9131 EDS2 Daughter Card and a brief description of the card's features.
- **Chapter 2. "Getting Started"** – This chapter provides information on the setup and operation of the KSZ9131 EDS2 Daughter Card.
- **Chapter 3. "Hardware"** – This chapter shows the different connection types found on the KSZ9131 EDS2 Daughter Card.
- **Chapter 4. "System Boot"** – This chapter explains how to utilize device tree overlays when booting the host system.
- **Appendix A. "Schematics"** – This section shows the schematic drawings of the KSZ9131 EDS2 Daughter Card.
- **Appendix B. "Bill of Materials"** – This section shows the Bill of Materials (BOM) for the KSZ9131 EDS2 Daughter Card.
- **Appendix C. "PCB Layers"** – This section shows the PCB layers of the KSZ9131 EDS2 Daughter Card.

CONVENTIONS USED IN THIS GUIDE

This manual uses the following documentation conventions:

DOCUMENTATION CONVENTIONS

Description	Represents	Examples
Arial font:		
Italic characters	Referenced books	*MPLAB® IDE User's Guide*
	Emphasized text	...is the *only* compiler...
Initial caps	A window	the Output window
	A dialog	the Settings dialog
	A menu selection	select Enable Programmer
Quotes	A field name in a window or dialog	"Save project before build"
Underlined, italic text with right angle bracket	A menu path	*File>Save*
Bold characters	A dialog button	Click **OK**
	A tab	Click the **Power** tab
N'Rnnnn	A number in verilog format, where N is the total number of digits, R is the radix and n is a digit.	4'b0010, 2'hF1
Text in angle brackets < >	A key on the keyboard	Press <Enter>, <F1>
Courier New font:		
Plain Courier New	Sample source code	`#define START`
	Filenames	`autoexec.bat`
	File paths	`c:\mcc18\h`
	Keywords	`_asm, _endasm, static`
	Command-line options	`-Opa+, -Opa-`
	Bit values	`0, 1`
	Constants	`0xFF, 'A'`
Italic Courier New	A variable argument	*`file`*`.o`, where *`file`* can be any valid filename
Square brackets [ ]	Optional arguments	`mcc18 [options]` *`file`* `[options]`
Curly brackets and pipe character: { | }	Choice of mutually exclusive arguments; an OR selection	`errorlevel {0|1}`
Ellipses...	Replaces repeated text	`var_name [, var_name...]`
	Represents code supplied by user	`void main (void) { ... }`

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- **General Technical Support** – Frequently Asked Questions (FAQs), technical support requests, online discussion groups, Microchip consultant program member listing
- **Business of Microchip** – Product selector and ordering guides, latest Microchip press releases, listing of seminars and events, listings of Microchip sales offices, distributors and factory representatives

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- **Emulators** – The latest information on Microchip in-circuit emulators.This includes the MPLAB REAL ICE and MPLAB ICE 2000 in-circuit emulators.
- **In-Circuit Debuggers** – The latest information on the Microchip in-circuit debuggers. This includes MPLAB ICD 3 in-circuit debuggers and PICkit 3 debug express.
- **MPLAB IDE** – The latest information on Microchip MPLAB IDE, the Windows Integrated Development Environment for development systems tools. This list is focused on the MPLAB IDE, MPLAB IDE Project Manager, MPLAB Editor and MPLAB SIM simulator, as well as general editing and debugging features.
- **Programmers** – The latest information on Microchip programmers. These include production programmers such as MPLAB REAL ICE in-circuit emulator, MPLAB ICD 3 in-circuit debugger and MPLAB PM3 device programmers. Also included are nonproduction development programmers such as PICSTART Plus and PIC-kit 2 and 3.

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- Local Sales Office
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Technical support is available through the website at:
http://www.microchip.com/support

DOCUMENT REVISION HISTORY

Revisions	Section/Figure/Entry	Correction
DS50003773A (11-26-24)	All	Initial release

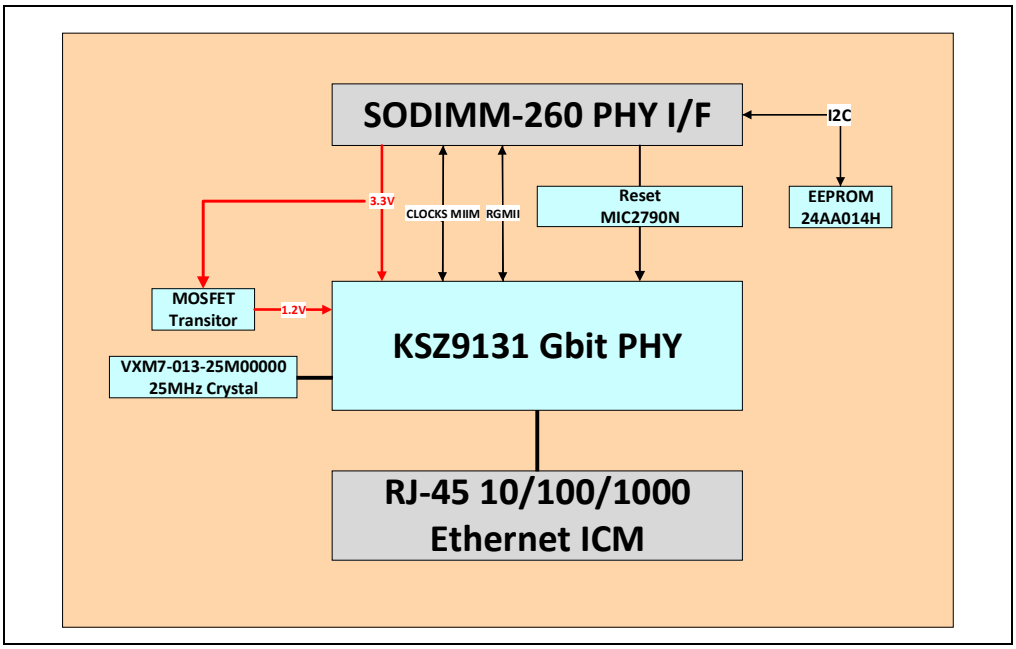
Chapter 1. Overview

1.1 INTRODUCTION

The KSZ9131 EDS2 Daughter Card is designed for evaluation of the Microchip KSZ9131 Gigabit Ethernet RGMII PHY when used with a Microchip EDS2-compatible host board. A SODIMM 260-pin connector for the EDS2 Host - KSZ9131 EDS2 Daughter Card Interface is used due to its high performance, high pin count, and low cost.

This document describes the KSZ9131 EDS2 Daughter Card setup and user interface features. A simplified block diagram is shown in Figure 1-1.

FIGURE 1-1: KSZ9131 EDS2 DAUGHTER CARD BLOCK DIAGRAM



1.2 FEATURES

Below are the features of the KSZ9131 EDS2 Daughter Card:

- Microchip KSZ9131 Gigabit Ethernet Transceiver with RGMII
- Microchip VXM7-9013-25M0000 crystal for 25 MHz
- Microchip MIC2790N Reset supervisor with Reset LED indicator
- Microchip 24AA014H I^2C Serial EEPROM for board identification
- 10/100/1000 Mb RJ45 Integrated Connector and Magnetics with LEDs
- MDC/MDIO Management Interface
- Compliant with the SODIMM EDS2 Interface Specification
- PHY Reset DIP switch feature to keep the KSZ9131 in Reset, useful for development
- Test points for GPIOs, Power rails, and GND

1.3 REFERENCES

Concepts and materials available in the following documents may be helpful when reading this document. Visit www.microchip.com for the latest documentation.

- *KSZ9131 Data Sheet*
- *KSZ9131 EDS2 Daughter Card Schematic*
- *KSZ9131 EDS2 Daughter Card Hardware Design Checklist*
- *KSZ9131 EDS2 Daughter Card User's Guide*
- *EDS2 SODIMM IF Development Guide*

1.4 ACRONYMS AND DEFINITIONS

Table 1-1 shows the terms used in this user guide.

TABLE 1-1: ACRONYMS AND DEFINITIONS

Term	Definition
ARP	Address Resolution Protocol
COM	Communications Port
DHCP	Dynamic Host Configuration Protocol
DIP	Dual In-line Package
DSUB	D - Subminiature
EP	Extended Page
GPIO	General Purpose Input/Output
ICM	Integrated Connector Magnetic
IEEE	Institute of Electrical and Electronics Engineers
I/O	Input/Output
IP	Internet Protocol
LAN	Local Area Network
LSB	Least Significant Byte/Bit
MAC	Media Access Controller
MDIO	Management/Data Input/Output
MII	Media Independent Interface
NIC	Network Interface Card
OUI	Organizationally Unique Identifier
PC	Personal Computer
PCB	Printed Circuit Board

TABLE 1-1: ACRONYMS AND DEFINITIONS (CONTINUED)

Term	Definition
PCS	Physical Coding Sublayer
PHY	Physical Layer Transceiver
USB	Universal Serial Bus
QSGMII	Quad Serial Gigabit Media Independent Interface
SGMII	Serial Gigabit Media Independent Interface
SODIMM	Small Outline Dual In-line Memory Module

NOTES:

Chapter 2. Getting Started

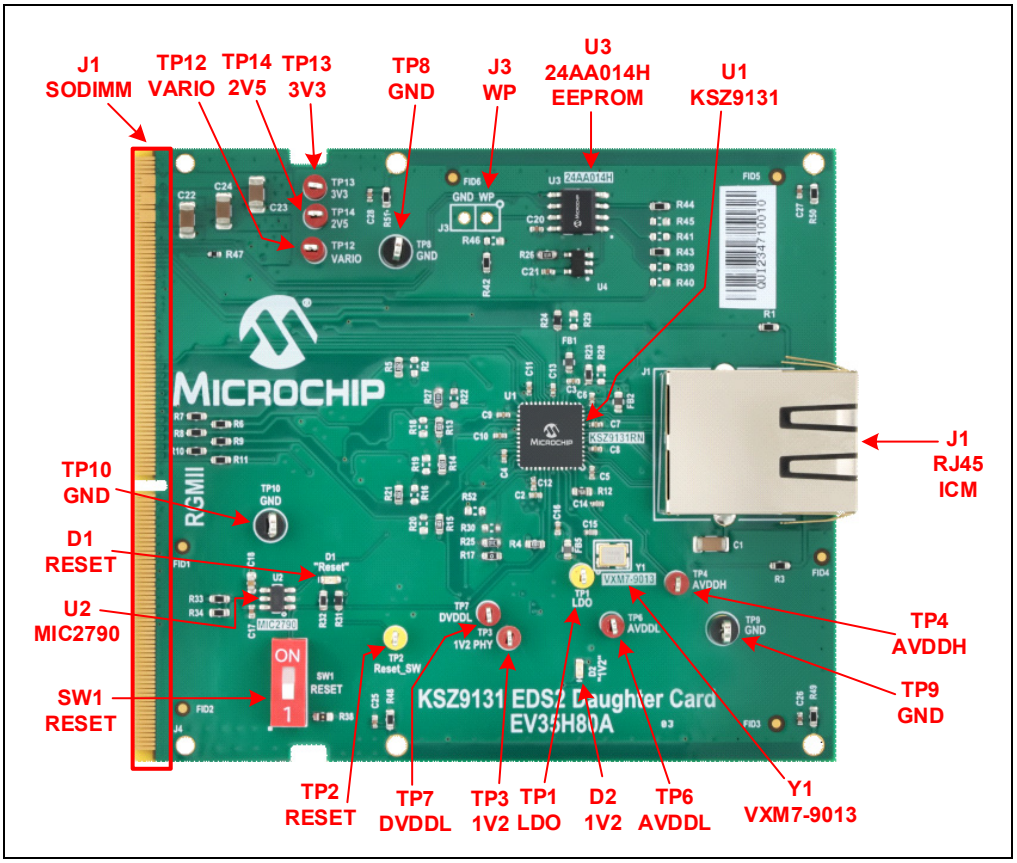
2.1 INTRODUCTION

This chapter provides a quick start guide for using the KSZ9131 EDS2 Daughter Card.

2.2 KSZ9131 EDS2 DAUGHTER CARD INSTALLATION

Figure 2-1 shows the KSZ9131 EDS2 Daughter Card key components, connectors, and test points.

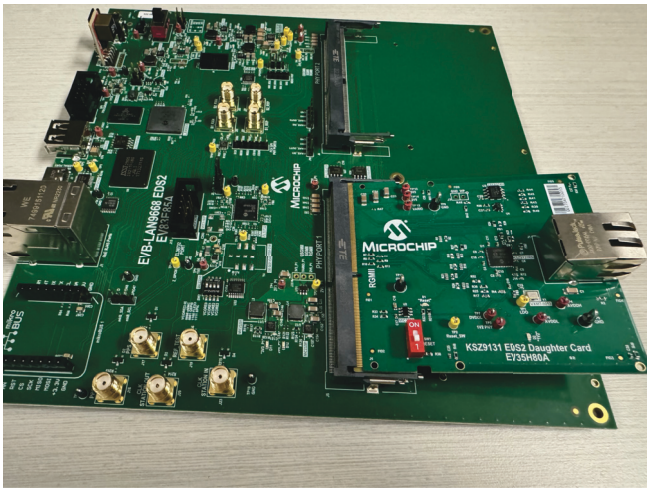
FIGURE 2-1: KSZ9131 EDS2 DAUGHTER CARD



Perform the following steps to install the KSZ9131 EDS2 Daughter Card in the SODIMM EDS2 connector:

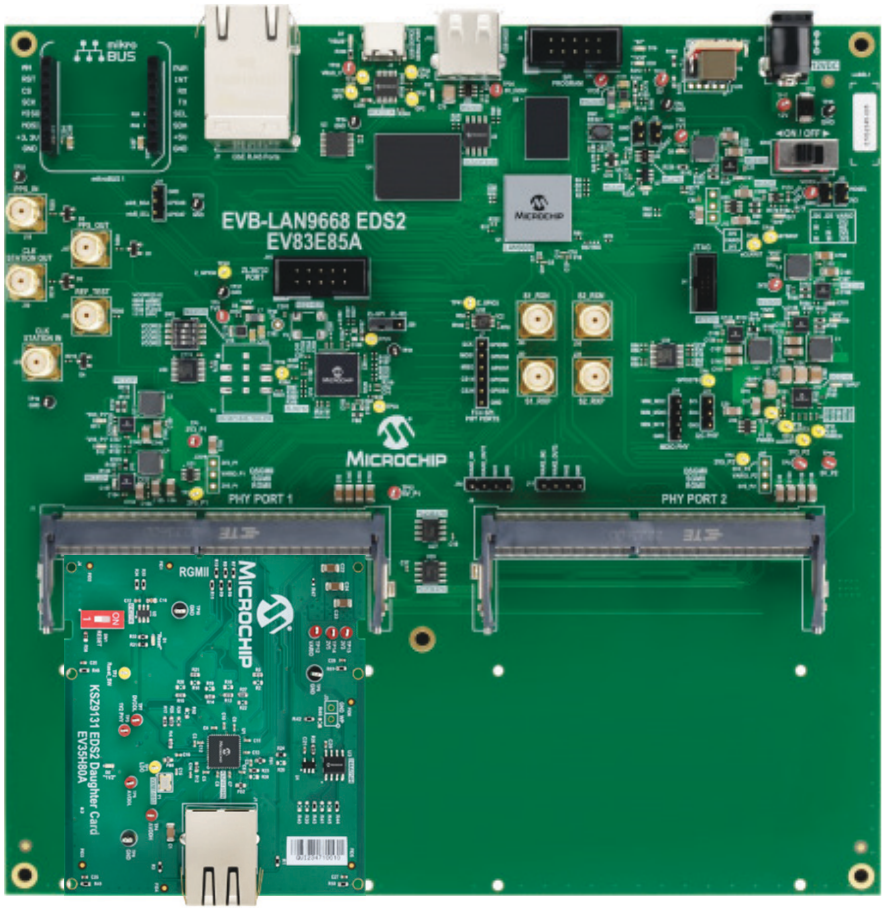
1. Verify that the host board power is OFF.
2. Grab the daughter card by its board edges. Align to SODIMM EDS2 receptacle and insert the edge of the board fingers at a 45-degree angle into the SODIMM connector as shown in Figure 2-2.

FIGURE 2-2: KSZ9131 EDS2 DAUGHTER CARD INSTALLATION



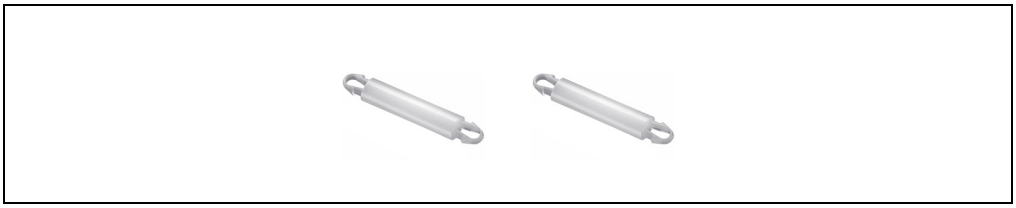
3. Push daughter card down until it latches into the SODIMM receptacle.
4. After installation, the boards should look as shown in Figure 2-3.

FIGURE 2-3: EVB-LAN9668 EDS2 WITH KSZ9131 EDS2



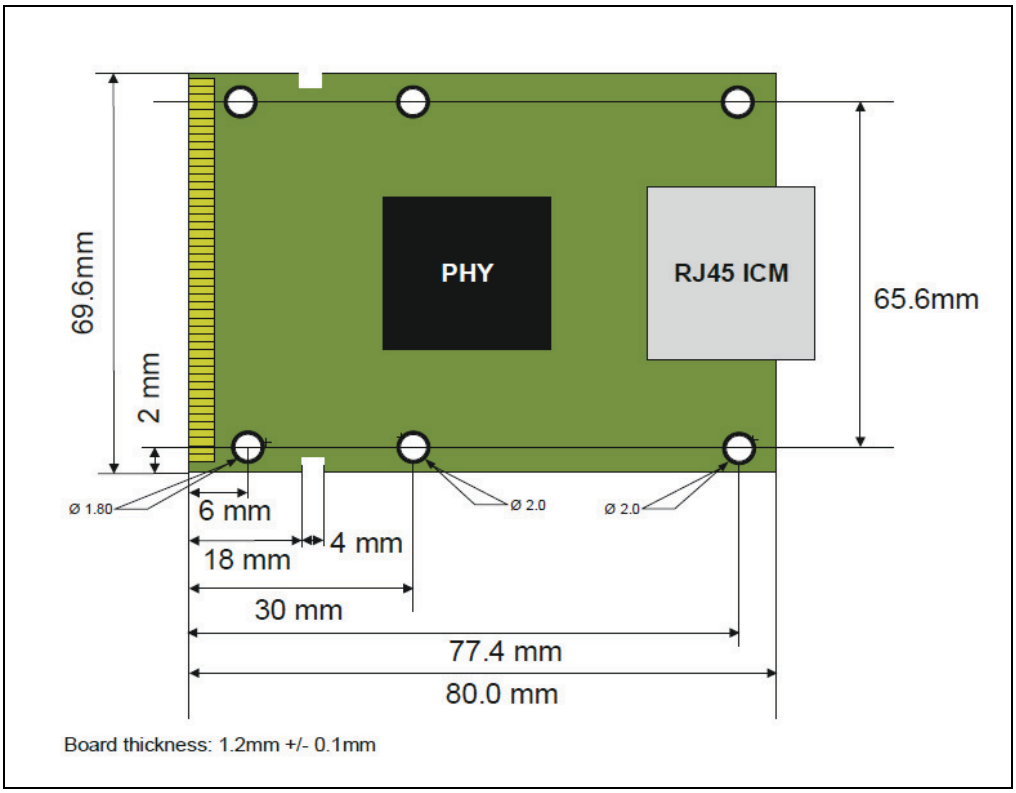
5. (Optional step) Secure the board with two snap lock pins (Wurth Elektronik part number 709652500). These pins prevent board movement and remove stress from the SODIMM connector due to the RJ45 cable weight and movement. See Figure 2-4.

FIGURE 2-4: SNAP LOCK PINS



6. The KSZ9131 EDS2 Daughter Card has four (4) snap lock mounting holes, two (2) at 30 mm from the edge of the board fingers, and two (2) at 77.4 mm from the edge of the board fingers as shown in Figure 2-5. If the EDS2 host has mounting holes at 77.4 mm, use those. Otherwise, use the ones at 30 mm.

FIGURE 2-5: KSZ9131 EDS2 DAUGHTER CARD SNAP LOCK MOUNTING HOLES



7. To use the snap lock pins, first install the snap lock pins on the host board. Then, insert the daughter card into the SODIMM EDS2 receptacle. Align the snap locks with the corresponding mounting holes and press the daughter card down until snap locks are fastened. A pair of long-nose pliers can be used to close the pin locks for easy board installation and removal.

2.3 QUICK START WITH EVB-LAN9668 EDS2 BASEBOARD

Perform the following steps to start using the KSZ9131 EDS2 Daughter Card:

1. Verify if the SW1 slide switch is set as shown in Figure 2-6.

FIGURE 2-6: SW1 SLIDE SWITCH

2. Connect a USB-C serial cable to EVB-LAN9668 EDS2 and host PC for the terminal console.
3. Connect a 12V supply with a DC plug to EVB-LAN9668 EDS2.
4. Power-Up the EVB-LAN9668 EDS2 host board.
5. Connect the Ethernet cable to the RJ45 connector on the KSZ9131 EDS2 Daughter Card.
6. See **Chapter 4. "System Boot"** for details of the boot process.

Note: The KSZ9131 EDS2 Daughter Card is also compatible with other EDS2 baseboards. However, the start-up sequence may vary. Refer to the documentation for the specific baseboard being used for more details.

2.4 KSZ9131 EDS2 DAUGHTER CARD REMOVAL

To remove the KSZ9131 EDS2 Daughter Card from the SODIMM EDS2 receptacle:

1. Verify that the host board power is OFF.
2. Disconnect the RJ45 cable.
3. If snap locks are used, release them from the daughter card. A pair of long-nose plier can be used to close the latch pins for easy release.
4. Gently pull the SODIMM receptacle arms away from the daughter card; it should snap upwards.
5. Grab the daughter card by its edges and remove it from the SODIMM EDS2 receptacle.

Chapter 3. Hardware

3.1 INTRODUCTION

This section provides a description of the KSZ9131 EDS2 Daughter Card hardware, including headers, test points, LEDs, and switches on the board.

The top side and bottom side of the KSZ9131 EDS2 Daughter Card are shown in Figure 3-1 and Figure 3-2, respectively.

FIGURE 3-1: KSZ9131 EDS2 DAUGHTER CARD (TOP SIDE)

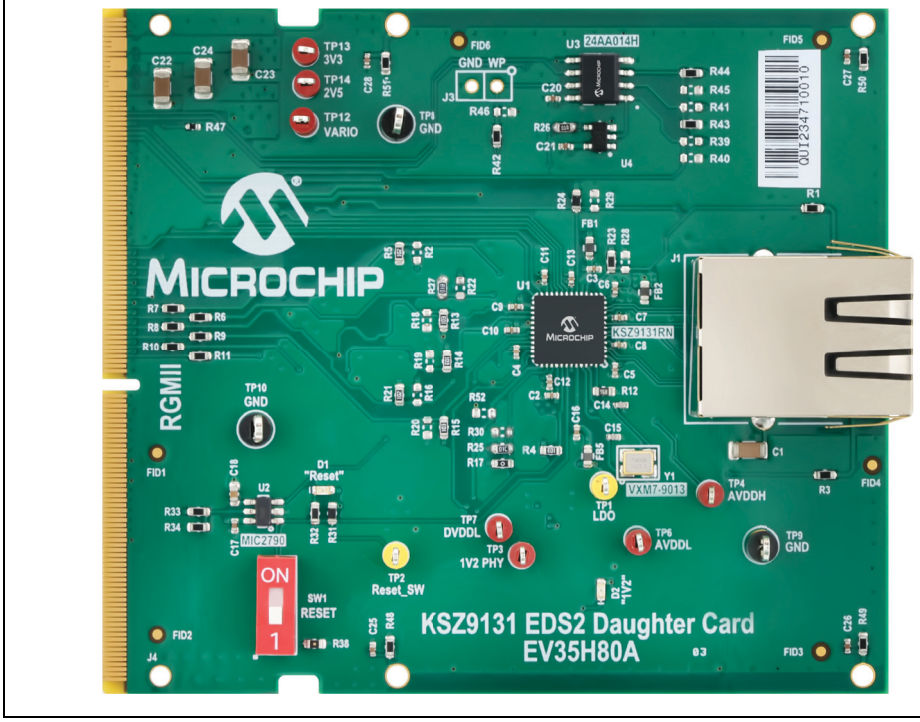
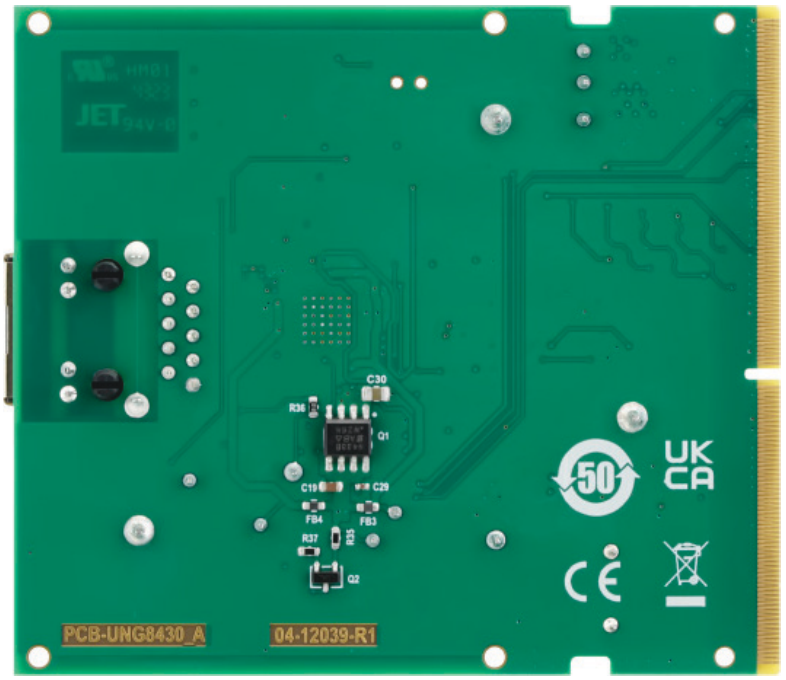


FIGURE 3-2: KSZ9131 EDS2 DAUGHTER CARD (BOTTOM SIDE)



3.2 CONNECTORS

Table 3-1 describes the connectors on the KSZ9131 EDS2 Daughter Card.

TABLE 3-1: KSZ9131 EDS2 DAUGHTER CARD CONNECTORS

Reference Designator	Name	Description
J1	RJ45 ICM	Ethernet RJ45 1Gb connector with integrated magnetics.
J3	WP Header 1x2	EEPROM Write Protect footprint (header not installed). Used to disable write protection during factory programming.
J4	SODIMM-260 pin Edge Connector	Provides power and signals for operation. Connects to Microchip EDS2 compatible host.

3.3 TEST POINTS

Table 3-2 lists the test points on the KSZ9131 EDS2 Daughter Card.

TABLE 3-2: KSZ9131 EDS2 DAUGHTER CARD TEST POINTS

Test Point	Color	Description
TP1	Yellow	LDO
TP2	Yellow	Reset_SW
TP3	Red	1V2
TP4	Red	AVDDH
TP6	Red	AVDDL
TP7	Red	DVDDL

TABLE 3-2: KSZ9131 EDS2 DAUGHTER CARD TEST POINTS (CONTINUED)

Test Point	Color	Description
TP8	Black	GND
TP9	Black	GND
TP10	Black	GND
TP12	Red	VARIO
TP13	Red	3V3
TP14	Red	2V5

3.4 LEDS

Table 3-3 describes the LEDS on the KSZ9131 EDS2 Daughter Card.

TABLE 3-3: KSZ9131 EDS2 DAUGHTER CARD LEDS

Reference Designator	Name	Description
D1	RESET	Red LED RESET indicator
D2	1V2	Green LED 1V2 indicator
J1 - Left	RJ45 - Left	Green LED connected to KSZ9131 LED1/AD0
J1 - Right	RJ45 - Right	Yellow LED connected to KSZ9131 LED2/AD1

3.5 CONFIGURATION STRAPS

Table 3-4 lists the configuration straps on the KSZ9131 EDS2 Daughter Card.

TABLE 3-4: KSZ9131 EDS2 DAUGHTER CARD CONFIGURATION STRAPS

Reference Designator PU/PD	Name	Description
R22/R27*	PHYAD2	0* – AD2 = 0 1 – AD2 = 1
R23*/R28	PHYAD1	This connects to external signal PHYID to support two daughter cards on the same EDS2 host.
R24*/R29	PHYAD0	0 – AD0 = 0 1* – AD0 = 1
R25*/R30	ALLPHYADD	0 – Responds to PHY address 0 1* – Does not respond to PHY address 0
R13*/R18	MODE3	MODE[3:0] 1100 – 10/100 FDX/HDX, 100BT Full (RGMII) For details in other modes, see data sheet.
R14*/R19	MODE2	
R15*/R20	MODE1	
R16/R21*	MODE0	
R2*/R5	CLK125_EN	0 – 125 MHz clock output on pin 33 disabled 1* – 125 MHz clock output on pin 33 enabled
R4*	LED_MODE	0 – Tri-color LED 1* – Individual LED

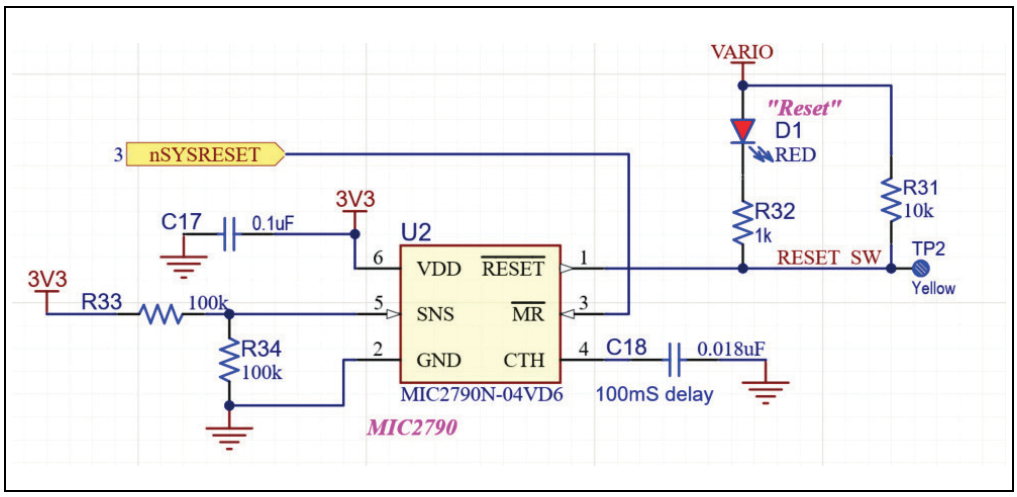
Note 1: Only one of the two PU/PD resistors is installed.

2: * indicates default.

3.6 RESET

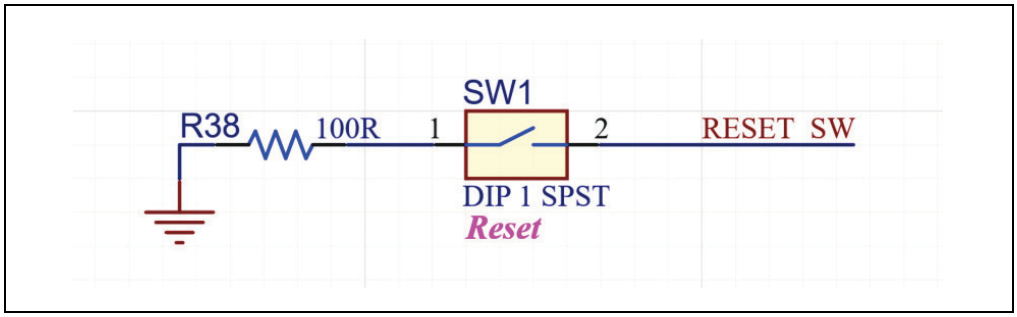
The KSZ9131 EDS2 Daughter Card includes a Reset circuit using the Microchip MIC2790 Reset supervisor as shown in Figure 3-3. The system Reset signal, nSYSRESET, is driven from the SODIMM EDS2 host interface and is connected to the MIC2790 master Reset input MR. When MR goes low, the MIC2790 Reset output on net RESET_SW goes low, resetting the KSZ9131 and turning on the Reset LED D2. The RESET_SW net will go high 100 milliseconds after nSYSRESET goes high, turning the Reset LED off and releasing the KSZ9131 from Reset. The configuration straps are sampled when RESET_SW goes high.

FIGURE 3-3: KSZ9131 EDS2 DAUGHTER CARD RESET CIRCUIT



The Reset switch SW1, as shown in Figure 3-4, can be used to place the KSZ9131 EDS2 Daughter Card in Reset without affecting the rest of the system. This is useful when testing and updating the KSZ9131 Linux® driver after the system has booted up.

FIGURE 3-4: KSZ9131 EDS2 RESET SWITCH SW1



3.7 CLOCKS

The KSZ9131 EDS2 Daughter Card uses a Microchip VXM7-9013-25M0000 25 MHz crystal for the KSZ9131 clock reference.

The KSZ9131 generates a 125 MHz clock for Synchronous Ethernet (SyncE) applications. The clock is buffered with a Microchip PL102-10TC buffer to drive to the SODIMM EDS2 connector.

3.8 POWER

The KSZ9131 EDS2 Daughter Card requires 3.3V, 2.5V, and 1.2V. The EDS2 SODIMM EDS2 interface provides 3.3V, 2.5V, and VARIO (3.3V or 2.5V). The KSZ9131 LDO is driven through a MOSFET to generate the 1.2V required by the KSZ9131 analog, digital core, and PLL power inputs.

3.9 KSZ9131 EDS2 DAUGHTER CARD EEPROM

The KSZ9131 EDS2 Daughter Card includes a Microchip 24AA014H EEPROM with half array write protection (40H to 7Fh) for identification. Only some locations in the protected area starting at 40h are programmed as shown in Figure 3-5. Details on these fields are specified in Table 3-5.

FIGURE 3-5: KSZ9131 EDS2 DAUGHTER CARD EEPROM CONTENTS

```
Offset(h)  00 01 02 03 04 05 06 07 08 09 0A 0B 0C 0D 0E 0F
00000000   FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF
00000010   FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF
00000020   FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF
00000030   FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF
00000040   A3 01 00 01 0A 00 91 31 01 00 45 56 31 36 54 36
00000050   30 41 41 30 FF FF FF FF FF FF FF FF FF FF FF FF
00000060   FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF
00000070   FF FF FF FF FF FF FF FF FF FF FF FF AA 00 00 AA
```

TABLE 3-5: KSZ9131 EDS2 DAUGHTER CARD EEPROM

Byte Address	Name	Type	Description
40	KEY	INT	Magic number = A3h
41	REV	INT	EEPROM Revision
42	DCTYPE	INT	Daughter Card type: 0 = PHY, 1 = SWITCH
43	NPORTS	INT	Number of ports
44	MACIF	INT	MAC Interface: RMII 07h RGMII 09h RGMII_ID 0Ah RGMII_RXID 0Bh RGMII_TXID 0Ch SGMII 04h QSGMII 13h
45	DPN_PNUM	INT	Device Part number: 23:20 Product Family 0 - KSZ 1 - LAN 2 - VSC 19:16 Part Number upper 4 bits
46			Device Part number bits 15:8
47			Device Part number bits 7:0

TABLE 3-5: KSZ9131 EDS2 DAUGHTER CARD EEPROM (CONTINUED)

Byte Address	Name	Type	Description
48	CTRLIF	INT	Control interface: 7:5 Reserved 4:3 SPI Mode 2 SPI Control available 1 I^2C Control available 0 MIIM Control available
49	SPIR	INT	SPI rate
4A	DEVT	ASCII	Dev Tools Part number
4B			
4C			
4D			
4E			
4F			
50			
51			
52	BREVU	ASCII	UNG Board Revision Letter
53	BREVD	ASCII	Dev Tools Board Revision Number
7C	IDBYTE0	INT	ID BYTE 1 = AAh
7D	IDBYTE1	INT	ID BYTE 2 = 00h
7E	IDBYTE2	INT	ID BYTE 3 = 00h
7F	CHECKSUM	INT	CHECKSUM = AAh

Chapter 4. System Boot

4.1 INTRODUCTION

This chapter describes the boot process using the EVB-LAN9668 EDS2 host using Linux software running on the LAN9668. The boot process for other EDS2 host platforms should be similar.

The EDS2 host board should be properly configured with Linux and the driver supporting the KSZ9131 EDS2. Refer to the software documentation for each EDS2 host platform for specific configuration and software details.

Note: The KSZ9131 EDS2 Daughter Card is compatible with various EDS2 baseboards. While this guide focuses on the EVB-LAN9668-EDS2 baseboard, other EDS2 baseboards are also supported.

4.2 EVB-LAN9668 EDS2 SYSTEM POWER-UP

At this point the KSZ9131 EDS2 should be installed in the correct SODIMM EDS2 connector. Perform the following steps to power-up the EVB-LAN9668 EDS2:

1. Verify that the EVB-LAN9668 EDS2 power switch is set to OFF (right) position. See Figure 4-1.

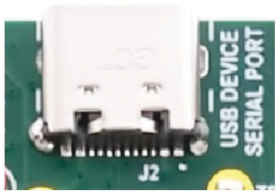
FIGURE 4-1: LAN9668 POWER SWITCH

2. Connect 12V 1A (minimum) power supply with a DC plug to DC Jack J8 on the EVB-LAN9668 EDS2. See Figure 4-2.

FIGURE 4-2: LAN9668 DC JACK

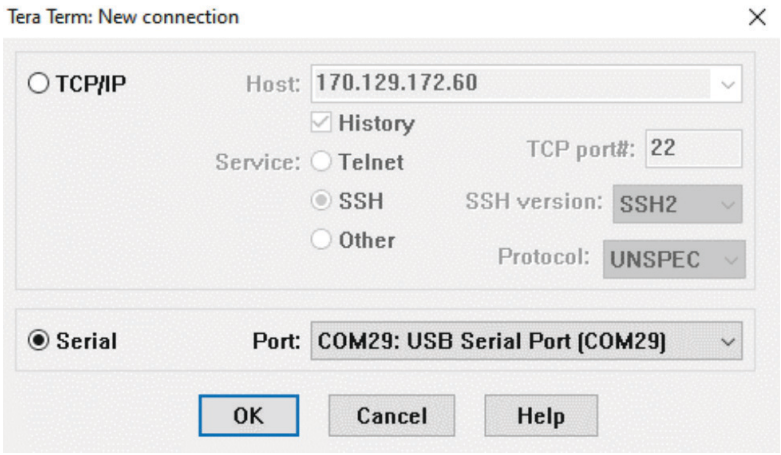
3. Connect a USB-C cable into the USB-C receptacle J2 on the EVB-LAN9668 EDS2 and then insert the other end into a PC. See Figure 4-3.

FIGURE 4-3: EVB-LAN9668 EDS2 USB-C RECEPTACLE



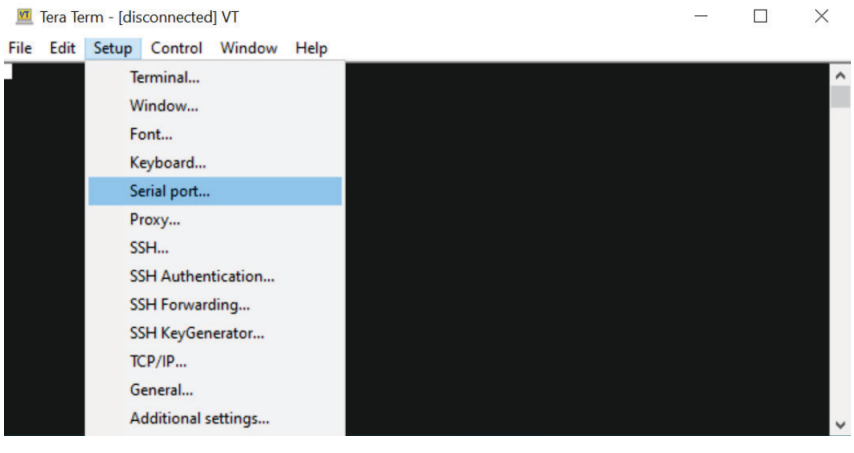
4. Slide the EVB-LAN9668 EDS2 power switch SW3 to the left ON position to turn on board power.
5. Open Tera Term. Select Serial radial button and look for COMx:USB Serial Port.
6. COM29 is shown in Figure 4-4. Windows may assign a different port number. Click **OK**.

FIGURE 4-4: TERA TERM SERIAL PORT SELECTION



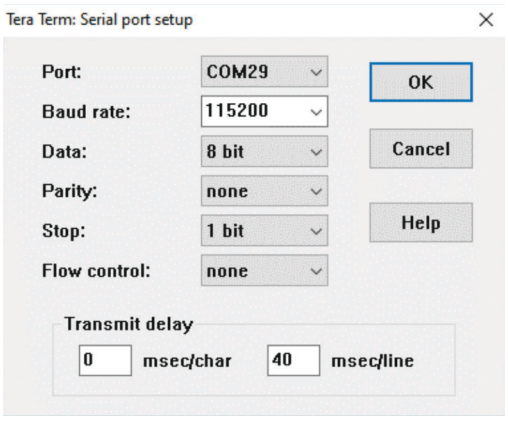
7. Go to the Setup menu and select Serial port. See Figure 4-5.

FIGURE 4-5: TERA TERM SETUP MENU



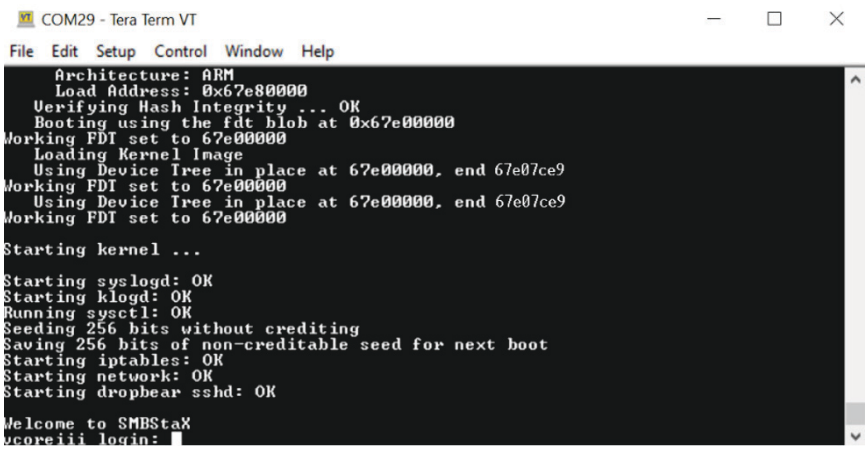
8. Set the selected port to 115200, 8-bit, no parity, 1 stop bit, no flow control, and 40 msec/line. Click **OK**. See Figure 4-6.

FIGURE 4-6: TERA TERM SERIAL PORT SETUP



9. Check if the Tera Term screen appears with a login prompt. See Figure 4-7.

FIGURE 4-7: TERA TERM LOGIN PROMPT



10. At login prompt, enter `root`. See Figure 4-8.

Note: For the succeeding steps, it is assumed that a host PC with an Ethernet port that can be pinged at `192.168.0.80` is available.

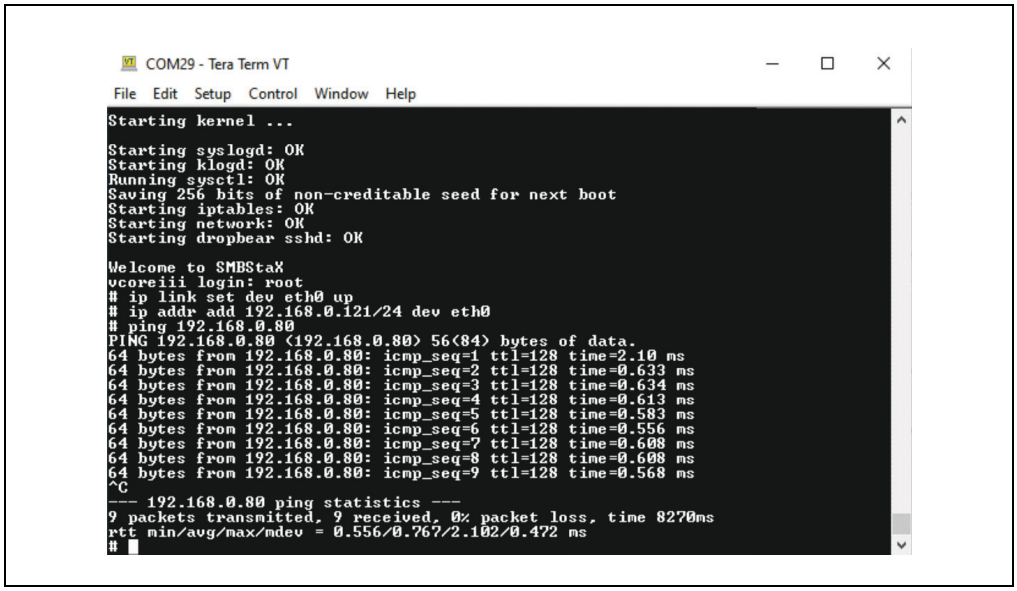
11. If the daughter card is on the right receptacle (PHY PORT2), replace `eth0` with `eth1` in the commands. Enter the following commands:

```
#ip link set dev eth0 up
#ip addr add 192.168.0.121/24 dev eth0
```

12. Connect Ethernet cable to the KSZ9131 EDS2 Daughter Card RJ45 port. Then, enter the following command:

```
#ping 192.168.0.80
```

FIGURE 4-8: LINUX® PING



Appendix A. Schematics

A.1 INTRODUCTION

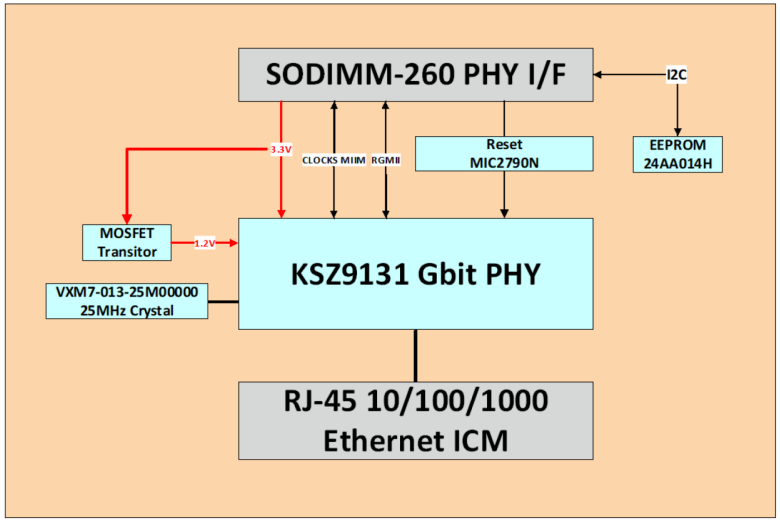
This appendix shows the KSZ9131 EDS2 Daughter Card schematics.

FIGURE A-1: KSZ9131 EDS2 DAUGHTER CARD

KSZ9131 Title Page

Table of Contents	
Sheet	Description
1	KSZ9131 Title Page
2	KSZ9131 PHY
3	KSZ9131 SODIMM_RGMII Interface

Revision History			
Revision	Date	Revision Summary	Author
A0	08/01/2023	Import circuitry EDS1 Design. Intial draft developed	Alexys Antell
A1	02/01/2024	Updated PHY straps. Pepared or release	Alexys Antell



Project Owner: Alexys Antell			
PCB Layout Contact: Alexys Antell			
PartNumber: EV35H80A	Project Title: *KSZ9131 EDS2 Daughter Card*	Variant: Standard	
Sheet Title: Table of Contents, Block Diagram, Revision History			
Size: B	SCH #: 02-00968	Rev: A1	Date: 2/1/2024
	PCB #: 04-12039	Rev: A1	Sheet 1 of 3
File: 1 KSZ9131 Title Page.SchDoc			

FIGURE A-2: KSZ9131 EDS2 DAUGHTER CARD PHY

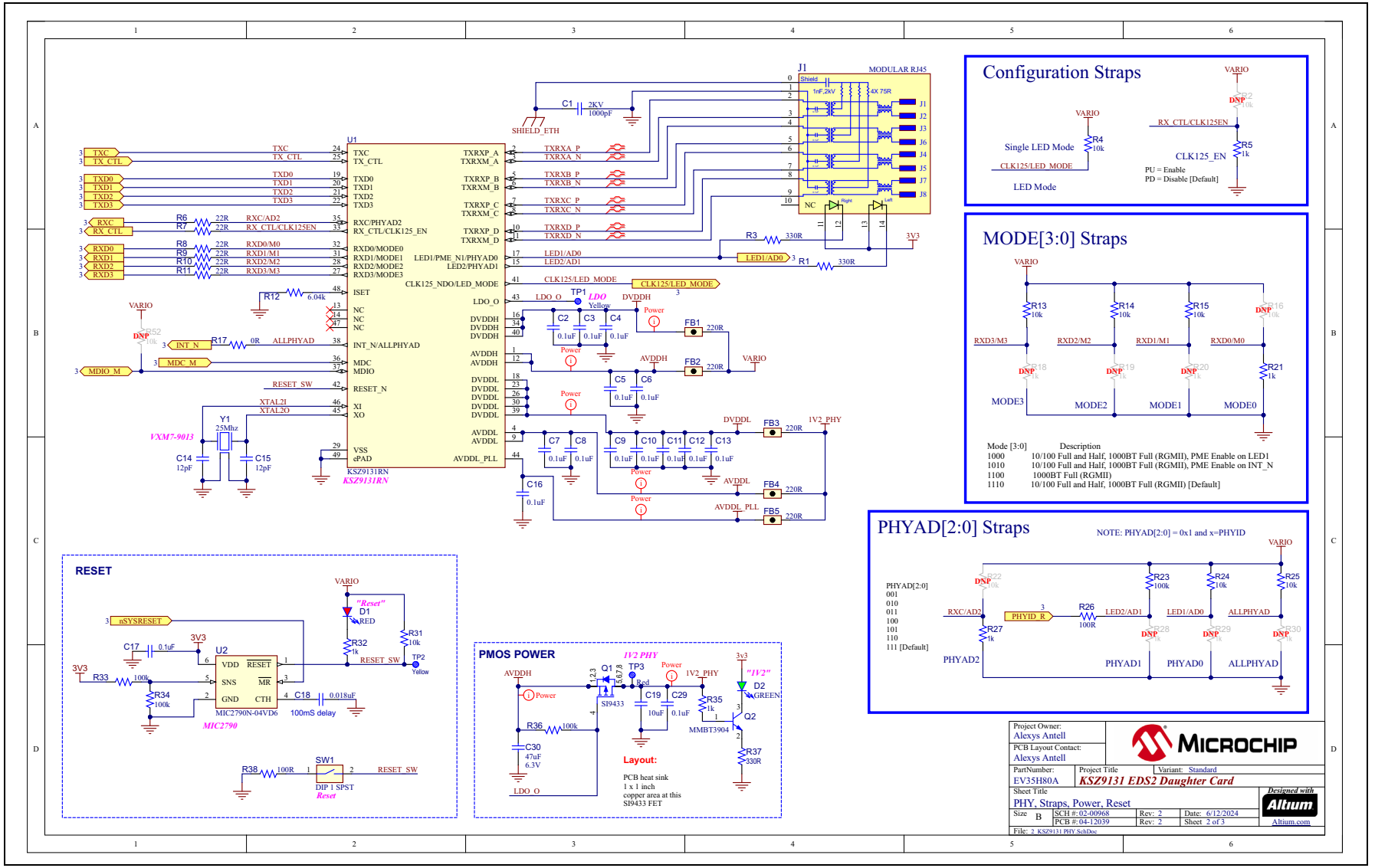
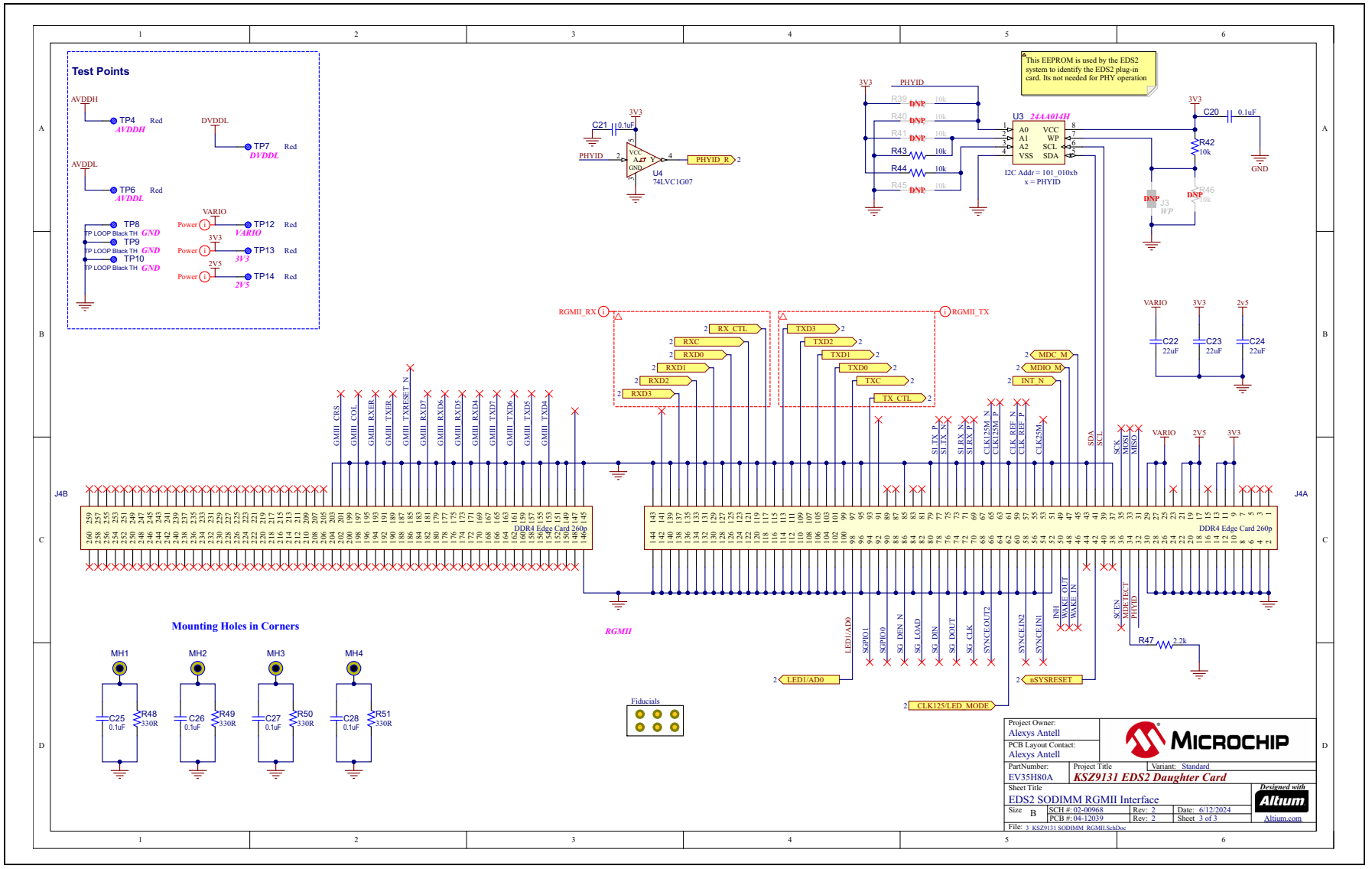


FIGURE A-3: KSZ9131 EDS2 DAUGHTER CARD SODIMM_RGMII INTERFACE



Appendix B. Bill of Materials

B.1 INTRODUCTION

This appendix contains the KSZ9131 Bill of Materials (BOM).

TABLE B-1: KSZ9131 EDS2 DAUGHTER CARD BILL OF MATERIALS (BOM)

Item	Qty	Reference	Description	Populated	Manufacturer	Manufacturer Part Number
1	1	C1	CAP CER 1000pF 2KV 10% X7R SMD 1206	Yes	—	—
2	13	C2, C3, C4, C5, C6, C7, C8, C9, C10, C11, C12, C13, C16	CAP CER 0.1uF 16V 10% X7R SMD 0402	Yes	Murata	GRM155R71C104KA88D
3	2	C14, C15	CAP HiQ 12pF 50V 5% NP0 2.56GHz SMD 0402	Yes	—	—
4	8	C17, C20, C21, C25, C26, C27, C28, C29	CAP CER 0.1uF 50V 10% X7R SMD 0402	Yes	Taiyo Yuden, [NoParam]	UMK105B7104KV-FR, [NoParam]
5	1	C18	CAP CER 0.018uF 50V 10% X7R SMD 0603	Yes	—	—
6	1	C19	CAP CER 10UF 25V 20% X5R SMD 0603	Yes	—	—
7	3	C22, C23, C24	CAP CER 22uF 10V 10% X7R SMD 1206	Yes	Murata	GRM31CR71A226KE15L
8	1	C30	CAP CER 47uF 6.3V 20% X5R SMD 0805	Yes	—	—
9	1	D1	DIO RED 2V 20mA 54mcd CLEAR SMD 0603	Yes	—	—
10	1	D2	DIO LED GREEN 2V 30mA 35mcd Clear SMD 0603	Yes	Ledtech	LT8A23-54-SB96-T5
11	5	FB1, FB2, FB3, FB4, FB5	FERRITE 220R @ 100MHz 2A SMD 0603	Yes	—	—
12	1	J1	CON MODULAR JACK RJ45 1000 MAGNETICS 2xLEDs TH R/A	Yes	—	—
13	0	J3	CON HDR-2.54 Male 1x2 Gold 5.84MH TH VERT	No	FCI	68001-202HLF
14	1	Q1	TRANS FET P-CH SI9433 20V 4.5A 1.3W 0.040R SOIC-8	Yes	—	—
15	1	Q2	TRANS BJT NPN MMBT3904 40V 200mA 310mW SOT-23-3	Yes	Diodes Incorporated	MMBT3904-7-F
16	7	R1, R3, R37, R48, R49, R50, R51	RES TKF 330R 1% 1/10W SMD 0603	Yes	Stackpole Electronics Inc	RMCF0603FT330R
17	0	R2, R16, R52	RES TKF 10k 5% 1/10W SMD 0603	No	Yageo	RC0603JR-0710KL
18	4	R4, R13, R14, R15	RES TKF 10k 5% 1/10W SMD 0603	Yes	Yageo	RC0603JR-0710KL
19	1	R5	RES TKF 1k 5% 1/10W SMD 0603	Yes	—	—
20	6	R6, R7, R8, R9, R10, R11	RES TKF 22R 1% 1/10W SMD 0603	Yes	—	—
21	1	R12	RES TKF 6.04k 1% 1/10W SMD 0603	Yes	Stackpole Electronics Inc	RMCF 1/16 6.04K 1% TR
22	1	R17	RES TKF 0R 1/10W SMD 0603 AEC-Q200	Yes	Vishay	CRCW06030000Z0EB
23	0	R18, R19, R20	RES TKF 1k 5% 1/10W SMD 0603	No	Panasonic	ERJ-3GSYJ102V
24	1	R21	RES TKF 1k 5% 1/10W SMD 0603	Yes	Panasonic	ERJ-3GSYJ102V
25	0	R22, R39, R40, R41, R45, R46	RES TKF 10k 1% 1/10W SMD 0603	No	ROHM, TE Connectivity	MCR03EZPFX1002, CRG0603F10K
26	3	R23, R33, R34	RES TKF 100k 1% 1/10W AEC-Q200 SMD 0603	Yes	Vishay	CRCW0603100KFKEA
27	6	R24, R25, R31, R42, R43, R44	RES TKF 10k 1% 1/10W SMD 0603	Yes	ROHM, TE Connectivity	MCR03EZPFX1002, CRG0603F10K
28	1	R26	RES TKF 100R 5% 1/10W SMD 0603	Yes	ROHM	MCR03EZPJ101

TABLE B-1: KSZ9131 EDS2 DAUGHTER CARD BILL OF MATERIALS (BOM) (CONTINUED)

Item	Qty	Reference	Description	Populated	Manufacturer	Manufacturer Part Number
29	3	R27, R32, R35	RES TKF 1k 1% 1/10W SMD 0603	Yes	ROHM, Yageo	MCR03EZPFX1001, RC0603FR-071KL
30	0	R28, R29, R30	RES TKF 1k 1% 1/10W SMD 0603	No	ROHM	MCR03EZPFX1001
31	1	R36	RES TF 100k 1% 1/8W SMD 0603	Yes	—	—
32	1	R38	RES TKF 100R 1% 1/10W SMD 0603 AEC-Q200	Yes	Yageo	AC0603FR-07100RL
33	1	R47	RES TKF 2.2k 1% 1/10W SMD 0402	Yes	—	—
34	1	SW1	SWITCH DIP 1 SPST 24V 25mA 418117270901 TH	Yes	—	—
35	2	TP1, TP2	MISC, TEST POINT PC MINI, 0.040" D YELLOW	Yes	FuZhou XiXiang	CONN00197B01
36	7	TP3, TP4, TP6, TP7, TP12, TP13, TP14	MISC, TEST POINT MULTI PURPOSE MINI RED	Yes	—	—
37	3	TP8, TP9, TP10	CON TP LOOP Black TH	Yes	—	—
38	1	U1	MCHP INTERFACE KSZ9131RNX 10/100/1000BASE-T QFN-48	Yes	Microchip Technology	KSZ9131RNXC
39	1	U2	MCHP ANALOG SUPERVISOR 0.4V to 5.5V MIC2790N-04VD6 SOT-23-3	Yes	—	—
40	1	U3	MCHP MEMORY SERIAL EEPROM 1kb I2C 24AA014H-I/SN 8SOIC	Yes	—	—
41	1	U4	IC BUFFER NON-INVERT SN74LVC1G07DBVR SOT-23-5	Yes	—	—
42	1	Y1	MCHP CRYSTAL 25Mhz 10pF SMD L3.2W2.5H0.8	Yes	—	—

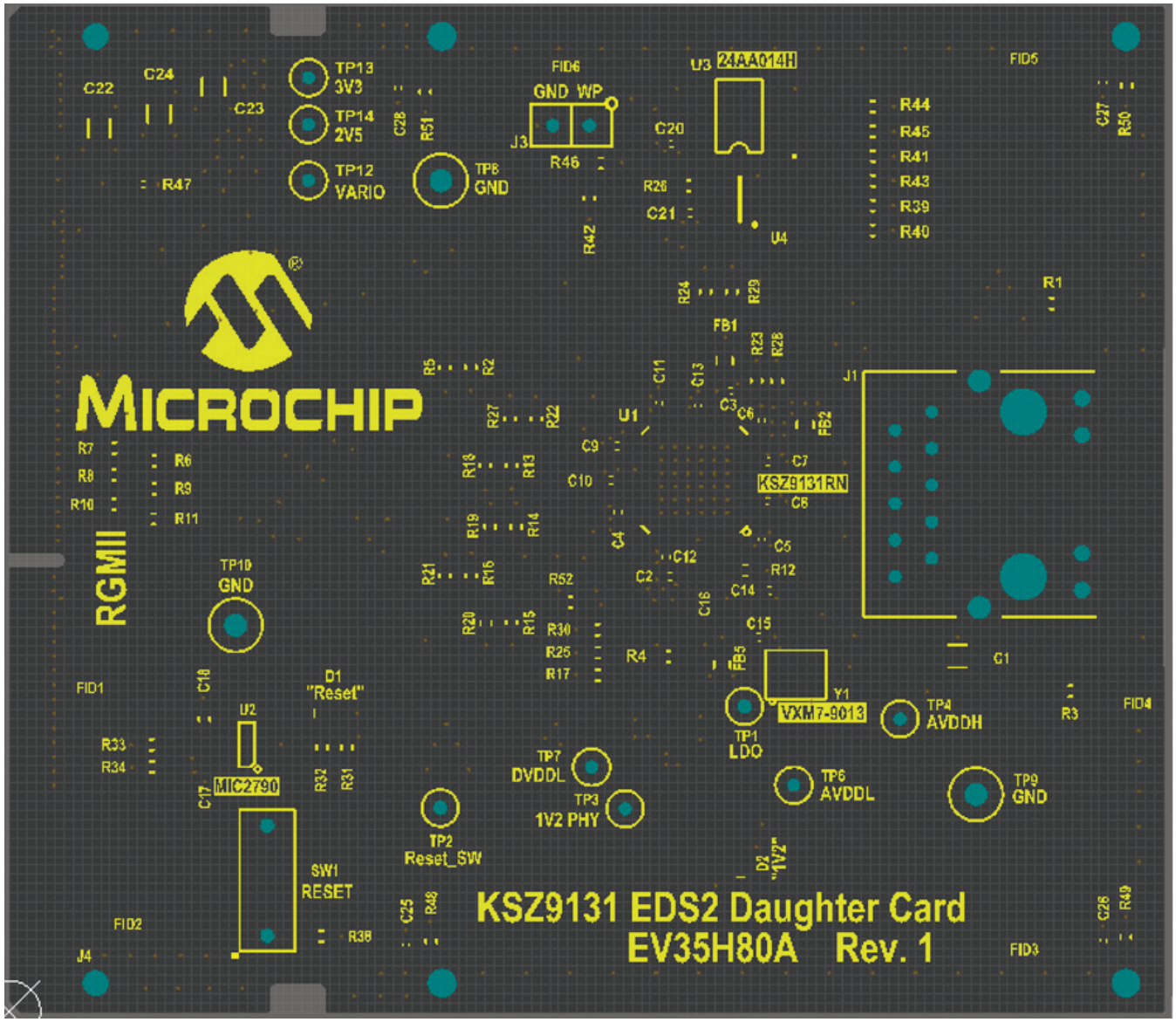
NOTES:

Appendix C. PCB Layers

C.1 INTRODUCTION

This appendix contains the KSZ9131 EDS2 Daughter Card's silkscreen top and bottom layers.

FIGURE C-1: KSZ9131 EDS2 DAUGHTER CARD TOP SILK SCREEN



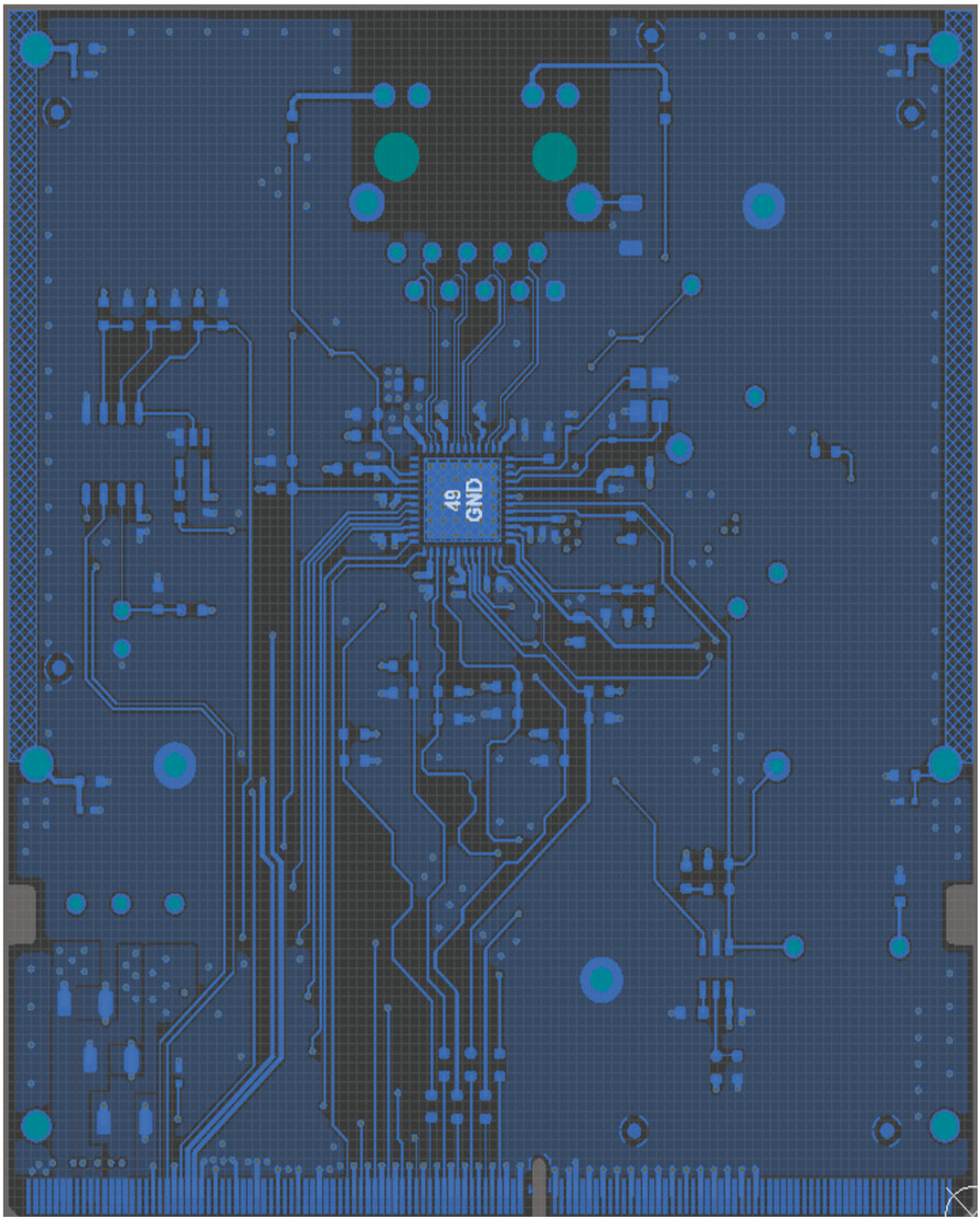


FIGURE C-2: KSZ9131 EDS2 DAUGHTER CARD TOP COPPER

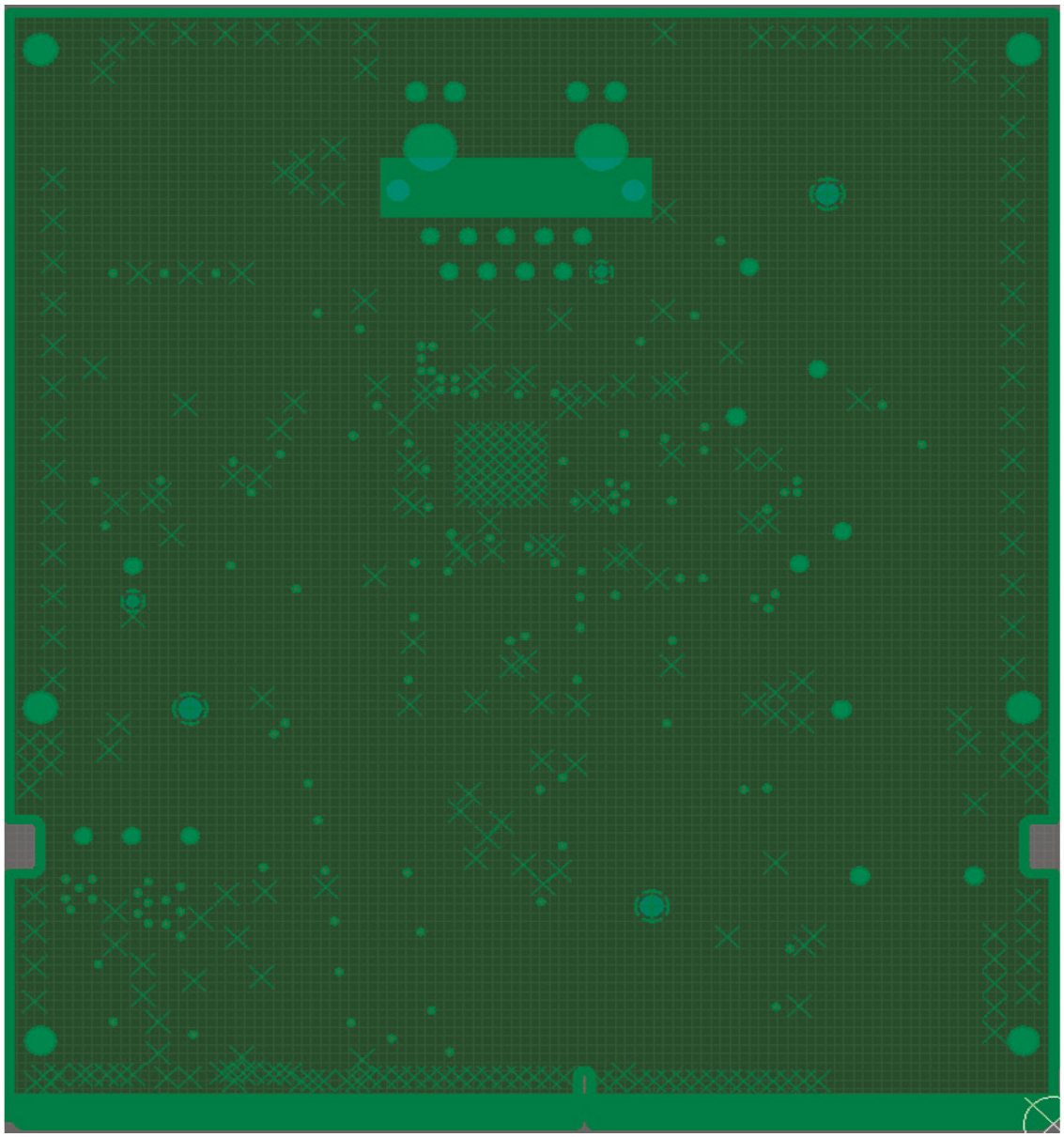


FIGURE C-3: KSZ9131 EDS2 DAUGHTER CARD GND

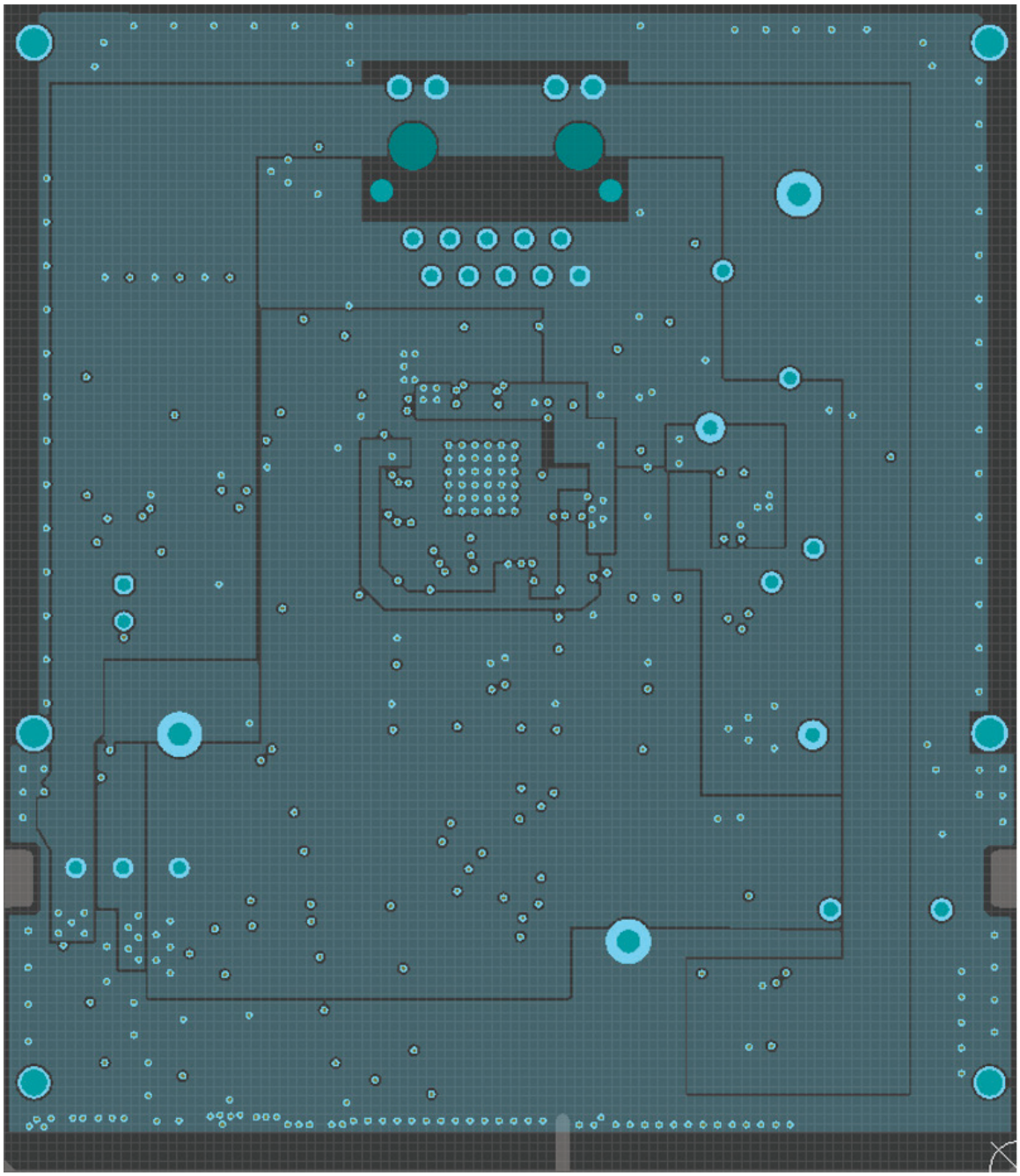


FIGURE C-4: KSZ9131 EDS2 DAUGHTER CARD POWER

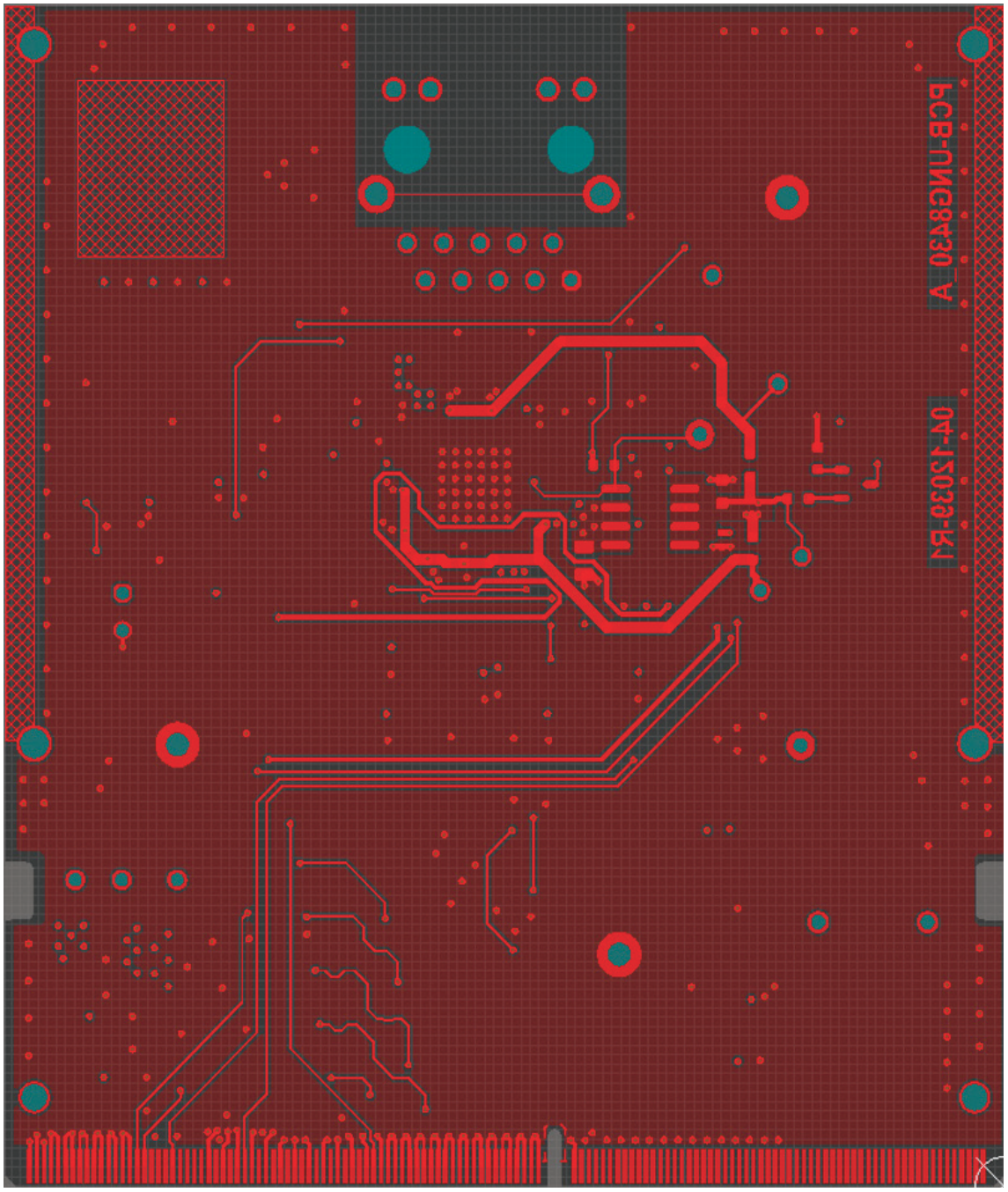


FIGURE C-5: KSZ9131 EDS2 DAUGHTER CARD SIGNAL

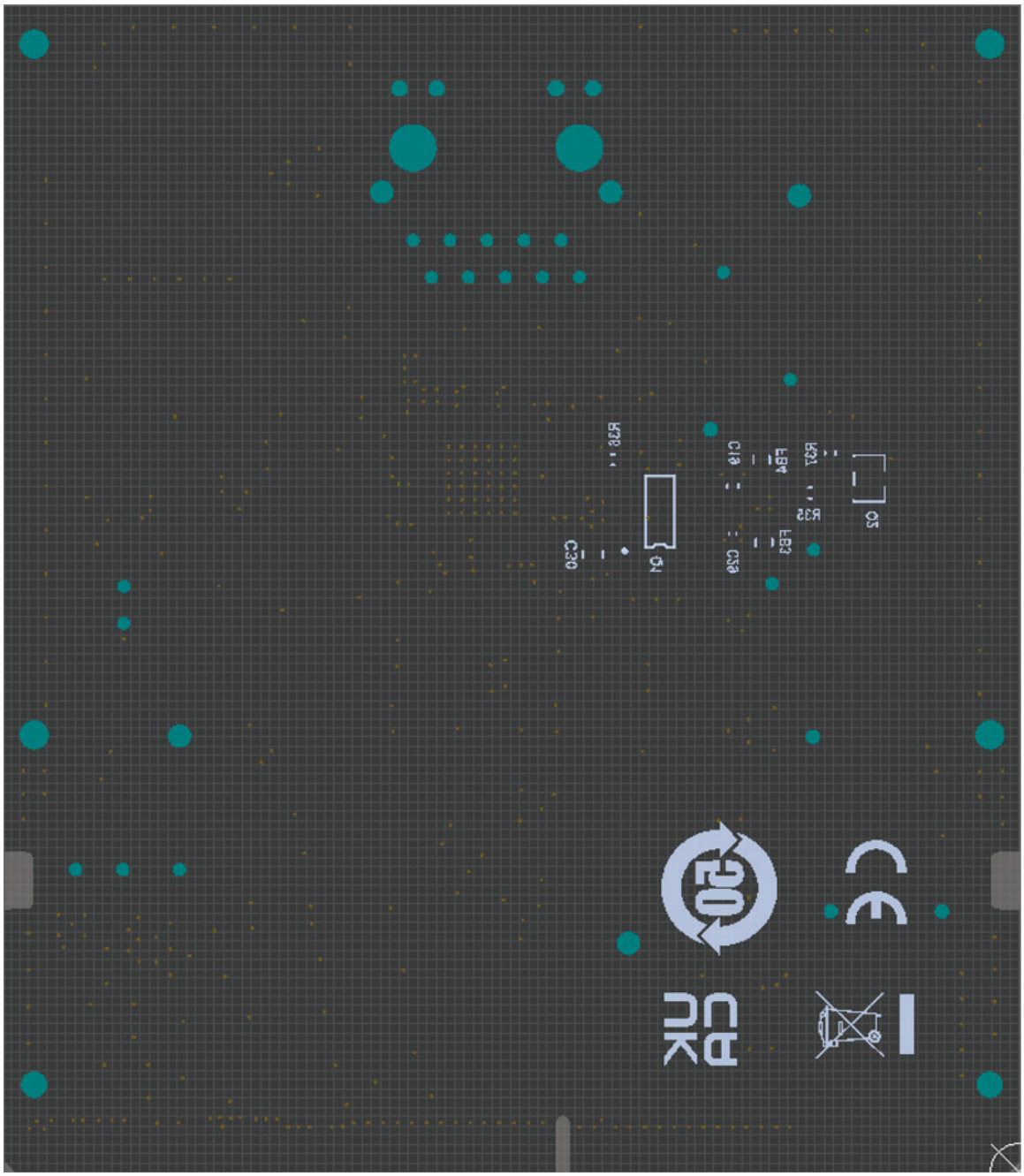


FIGURE C-6: KSZ9131 EDS2 DAUGHTER CARD BOTTOM SILK

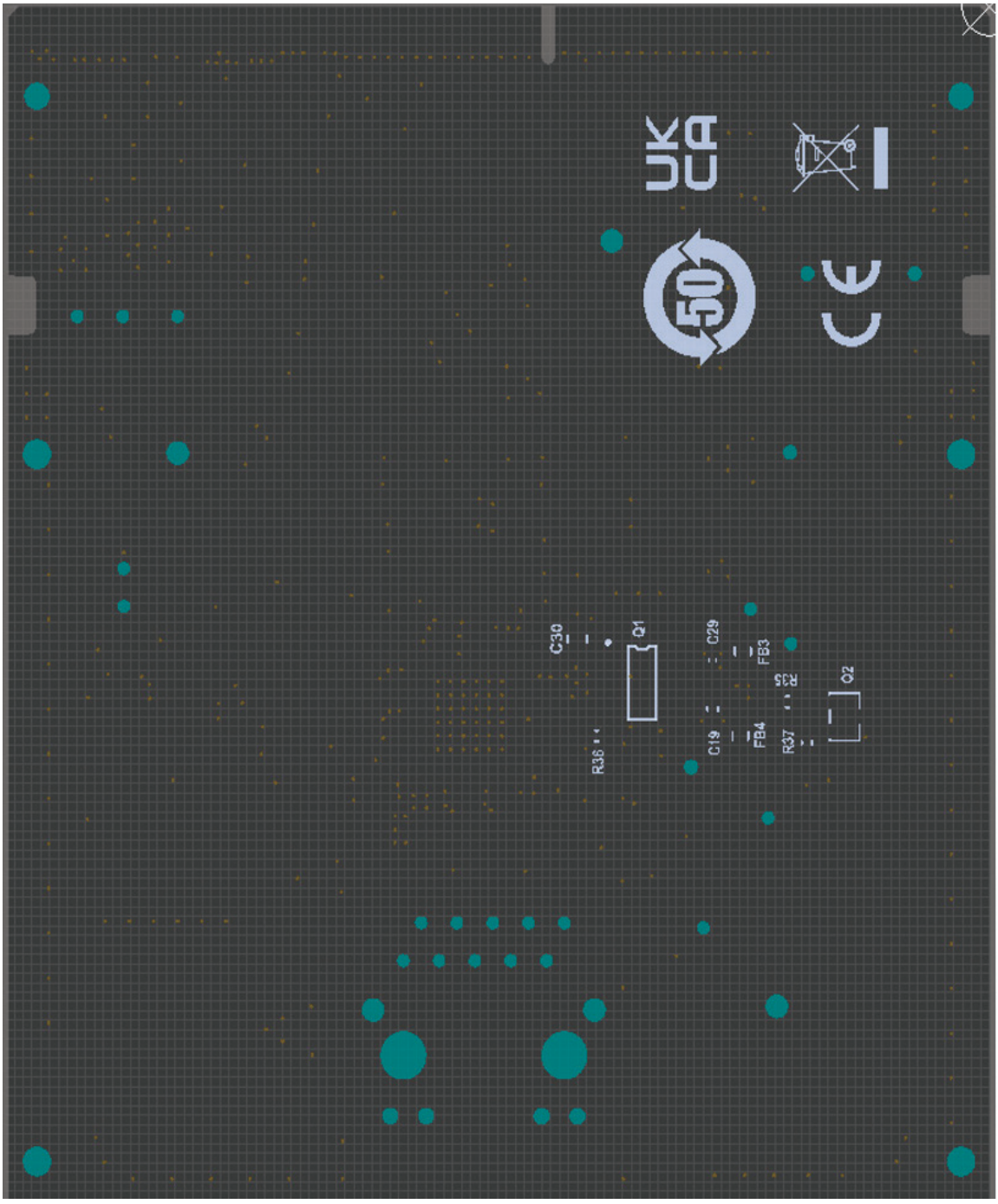


FIGURE C-7: KSZ9131 EDS2 DAUGHTER CARD BOTTOM SILK MIRRORED