14–19GHz 50W GaN PA MMIC

ICP1747

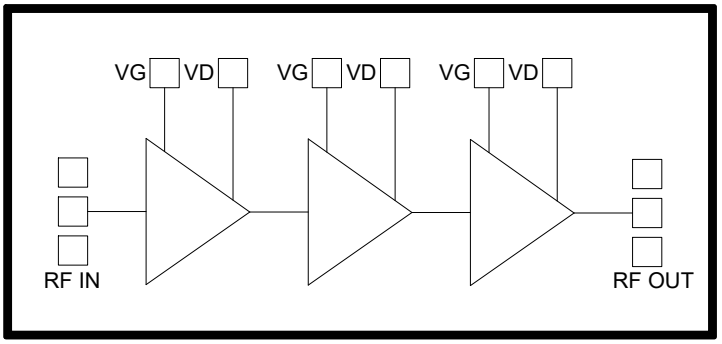
Product Overview

ICONICRF's ICP1747 is a three-stage MMIC power amplifier in bare die form, fabricated using GaN on SiC technology. ICP1747 operates from 14-19GHz with 47dBm output power, 35% PAE, and 23dB small signal gain. ICP1747 is well suited to a variety of Test and Measurement and Aerospace and Defense applications.

Key Features

- **Frequency range: 14-19GHz**
- **P_{out}: 47dBm @27dBm P_{in}**
- **PAE: 35%**
- **Small signal gain: 23dB**
- **Bias: V_D=28V, I_{DQ}=450mA**
- **Technology: GaN on SiC**
- **Lead-free and RoHS compliant**
- **Die Size: 4.25mm x 6.5mm**

Functional Block Diagram



Applications

- Test and Measurement
- Aerospace and Defense
- Datalinks

Electrical Specifications

Parameter	Min.	Typ.	Max.	Units	Conditions(1)
Frequency	14		19	GHz	
Saturated output power, P_{sat}		47		dBm	P_{in} = 27 dBm
Power added efficiency, PAE		35		%	P_{in} = 27 dBm
Small signal gain, S_{21}		23		dB	
Input return loss		10		dB	
Output return loss		10		dB	

Note: (1) Test conditions unless otherwise stated V_{DQ}=28V, I_{DQ}=450mA, T_A=25°C, Pulsed 100µs, 10%

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1. Electrical Specification

1.1 Absolute Maximum Ratings

Parameter	Absolute Maximum
Drain voltage (V_{DG})	32V
Power dissipation (CW)	TBC
CW input power	+29dBm
Channel temperature	275°C
Storage temperature	–65°C to +150°C

Note:
Exceeding any one or combination of these limits may cause permanent damage to this device.

Microchip Technology Inc. does not recommend sustained operation near these survivability limits.

1.2 Small Signal Performance

Typical Power Data over Temperature

Test conditions: V_D=28V, I_{DQ}=450mA

Figure 1-1. S_{21} vs Freq

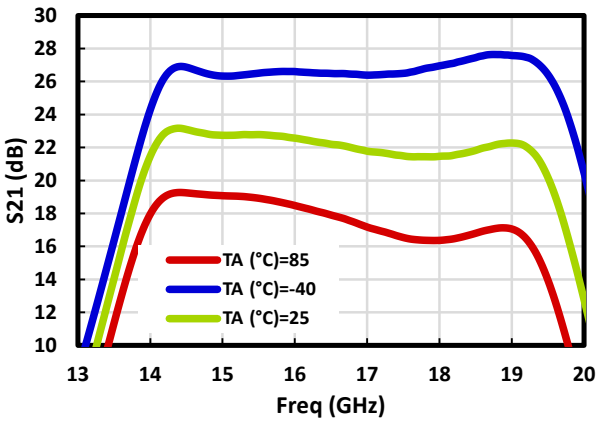


Figure 1-2. S_{11} vs Freq

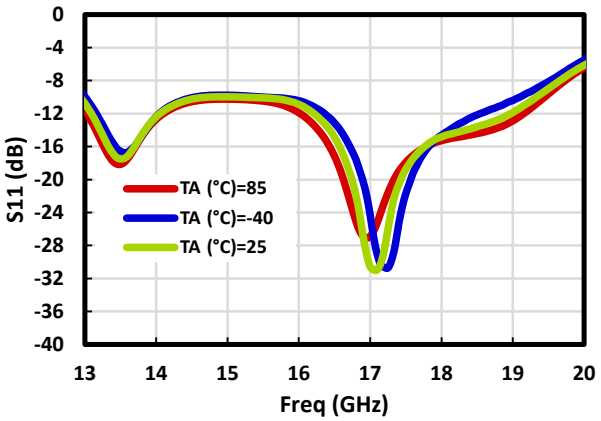
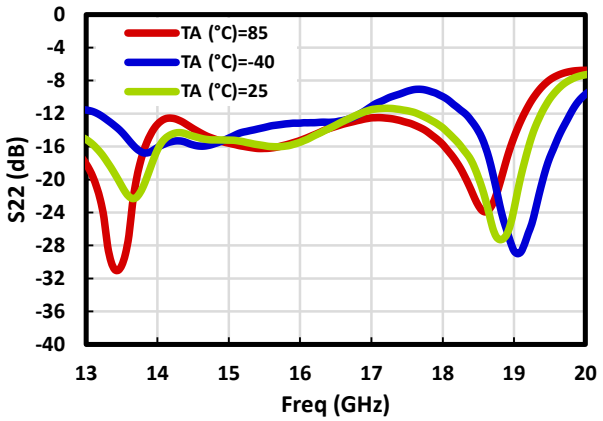


Figure 1-3. S_{22} vs Freq



1.3 Large Signal Performance

Typical Pulsed Power Data at T_A=25°C

Test conditions: V_D=28V, I_{DQ}=450mA, Pulsed 100µs/10%

Figure 1-4. P_{out} vs. P_{in}

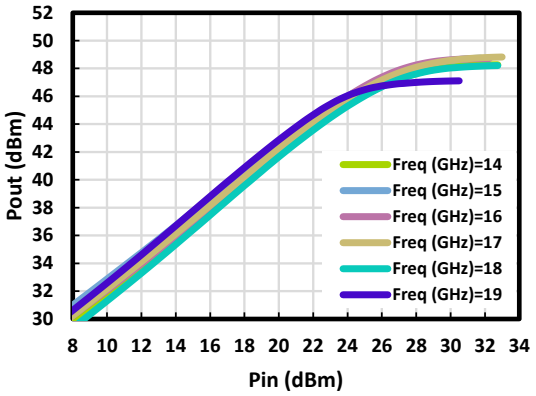


Figure 1-5. Gain vs. P_{out}

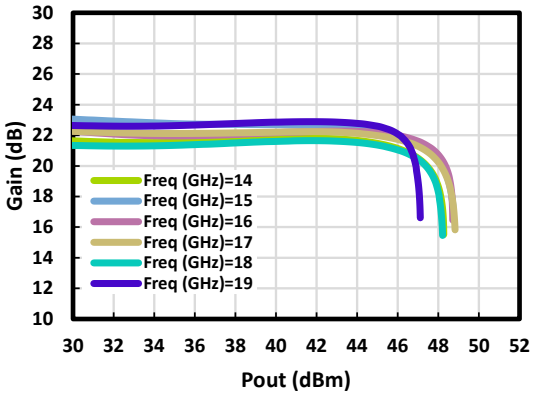


Figure 1-6. PAE vs. P_{out}

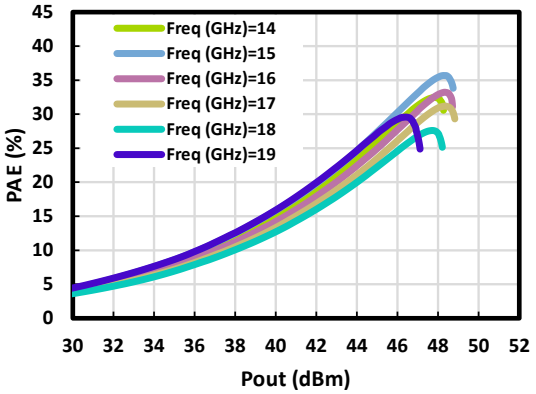


Figure 1-7. I_D vs. P_{out}

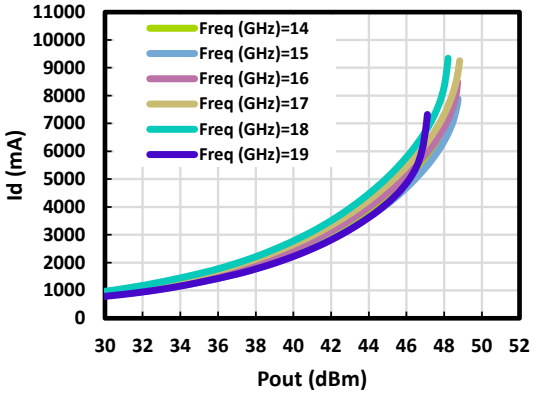


Figure 1-8. P_{out} vs. Freq

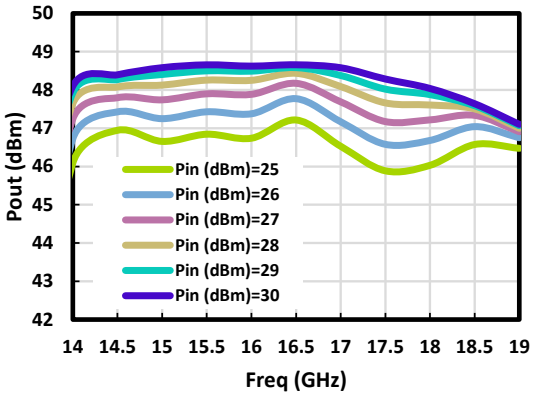
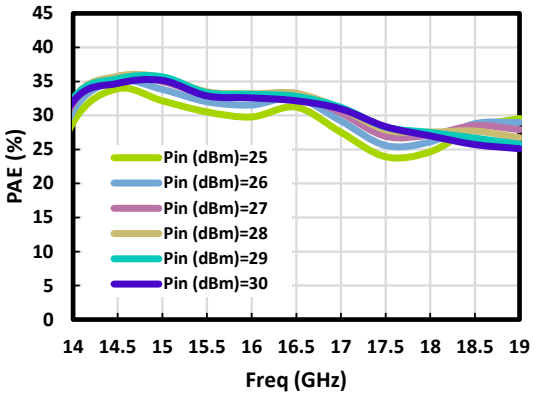


Figure 1-9. PAE vs. Freq



Typical Pulsed Power Data at T_A=85°C

Test conditions: V_D=28V, I_{DQ}=450mA, Pulsed 100µs/10%

Figure 1-10. P_{out} vs. P_{in}

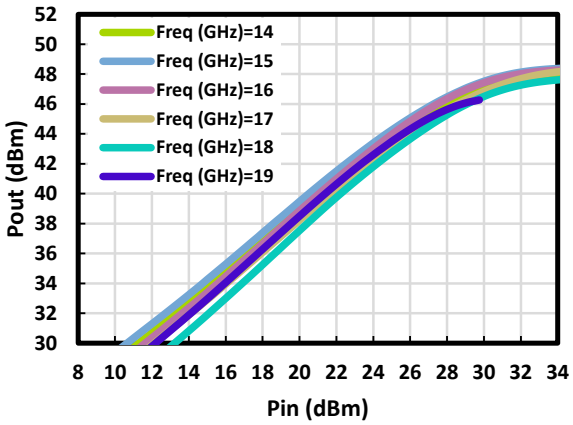


Figure 1-11. Gain vs. P_{out}

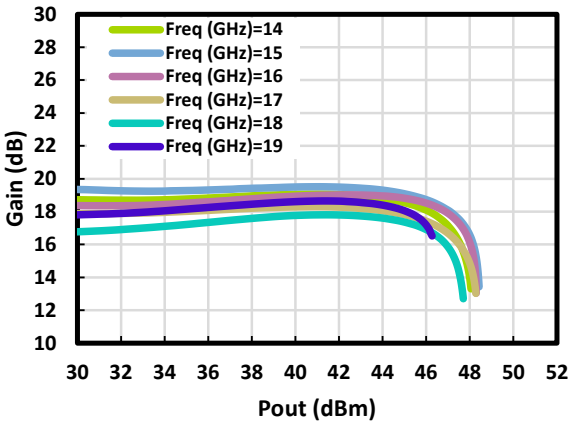


Figure 1-12. PAE vs. P_{out}

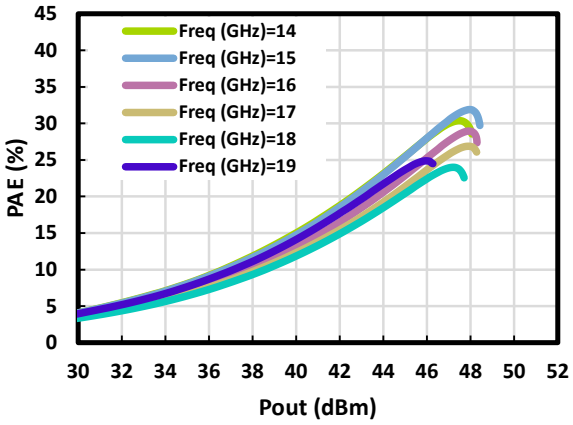


Figure 1-13. I_D vs. P_{out}

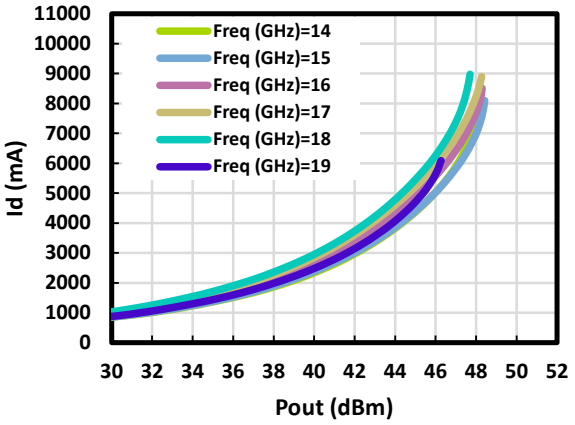


Figure 1-14. P_{out} vs. Freq

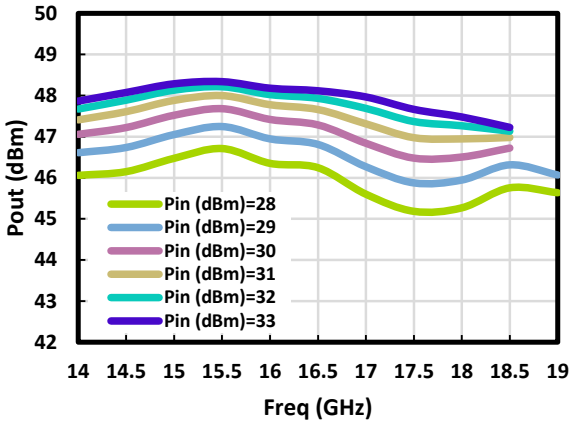
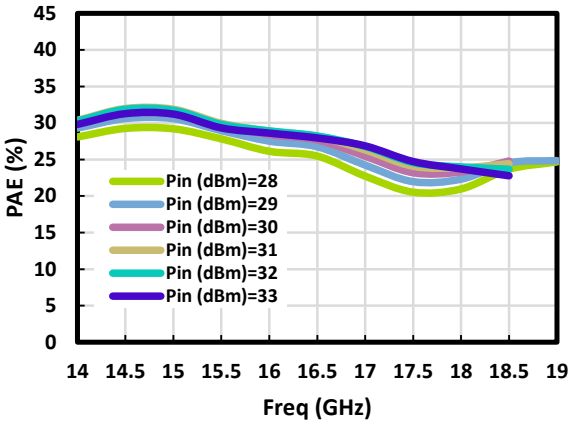


Figure 1-15. PAE vs. Freq



Typical Pulsed Power Data at T_A=-40°C

Test conditions: V_D=28V, I_{DQ}=450mA, Pulsed 100µs/10%

Figure 1-16. P_{out} vs. P_{in}

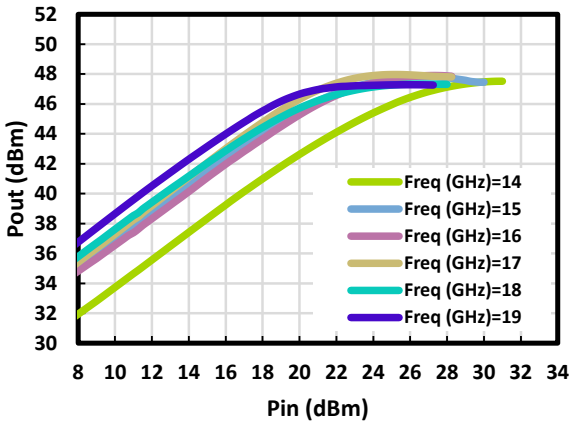


Figure 1-17. Gain vs. P_{out}

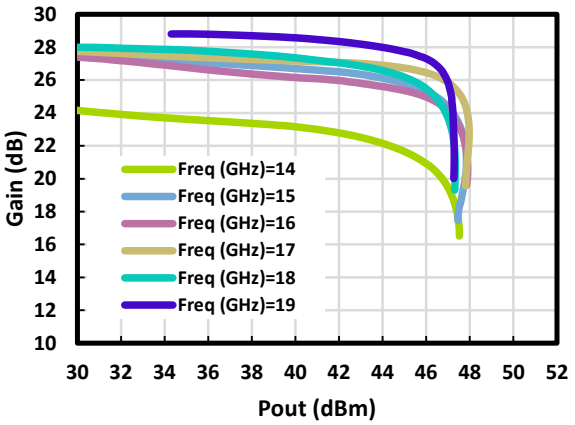


Figure 1-18. PAE vs. P_{out}

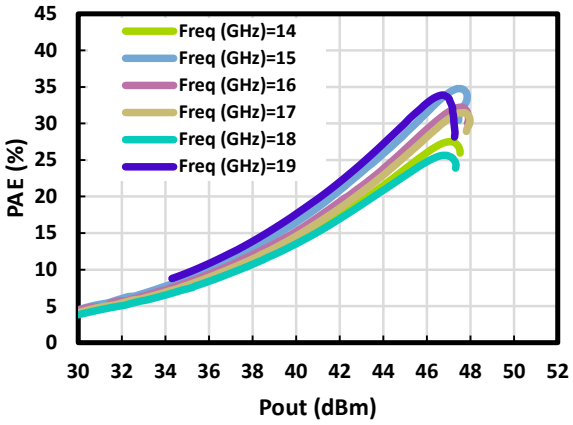


Figure 1-19. I_D vs. P_{out}

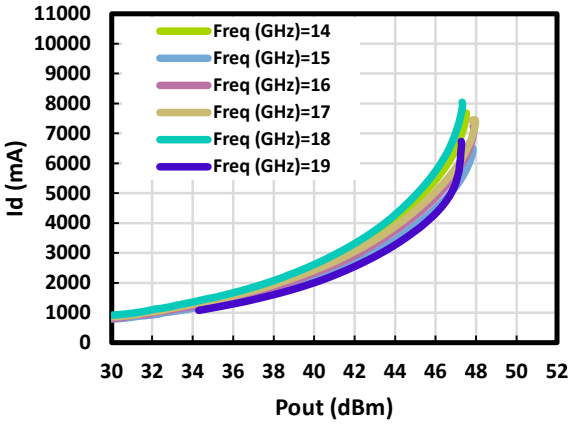


Figure 1-20. P_{out} vs. Freq

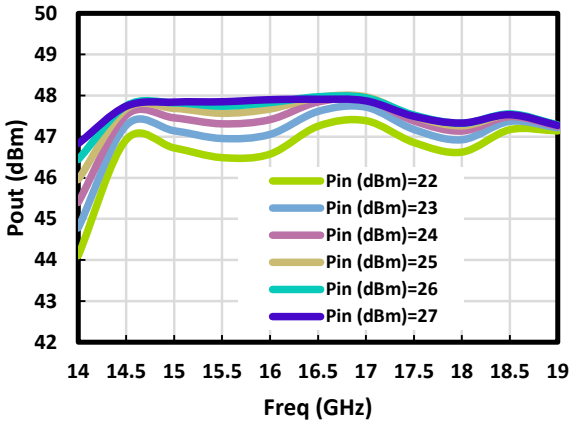
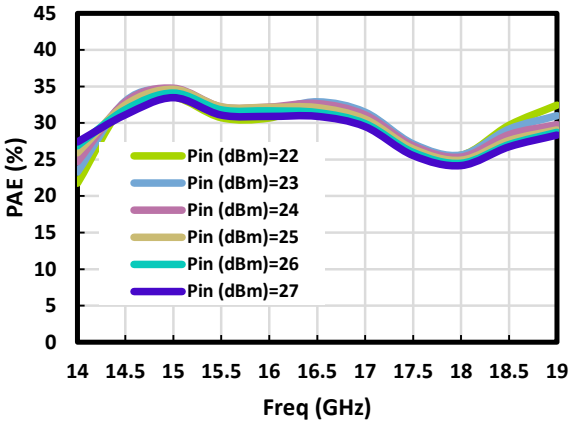
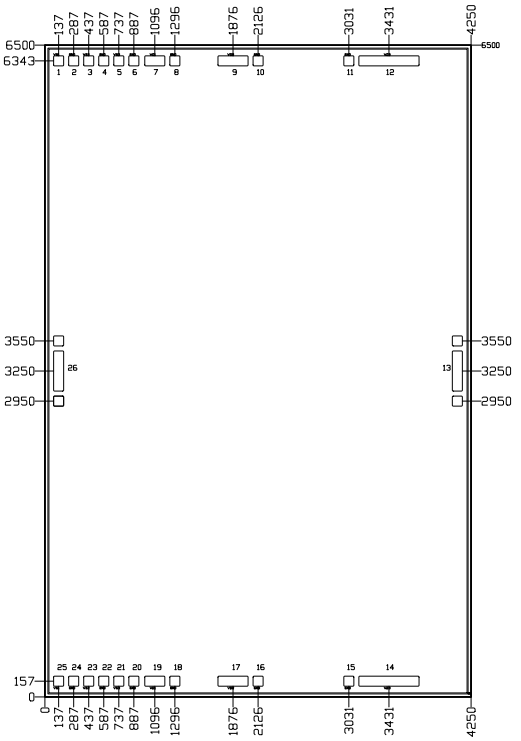


Figure 1-21. PAE vs. Freq



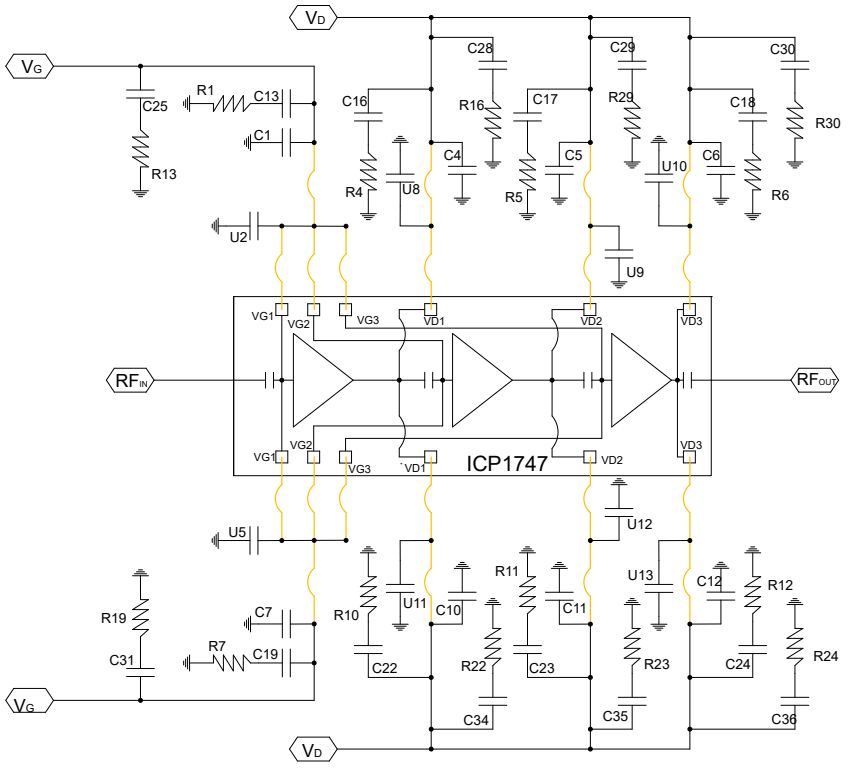
2. Mechanical Drawing



Units: µm | Thickness: 100µm | Backside of Die is RF and DC ground

Pad No	Pad size (µm)	Function	Description
1,25	100x100	VG1	First stage gate bias, decoupling and bypass caps required
2,24	100x100	GND	Ground Pads
3,23	100x100	VG2	Second stage gate bias, decoupling and bypass caps required
4,22	100x100	GND	Ground Pads
5,21	100x100	VG3	Third stage gate bias, decoupling and bypass caps required
6,20	100x100	GND	Ground Pads
7,19	200x100	VD1	First stage drain voltage, decoupling and bypass caps required
8,18	100x100	GND	Ground Pads
9,17	300x100	VD2	Second stage drain voltage, decoupling and bypass caps required
10,16	100x100	GND	Ground Pads
11,15	100x100	GND	Ground Pads
12,14	600x100	VD3	Third stage drain voltage, decoupling and bypass caps required
13	100x400	RF OUT	RF Output
26	100x400	RF IN	RF Input

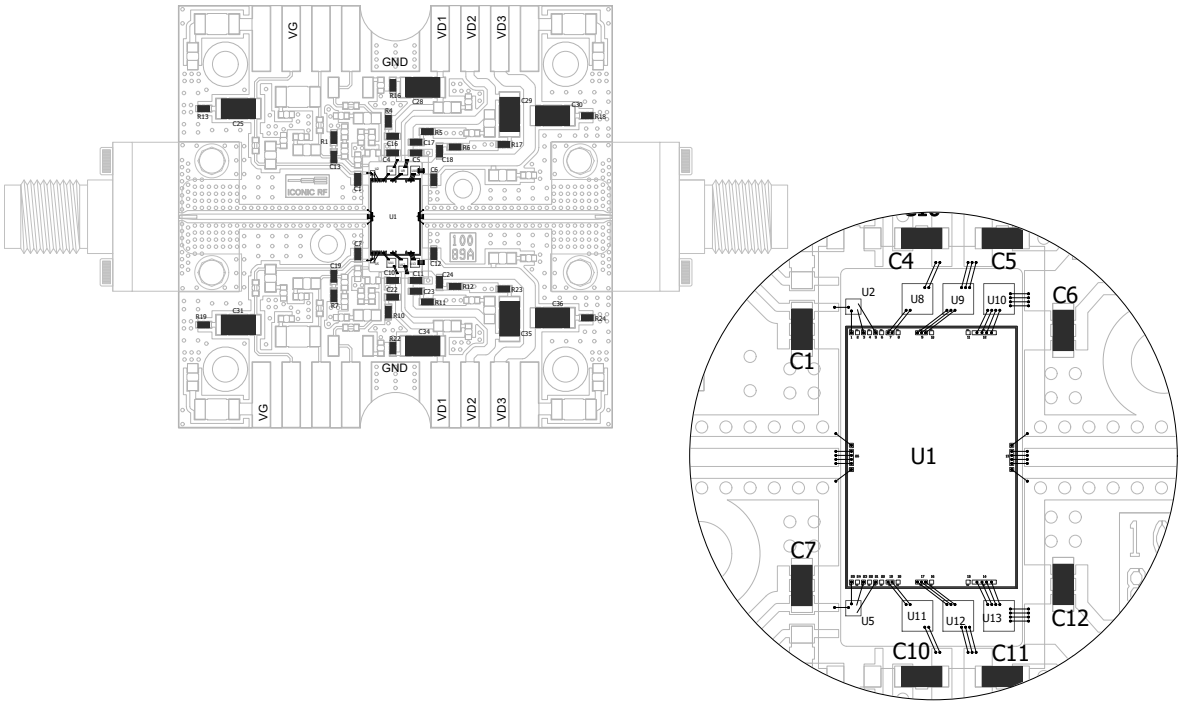
3. Application Circuit



Bill of materials

Component ID	Value	Details	Qty	Manufacturer Part No.
U2, U5	100pF	100pF SLC	2	Johanson Dielectrics Inc.
U8 - U13	10nF	10nF SLC	6	Johanson Dielectrics Inc.
C1, C4 - C7, C10 - C12	10nF	10nF Capacitor,10%,50V,0402	8	Various
C13, C16 - C19, C22 - C24	100nF	100nF Capacitor,10%,50V,0402	8	Various
C25, C28 - C31, C34 - C36	10µF	10µF Capacitor,10%,50V,1206	8	Various
R4 - R6, R10 - R12, R16 - R18, R22 - R24	0Ω	0 Ohms Resistor,0402	12	Various
R1, R7, R13, R19	5.1Ω	5.1 ohm resistor, 0402	4	Various

4. Evaluation Board



PCB Fabrication

PCB Construction	Details
Top & Bottom Layer	0.5oz Cu + ENEPIG
Electroless Nickel	3-6µm
Electroless Palladium	0.05-0.3µm
Immersion Gold	0.04-0.06µm

Key Features	Details
Dielectric	RO4003C
Overall Thickness	Approx 0.27mm
VIA Plating Thickness	>15µm

5. Other considerations

Assembly Guidance

Interconnect assembly Notes

- Ball Bonding is preferred technique.
- Force, time and ultrasonic parameters are critical.
- Aluminum wire bonding is not recommended.
- Bond Wire diameter of 1mil is recommended.

Die attach of component using adhesive

- Vacuum collets are preferred method of pickup.
- Pickup method must consider the avoidance of die air bridges.
- Die suitable for Eutectic and Epoxy die attach.
- Where Epoxy is used, high thermal conductivity,
- Silver Sintered Epoxy is recommended:
  - Namics H9889–1
  - Kyocera CT2700R7S

Die attach using Eutectic

- Flux-less gold-tin (AuSn) (80% Au, 20% Sn with a melting point of 280ºC) preform is preferred between the die and attached surface.
- Recommended preform should be approximately 0.0012” thick.
- Die bonder using heated collet with a temperature of 310ºC and die scrubbing should be used to ensure wetting and prevent formation of voids.
- Exposure to extreme temperature should be kept to a minimum.
- The optimum die attach environment is nitrogen atmosphere.

Reflow Process

- Maximum temperature 320ºC for 30 seconds.
- Material matching for coefficient of thermal expansion is crucial for long-term reliability.

For optimum RF and thermal performance IconicRF recommends the die assembly base plate is adequately bolted to an forced air heat sink using a thermal graphite interface pad (Graphite Interface Material GCSP-017-G 170µm thick) for optimal heat transfer. There are many variables of the second level assembly between the die base plate and heat sink that IconicRF are unable to control and the following guidance is provided as information only. Fixing bolts should be provided as close to the die as possible to ensure an optimum pressure between the base plate and the heat sink. The bolting screws used to attach the PCB assembly to the heat sink must include washers and be tightened with a suitable tightening pattern to ensure a uniform pressure. It is advised all surfaces be cleaned and be free of grease and dust prior to fully aligning the assembly with all screws located and tightened to finger tight. Further torquing of the screws must be achieved in multiple phases using a star shaped pattern to a recommended torque of 2.5N/m.

Bias-up procedure

1. Set V_G to -5V
2. Set V_D to 28V
3. Adjust V_G positive until I_D quiescent is 450mA
4. Limit I_D to 9A
5. Apply RF signal

Bias-down procedure

1. Turn off RF
2. Turn off V_D, allow drain capacitors to discharge
3. Turn off V_G

6. Ordering, Shipping, and Handling

Handling Recommendations

Integrated circuits are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. It is recommended to follow all procedures and guidelines outlined in the Microsemi application note AN01: GaAs MMIC Handling and Die Attach Recommendations.

Ordering Information

For additional ordering information, contact your Microchip sales representative.

Part Number	Package	Standard Packing Format
ICP1747-1-110I	Die	Gel Pack
ICP1747-1-101I	Die	Wafer on expander ring
ICP1747-1-103I	Die	Wafer on metal frame
EV98J27A	EVB	Evaluation board with connector SMA (ICP1747-1-110I PCB Assembly)

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