

8.5-11GHz 70W GaN PA MMIC

ICP1048



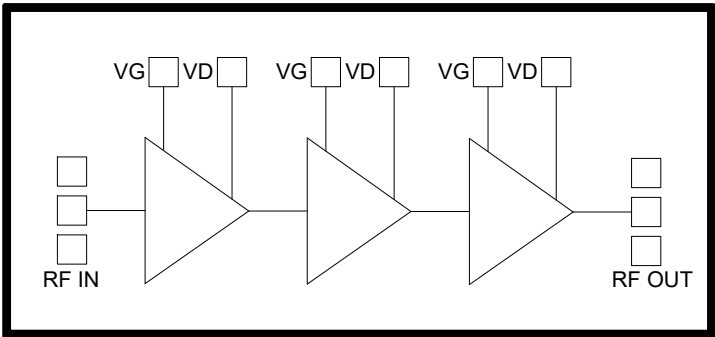
Product Overview

ICONICRF's ICP1048 is a three stage MMIC power amplifier in bare die form, fabricated using GaN on SiC technology. ICP1048 operates from 8.5-11GHz with 48.5dBm output power, 35% PAE and 24dB small signal gain. ICP1048 is well suited to a variety of Communication Infrastructure and Aerospace & Defense applications

Key Features

- **Frequency Range:** 8.5-11GHz
- **P_{out}:** 48.5dBm @26dBm P_{in}
- **PAE:** 35% @26dBm P_{in}
- **Small Signal Gain:** 24dB
- **Bias:** V_D=28V, I_{DQ}=400mA
- **Technology:** GaN on SiC
- **Lead-free and RoHS compliant**
- **Die Size:** 4.7mm x 4.55mm

Functional Block Diagram



Applications

- Communication Infrastructure
- Aerospace & Defense

Electrical Specifications

Parameter	Min.	Typ.	Max.	Units	Conditions ⁽¹⁾
Frequency	8.5		11	GHz	
Output Power at P _{sat}		48.5		dBm	P _{in} = 26dBm
Power Added Efficiency, PAE at P _{sat}		35		%	P _{in} = 26dBm
Small Signal Gain, S ₂₁		24		dB	
Input Return Loss		10		dB	
Output Return Loss		6		dB	
I _{DQ}		400		mA	

Note: (1) Test conditions unless otherwise stated V_D=28V, I_{DQ}=400mA, T_A=25°C, Pulsed 10% (100µs/1ms)

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1. Electrical Specifications

1.1 Absolute Maximum Ratings

Parameter	Absolute Maximum
Drain Voltage (V_D)	30V
Gate Voltage (V_G)	-5 to 0V
Channel Temperature	275°C
Storage Temperature	-65°C to +150°C

Note:

Exceeding any one or combination of these limits may cause permanent damage to this device.

Microchip Technology Inc. does not recommend sustained operation near these survivability limits.

1.2 Small Signal Performance

Typical Power Data over Temperature

Test conditions: $V_D=28V$, $I_{DQ}=400mA$

Figure 1-1. S_{21} vs Freq

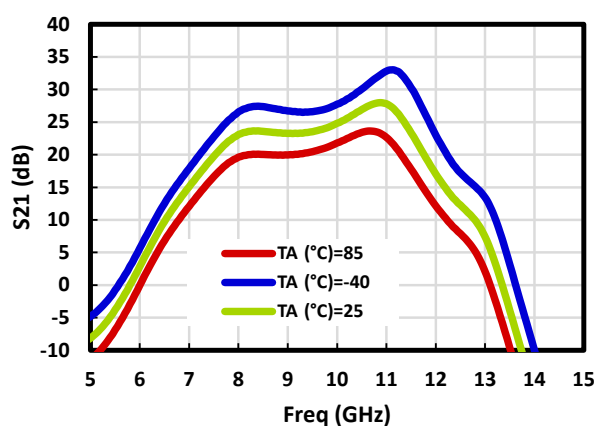


Figure 1-2. S_{11} vs Freq

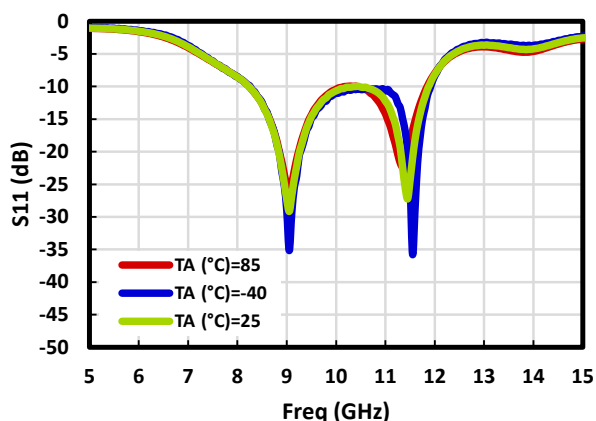
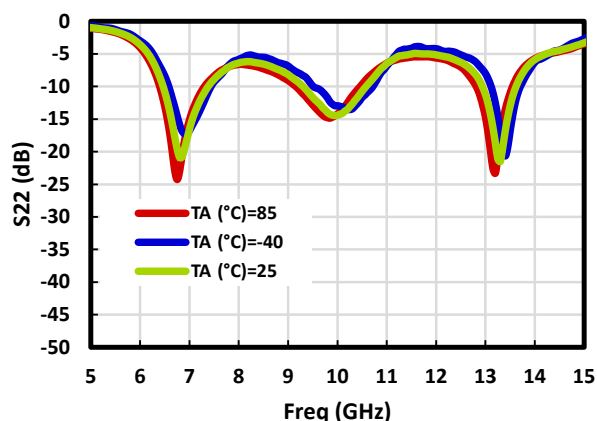


Figure 1-3. S_{22} vs Freq



1.3 Large Signal Performance

Typical Pulsed Power Data

Test conditions: $V_D=28V$, $I_{DQ}=400mA$, $T_A=25^\circ C$, Pulsed 10% (100 μs /1ms)

Figure 1-4. P_{out} vs. P_{in}

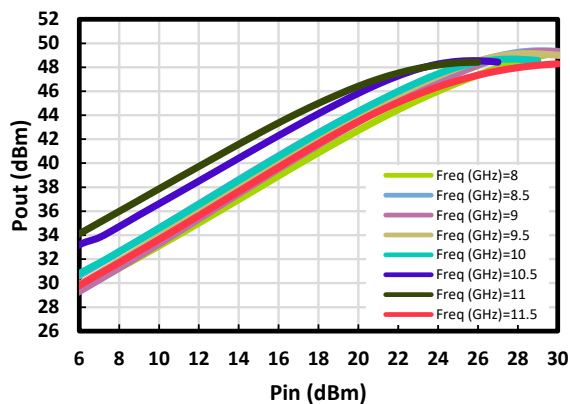


Figure 1-5. Gain vs. P_{out}

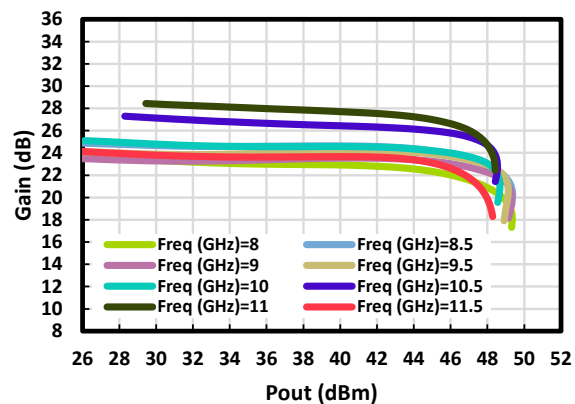


Figure 1-6. PAE vs. P_{out}

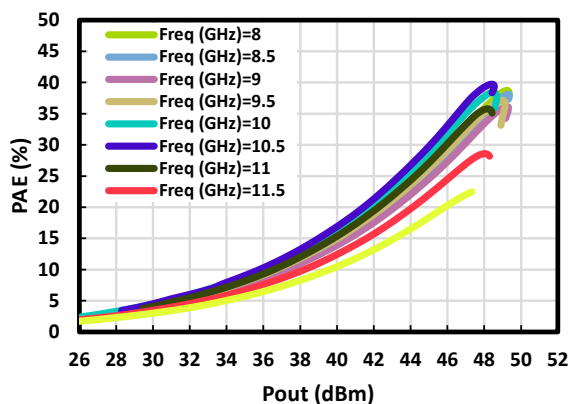


Figure 1-7. I_D vs. P_{out}

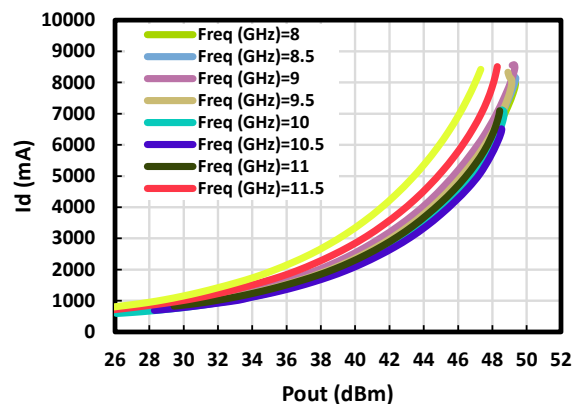


Figure 1-8. P_{out} vs. Freq

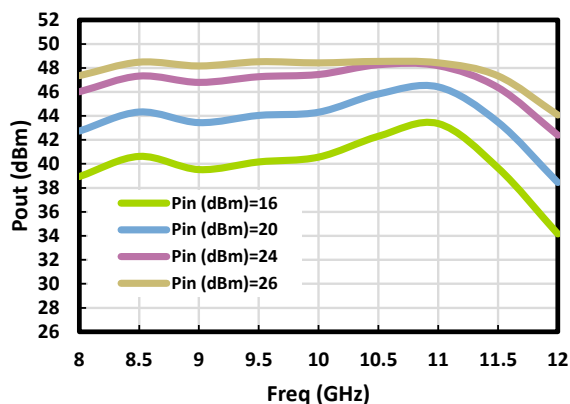
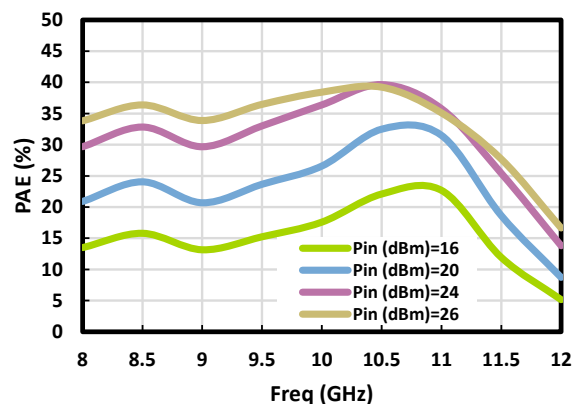


Figure 1-9. PAE vs. Freq



Typical Pulsed Power Data over T_A Conditions

Test conditions: $V_D=28V$, $I_{DQ}=400mA$, Pulsed 10% (100 μs /1ms)

Figure 1-10. P_{out} vs. P_{in} , Freq=8GHz

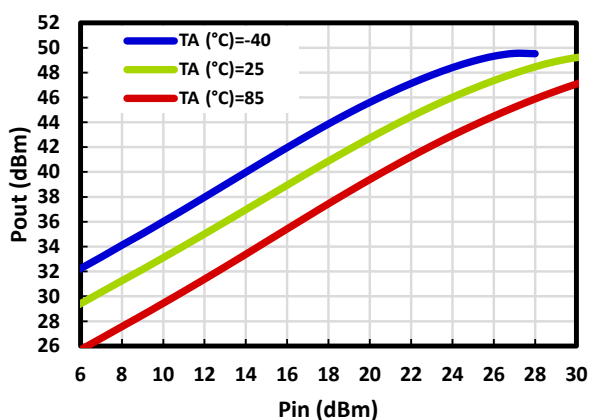


Figure 1-11. P_{out} vs. P_{in} , Freq=9GHz

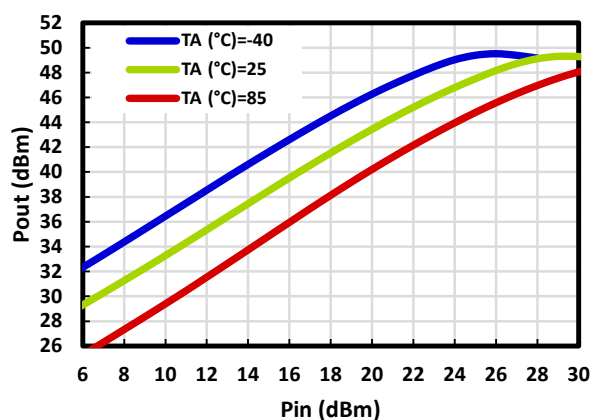


Figure 1-12. P_{out} vs. P_{in} , Freq=10GHz

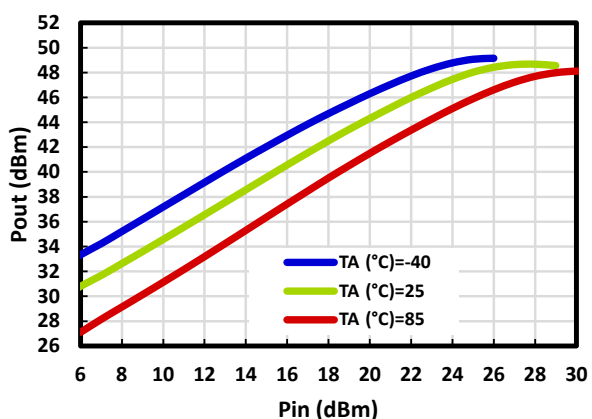


Figure 1-13. P_{out} vs. P_{in} , Freq=11GHz

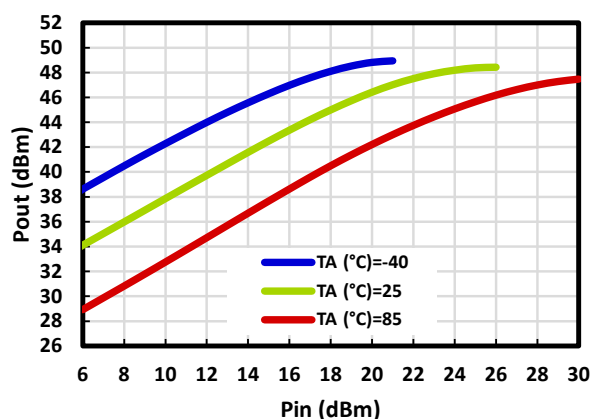


Figure 1-14. P_{out} vs. Freq

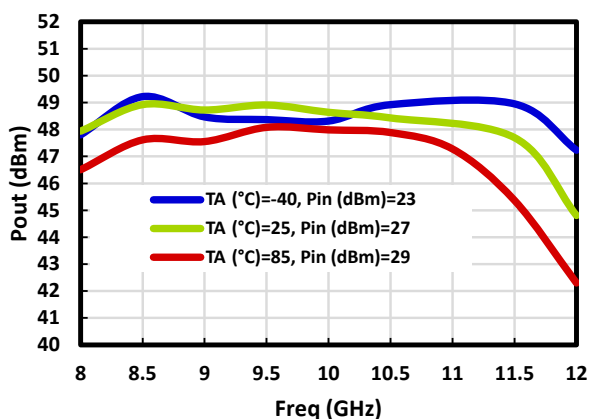
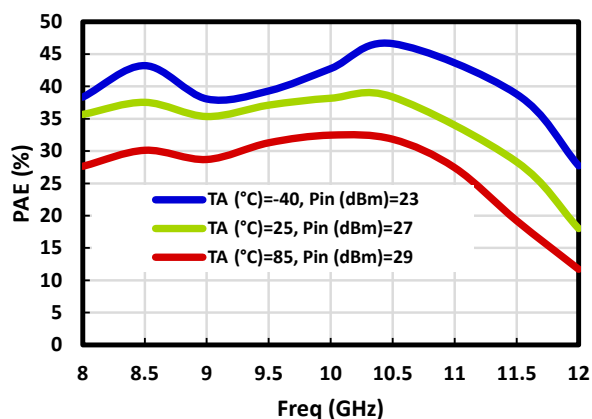
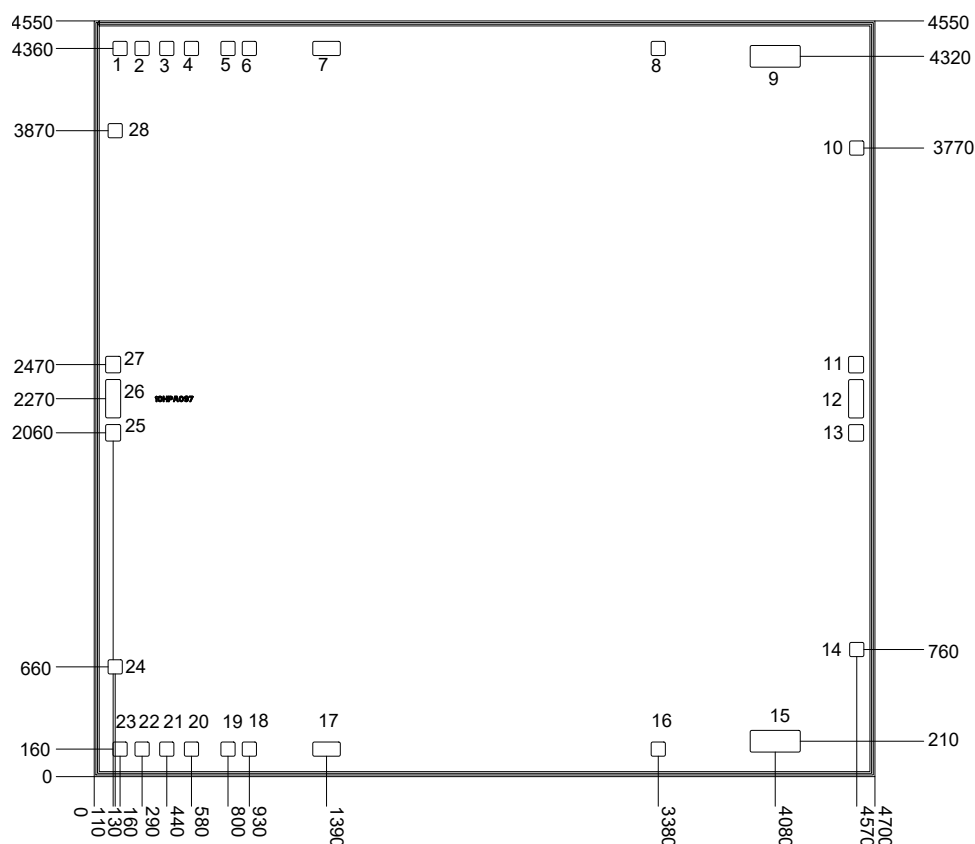


Figure 1-15. PAE vs. Freq



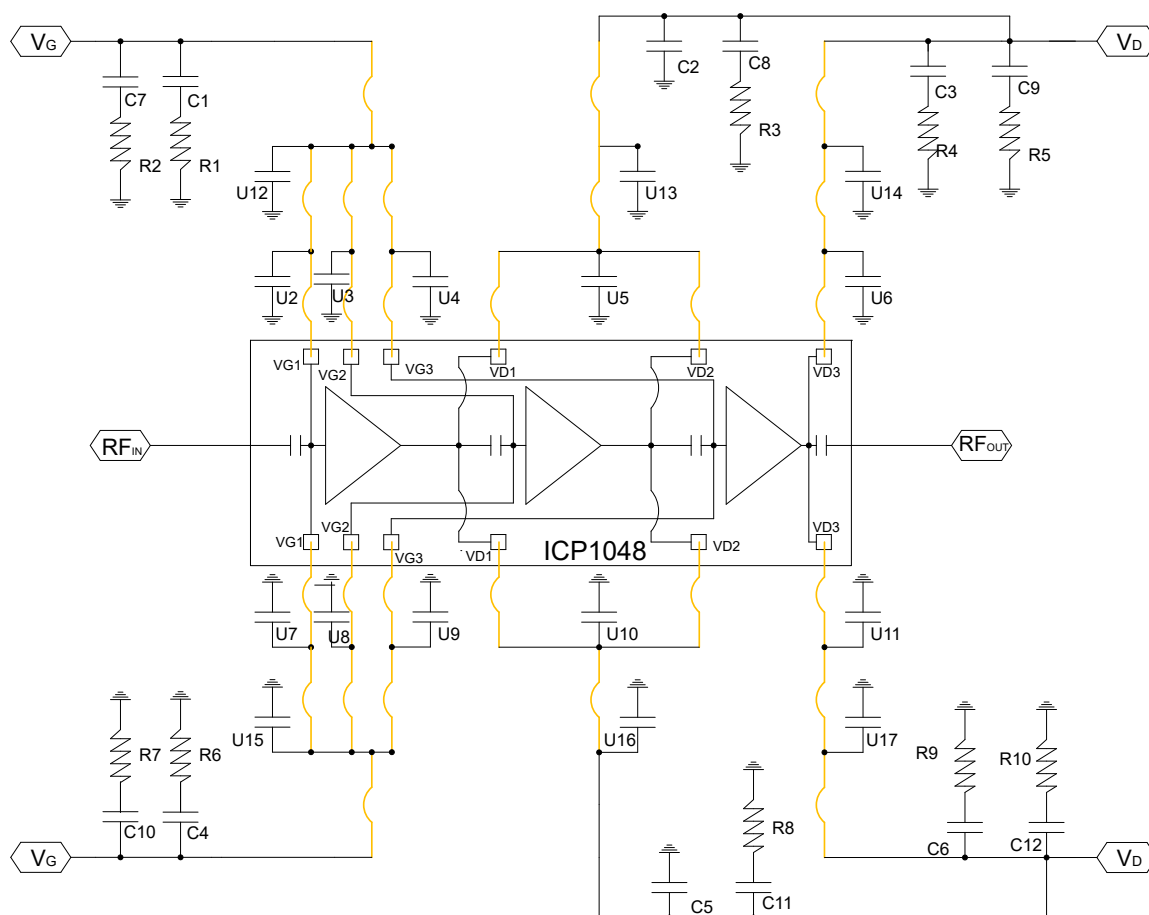
2. Mechanical Drawing



Units: μm | Thickness: 0.1mm | Backside of Die is RF and DC ground

Pad No	Pad size (μm)	Function	Description
1, 6, 8, 10, 14, 16, 18, 22, 24, 28	85 x 85	No Connect	Pad can be connected to ground or left open circuit
2, 22	85 x 85	V_{G1}	Gate bias, decoupling and bypass caps required. Bias must be applied to both pins
3, 21	85 x 85	V_{G2}	Gate bias, decoupling and bypass caps required. Bias must be applied to both pins
4, 20	85 x 85	V_{G3}	Gate bias, decoupling and bypass caps required. Bias must be applied to both pins
5, 19	85 x 85	V_{D1}	Drain bias, decoupling and bypass caps required. Bias must be applied to both pins
7, 17	165 x 85	V_{D2}	Drain bias, decoupling and bypass caps required. Bias must be applied to both pins
9, 15	300 x 130	V_{D3}	Drain bias, decoupling and bypass caps required. Bias must be applied to both pins
11, 13, 25, 27	99 x 90	GND	Ground connection
12	90 x 230	RF_{out}	50 Ω RF output. DC blocked
26	90 x 230	RF_{in}	50 Ω RF input. DC blocked
Backside of Chip	4700 x 4550	GND	RF and DC ground

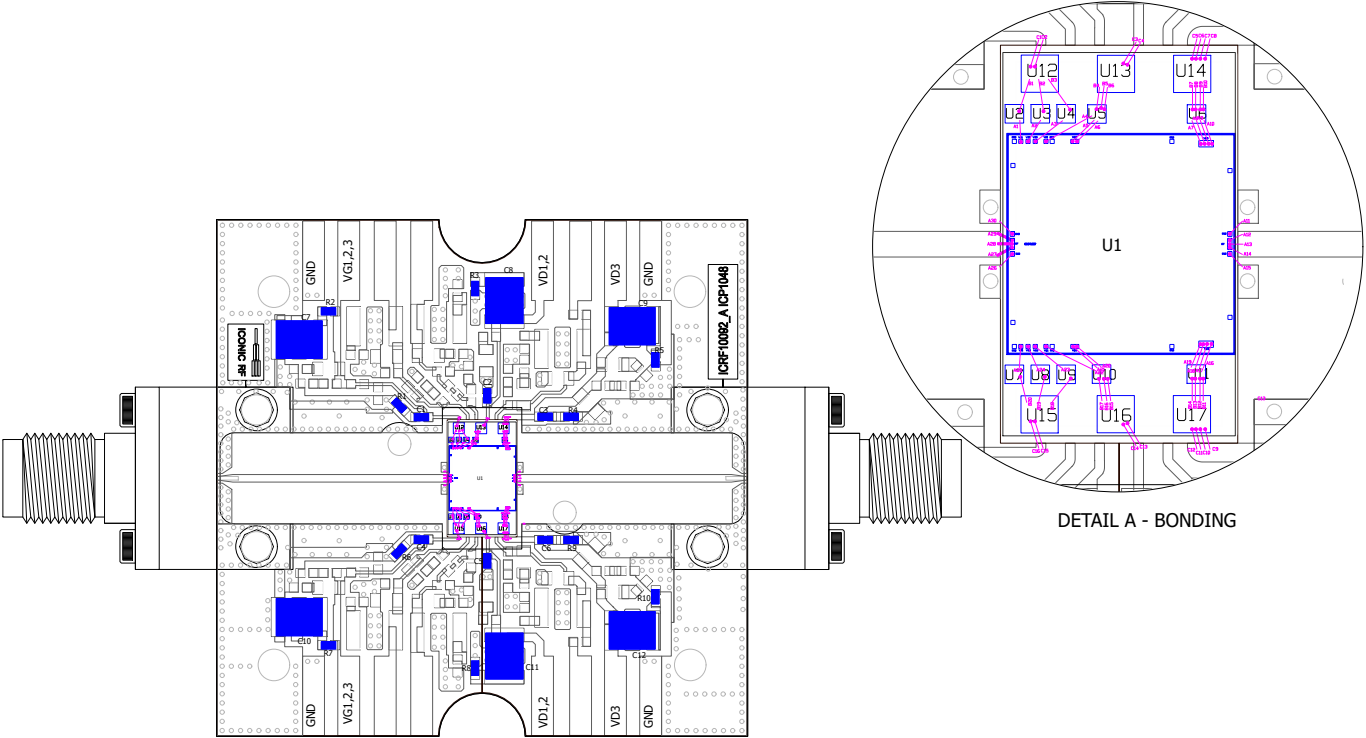
3. Application Circuit



Bill of materials

Component ID	Value	Details	Manufacturer Part No.
U2 - U11	100pF	MIM Capacitor	Various
U12 - U17	10nF	MIM Capacitor	Various
C1 - C6	10nF	10nF Capacitor,10%,50V,0402	Various
C7 - C12	10μF	10μF Capacitor,10%,50V,1206	Various
R1 - R10	5.1Ω	5.1Ω Resistor, 0402	Various

4. Evaluation Board



Die Attach Methods

PCB Construction	Details
Top & Bottom Layer	0.5oz Cu + ENEPIG
Electroless Nickel	3-6µm
Electroless Palladium	0.05-0.3µm
Immersion Gold	0.04-0.06µm

Key Features	Details
Dielectric	RO4003C
Overall Thickness	Approx 0.27mm
VIA Plating Thickness	>15µm

5. Other considerations

Assembly Guidance

Interconnect assembly Notes	Die attach using Eutectic
- Ball Bonding is preferred technique - Force, time and ultrasonic parameters are critical. - Aluminum wire bonding is not recommended. - Bond Wire diameter of 1mil is recommended.	- Flux-less gold-tin (AuSn) (80% Au, 20% Sn with a melting point of 280°C) preform is preferred between the die and attached surface. - Recommended preform should be approximately 0.0012" thick. - Die bonder using heated collet with a temperature of 310°C and die scrubbing should be used to ensure wetting and prevent formation of voids. - Exposure to extreme temperature should be kept to a minimum. - The optimum die attach environment is nitrogen atmosphere.
Die attach of component using adhesive	Re-flow Process
- Vacuum collets are preferred method of pickup. - Pickup method must consider the avoidance of die air bridges. - Die suitable for Eutectic and Epoxy die attach. - Where Epoxy is used, high thermal conductivity Silver Sintered Epoxy is recommended:- - Kyocera CT2700R7S - Namics H9889-1	- Maximum temperature 320°C for 30 seconds. - Material matching for coefficient of thermal expansion is crucial for long-term reliability

Optimum RF power performance achieved by minimizing output RF bond wire length.

For optimum RF and thermal performance IconicRF recommends the die assembly base plate is adequately bolted to an forced air heat sink using a thermal graphite interface pad (Graphite Interface Material GCSP-017-G 170µm thick) for optimal heat transfer. There are many variables of the second level assembly between the die base plate and heat sink that IconicRF are unable to control and the following guidance is provided as information only. Fixing bolts should be provided as close to the die as possible to ensure an optimum pressure between the base plate and the heat sink. The bolting screws used to attach the PCB assembly to the heat sink must include washers and be tightened with a suitable tightening pattern to ensure a uniform pressure. It is advised all surfaces be cleaned and be free of grease and dust prior to fully aligning the assembly with all screws located and tightened to finger tight. Further torquing of the screws must be achieved in multiple phases using a star shaped pattern to a recommended torque of 2.5N/m.

Bias-up procedure

1. Set V_G to -5V
2. Set V_D to 28V
3. Adjust V_G positive until I_D quiescent is 400mA
4. Limit I_D to 10A
5. Apply RF signal

Bias-down procedure

1. Turn off RF
2. Turn off V_D , allow drain capacitors to discharge
3. Turn off V_G

6. Ordering, Shipping, and Handling

Handling Recommendations

Integrated circuits are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. It is recommended to follow all procedures and guidelines outlined in the Microsemi application note AN01: GaAs MMIC Handling and Die Attach Recommendations.

Ordering Information

For additional ordering information, contact your Microchip sales representative.

Part Number	Description
ICP1048-1-110I	Gel Pak Au Backed
ICP1048-1-101I	Wafer on expander ring
ICP1048-1-103I	Wafer on metal frame
EV48G16A	Evaluation Board with SMA connectors (ICP1048-1-110I PCB Assembly)

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