HT0440

Dual High-Voltage Isolated MOSFET Driver

Features

- ±400V Input to Output Isolation
- ±700V Isolation between Outputs
- No External Voltage Supply Required
- Dual Isolated Output Drivers
- Internal and External Clock Options

Applications

- Telecommunications
- Modems
- Solid-state Relays
- High-side Switches
- High-end Audio Switches
- Avionics
- Automatic Test Equipment

General Description

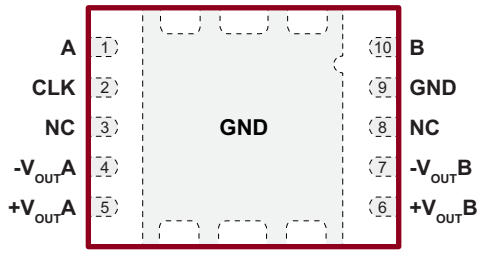
HT0440 is a dual high-voltage isolated MOSFET driver that uses HVCMOS technology. It is designed to drive discrete MOSFETs configured as bidirectional or unidirectional switches. In addition, it can drive N-channel MOSFETs as high-side switches up to 400V. The HT0440 generates two independent DC-isolated voltages to the outputs $V_{OUT}A$ and $V_{OUT}B$ when logic inputs A and B are at logic high.

The internal clock of the HT0440 can be disabled by applying an external clock signal to the CLK pin. This allows the power dissipation and AC characteristics to be customized to meet specific needs. The CLK pin should be connected to ground when not in use. The HT0440 does not require any external power supplies. The internal supply voltage is provided by either of the two logic inputs, A or B, when these inputs are at logic high.

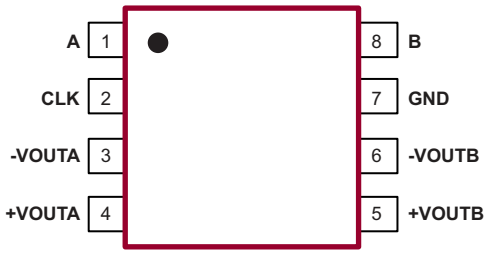
For detailed circuit application information, please refer to application note, *AN-D26 High-Voltage Isolated MOSFET Driver*.

Package Types

10-lead (3 X 4) DFN
(Top View)

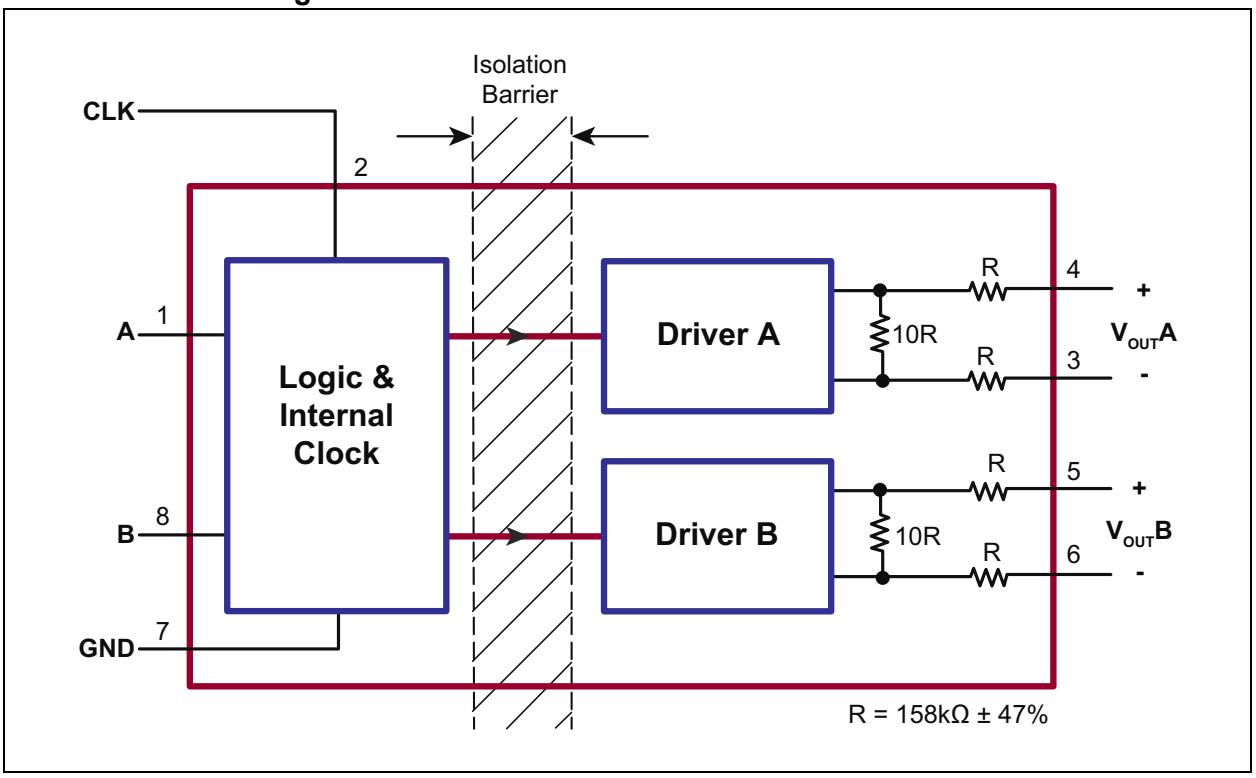


8-lead SOIC (Narrow Body)
(Top View)



Refer to Table 2-1 and Table 2-2 for pin information.

Functional Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings†

Input to Output Isolation Voltage, V_{ISO} ..... ±400V
Logic Input Voltage, V_A, V_B ..... –0.5V to +7V
Maximum Junction Temperature, T_{JMAX} ..... +125°C
Storage Temperature, T_S ..... –55°C to +150°C
Maximum Junction Temperature, T_J ..... +125°C

† Notice: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
External Clock Frequency	CLK	0.5	—	2	MHz	
Clock Input High Voltage	V_{IHCLK}	3.15	—	5.5	V	
Clock Input Low Voltage	V_{ILCLK}	0	—	0.5	V	
Logic Input High Voltage	V_{IH}	3.15	—	5.5	V	
Logic Input Low Voltage	V_{IL}	0	—	0.5	V	
Operating Temperature	T_A	–40	—	+85	°C	

DC ELECTRICAL CHARACTERISTICS

Electrical Specifications: T_A = 25°C unless otherwise indicated.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Total Logic High Input Current	$I_{HA} + I_{HB}$	—	—	300	µA	V_A = 3.5V, V_B = 3.5V, CLK = 0V
		—	—	500	µA	V_A = 3.5V, V_B = 3.5V, CLK = 500 kHz
		—	—	2	mA	V_A = 3.5V, V_B = 3.5V, CLK = 2 MHz
		—	—	1	mA	V_A = 5.5V, V_B = 5.5V, CLK = 0V
		—	—	2	mA	V_A = 5.5V, V_B = 5.5V, CLK = 500 kHz
Output Voltage	V_{OUTA}, V_{OUTB}	6	—	—	V	V_A = 3.15V, V_B = 3.15V, CLK = 0V, No load
		5	—	—	V	V_A = 3.15V, V_B = 3.15V, CLK = 500 kHz, No load
		6	—	—	V	V_A = 3.15V, V_B = 3.15V, CLK = 2 MHz, No load
		10	—	—	V	V_A = 4.5V, V_B = 4.5V, CLK = 0V, No load
		8	—	—	V	V_A = 4.5V, V_B = 4.5V, CLK = 500 kHz, No load
Logic Low Input A Current	I_{ILA}	—	—	10	µA	V_A = 0.5V, V_B = High
Logic Low Input B Current	I_{ILB}	—	—	10	µA	V_A = High, V_B = 0.5V
Quiescent Current	I_{ILQ}	—	—	10	µA	V_A = 0.5V, V_B = 0.5V
Input to Output Isolation Voltage	V_{ISO}	±400	—	—	V	
Output to Output Isolation Voltage	V_{CISO}	±700	—	—	V	

AC ELECTRICAL CHARACTERISTICS

Electrical Specifications: T_A = 25°C unless otherwise indicated.						
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Turn-on Delay Time	$t_{d(ON)}$	—	—	50	µs	See **Timing Waveforms** and **Test Circuit**. CLK = 0V, CL = 600 pF
Rise Time	t_r	—	—	650	µs	
Turn-off Delay Time	$t_{d(OFF)}$	—	—	150	µs	
Fall Time	t_f	—	—	3	ms	

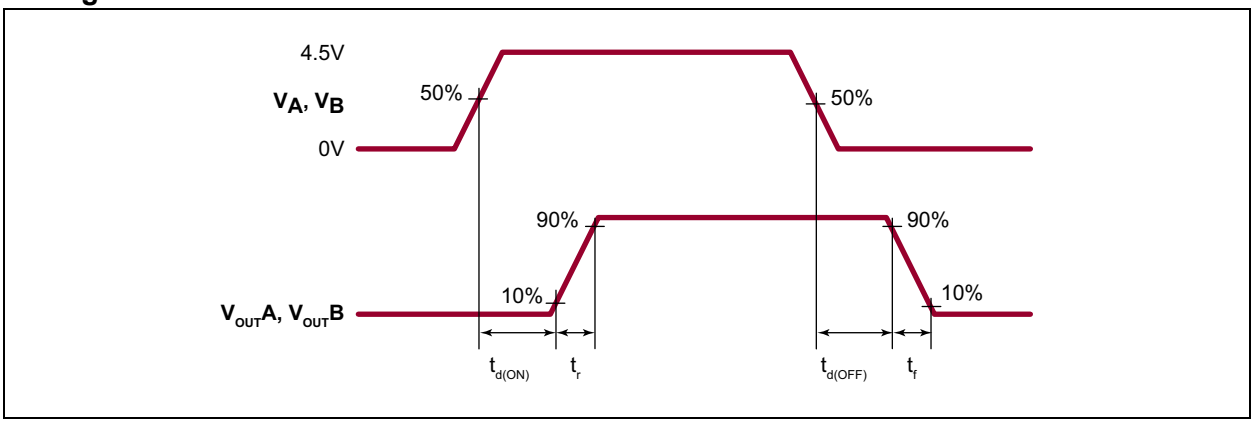
TEMPERATURE SPECIFICATIONS

Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
TEMPERATURE RANGES						
Junction Temperature	T_J	—	—	+125	°C	
Operating Temperature	T_A	–40	—	+85	°C	
Storage Temperature	T_S	–55	—	+150	°C	
PACKAGE THERMAL RESISTANCES						
10-lead DFN	θ_{JA}	—	40	—	°C/W	
8-lead SOIC (Narrow Body)	θ_{JA}	—	101	—	°C/W	

TABLE 1-1: TRUTH TABLE

A	**B**	**CLK**	**V_{OUT}A**	**V_{OUT}B**	**Internal Clock**
0	0	0	OFF	OFF	OFF
0	⌐¬	0	OFF	ON	ON
⌐¬	0	0	ON	OFF	ON
1	1	0	ON	ON	ON
0	0	CLK	OFF	OFF	OFF
0	⌐¬	CLK	OFF	ON	OFF
⌐¬	0	CLK	ON	OFF	OFF
1	1	CLK	ON	ON	OFF

Timing Waveforms



2.0 PIN DESCRIPTION

The details on the pins of HT0440 are listed in Table 2-1 and Table 2-2. Refer to **Package Types** for the location of pins.

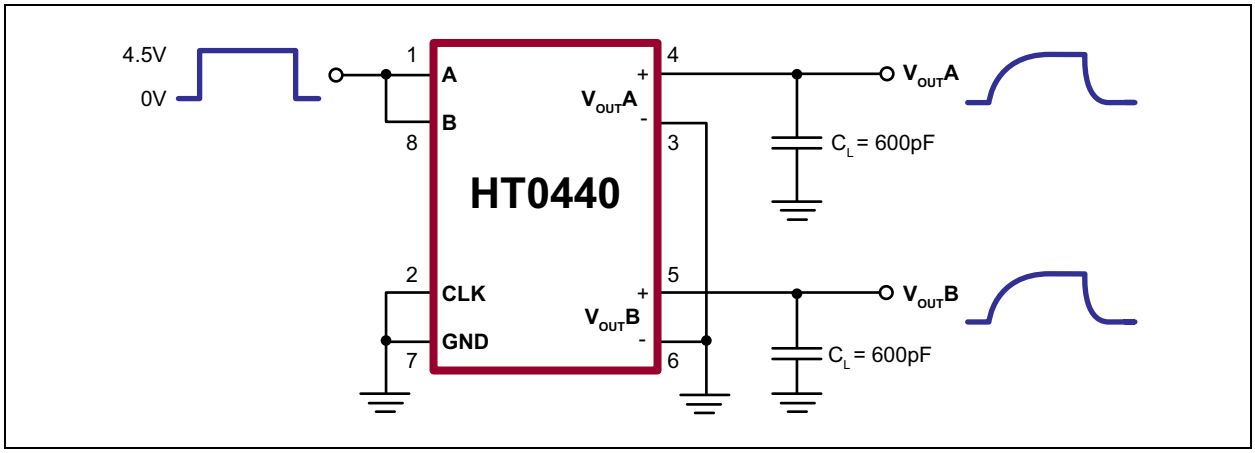
TABLE 2-1: 10-LEAD DFN PIN TABLE

Pin Number	Pin Name	Description
1	A	Logic input for controlling Output A.
2	CLK	Clock input for the IC. Connect to GND to use internal clock. Connect to external clock signal to use external Clock. External clock frequency should be between 500 kHz and 2 MHz.
3	NC	No connect pin. Leave unconnected.
4	–VOUTA	Channel A isolated output. +VOUTA is the positive terminal and –VOUTA is the negative terminal. Connect to the load.
5	+VOUTA	
6	+VOUTB	Channel B isolated output. +VOUTB is the positive terminal and –VOUTB is the negative terminal. Connect to the load.
7	–VOUTB	
8	NC	No connect pin. Leave unconnected.
9	GND	GND connection. Connect to GND of the input digital signals.
10	B	Logic input for controlling Output B.
Thermal pad	GND	GND connection. Connect to GND of the input digital signals.

TABLE 2-2: 8-LEAD SOIC PIN TABLE

Pin Number	Pin Name	Description
1	A	Logic input for controlling Output A.
2	CLK	Clock input for the IC. Connect to GND to use internal clock. Connect to external clock signal to use external Clock. External clock frequency should be between 500 kHz and 2 MHz.
3	–VOUTA	Channel A isolated output. +VOUTA is the positive terminal and –VOUTA is the negative terminal. Connect to the load.
4	+VOUTA	
5	+VOUTB	Channel B isolated output. +VOUTB is the positive terminal and –VOUTB is the negative terminal. Connect to the load.
6	–VOUTB	
7	GND	GND connection. Connect to GND of the input digital signals.
8	B	Logic input for controlling Output B.

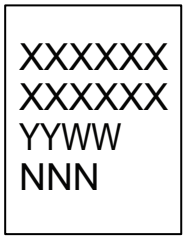
Test Circuit



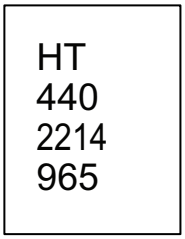
3.0 PACKAGING INFORMATION

3.1 Package Marking Information

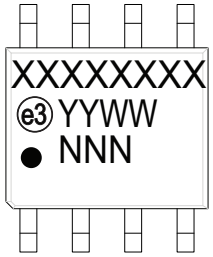
10-lead DFN



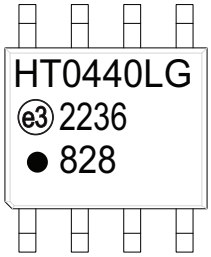
Example



8-lead SOIC



Example

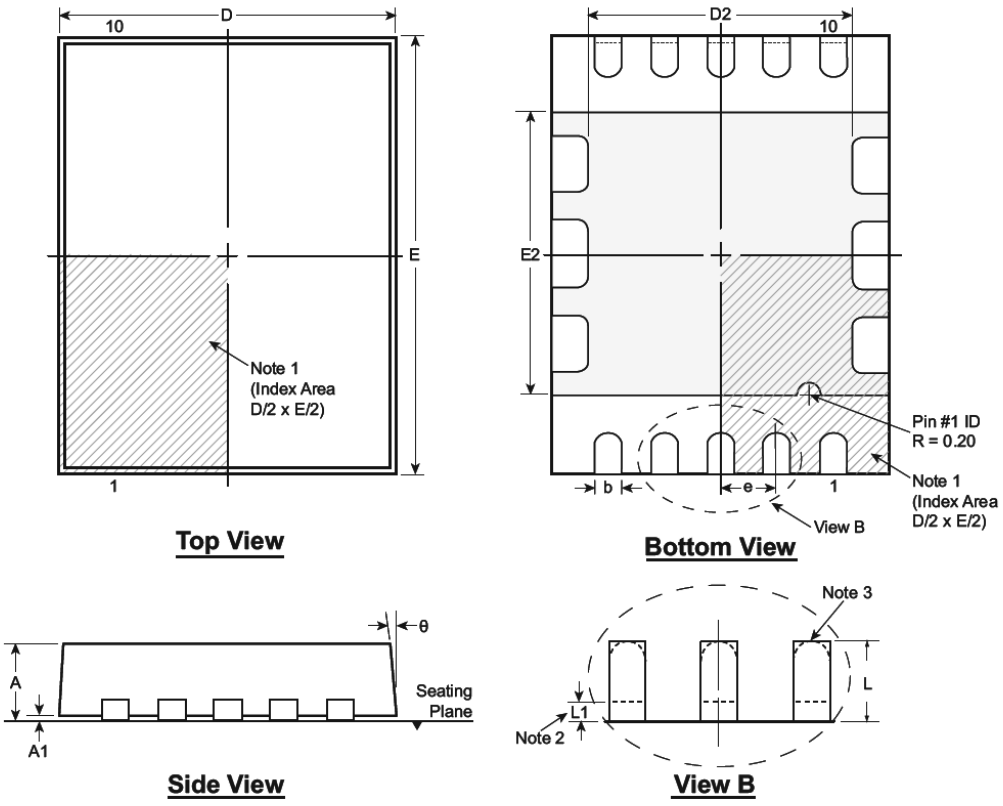


Legend:	XX...X	Product Code or Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for product code or customer-specific information. Package may or not include the corporate logo.

10-Lead DFN Package Outline (K6)

3.00x4.00mm body, 1.00mm height (max), 0.50mm pitch



Note: For the most current package drawings, see the Microchip Packaging Specification at www.microchip.com/packaging.

Notes:

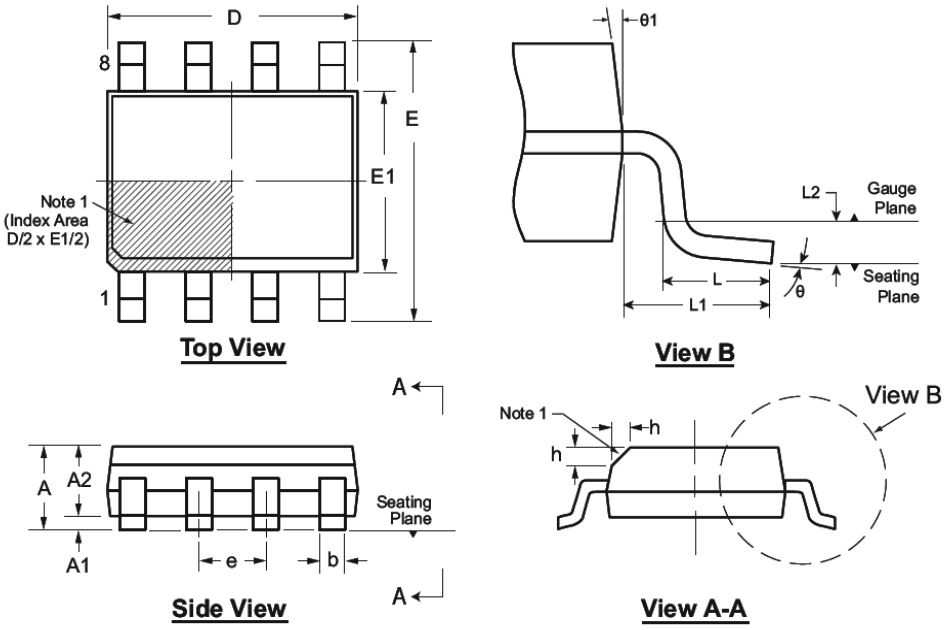
1. *A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*
2. *Depending on the method of manufacturing, a maximum of 0.15mm pullback (L1) may be present.*
3. *The inner tip of the lead may be either rounded or square.*

Symbol		A	A1	b	D	D2	E	E2	e	L	L1	θ
Dimension (mm)	MIN	0.80	0.00	0.18	2.95	2.20	3.95	2.50	0.50 BSC	0.30	0.00	0°
	NOM	0.90	0.02	0.25	3.00	2.35	4.00	2.65		0.40	-	-
	MAX	1.00	0.05	0.30	3.05	2.45	4.05	2.75		0.50	0.15	14°

Drawings not to scale.

8-Lead SOIC (Narrow Body) Package Outline (LG/TG)

4.90x3.90mm body, 1.75mm height (max), 1.27mm pitch



Note: For the most current package drawings, see the Microchip Packaging Specification at www.microchip.com/packaging.

Note:

1. This chamfer feature is optional. A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.

Symbol		A	A1	A2	b	D	E	E1	e	h	L	L1	L2	θ	θ1
Dimension (mm)	MIN	1.35*	0.10	1.25	0.31	4.80*	5.80*	3.80*	1.27 BSC	0.25	0.40	1.04 REF	0.25 BSC	0°	5°
	NOM	-	-	-	-	4.90	6.00	3.90		-	-			-	-
	MAX	1.75	0.25	1.65*	0.51	5.00*	6.20*	4.00*		0.50	1.27			8°	15°

JEDEC Registration MS-012, Variation AA, Issue E, Sept. 2005.

** This dimension is not specified in the JEDEC drawing.*

Drawings are not to scale.

APPENDIX A: REVISION HISTORY

Revision A (September 2022)

- Converted Supertex Doc# DSFP-HT440 to Microchip DS20005606A.
- Made minor text changes throughout the document.

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

PART NO.	XX	-	X	-	X
Device	Package Options		Environmental		Media Type

Device:	HT0440	=	Dual High-Voltage Isolated MOSFET Driver
Package:	K6	=	10-lead (3 x 4) DFN
	LG	=	8-lead SOIC
Environmental:	G	=	Lead (Pb)-free/RoHS-compliant Package
Media Type:	(blank)	=	3300/Reel for an KG Package
			3300/Reel for an LG Package

Examples:

a) HT0440K6-G: Dual High-Voltage Isolated MOSFET Driver, 10-lead (3 x 4) DFN Package, 3300/Reel

b) HT0440LG-G: Dual High-Voltage Isolated MOSFET Driver, 8-lead SOIC Package, 3300/Reel

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