ASFLMPA series

Plastic SMD MEMS Clock Oscillator

Description

The Abracon ASFLMPA series is a programmable MEMS oscillator, with a continuous operating power supply ranging from 2.25V to 3.63V. This series features low power consumption, a wide frequency range, exceptional phase noise, tight stabilities, and short lead times for industrial, consumer, and other applications. The ASFLMPA series comes in a 5.0 x 3.2 mm compact package with CMOS, HCSL, LVDS, or LVPECL output logic.

Features

- Extended Operating Temperature at -40 to +125°C (LVDS and CMOS only)
- MIL-STD-883 shock and vibration compliant
- Durable QFN Plastic Compact Packaging
- Tri-State or Power Down functions
- PCIe Gen1-6 Compliant Output
- Low RMS Jitter 650 fs (typ.)
- REACH/RoHS II Compliant | MSL Level 1

Applications

- Storage Area Networks (SATA, SAS, Fiber Channel)
- Passive Optical Networks (EPON, 10G-EPON, GPON, 10G-PON)
- Ethernet (1G, 10GBASE-T,/KR/LR/SR, FCoE)
- PCI Express
- Display port

Key Electrical Specifications

Parameters		Min.	Typ.	Max.	Units	Notes
Frequency Range	CMOS	2.5000		170.0000	MHz	-20 ~ +70°C -40 ~ +85°C -40 ~ +105°C -40 ~ 125°C
	LVPECL	2.5000		450.0000		-20 ~ +70°C -40 ~ +85°C -40 ~ +105°C
	LVDS	2.3000		450.0000		-20 ~ +70°C -40 ~ +85°C -40 ~ +105°C -40 ~ +125°C
	HCSL	2.3000		450.0000		-20 ~ +70°C -40 ~ +85°C -40 ~ +105°C
Operating Temperature		-20		+70	°C	See options
Storage Temperature		-55		+150	°C	
Overall Frequency Stability Note 4		-50		+50	ppm	See options
Supply Voltage (V_{dd}) Note 1		+2.25		+3.63	V	
Startup Time (t_{SU}) Note 2			5.5	6	ms	
Enable Time (t_{EN})				350	ns	OE Option
				6	ms	Power Down Option

Key Electrical Specifications Cont. - CMOS, LVPECL, LVDS, and HCSL

Parameters	Min.	Typ.	Max.	Units	Notes
Disable Time (t_{DA}) Note 3			25	ns	
Disable Current		2.5	5	µA	Power Down Option
		23		mA	OE Option
Tri-state Function (Standby/Disable)	"1" (VIH≥0.75*Vdd) or Open: Oscillation "0" (VIL<0.25*Vdd): Hi Z			V	1.5MΩ pull-up resistor embedded
Aging	-5.0		+5.0	ppm	First year @ 25°C
	-1.0		+1.0		Note 5

Note 1: VDD pin should be filtered with 0.1 µF capacitor.
Note 2: tSU is time to 100 ppm stable output frequency after VDD is applied and outputs are enabled.
Note 3: tDA: See the Output Waveforms and the Test Circuits sections for more information.
Note 4: Includes frequency variations due to initial tolerance, temperature and power supply voltage.
Note 5: Per year after first year

Key Electrical Specifications - CMOS (VDD = 2.5V±10% or 3.3V±10%, T=-40 ~ +125°C)

Parameters		Min.	Typ.	Max.	Units	Notes
Supply Current (Idd)			27		mA	CL= No Load, 100MHz
Output Logic Level	V_{OH}	0.8*Vdd			V	I_{OH}/I_{OL}=±12mA
	V_{OL}			0.2*Vdd	V	
Rise Time	Tr		1.2		ns	CL=15pF 20% to 80%
Fall Time	Tf		1.1		ns	
Duty Cycle		45		55	%	
Integrated Phase Jitter (J_{PH})			0.65		ps_{RMS}	12kHz ~ 20MHz @ 100MHz
Period Jitter (J_{PTP}, pk-pk)			25		ps	@100MHz
Cycle-to-Cycle Jitter (J_{CC}, Peak)			22		ps	@100MHz

Key Electrical Specifications – LVPECL (VDD = 2.5V±10% or 3.3V±10%, T =-40 ~ +105°C)

Parameters		Min.	Typ.	Max.	Units	Notes
Supply Current (Idd)			50		mA	RL = 50Ω
Output Logic Level	V_{OH}	V_{dd}-1.145			V	RL = 50Ω
	V_{OL}			V_{dd}-1.695	V	
Peak to Peak Output Swing (Vpp)			800		mV	Single ended
Rise Time	Tr		200	250	ps	RL=50Ω, 20% to 80%
Fall Time	Tf		250	300		
Duty Cycle		48		52	%	Differential
Integrated Phase Jitter (J_{PH})			0.65		ps_{RMS}	12kHz ~ 20MHz, @ 156.25MHz
Period Jitter RMS (J_{PER})			2.0		ps	10k cycles, @156.25MHz
Period Jitter (J_{PTP}, pk-pk)			20		ps	10k cycles, @156.25MHz

Key Electrical Specifications – LVDS (VDD = 2.5V±10% or 3.3V±10%, T =-40 ~ +105°C)

Parameters		Min.	Typ.	Max.	Units	Notes
Supply Current (Idd)			32		mA	RL = 100Ω
Output Offset Voltage (V_{OS})		1.15	1.25	1.35	V	RL = 100Ω differential
Peak to Peak Output Swing (Vpp)		250	350	450	mV	Single ended
Rise Time	Tr	120	170	220	ps	RL=100Ω, 20% to 80%
Fall Time	Tf					
Duty Cycle		48		52	%	Differential
Integrated Phase Jitter (J_{PH})			0.65		ps_{RMS}	12kHz ~ 20MHz, @156.25MHz, T =-40 ~ +105°C
			0.9			2kHz ~ 20MHz, @156.25MHz, T =-40 ~ +105°C
Phase Jitter (J_{RMS-CC})			0.025	0.1	ps_{RMS}	PCIe Gen 6.0, 64 GT/s
Period Jitter RMS (J_{PER})			2.5		ps	10k cycles, @156.25MHz
Period Jitter (J_{PTP}, pk-pk)			20			10k cycles, @156.25MHz
Period Jitter RMS (J_{PER})			3.0			T =-40 ~ +105°C, @156.25MHz
Period Jitter (J_{PTP}, pk-pk)			25			T =-40 ~ +105°C, @156.25MHz

Key Electrical Specifications – HCSL (VDD = 2.5V±10% or 3.3V±10%, T =-40 ~ +105°C)

Parameters		Min.	Typ.	Max.	Units	Notes
Supply Current (Idd)			40		mA	RL = 50Ω
Output Logic Level	V_{OH}	0.64			V	RL = 50Ω
	V_{OL}			0.1	V	
Peak to Peak Output Swing (Vpp)			750		mV	Single ended
Rise Time	Tr	200	260	400	ps	RL=50Ω, 20% to 80%
Fall Time	Tf	250	370	500		
Duty Cycle		48		52	%	Differential
Integrated Phase Jitter (J_{PH})			0.617		ps_{RMS}	12 kHz to 20 MHz, @100 MHz T = –40°C to +105°C
			0.460			100 kHz to 20 MHz, @100 MHz T = –40°C to +105°C
			0.212			1.875 MHz to 20 MHz, @100 MHz, T = –40°C to +105°C
Phase Jitter	T_J Note 6		3.42	86	ps_{PP}	PCIe Gen 1.1, TJ = DJ +14.069 x RJ (BER 10–12)
	$J_{RMS-CCHF}$ Note 6		0.247	3.1	PS_{RMS}	PCIe Gen 2.1, 1.5 MHz to Nyquist
	$J_{RMS-CCHF}$ Note 6		0.08	3.0	PS_{RMS}	PCIe Gen 2.1, 10 kHz to 1.5 MHz
	J_{RMS-CC}		0.107	1.0	PS_{RMS}	PCIe Gen 3.0 Note 6
			0.107	0.30		PCIe Gen 4.0, 16 GT/s
			0.043	0.12		PCIe Gen 5.0, 32 GT/s
			0.054	0.1		PCIe Gen 6.0, 64 GT/s
Period Jitter RMS (J_{PER})			2		ps	T =-40 ~ +105°C, @100MHz
Period Jitter (J_{PTP}, pk-pk)			16		ps	T =-40 ~ +105°C, @100MHz

Note 6: Jitter limits are established by Gen 1.1, Gen 2.1, and Gen 3.0 PCIe standards

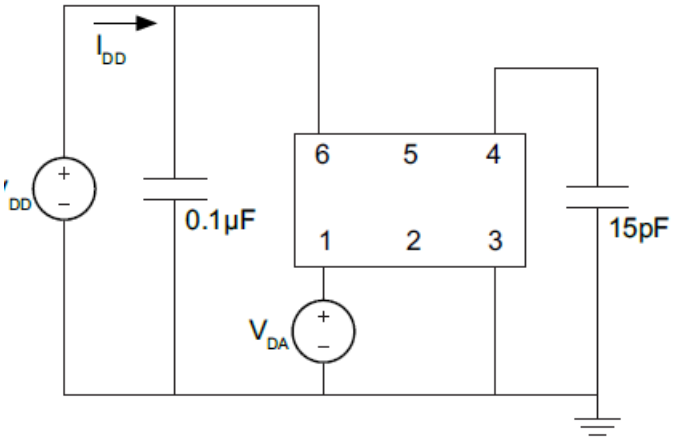
Absolute Maximum Ratings

Item	Min.	Max.	Units
Supply voltage	-0.3	+4.0	V
Input voltage	-0.3	Vdd+0.3	V
Junction Temp.		+150	°C
Storage Temp.	-55	+150	°C
Soldering Temp.		+260	°C
ESD HBM MM CDM		 4,000 400 1,500	V

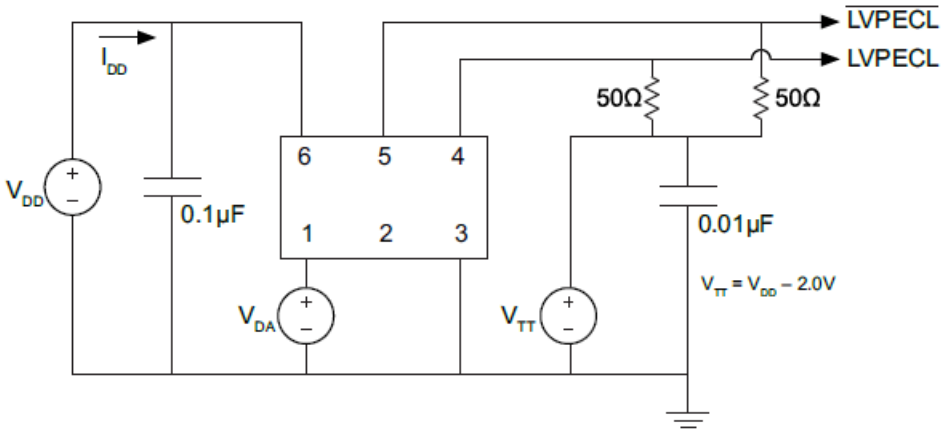
Note: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability. The data sheet limits are not guaranteed if the device is operated beyond the recommended operating conditions.

Recommended Test Circuit (Unless specified otherwise: T=25° C, VDD=3.3 V)

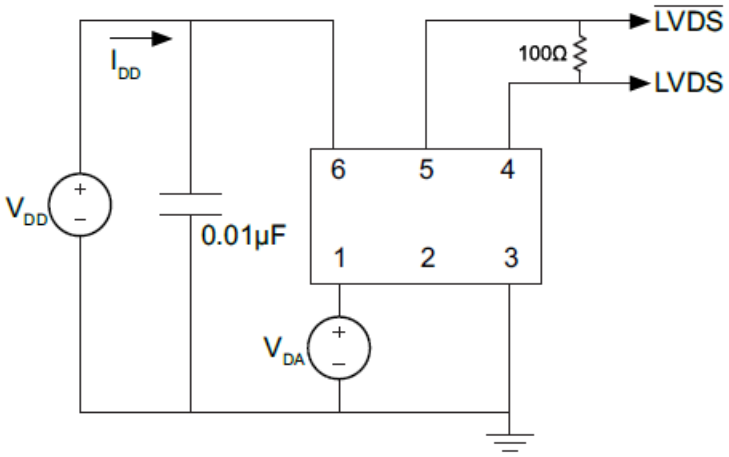
CMOS Test Circuit



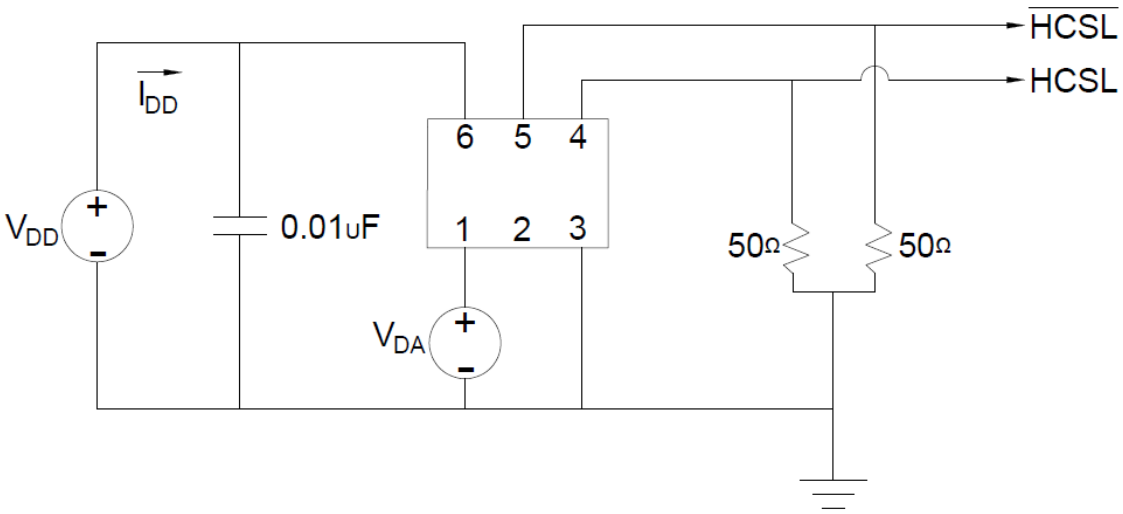
LVPECL Test Circuit



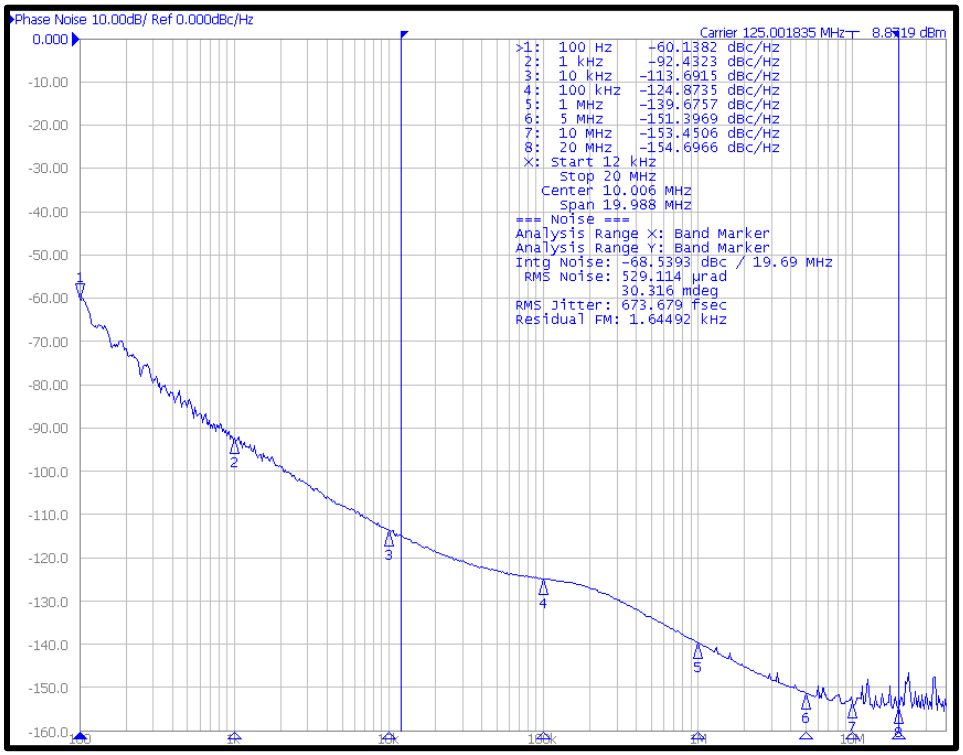
LVDS Test Circuit



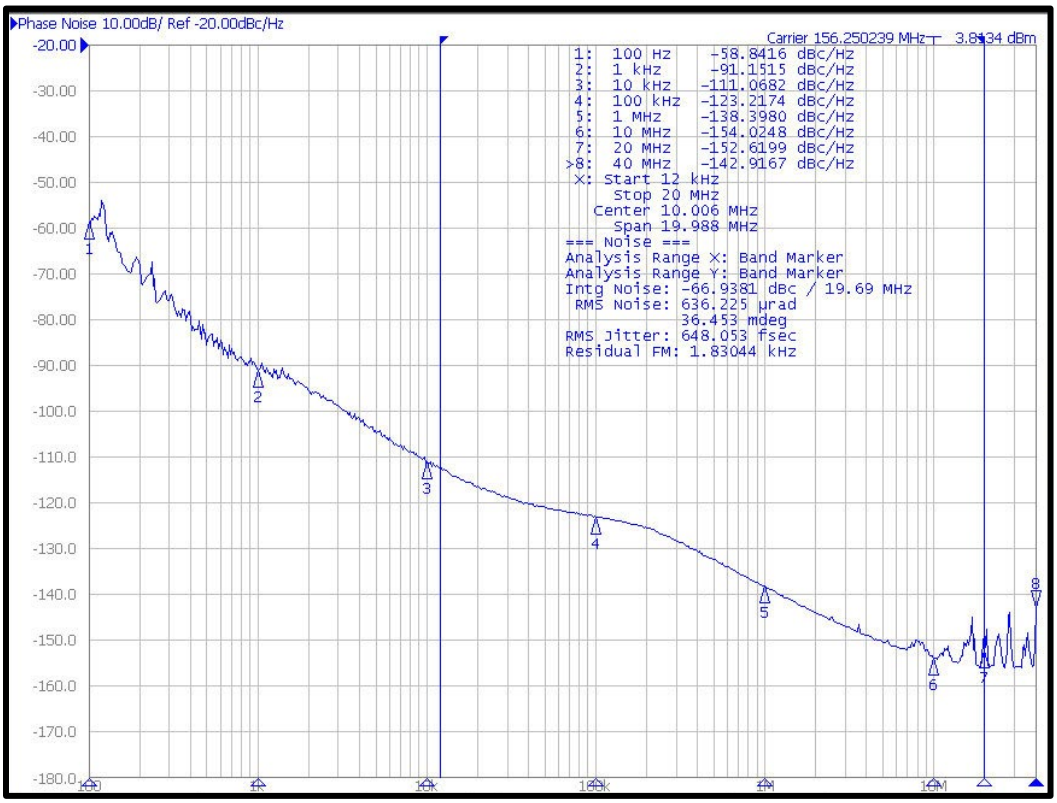
HCSL Test Circuit



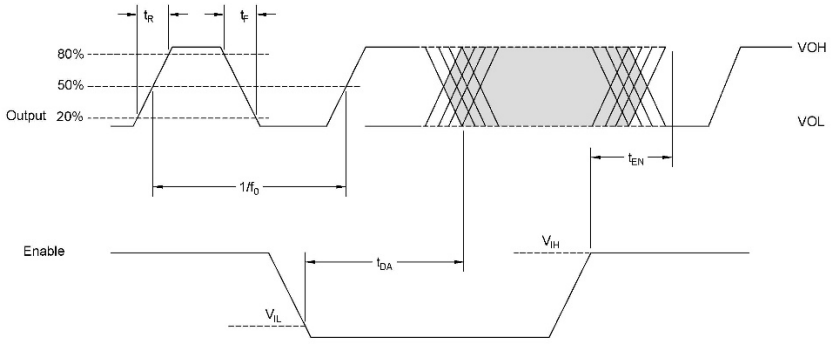
Phase Noise - CMOS (Unless specified otherwise: T=25° C, VDD=3.3 V, 125MHz)



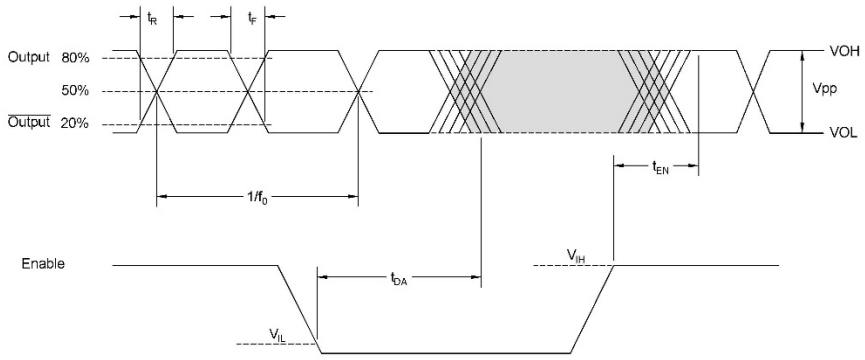
Phase Noise – LVDS, LVPECL, HCSL (Unless specified otherwise: T=25° C, VDD=3.3 V, 156.25MHz)



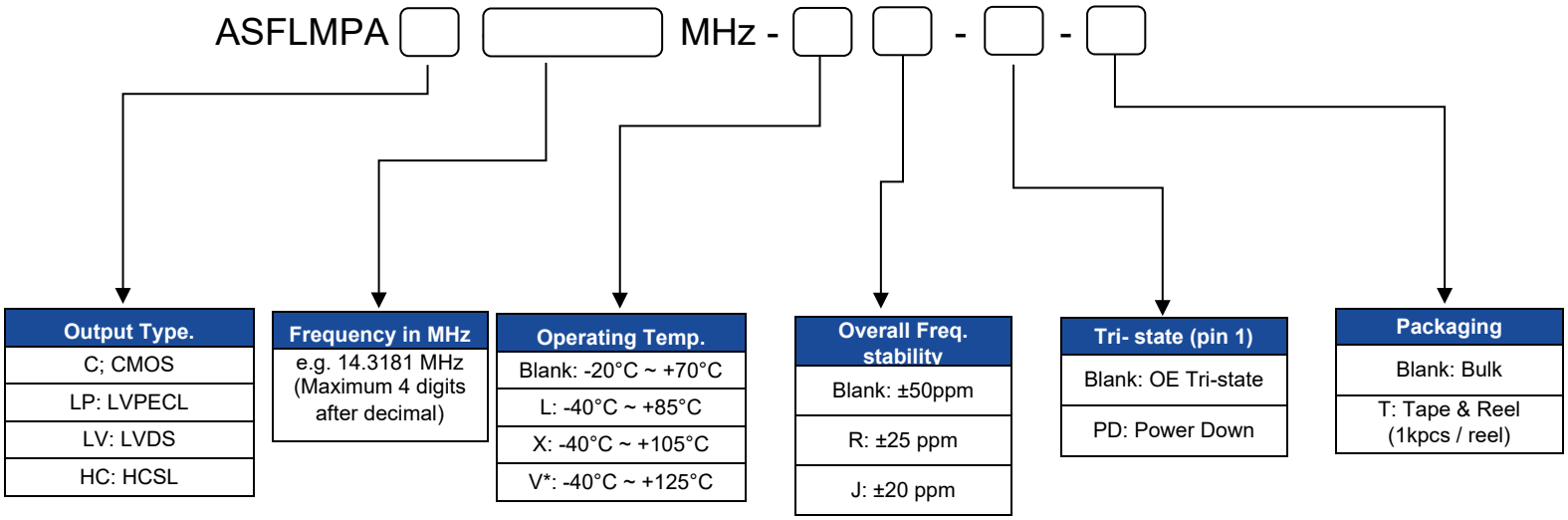
Output Waveform (CMOS)



Output Waveform (LVPECL, LVDS, and HCSL)



Options and Part Identification (left blank if standard)



Output Type.
C; CMOS
LP: LVPECL
LV: LVDS
HC: HCSL

Frequency in MHz
e.g. 14.3181 MHz (Maximum 4 digits after decimal)

Operating Temp.
Blank: -20°C ~ +70°C
L: -40°C ~ +85°C
X: -40°C ~ +105°C
V*: -40°C ~ +125°C

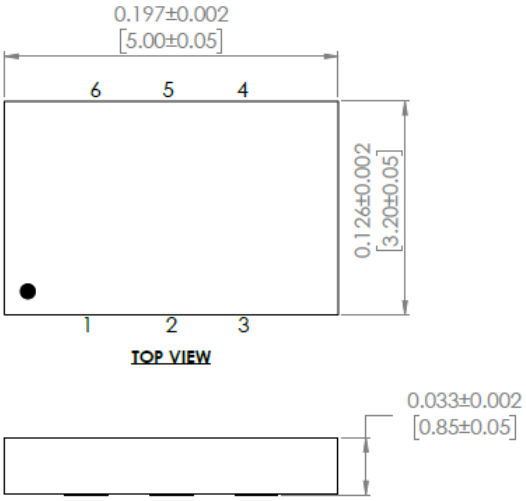
Overall Freq. stability
Blank: ±50ppm
R: ±25 ppm
J: ±20 ppm

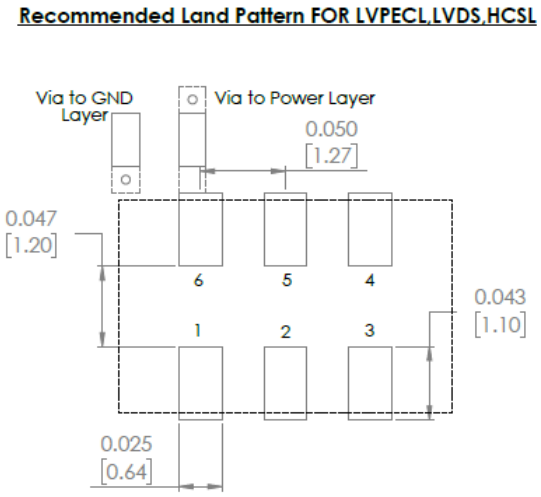
Tri- state (pin 1)
Blank: OE Tri-state
PD: Power Down

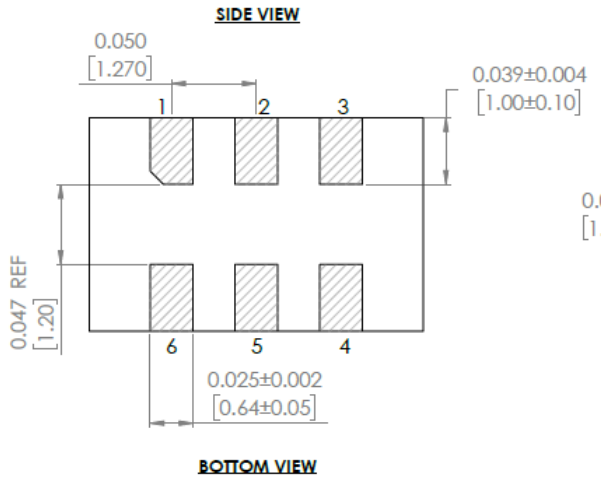
Packaging
Blank: Bulk
T: Tape & Reel (1kpcs / reel)

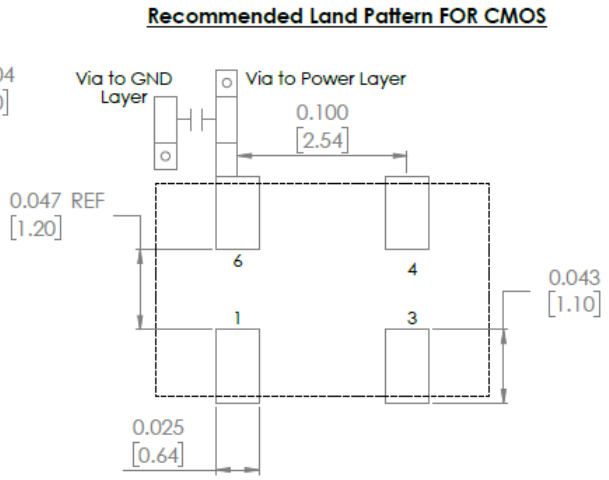
*LVDS and CMOS output only

Mechanical Dimensions









Pin #	Function
1	Tri-State or Power Down
2	NC
3	GND
4	Output
5	NC (CMOS) Output (LVPECL, LVDS, HCSL)
6	Vdd

Note: Recommended using an approximately 0.01µF bypass capacitor between PIN 6 and 3

Dimensions: Inches[mm]

Reflow Profile [JEDEC J-STD-020]

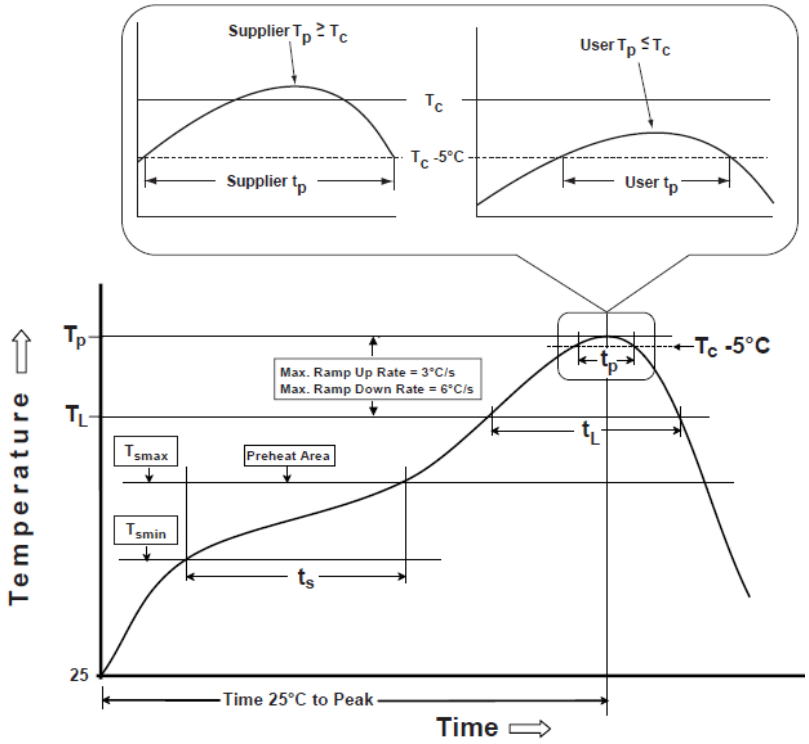


Table 1

SnPb Eutectic Process Classification Temperatures (T_c)		
Package Thickness	**Volume mm³ <350**	**Volume mm³ ≥350**
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2

Pb-Free Process Classification Temperatures (T_c)			
Package Thickness	**Volume mm³ <350**	**Volume mm³ 350-2000**	**Volume mm³ >2000**
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm - 2.5 mm	260 °C	250 °C	245 °C
>2.5 mm	250 °C	245 °C	245 °C

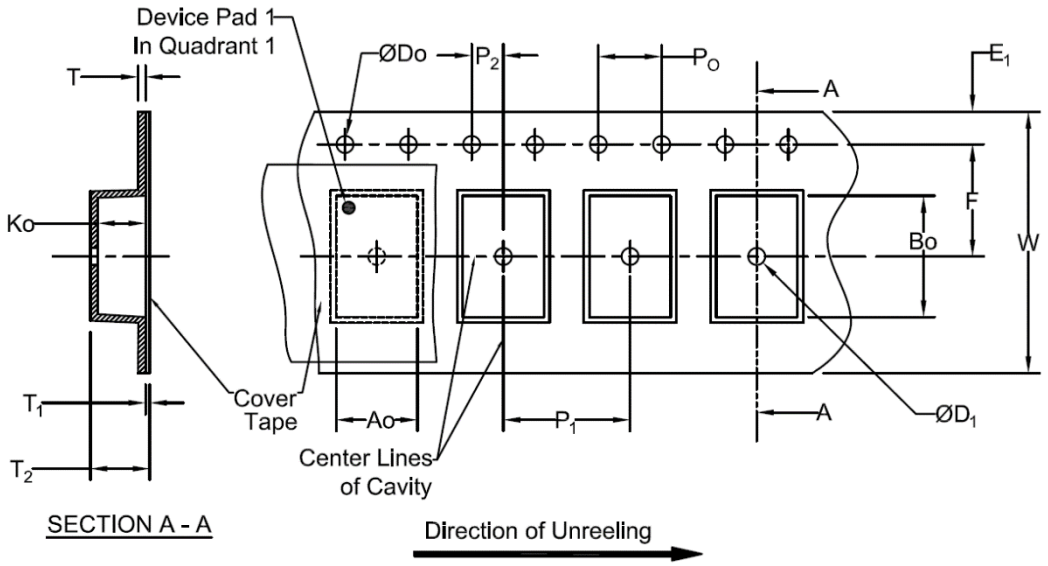
Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat / soak		
Temperature minimum (T_{smin})	100°C	150°C
Temperature maximum (T_{smax})	150°C	200°C
Time (T_{smin} to T_{smax}) (t_s)	60 - 120 sec.	60 - 120 sec.
Average ramp-up rate (T_{smax} to T_P)	3°C/sec. max	3°C/sec. max
Liquidous temperature (T_L)	183°C	217°C
Time at liquidous (t_L)	60 - 150 sec.	60 - 150 sec.
Peak package body temperature (T_P)*	**see Table 1**	**see Table 2**
Time (t_p)** within 5°C of the specified classification temperature (T_C)	20 sec.	30 sec.
Ramp-down rate (T_p to T_{smax})	6°C/sec. max	6°C/sec. max
Time 25°C to peak temperature	6 min. max	8 min. max
Reflow cycles	2 max	2 max

*Tolerance for peak profile temperature (T_p) is defined as a supplier minimum and a user maximum.

**Tolerance for time at peak profile temperature (t_p) is defined as supplier minimum and a user maximum.

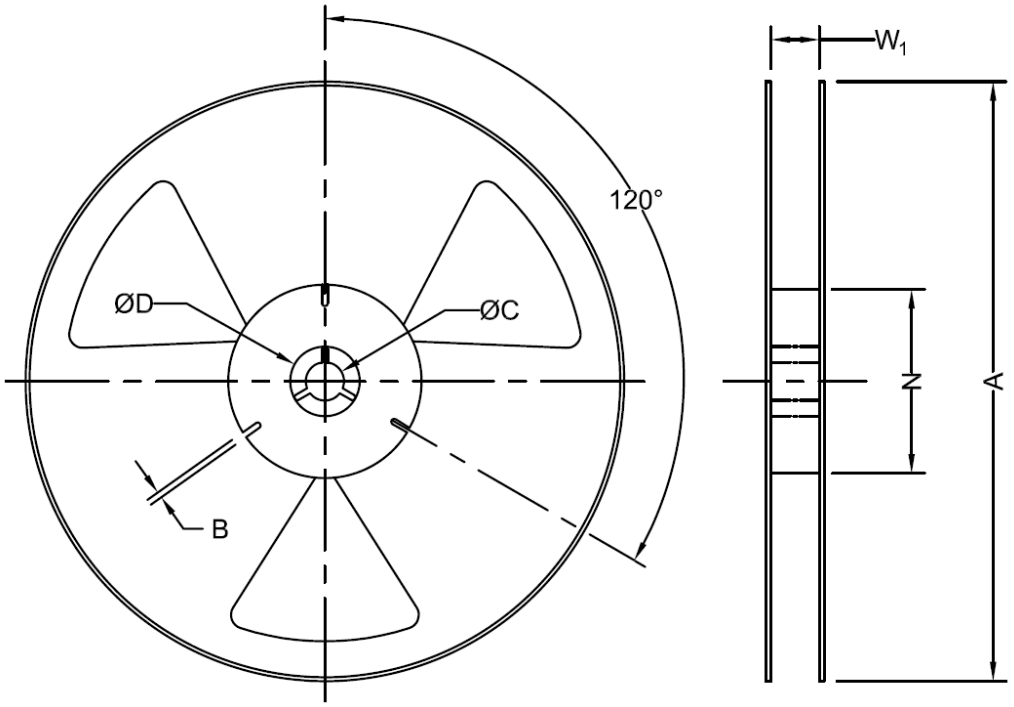
Packaging

T: 1,000pcs/reel



Tape Specifications (mm)							
Width	Ao	Bo	Do	D_1 (Min)	E_1	F	Ko
12mm	*	*	1.5+0.1/-0.0	1.0	1.75±0.1	5.5±0.05	*
Width	P1	P2	P0	T (Max)	T1 (Max)	T2 (Max)	W (Max)
12mm	8.0±0.1	2.0±0.05	4.0±0.1	0.6	0.1	6.5	12.3
***Note: Compliant to EIA-481**							

Dimension: mm



Reel Specifications (mm)							
Width	Qty/Reel	A (Nom)	B (Min)	C (Min)	D (Min)	N (Min)	*W_1
12mm	1000	178	1.5	13.0+0.5/-0.2	20.2	50	12.4+2.0/-0.0
***Note: Measured at Hub**							

Dimension: mm