- For functional characteristics and the programming model, see i.*MX 93 Applications Processor Reference Manual* (IMX93RM).

1 i.MX 93 introduction

The i.MX 93 family represents NXP's latest power-optimized processors for smart home, building control, contactless HMI, IoT edge, Automotive, and Industrial applications.

The i.MX 93 includes powerful dual Arm® Cortex®-A55 processors with speeds up to 1.7 GHz integrated with a NPU that accelerates machine learning inference. A general-purpose Arm® Cortex®-M33 running up to 250 MHz is for real-time and low-power processing. Robust control networks are possible via CAN-FD interface. Also, dual 1 Gbps Ethernet controllers, one supporting Time Sensitive Networking (TSN), drive gateway applications with low latency.

The i.MX 93 Automotive qualified part is particularly useful for applications such as:

- Driver monitoring system (DMS)
- Cost optimized gateway
- General purpose compute

Table 1. Features

Subsystem	Features
Cortex®-A55 MPCore platform	Two Cortex®-A55 processors operating up to 1.7 GHz • 32 KB L1 Instruction Cache • 32 KB L1 Data Cache • 64 KB per-core L2 cache • Media Processing Engine (MPE) with Arm® Neon™ technology supporting the Advanced Single Instruction Multiple Data architecture • Floating Point Unit (FPU) with support of the Arm® VFPv4-D16 architecture
	Supports of 64-bit Arm® v8.2-A architecture
	256 KB cluster L3 cache
	Parity/ECC protection on L1 cache, L2 cache, and TLB RAMs
Cortex®-M33 core platform	• Stand by monitoring with Cortex®-A55 and other high-power modules power gated
	Cortex®-M33 CPU operating up to 250 MHz • Supports FPU • Supports MPU • Supports NVIC • Supports FPB • Supports DWT and ITM • Two-way set-associative 16 KB System Cache with parity support • Two-way set-associative 16 KB Code Cache with parity support • 256 KB tightly coupled memory (TCM)
Neural Processing Unit (NPU)	Neural Network performance (256 MACs operating up to 1.0 GHz and 2 OPS/MAC)

Table continues on the next page...

Table 1. Features *...continued*

Subsystem	Features
	• NPU targets 8-bit and 16-bit integer RNN • Handles 8-bit weights
Image Sensor Interface (ISI)	• Standard pixel formats commonly used in many camera input protocols • Programmable resolutions up to 2K • Image processing for: — Supports one source of up to 2K horizontal resolution — Supports pixel rate up to 200 Mpixel/s • Image down scaling via decimation and bi-phase filtering • Color space conversion • Interlaced to progressive conversions
On-chip memory	Boot ROM (256 KB) for Cortex®-A55
	Boot ROM (256 KB) for Cortex®-M33
	On-chip RAM (640 KB)
External memory interface	16-bit DRAM interface: • LPDDR4X/LPDDR4 with inline ECC • Supports up to 2 Gbyte DDR memory space
	Three Ultra Secure Digital Host Controller (uSDHC) interfaces: • One eMMC 5.1 (8-bit) compliance with HS400 DDR signaling to support up to 400 MB/sec • One SDXC (4-bit, no eMMC5.1, with extended capacity) • One SDIO (4-bit, SD/SDIO 3.01 compliance with 200 MHz SDR signaling and up to 100 MB/sec)
	FlexSPI Flash with support for XIP (for Cortex®-A55 in low-power mode) and support for either one Octal SPI or Quad SPI FLASH device. It also supports both Serial NOR and Serial NAND flash using the FlexSPI.
Pixel Pipeline (PXP)	• BitBlit • Flexible image composition options—alpha, chroma key • Porter-Duff operation • Image rotation (90°, 180°, 270°) • Image resize • Color space conversion • Multiple pixel format support (RGB, YUV444, YUV422, YUV420, YUV400)

Table continues on the next page...

Table 1. Features *...continued*

Subsystem	Features
	• Standard 2D-DMA operation
LCDIF Display Controller	The LCDIF can drive any of three displays: • MIPI DSI: up to 1920x1200p60 • LVDS Tx: up to 1366x768p60 or 1280x800p60 • Parallel display: up to 1366x768p60 or 1280x800p60
MIPI CSI-2 Interface	One 2-lane MIPI CSI-2 camera input: • Complaint with MIPI CSI-2 specification v1.3 and MIPI D-PHY specification v1.2 • Supports up to 2 Rx data lanes (plus 1 Rx clock lane) • Supports 80 Mbps – 1.5 Gbps per lane data rate in high speed operation • Supports 10 Mbps data rate in low power operation
MIPI DSI Interface	One 4-lane MIPI DSI display with data supplied by the LCDIF • Compliant with MIPI DSI specification v1.2 and MIPI D-PHY specification v1.2 • Capable of resolutions achievable with a 200 MHz pixel clock and active pixel rate of 140 Mpixel/s with 24-bit RGB. • Supports 80 Mbps—1.5 Gbps data rate per lane in high speed operation • Supports 10 Mbps data rate in low power operation
Audio	• Three SAI interfaces: — SAI1 supports 2-lane and SAI3 supports 1 lane — SAI2 supports 4 lanes — SAI2 and SAI3 support glue-less switching between PCM and stereo DSD operation • One SPDIF supports raw capture mode that can save all the incoming bits into audio buffer • 24-bit PDM supports up to 8-microphones (4 lanes)
GPIO and input/output multiplexing	General-purpose input/output (GPIO) modules with interrupt capability
	Input/output multiplexing controller (IOMUXC) to provide centralized pad control
Power management	Temperature sensor with programmable trip points
	Flexible power domain partitioning with internal power switches to support efficient power management
Connectivity	Two USB 2.0 controllers and PHYs interfaces
	Two Controller Area Network (FlexCAN) modules, each optionally supporting flexible data-rate (FD)

Table continues on the next page...

Table 1. Features *...continued*

Subsystem	Features
	Two Improved Inter Integrated Circuit (I3C) modules
	Two 32-pin FlexIO modules
	Three Ultra Secure Digital Host Controller (uSDHC) interfaces
	Two Ethernet controllers (capable of simultaneous operation): • One Gigabit Ethernet controller with support for Energy Efficient Ethernet (EEE), Ethernet AVB, and IEEE 1588 • One Gigabit Ethernet controller with support for TSN in addition to EEE, Ethernet AVB, and IEEE 1588
	Eight Low Power SPI (LPSPI) modules
	Eight Low Power I2C modules
	Eight Low Power Universal Asynchronous Receiver/Transmitter (LPUART) modules: • Programmable baud rates up to 5 Mbps
	One Analog-to-Digital Converter (SAR ADC) module • 12-bit 4-channel with 1 MS/s
Security	Trusted Resource Domain Controller (TRDC) • Supports 16 domains
	Arm® TrustZone® (TZ) architecture, including both Trustzone-A and Trustzone-M
	On-chip RAM (OCRAM) secure region protection using OCRAM controller
	EdgeLock® secure enclave
	Battery Backed Security Module (BBSM) • Secure real-time clock (RTC)
System debug	Arm® CoreSight™ debug and trace technology
	Embedded Trace FIFO (ETF) with 4 KB internal storage to provide trace buffering
	Unified trace capability for dual core Cortex®-A55 and Cortex®-M33 CPUs
	Cross Triggering Interface (CTI)
	Support for 4-pin (JTAG) debug interface and SWD

1.1 Ordering information

Table 2 provides examples of orderable part numbers covered by this Data Sheet.

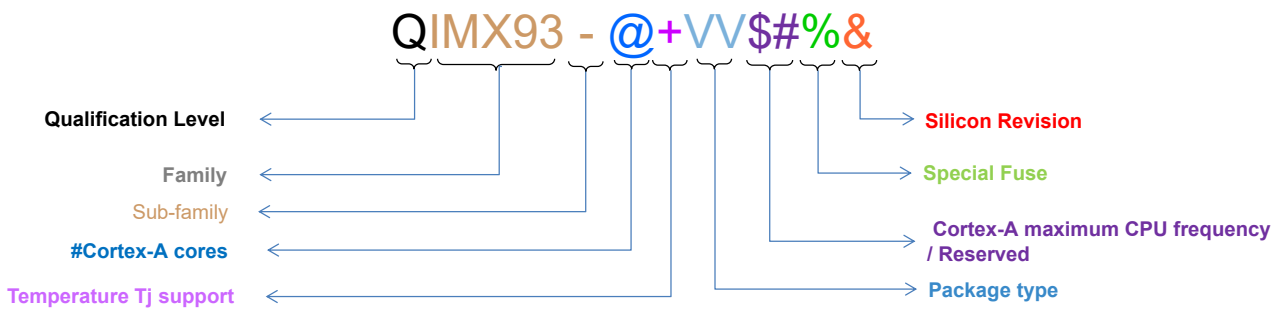
Table 2. Ordering information

Part number	Part differentiator	Number of Cores (A55)	Max speed	NPU	GDET	Camera	Display	Connectivity	Audio	DDR	Package
MIMX9352AVTXMAC	5	2	1.7 GHz	NPU	Disabled	• 2-lane 1080p30 MIPI CSI • Parallel camera	• 4-lane 1080p60 MIPI DSI • 4-lane LVDS • Parallel display	• 2x GbE • 2x USB 2.0	7x I2S TDM	3.7 GT/s	14 x 14 mm, 0.65 mm pitch
MIMX9352AVTXMBC	5	2	1.7 GHz	NPU	Enabled	• 2-lane 1080p30 MIPI CSI • Parallel camera	• 4-lane 1080p60 MIPI DSI • 4-lane LVDS • Parallel display	• 2x GbE • 2x USB 2.0	7x I2S TDM	3.7 GT/s	14 x 14 mm, 0.65 mm pitch
MIMX9351AVTXMAC	5	1	1.7 GHz	NPU	Disabled	• 2-lane 1080p30 MIPI CSI • Parallel camera	• 4-lane 1080p60 MIPI DSI • 4-lane LVDS • Parallel display	• 2x GbE • 2x USB 2.0	7x I2S TDM	3.7 GT/s	14 x 14 mm, 0.65 mm pitch
MIMX9332AVTXMAC	3	2	1.7 GHz	—	Disabled	• 2-lane 1080p30 MIPI CSI • Parallel camera	• 4-lane 1080p60 MIPI DSI • 4-lane LVDS • Parallel display	• 2x GbE • 2x USB 2.0	7x I2S TDM	3.7 GT/s	14 x 14 mm, 0.65 mm pitch
MIMX9331AVTXMAC	3	1	1.7 GHz	—	Disabled	• 2-lane 1080p30 MIPI CSI • Parallel camera	• 4-lane 1080p60 MIPI DSI • 4-lane LVDS • Parallel display	• 2x GbE • 2x USB 2.0	7x I2S TDM	3.7 GT/s	14 x 14 mm, 0.65 mm pitch

Figure 1 describes the part number nomenclature so that characteristics of a specific part number can be identified (for example, cores, frequency, temperature grade, fuse options, and silicon revision). The primary characteristic which describes which data sheet applies to a specific part is the temperature grade (junction) field.

- The i.MX 93 Applications Processors for Commercial Products Data Sheet (IMX93CEC) covers parts listed with a "D (Commercial temp)"
- The i.MX 93 Applications Processors for Industrial Products Data Sheet (IMX93IEC) covers parts listed with a "C (Industrial temp)"
- The i.MX 93 Applications Processors for Extended Industrial Products Data Sheet (IMX93XEC) covers parts listed with a "X (Extended Industrial temp)"
- The i.MX 93 Applications Processors for Automotive Products Data Sheet (IMX93AEC) covers parts listed with an "A (Automotive temp)"

Ensure to have the proper data sheet for specific part by verifying the temperature grade (junction) field and matching it to the proper data sheet. If there are any questions, visit the web page nxp.com/IMX or contact an NXP representative for details.



Qualification level	Q
Samples	P
Mass Production	M
Special	S

Family	93
i.MX9300	93

Temperature Tj support	+
Commercial: 0˚C to +95°C	D
Industrial: -40˚C to +105°C	C
Extended Industrial: -40˚C to +125°C	X
Automotive: -40˚C to +125˚C	A

Cortex-A maximum CPU frequency	#
1.7 GHz	M
900 MHz	D

Sub-family	93 11 x 11 mm	93 14 x 14 mm	93 9 x 9 mm
With NPU (Full-featured)	5	5	2
Without NPU	3	3	1
Reduced feature/performance	0		

Package type	VV
14 x 14 mm, 0.65 mm pitch, FCBGA306	VT
11 x 11 mm, 0.5 mm pitch, FCBGA306	VV
9 x 9 mm, 0.5 mm pitch, FCBGA208	VX

Reserved	$
Can be used to designate special versions, e.g., reduced GPU performance	
No additional information required	X
Reserved	Z

#Cortex-A cores	@
Dual-core	2
Single core	1

Silicon Rev	&
Rev 1.0	A
Rev. 2.0	B
Rev. 3.0	C

Special Fuse	%
No special fuse	A
Full featured with GDET enabled	B

Figure 1. Part number nomenclature—i.MX 93 processors

2 Block diagram

Figure 2 shows the functional modules in the i.MX 93 processor system.[1]

[1] Some modules shown in this block diagram are not offered on all derivatives. This block diagram may also show less modules than available in some derivatives. See Table 2 for details.

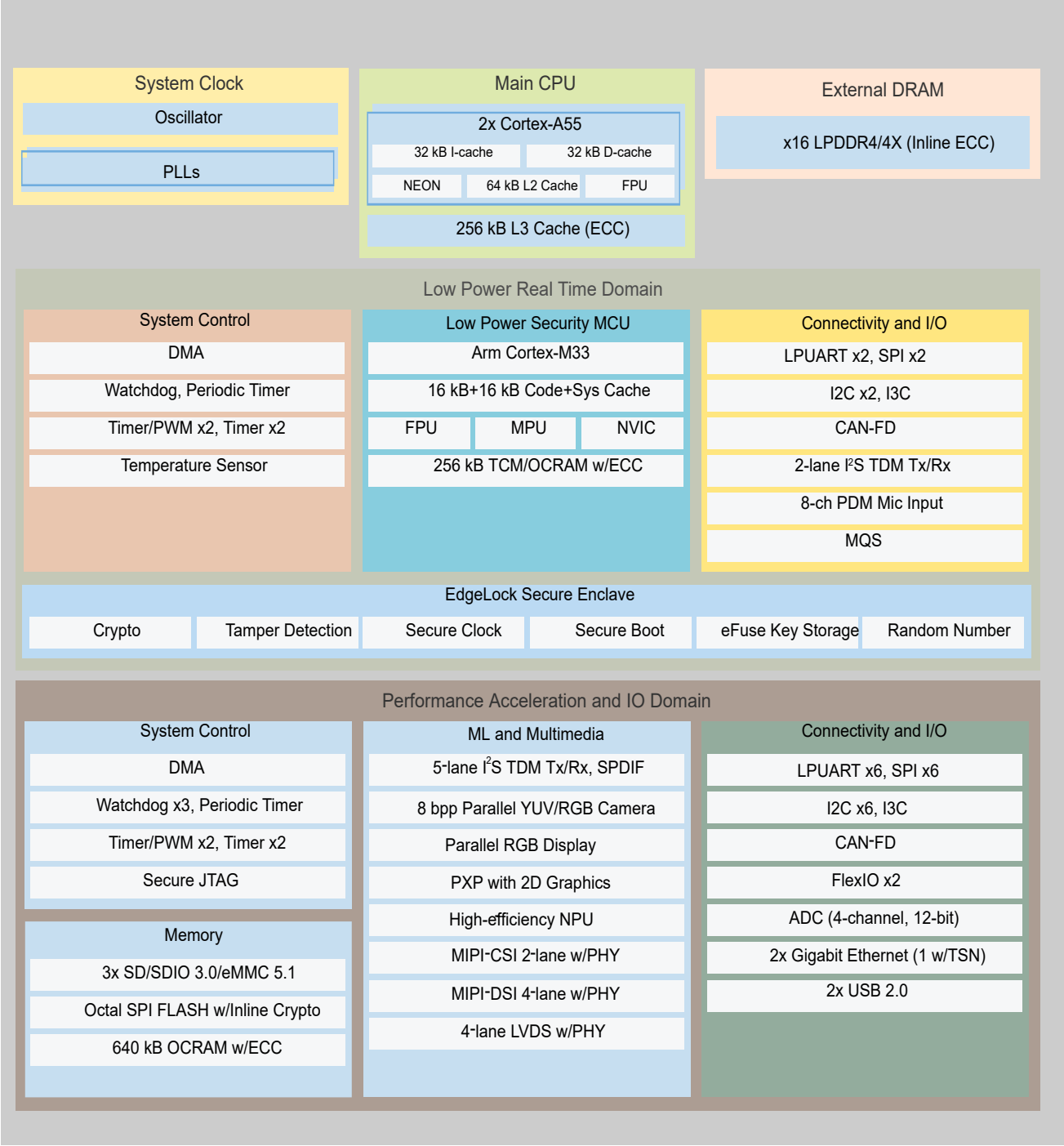


Figure 2. i.MX 93 system block diagram

3 Special signal considerations

Table 3 lists special signal considerations for the i.MX 93 processors. The signal names are listed in alphabetical order.

The package contact assignments can be found in Package information and contact assignments. Signal descriptions are provided in the *i.MX 93 Reference Manual* (IMX93RM).

Table 3. Special signal considerations

Signal Name	Remarks
CLKIN1/CLKIN2	CLKIN1 and CLKIN2 are input pins without internal pull-up and pull-down. An external 10K pull-down resistor is recommended if they are not used.
NC	These signals are No Connect (NC) and should be unconnected in the application.
ONOFF	A brief connection to GND in the OFF mode causes the internal power management state machine to change the state to ON. In the ON mode, a brief connection to GND generates an interrupt (intended to be a software-controllable power-down). A connection to GND for a period of time longer than the value configured in the BBNSM_CTRL[BTN_TIMEOUT] causes a forced OFF (PMIC_ON_REQ output “L”), as long as there is no pending RTC alarm event or tamper event.
POR_B	POR_B has no internal pull-up/down resistor, and requires external pull-up resistor to NVCC_BBSM_1P8. It is recommended that POR_B is properly handled during power up/down. Please see the EVK design for details.
RTC_XTALI/RTC_XTALO	To hit the exact oscillation frequency, the board capacitors must be reduced to account for the board and chip parasitics. The integrated oscillation amplifier is self-biasing, but relatively weak. Care must be taken to limit the parasitic leakage from RTC_XTALI and RTC_XTALO to either the power or the ground (> 100 MΩ). This de-biases the amplifier and reduces the start-up margin. If you want to feed an external low-frequency clock into RTC_XTALI, the RTC_XTALO pin must remain unconnected or driven by a complementary signal. The logic level of this forcing clock must not exceed the NVCC_BBSM_1P8 level and the frequency shall be < 50 kHz under the typical conditions.
XTALI_24M/XTALO_24M	The system requires 24 MHz on XTALI/XTALO. The crystal cannot be eliminated by an external 24 MHz oscillator. If this clock is used as a reference for USB, then there are strict frequency tolerance and jitter requirements. See Clock sources and relevant interface specifications chapters for details.

3.1 Unused input and output guidance

If a function of the i.MX 93 is not used, the I/Os and power rails of that function can be terminated to reduce overall board power. Table 4 is recommended connectivities for LVDS and other digital I/Os. Table 5 is recommended connectivities for MIPI. Table 6 is recommended connectivities for USB.

Table 4. Unused function strapping recommendations

Function	Ball name	Recommendations if unused
ADC	ADC_IN0, ADC_IN1, ADC_IN2, ADC_IN3	Tie to ground
TAMPER	TAMPER0, TAMPER1	Tie to ground
LVDS	VDD_LVDS_1P8, LVDS_CLK_P, LVDS_CLK_N, LVDS_Dx_P, LVDS_Dx_N,	Tie to ground through 10 KΩ resistors

Table continues on the next page...

Table 4. Unused function strapping recommendations *...continued*

Function	Ball name	Recommendations if unused
Digital I/O supplies	NVCC_GPIO, NVCC_WAKEUP, NVCC_AON, NVCC_SD2	Tie to ground through 10 KΩ resistors if entire bank is not used

Table 5. MIPI strapping recommendations

Function	Ball name	Recommendations
Only MIPI_CSI used	VDD_MIPI_0P8, VDD_MIPI_1P8	Supply
	MIPI_DSI1_CLK_P, MIPI_DSI1_CLK_N, MIPI_DSI1_Dx_P, MIPI_DSI1_Dx_N	Not connected
Only MIPI_DSI used	VDD_MIPI_0P8, VDD_MIPI_1P8	Supply
	MIPI_CSI1_CLK_P, MIPI_CSI1_CLK_N, MIPI_CSI1_Dx_P, MIPI_CSI1_Dx_N	Not connected
Neither MIPI_CSI nor MIPI_DSI used	VDD_MIPI_0P8, VDD_MIPI_1P8	Tie to ground
	MIPI_CSI1_CLK_P, MIPI_CSI1_CLK_N, MIPI_CSI1_Dx_P, MIPI_CSI1_Dx_N	Not connected
	MIPI_DSI1_CLK_P, MIPI_DSI1_CLK_N, MIPI_DSI1_Dx_P, MIPI_DSI1_Dx_N	Not connected
	MIPI_REXT	Tie to ground

Table 6. USB strapping recommendations

Function	Ball name	Recommendations
Only USB1 used	VDD_USB_3P3, VDD_USB_1P8, VDD_USB_0P8	Supply
	USB2_VBUS, USB2_D_P, USB2_D_N, USB2_ID, USB2_TXRTUNE	Not connected
Only USB2 used	VDD_USB_3P3, VDD_USB_1P8, VDD_USB_0P8	Supply
	USB1_VBUS, USB1_D_P, USB1_D_N, USB1_ID, USB1_TXRTUNE	Not connected
Neither USB1 nor USB2 used	VDD_USB_3P3, VDD_USB_1P8, VDD_USB_0P8	Tie to ground
	USB1_VBUS, USB1_D_P, USB1_D_N, USB1_ID, USB1_TXRTUNE	Not connected
	USB2_VBUS, USB2_D_P, USB2_D_N, USB2_ID, USB2_TXRTUNE	Not connected

4 Electrical characteristics

This section provides the device and module-level electrical characteristics for the i.MX 93 family of processors.

4.1 Chip-level conditions

This section provides the device-level electrical characteristics for the IC. See Table 7 for a quick reference to the individual tables and sections.

Table 7. i.MX 93 chip-level conditions

For these characteristics, …	Topic appears …
Absolute maximum ratings	Absolute maximum ratings
Thermal resistance	Thermal resistance
Operating ranges	Operating ranges
Clock sources	Clock sources
Maximum supply currents	Maximum supply currents
Power modes	Power modes
Power supplies requirements and restrictions	Power supplies requirements and restrictions

4.1.1 Absolute maximum ratings

CAUTION

Stresses beyond those listed in the following table may reduce the operating lifetime or cause immediate permanent damage to the device. The table below does not imply functional operation beyond those indicated in the operating ranges and parameters table.

Table 8. Absolute maximum ratings

Parameter description	Symbol	Min	Max	Unit	Notes
Core supplies input voltages	VDD_SOC	-0.3	1.15	V	—
GPIO supply voltage	NVCC_GPIO, NVCC_WAKEUP, NVCC_AON	-0.3	3.8	V	—
I/O supply for SD2	NVCC_SD2	-0.3	3.8	V	—
DDR PHY supply voltage	VDD2_DDR	-0.3	1.575	V	—
DDR I/O supply voltage	VDDQ_DDR	-0.3	1.575	V	—
I/O supply and I/O Pre-driver supply for BBSM bank	NVCC_BBSM_1P8	-0.3	2.15	V	—
USB VBUS input detected	USB1_VBUS, USB2_VBUS	-0.3	3.95	V	—
Power for USB OTG PHY	VDD_USB_0P8	-0.3	1.15	V	—

Table continues on the next page...

Table 8. Absolute maximum ratings *...continued*

Parameter description	Symbol	Min	Max	Unit	Notes
	VDD_USB_1P8	-0.3	2.15	V	—
	VDD_USB_3P3	-0.3	3.95	V	—
MIPI PHY supply voltage	VDD_MIPI_0P8	-0.3	1.15	V	—
	VDD_MIPI_1P8	-0.3	2.15	V	—
LVDS PHY supply voltage	VDD_LVDS_1P8	-0.3	2.15	V	—
Analog core supply voltage	VDD_ANA_0P8	-0.3	1.15	V	—
	VDD_ANAx_1P8	-0.3	2.15	V	[1]
Input/output voltage range	V_{in}/V_{out}	-0.3	OVDD[2] + 0.3	V	—
Storage temperature range	$T_{STORAGE}$	-40	150	ºC	—

1. VDD_ANAx_1P8 refers to VDD_ANA0_1P8, VDD_ANA1_1P8, and VDD_ANAVDET_1P8.
2. OVDD is the I/O supply voltage.

Table 9. Electrostatic discharge and latch-up ratings

Parameter description		Rating	Reference	Comment
Electrostatic Discharge (ESD)	Human Body Model (HBM)	±1000 V	JS-001	—
	Charged Device Model (CDM)	±250 V	JS-002	—
Latch-up (LU)	Immunity level: • Class I @ 25 °C ambient temperature • Class II @ 125 °C ambient temperature	A A	JESD78	—

4.1.2 Thermal resistance

4.1.2.1 14 x 14 mm FCBGA package thermal characteristics

Table 10 lists the 14 x 14 mm FCBGA package thermal resistance data.

Table 10. 14 x 14 mm FCPBGA thermal resistance data

Rating	Board Type[1]	Symbol	Values	Unit
Junction to Ambient Thermal Resistance[2]	JESD51-9, 2s2p	$R_{\theta JA}$	21.7	°C/W
Junction-to-Top of Package Thermal Characterization parameter[3]	JESD51-9, 2s2p	Ψ_{JT}	0.1	°C/W

Table continues on the next page...

Table 10. 14 x 14 mm FCPBGA thermal resistance data...*continued*

Rating	Board Type[1]	Symbol	Values	Unit
Junction to Case Thermal Resistance[3]	JESD51-9, 1s	$R_{\theta JC}$	5.4	°C/W

1. Thermal test board meets JEDEC specification for this package (JESD51-9). Test board has 40 vias under die shadow mapped according to BGA layout under die. Each via is 0.2 mm in diameter and connects top layer with the first buried plane layer.
2. Determined in accordance to JEDEC JESD51-2A natural convection environment. Thermal resistance data in this report is solely for a thermal performance comparison of one package to another in a standardized specified environment. It is not meant to predict the performance of a package in an application-specific environment.
3. Junction-to-Case thermal resistance determined using an isothermal cold plate. Case temperature refers to the package top side surface temperature.

4.1.3 Power architecture

The power architecture of i.MX 93 is defined based on the assumption that systems are constructed for the case where the PMIC is used to supply all the power rails to the processor. The SoC may be powered from discrete parts rather than a PMIC, but a discrete-based solution is not necessarily BOM cost-optimized.

NVCC_BBSM_1P8 must be powered first and stay until the last.

The digital logic inside chip will be supplied with VDD_SOC, which can be nominal or overdrive voltage or a "Low Drive" voltage.

The DRAM controller and PHY have multiple external power supplies:

Table 11. Power supplies of the DRAM controller and PHY

Power supplies	Modules
VDD_SOC	SoC synthesized DRAM controller digital logic
VDD_ANA_0P8	DRAM PLL and PHY digital logic
VDD_ANAx_1P8	DRAM PLL and PHY analog circuitry
VDD2_DDR	1.1 V DRAM PHY I/O supply
VDDQ_DDR	0.6 V DRAM PHY I/O supply for LPDDR4X

For all the integrated analog modules, their 1.8 V analog power will be supplied externally through power pads. These supplies are separated with other power pads on the package to keep them clean, but they can be directly shared with other power rails on the board to reduce the number of power supplies from the PMIC.

For the integrated LVDS PHY, MIPI PHY, and USB PHYs, their 3.3 V (where supported), 1.8 V, and digital power will be supplied externally through power pads. The powers to those PHYs are separated with other power pads on the package to keep them clean, but they can be directly shared with other power rails on the board to reduce the number of power supplies from the PMIC.

For BBSM/RTC, the 1.8 V I/O pre-driver supply and 1.8 V I/O pad supply will also be supplied externally. The BBSM_LP core digital domain logic is supplied by an internal LDO.

Figure 3 is the power architecture diagram for the whole chip. Note that it only shows power supplies, and does not show capacitors that may be required for internal LDO regulators.

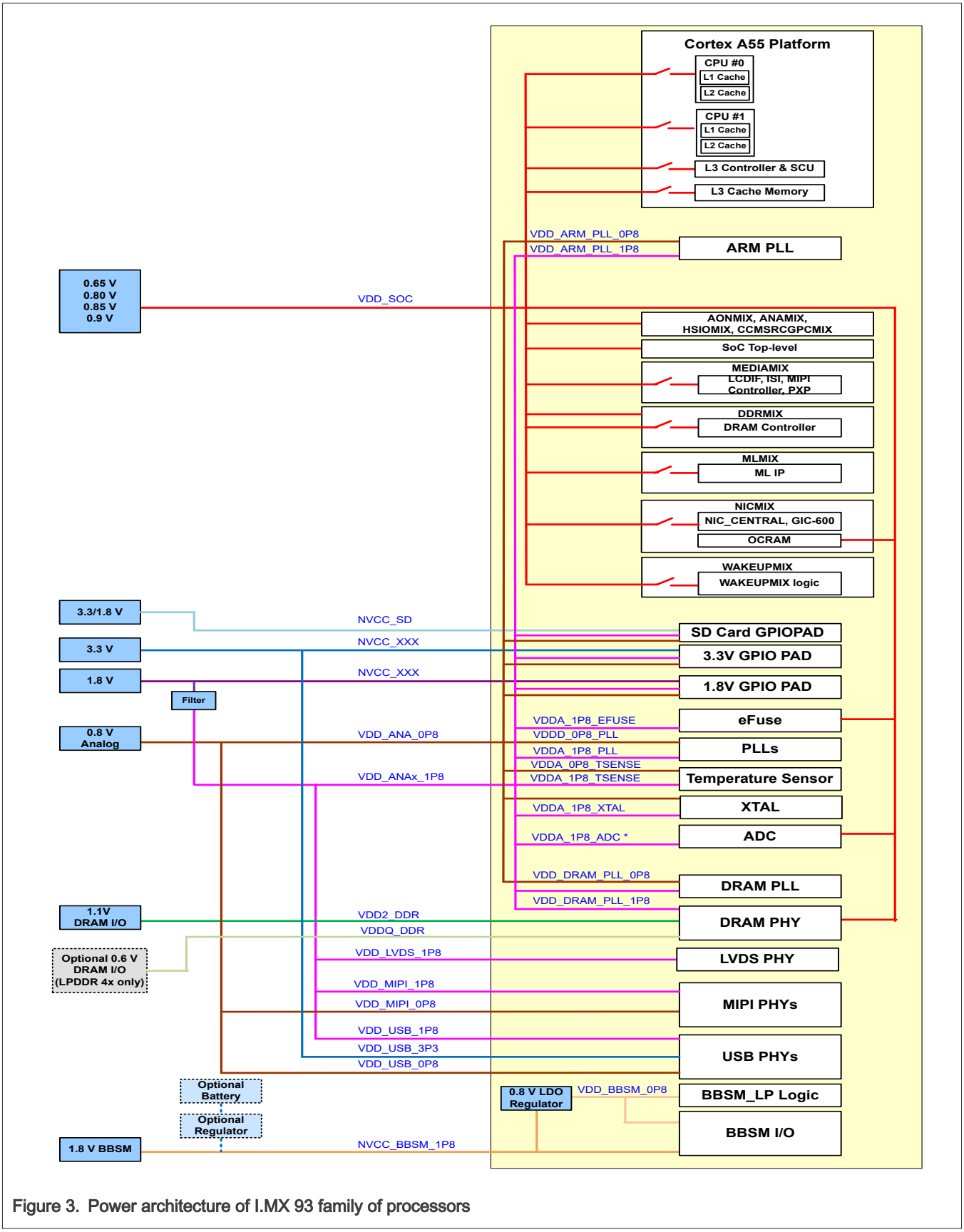


Figure 3. Power architecture of I.MX 93 family of processors

NOTE

If ADC is used, external voltage reference is recommended for VDD_ANAx_1P8 to improve the ADC ENOB.

4.1.4 Operating ranges

Table 12 provides the operating ranges of the i.MX 93 processors. For details on the chip's power structure, see the "Clock and Power Overview" chapter of the *i.MX 93 Reference Manual* (IMX93RM).

Table 12. Operating ranges

Parameter Description	Symbol	Min	Typ	Max[1]	Unit	Comment
Power supply for SoC logic and Arm core	VDD_SOC	0.85	0.90	0.95	V	Power supply for SoC, overdrive mode
		0.80	0.85	0.90	V	Power supply for SoC, nominal mode
		0.76	0.80	0.84	V	Power supply for SoC, low drive mode
		0.61	0.65	0.70	V	Power supply for SoC, suspend mode
Digital supply for PLLs, temperature sensor, LVCMOS I/O, MIPI, and USB PHYs	VDD_ANA_0P8	0.76	0.80	0.84	V	—
	VDD_MIPI_0P8					
	VDD_USB_0P8					
1.8 V supply for PLLs, eFuse, Temperature sensor, LVCMOS voltage detect reference, ADC, 24 MHz XTAL, LVDS, MIPI, and USB PHYs	VDD_ANAx_1P8	1.71	1.80	1.89	V	[2]
	VDD_LVDS_1P8					
	VDD_MIPI_1P8					
	VDD_USB_1P8					
3.3 V supply for USB PHY	VDD_USB_3P3	3.069	3.30	3.45	V	—
Voltage supply for DRAM PHY	VDD2_DDR	1.06	1.10	1.14	V	—
Voltage supply for DRAM PHY I/O	VDDQ_DDR	1.06	1.10	1.14	V	LPDDR4
		0.57	0.60	0.67	V	LPDDR4X
I/O supply and I/O pre-driver supply for GPIO in BBSM bank	NVCC_BBSM_1P8	1.62	1.80	1.98	V	—
Power supply for GPIO when it is in 1.8 V mode	NVCC_AON NVCC_SD2	1.62	1.80	1.98	V	—

Table continues on the next page...

Table 12. Operating ranges *...continued*

Parameter Description	Symbol	Min	Typ	Max[1]	Unit	Comment
Power supply for GPIO when it is in 3.3 V mode	NVCC_GPIO NVCC_WAKEUP	3.00	3.30	3.465	V	—
Temperature Ranges						
Junction temperature — Automotive	Tj[3]	-40	—	+125	°C	See the application note, i.MX 93 Product Lifetime Usage Estimates for information on product lifetime (power-on hours) for this processor.
Ambient temperature — Automotive	Ta	-40	—	+85		

1. Applying the maximum voltage results in maximum power consumption and heat generation. NXP recommends a voltage set point = (V_{min} + the supply tolerance). This result in an optimized power/speed ratio.
2. VDD_ANAx_1P8 refers to VDD_ANA0_1P8, VDD_ANA1_1P8, and VDD_ANAVDET_1P8.
3. Tj minimum temperature supported at startup where Tj = Ta.

4.1.5 Maximum frequency of main modules

Table 13 provides the maximum frequency of main modules in the i.MX 93 of processors.

Table 13. Maximum frequency of main modules[1]

Main modules	Frequency (Low Drive mode)	Frequency (Nominal mode)	Frequency (Overdrive mode)
EdgeLock® Secure Enclave	133 MHz	200 MHz	250 MHz
Cortex®-M33 core	133 MHz	200 MHz	250 MHz
Cortex®-A55 cores	0.9 GHz	1.4 GHz	1.7 GHz
DRAM	933 MHz	1400 MHz	1866 MHz
NPU	500 MHz	800 MHz	1000 MHz

1. For more detailed information about clock, see Chapter Clock Controller Module (CCM) of *i.MX 93 Applications Processor Reference Manual*.

4.1.6 Clock sources

4.1.6.1 External clock sources

The i.MX 93 processor is designed to function with quartz crystals to generate the frequencies necessary for operation. 24 MHz for the main clock source and 32.768 kHz for the real time clock. External clock can be injected into RTC_XTALI if the frequency precision and jitter precision are sufficient.

The XTAL input is used to synthesize all of the clocks in the system with the RTC_XTAL input contribution to time keeping and low frequency operations.

Table 14 shows the interface frequency requirements.

Table 14. External input clock frequency

Parameter Description	Symbol	Min	Typ	Max	Unit
RTC_XTALI Oscillator[1]	f_{ckil}	—	32.768[2]	—	kHz

1. External oscillator or a crystal with internal oscillator amplifier.
2. Recommended nominal frequency is 32.768 kHz.

Table 15 shows the maximum frequency of external clock.

Table 15. Audio external clock frequency

Parameter Description	Symbol	Low drive mode	Nominal mode	Overdrive mode	Unit
EXT_CLK maximum frequency	f_{ext_clk}[1]	133	200	200	MHz

1. Audio EXT_CLK signal muxed on either pin SD2_VSELECT or PDM_BIT_STREAM1.

Table 16 shows the external input clock for OSC32K.

Table 16. RTC_OSC

	Symbol	Min	Typ	Max	Unit
Frequency	f	—	32.768	—	kHz
RTC_XTALI	V_{IH}	0.9 x NVCC_BBSM_1P8	—	NVCC_BBSIM_1P8	V
	V_{IL}	0	—	0.1 x NVCC_BBSM_1P8	V
	Duty cycle	45	—	55	%

For the case where an external clock is desired to be the source of the 32.768 kHz clock, the RTC_XTALI pin may be driven with the RTC_XTALO pin disconnected.

4.1.6.2 On-chip oscillators

An external 24 MHz crystal is used in conjunction with the integrated amplifier to form a crystal oscillator that is used as the reference clock for all frequency synthesis on the processor.

Table 17. 24M quartz specifications[1]

Symbol	Parameter Description	Min	Typ	Max	Unit
fXTAL	Frequency	—	24	—	MHz
CLOAD	Cload	—	12	—	pF
DL	Drive level	—	—	100	µW
ESR	ESR	—	—	120	Ω

1. An external 24 MHz crystal is used in conjunction with the integrated amplifier to form a crystal oscillator that is used as the reference clock for all frequency synthesis on the processor.

Table 18 shows 32K oscillator specifications.

Table 18. 32.768 kHZ quartz specifications

Symbol	Parameter Description	Min	Typ	Max	Unit
fXTAL	Frequency (crystal mode) [1]	—	32.768	—	kHz
CLOAD	Cload	—	12.5	—	pF
ESR	ESR	—	—	90	KΩ

1. Actual working drive level is dependent on real design. Please contact crystal vendor for selecting drive level of crystal.

4.1.7 Maximum supply currents

Power consumption is highly dependent on the application. Estimating the maximum supply currents required for power supply design is difficult because the use cases that requires maximum supply current is not a realistic use cases.

To help illustrate the effect of the application on power consumption, data was collected while running commercial standard benchmarks that are designed to be compute and graphic intensive. The results provided are intended to be used as guidelines for power supply design.

Table 19. Maximum supply currents

Power rail	Max current	Unit
VDD_SOC	2700	mA
VDD_ANA_0P8	50	mA
VDD_ANAx_1P8 [1]	250	mA
NVCC_BBSM_1P8	2	mA
NVCC_GPIO, NVCC_WAKEUP, NVCC_AON	I_{max} = N x C x V x (0.5 x F) Where: N—Number of IO pins supplied by the power line C—Equivalent external capacitive load V—IO voltage (0.5 x F)—Data change rate. Up to 0.5 of the clock rate (F). In this equation, I_{max} is in Amps, C in Farads, V in Volts, and F in Hertz.	
VDDQ_DDR	160	mA
VDD2_DDR	525	mA
VDD_MIPI_0P8 (for MIPI CSI-2 2-lane Rx PHY)	18	mA
VDD_MIPI_0P8 (for MIPI-DSI 4-lane Tx PHY)	33	mA
VDD_MIPI_1P8 (for MIPI CSI-2 2-lane Rx PHY)	2.5	mA

Table continues on the next page...

Table 19. Maximum supply currents *...continued*

Power rail	Max current	Unit
VDD_MIPI_1P8 (for MIPI-DSI 4-lane Tx PHY)	9.5	mA
VDD_USB_3P3 (for USB PHY)	25.2	mA
VDD_USB_1P8 (for USB PHY)	36.2	mA
VDD_USB_0P8 (for USB PHY)	22.2	mA
VDD_LVDS_1P8	Max dynamic current 45	mA

1. VDD_ANAx_1P8 refers to VDD_ANA0_1P8, VDD_ANA1_1P8, and VDD_ANAVDET_1P8.

4.2 Power modes

This section introduces the power modes used in the i.MX 93.

4.2.1 Power mode definition

The i.MX 93 supports the following power modes:

- RUN Mode: All external power rails are on, the Cortex-A55 is active and running; other internal modules can be on/off based on application.
- Low Power RUN Mode: This mode is defined as a very low power run mode with all external power rails are on. In this mode, all the unnecessary power domain (MIX) can be off, except AONMIX and the internal modules required, such as OSC24M/PLL. Cortex-M33 CPU in AONMIX handles all the computing and data processing. Cortex-A55 is power down and DRAM can be in self-refresh/retention mode. All the modules in the AONMIX, such as SAI/CAN/LPUART, can be used directly. To use modules in other power domain, such as WAKEUPMIX, the user can turn on additional peripherals and related power by Cortex-M33 as needed. Additional low power modes are also supported, but do not have power characterized in the Data Sheet. See the Reference Manual for a full set of power management capabilities.
- IDLE Mode: This mode is defined as a mode, which the Cortex-A55 can automatically enter when there is no thread running and all high-speed devices are not active. The Cortex-A55 can be put into power gated state but with L3 data retained, DRAM and the bus clock are reduced. Most of the internal logic is clock gated, but still remains powered. Compared with RUN mode, all the external power rails from the PMIC remain the same and most of the modules still remain in their state, so the interrupt response in this mode is very small.
- SUSPEND Mode: This mode is defined as the most power saving mode where all the clocks are off (including the Cortex-M33 CPU), all the unnecessary power supplies are off and all power gateable portions of the SoC are power gated. The Cortex-A55 CPU are fully power gated, all internal digital logic and analog circuit that can be powered down will be off, and all PHYs are power gated. DRAM is set at self-refresh/retention mode. VDD_SOC (and related digital supply) voltage is reduced to the "Suspend mode" voltage. The exit time from this mode will be much longer than IDLE, but the power consumption will also be much lower.
- BBSM Mode: This mode is also called RTC mode. Only the power for the BBSM domain remains on to keep RTC and BBSM logic alive.
- OFF Mode: All power rails are off.

NOTE

Beyond the modes defined here, additional options can be configured in software, such as to adjust clock frequencies or gate clocks through the CCM programming model, or to adjust on-die power-gating through the SRC or GPC programming model, or to adjust the voltage supplied to the VDD_SOC supply as per Operating ranges in the Data Sheet.

Table 20 summarizes the external power supply states in all the power modes.

Table 20. The power supply states

Power rail	OFF	BBSM	SUSPEND (Analog on)	IDLE	RUN/LP RUN
NVCC_BBSM_1P8	OFF	ON	ON	ON	ON
VDD_SOC	OFF	OFF	ON	ON	ON
VDD2_DDR VDDQ_DDR	OFF	OFF	ON	ON	ON
NVCC_<XXX>	OFF	OFF	ON	ON	ON
VDD_ANA_0P8 VDD_MIPI_0P8 VDD_USB_0P8	OFF	OFF	ON	ON	ON
VDD_ANAx_1P8 VDD_LVDS_1P8 VDD_MIPI_1P8 VDD_USB_1P8 VDD_USB_3P3	OFF	OFF	ON	ON	ON

4.2.2 Low power modes

The state of each module in the IDLE, SUSPEND, and BBSM mode are defined in the Table 21.

Table 21. Low power mode definition

	IDLE	SUSPEND	BBSM
CCM LPM mode	WAIT	STOP	N/A
Arm Cortex®-A55 CPU0	OFF	OFF	OFF
Arm Cortex®-A55 CPU1	OFF	OFF	OFF
Shared L3 cache	ON	OFF	OFF
Display	OFF	OFF	OFF
DRAM controller and PHY	ON	OFF	OFF
ARM_PLL	OFF	OFF	OFF
DRAM_PLL	OFF	OFF	OFF
SYSTEM_PLL 1/2/3	ON	OFF	OFF
XTAL	ON	OFF	OFF

Table continues on the next page...

Table 21. Low power mode definition ...continued

	IDLE	SUSPEND	BBSM
RTC	ON	ON	ON
External DRAM device	Self-Refresh	Self-Refresh	OFF
USB PHY	In Low Power State	OFF	OFF
DRAM clock	266 MHz	OFF	OFF
NOC clock	133 MHz	OFF	OFF
AXI clock	133 MHz	OFF	OFF
Module clocks	ON as needed	OFF	OFF
EdgeLock® Secure Enclave	ON	ON	ON
GPIO Wakeup	Yes	Yes	OFF
RTC Wakeup	Yes	Yes	Yes
USB remote wakeup	Yes	No[1]	No
Other wakeup source	Yes	No[2]	No
WAKEUPMIX	ON	OFF[3]	OFF
MLMIX	ON	OFF	OFF
NICMIX	ON as needed	OFF	OFF

1. USB remote wakeup can be "Yes" if required.
2. Other wakeup source can be "Yes" if required.
3. WAKEUPMIX can be "ON" if required.

NOTE

- Automatic enter self-refresh when there is no DRAM access.
- Put into self-refresh mode by software before entering low power mode.
- Turn off externally by PMIC when PMIC_STBY_REQ signal is asserted.
- Remote wakeup can be supported if the USB PHY power is on in this mode.

4.2.3 Chip power in different Low Power modes

Table 22 shows power consumption in different LP modes.

Table 22. Chip power in different LP modes

Mode	Supply	Voltage (V)	Power (mW)[1]
BBSM	NVCC_BBSM_1P8	1.8	0.14

Table continues on the next page...

Table 22. Chip power in different LP modes *...continued*

Mode	Supply	Voltage (V)	Power (mW)[1]
SUSPEND	NVCC_GPIO, NVCC_SD2	3.3	2.65
	NVCC_WAKEUP[2]	1.8	1.20
	VDDQ_DDR	0.6	< 0.01
	VDD2_DDR	1.1	0.25
	VDD_ANA*_1P8	1.8	1.85
	VDD_ANA_0P8	0.8	0.40
	VDD_MIPI_0P8	0.8	0.65
	VDD_USB_0P8	0.8	0.45
	VDD_USB_3P3	3.3	0.25
	VDD_SOC	0.65	7.40
	Total[3]	—	15.1

1. All the power numbers defined in the table are at 25ºC. Use case dependent.
2. To achieve this low power consumption values for I/O power rails in SUSPEND mode, it is recommended to configure the IOMUX of those pins to GPIO input and change the PAD control settings to pull-up or pull-down depends on the board design before entering SUSPEND mode.
3. Sum of the listed supply rails.

4.3 Power supplies requirements and restrictions

The system design must comply with power-up sequence, power-down sequence, and steady state guidelines as described in this section to guarantee the reliable operation of the device. Any deviation from these sequences may result in the following situations:

- Excessive current during power-up phase
- Prevention of the device from booting
- Irreversible damage to the processor (worst-case scenario)

Figure 4 illustrates an example about power sequence of i.MX 93 processors.

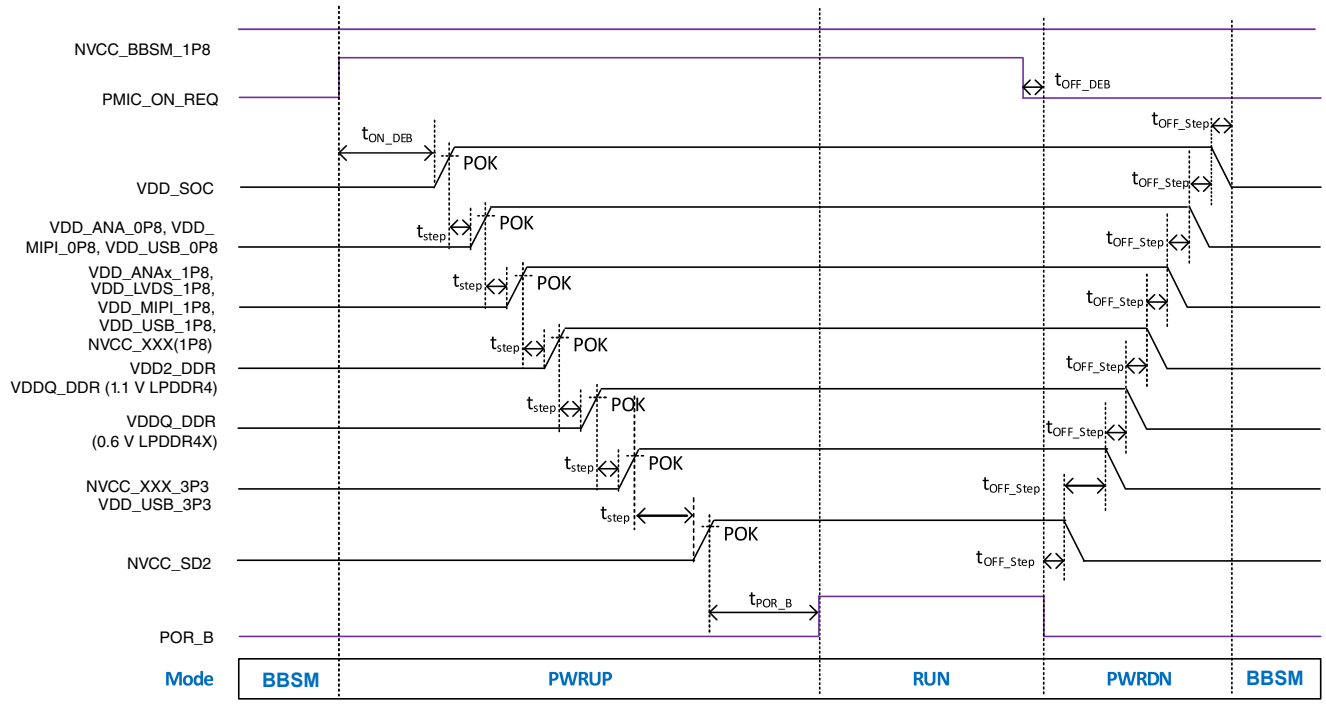


Figure 4. The power sequence of i.MX 93 processors

NOTE

POR_B must be asserted whenever VDD_SOC is powered down, but NVCC_BBSM_1P8 is powered up (when the processor is in BBSM mode).

4.3.1 Power-up sequence

The power-up sequence of i.MX 93 is defined as follows:

1. Turn on NVCC_BBSM_1P8
2. [The SoC will assert PMIC_ON_REQ at this point in time.]
3. Turn on VDD_SOC digital voltage supplies.
4. Turn on all VDD_*_0P8 analog, PHY, and PLL supplies.
5. Turn on all remaining 1.8 V supplies. This includes VDD_*_1P8 analog, PHY, PLL supplies, and any 1.8 V NVCC_XXX I/O supplies.
6. Turn on DDR I/O supplies.
7. Turn on 3.3 V supplies. This includes all 3.3 V NVCC_XXX I/O supplies and VDD_USB_3P3. [This 3.3 V supply step may be simultaneous with either the 1.8 V or the DDR supplies if desired.]
8. POR_B release (it should be asserted during the entire power-up sequence.)

4.3.2 Power-down sequence

The power-down sequence of i.MX 93 is defined as follows:

- Turn off NVCC_BBSM_1P8 last
- Turn off VDD_SOC after the other (non-BBSM) power rails or at the same time as other (non-BBSM) rails.
- No sequence for other power rails during power down.

4.4 PLL electrical characteristics

Table 23 shows the PLL electrical parameters.

Table 23. PLL electrical parameters

PLL type	Parameter	Value
AUDIO_PLL1	Clock output range	Up to 650 MHz
	Reference clock	24 MHz
	Lock time	50 µs
	Jitter	±1% of output period, ≥ 50 ps
VIDEO_PLL1	Clock output range	Up to 594 MHz
	Reference clock	24 MHz
	Lock time	50 µs
SYS_PLL1	Clock output range	312.5 MHz — 1 GHz
	Reference clock	24 MHz
	Lock time	70 µs
ARM_PLL	Clock output range	800 MHz — 1700 MHz
	Reference clock	24 MHz
	Lock time	70 µs
DRAM_PLL1	Clock output range	400 MHz — 1000 MHz
	Reference clock	24 MHz
	Lock time	50 µs

4.5 I/O DC parameters

This section includes the DC parameters of the following I/O types:

- General Purpose I/O (GPIO)
- Double Data Rate I/O (DDR) for LPDDR4 and LPDDR4X modes
- LVDS I/O

4.5.1 General purpose I/O (GPIO) DC parameters

Table 24 shows DC parameters for GPIO pads. The parameters Table 24 are guaranteed per the operating ranges in Table 12, unless otherwise noted.

Table 24. GPIO DC parameters

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
High-level output voltage	$V_{OH (1.8 V)}$	DS =1, IOH = 1.1 mA DS=6, IOH = 6.6 mA	0.8 x NVCC_xxx	—	NVCC_xxx	V
	$V_{OH (3.3 V)}$	DS =1, IOH = 2 mA DS=6, IOH = 12 mA	0.8 x NVCC_xxx	—	NVCC_xxx	V
Low-level output voltage	$V_{OL (1.8 V)}$	DS =1, IOL = 1.1 mA DS=6, IOL = 6.6 mA	0	—	0.2 x NVCC_xxx	V
	$V_{OL (3.3 V)}$	DS =1, IOL = 2 mA DS=6, IOL = 12 mA	0	—	0.2 x NVCC_xxx	V
Low-level input voltage	V_{IL}	NVCC_xxx = 1.65 - 3.465 V; Temp = -40 to 125°C	0	—	0.3 x NVCC_xxx	V
High-level input voltage	V_{IH}	NVCC_xxx = 1.65 - 3.465 V; Temp = -40 to 125°C	0.7 x NVCC_xxx	—	NVCC_xxx	V
Pull-down resistor	Rpd3.3v	NVCC_xxx = 3.0 - 3.465 V; Temp = -40 to 125°C	24	43	87	KΩ
Pull-up resistor	Rpu3.3v		18	37	72	KΩ
Pull-down resistor	Rpd1.8v	NVCC_xxx = 1.65 - 1.95 V; Temp = -40 to 125°C	13	23	48	KΩ
Pull-up resistor	Rpu1.8v		12	22	49	KΩ

NOTE

For GPIO pads, when the supplies are ramp-up or/and below operating level, the pad state values are undefined.

NOTE

For PHY pads, the PAD state values are undefined before POR_B is asserted.

Table 25. Additional leakage parameters

Parameter	Symbol	Condition	Min	Max	Unit
Leakage high	IIH	Non-PHY I/O, 1.65 V - 3.465 V, Temp = -40°C to 125°C | pad = VDDIO[1]	-5	5	µA
Leakage low	IIL	Non-PHY I/O, 1.65 V - 3.465 V, Temp = -40°C to 125°C | pad = VSS[1]	-5	5	

1. This specification does not apply to PHY, ANALOG, TAMPER0, TAMPER1 I/Os, PMIC_ON_REQ, and PMIC_STBY_REQ.

4.5.2 DDR I/O DC electrical characteristics

The DDR I/O pads support LPDDR4/LPDDR4X operational modes. The Double Data Rate Controller (DDRC) is compliant with JEDEC-compliant SDRAMs.

DDRC operation is contingent upon the board's DDR design adherence to the DDR design and layout requirements stated in the hardware development guide for the i.MX 93 application processors.

4.5.3 LVDS DC parameters

The LVDS interface complies with TIA/EIA 644-A standard. See TIA/EIA STANDARD 644-A, "Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits" for details.

Table 26 shows the Low Voltage Differential Signaling (LVDS) DC parameters.

Table 26. LVDS DC Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Output Differential Voltage	V_{OD}	Rload = 100 Ω between Pad P and Pad N	250	350	450	mV
Output High Voltage	V_{OH}	Rload = 100 Ω between Pad P and Pad N	1.25	—	1.6	V
Output Low Voltage	V_{OL}	Rload = 100 Ω between Pad P and Pad N	0.9	—	1.25	V
Offset common mode Voltage	V_{CM}	—	1.125	1.2	1.375	V
Tri-state I/O supply current	Icc-ovdd	VIN=OVDD or 0	0.016		1700	nA
Tri-state core supply current	Icc-vddi	VIN=VDDI or 0	—		1500	
Power Supply current	Icc	VIN=OVDD or 0 Rload=100 Ω	—		5	mA

4.6 I/O AC parameters

This section includes the AC parameters of the following I/O types:

- General Purpose I/O (GPIO)
- LVDS I/O

The GPIO load circuit and output transition time waveforms are shown in Figure 5 and Figure 6.

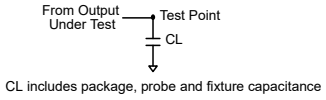


Figure 5. Load circuit for output

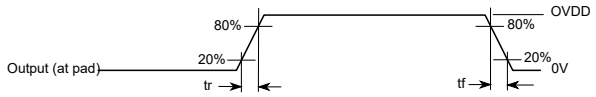


Figure 6. Output transition time waveform

4.6.1 General purpose I/O (GPIO) AC parameters

Table 27. General purpose I/O (GPIO) AC parameters

Symbol	Description	Min	Typ	Max	Unit	Condition
tR	TX rise time	3950	—	5950	ps	Slew rate FSEL1 = 11b, Fast Slew Rate (1.62 V, 1.8 V, 1.98 V), Drive strength x1
tF	TX fall time	4140	—	5600	ps	Slew rate FSEL1 = 11b, Fast Slew Rate (1.62 V, 1.8 V, 1.98 V), Drive strength x1
tR	TX rise time	1890	—	2820	ps	Slew rate FSEL1 = 11b, Fast Slew Rate (1.62 V, 1.8 V, 1.98 V), Drive strength x2
tF	TX fall time	1790	—	2560	ps	Slew rate FSEL1 = 11b, Fast Slew Rate (1.62 V, 1.8 V, 1.98 V), Drive strength x2
tR	TX rise time	675	—	1950	ps	Slew rate FSEL1 = 11b, Fast Slew Rate (1.62 V, 1.8 V, 1.98 V), Drive strength x3
tF	TX fall time	584	—	1730	ps	Slew rate FSEL1 = 11b, Fast Slew Rate (1.62 V, 1.8 V, 1.98 V), Drive strength x3
tR	TX rise time	521	—	1320	ps	Slew rate FSEL1 = 11b, Fast Slew Rate (1.62 V, 1.8 V, 1.98 V), Drive strength x4
tF	TX fall time	442	—	748	ps	Slew rate FSEL1 = 11b, Fast Slew Rate (1.62 V, 1.8 V, 1.98 V), Drive strength x4
tR	TX rise time	454	—	742	ps	Slew rate FSEL1 = 11b, Fast Slew Rate (1.62 V, 1.8 V, 1.98 V), Drive strength x5

Table continues on the next page...

Table 27. General purpose I/O (GPIO) AC parameters...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
tF	TX fall time	380	—	554	ps	Slew rate FSEL1 = 11b, Fast Slew Rate (1.62 V, 1.8 V, 1.98 V), Drive strength x5
tR	TX rise time	419	—	639	ps	Slew rate FSEL1 = 11b, Fast Slew Rate (1.62 V, 1.8 V, 1.98 V), Drive strength x6
tF	TX fall time	349	—	506	ps	Slew rate FSEL1 = 11b, Fast Slew Rate (1.62 V, 1.8 V, 1.98 V), Drive strength x6
tR	TX rise time	4030	—	5790	ps	Slew rate FSEL1 = 11b, Fast Slew Rate (3 V, 3.3 V, 3.465 V), Drive strength x1
tF	TX fall time	4410	—	6290	ps	Slew rate FSEL1 = 11b, Fast Slew Rate (3 V, 3.3 V, 3.465 V), Drive strength x1
tR	TX rise time	1870	—	2950	ps	Slew rate FSEL1 = 11b, Fast Slew Rate (1.62 V, 1.8 V, 1.98 V), Drive strength x2
tF	TX fall time	1900	—	3310	ps	Slew rate FSEL1 = 11b, Fast Slew Rate (3 V, 3.3 V, 3.465 V), Drive strength x2
tR	TX rise time	774	—	1930	ps	Slew rate FSEL1 = 11b, Fast Slew Rate (3 V, 3.3 V, 3.465 V), Drive strength x3
tF	TX fall time	719	—	2070	ps	Slew rate FSEL1 = 11b, Fast Slew Rate (3 V, 3.3 V, 3.465 V), Drive strength x3
tR	TX rise time	598	—	1360	ps	Slew rate FSEL1 = 11b, Fast Slew Rate (3 V, 3.3 V, 3.465 V), Drive strength x4
tF	TX fall time	490	—	1590	ps	Slew rate FSEL1 = 11b, Fast Slew Rate (3 V, 3.3 V, 3.465 V), Drive strength x4

Table continues on the next page...

Table 27. General purpose I/O (GPIO) AC parameters...*continued*

Symbol	Description	Min	Typ	Max	Unit	Condition
tR	TX rise time	543	—	1040	ps	Slew rate FSEL1 = 11b, Fast Slew Rate (3 V, 3.3 V, 3.465 V), Drive strength x5
tF	TX fall time	401	—	1160	ps	Slew rate FSEL1 = 11b, Fast Slew Rate (3 V, 3.3 V, 3.465 V), Drive strength x5
tR	TX rise time	505	—	887	ps	Slew rate FSEL1 = 11b, Fast Slew Rate (3 V, 3.3 V, 3.465 V), Drive strength x6
tF	TX fall time	356	—	747	ps	Slew rate FSEL1 = 11b, Fast Slew Rate (3 V, 3.3 V, 3.465 V), Drive strength x6

4.6.2 DDR I/O AC electrical characteristics

The DDR I/O pads support LPDDR4/LPDDR4X operational modes. The DDRC is compliant with JEDEC-compliant SDRAMs.

DDRC operation is contingent upon the board's DDR design adherence to the DDR design and layout requirements stated in the hardware development guide for the i.MX 93 application processor.

4.6.3 LVDS AC Parameters

The differential output transition time waveform is shown in Figure 7.

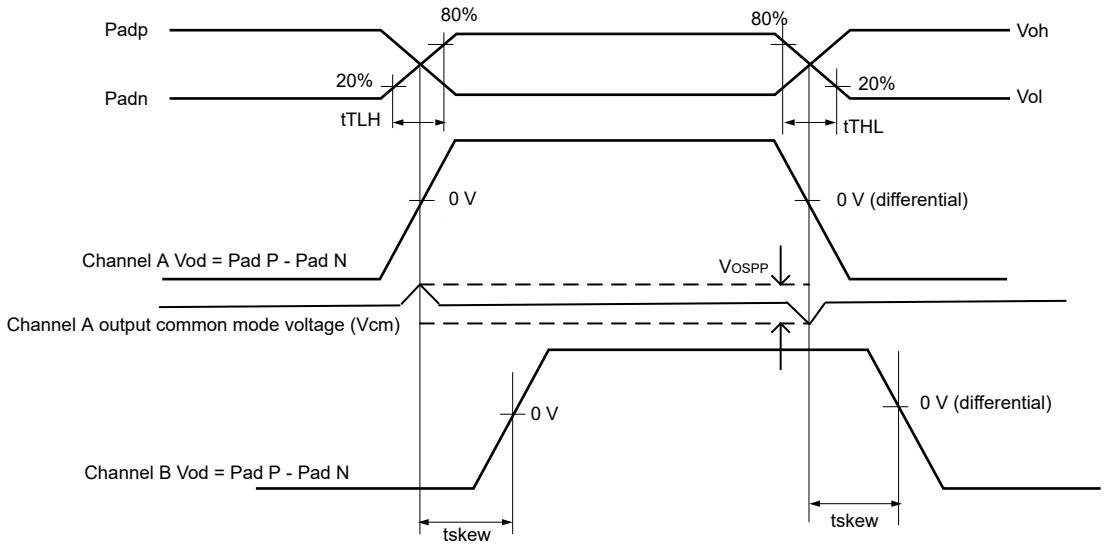


Figure 7. Output transition time waveform

Table 28 shows the AC parameters of LVDS.

Table 28. LVDS AC parameters

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Lane skew[1]	t_{SKew}	Rload = 100 Ω Cload = 2 pF	—	0.25[2]	—	ns
Transition Low to High time[3]	t_{TLH}		—	—	0.3	Unit Interval (UI)[4]
Transition High to Low time	t_{THL}		—	—	0.3	
Operating data rate[5]	f	—	—	—	560	Mbps
Offset peak to peak voltage imbalance	V_{ospp}	—	—	—	150	mV
Tri-state I/O supply current	Icc-ovdd	VIN=OVDD or 0	0.016	—	1700	nA
Tri-state core supply current	Icc-vddi	VIN=VDDI or 0	—	—	1500	
Power Supply current	Icc	VIN=OVDD or 0 Rload=100 Ω	—	—	5	mA

1. t_{SKew} is the differential time at V_{od} = 0 voltage between different channel.
2. This is typical maximum absolute delay between any two channels.
3. Measurement levels are 20–80% from output voltage.
4. This value is dependent on Operating data rate.
5. This is the maximum bit rate that defined by supported display types.

4.7 Differential I/O output buffer impedance

The Differential CCM interface is designed to be compatible with TIA/EIA 644-A standard. See, TIA/EIA STANDARD 644-A, *Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits* (2001) for details.

4.7.1 DDR I/O output impedance

DDR output driver and ODT impedances are controlled across PVT using ZQ calibration procedure with a 120 ohm ±1% resistor to ground. Programmable drive strength and ODT impedance targets available in the NXP DDR tool are detailed in the device IBIS model. Impedance deviation (calibration accuracy) is ±10% (Maximum/Minimum impedance) across PVT.

4.8 System modules timing

This section contains the timing and electrical parameters for the modules in each i.MX 93 processor.

4.8.1 Reset timing parameters

Figure 8 shows the reset timing and Table 29 lists the timing parameters.

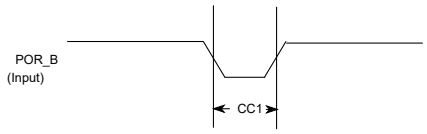


Figure 8. Reset timing diagram

Table 29. Reset timing parameters

ID	Parameter	Min	Max	Unit
CC1	Duration of POR_B to be qualified as valid. Note: POR_B rise/fall times must be 400 µs or less.	1	—	RTC_XTALI cycle

4.8.2 WDOG Reset timing parameters

Figure 9 shows the WDOG reset timing and Table 30 lists the timing parameters.

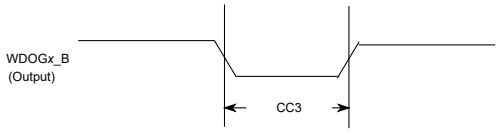


Figure 9. WDOGx_B timing diagram

Table 30. WDOG*x*_B timing parameters

ID	Parameter	Min	Max	Unit
CC3	Duration of WDOG1_B Assertion	1	—	RTC_XTALI cycle

NOTE

RTC_XTALI is approximately 32 kHz. RTC_XTALI cycle is one period or approximately 30 µs.

NOTE

WDOG*x*_B output signals (for each one of the Watchdog modules) do not have dedicated pins, but are muxed out through the IOMUX. See the IOMUXC chapter of the *i.MX 93 Applications Processor Reference Manual* (IMX93RM) for detailed information.

4.8.3 JTAG timing parameters

Figure 10 depicts the JTAG test clock input timing. Figure 11 depicts the JTAG boundary scan timing. Figure 12 depicts the JTAG test access port. Signal parameters are listed in Table 31.

The DSE[5:0] = 001111 and FSEL1[1:0] = 11 are required drive settings to meet the timing.

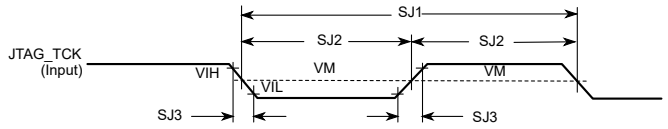


Figure 10. Test Clock Input Timing Diagram

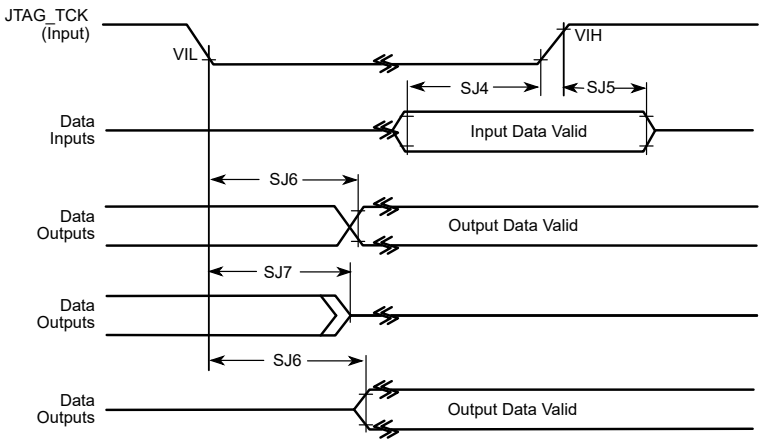


Figure 11. Boundary system (JTAG) timing diagram

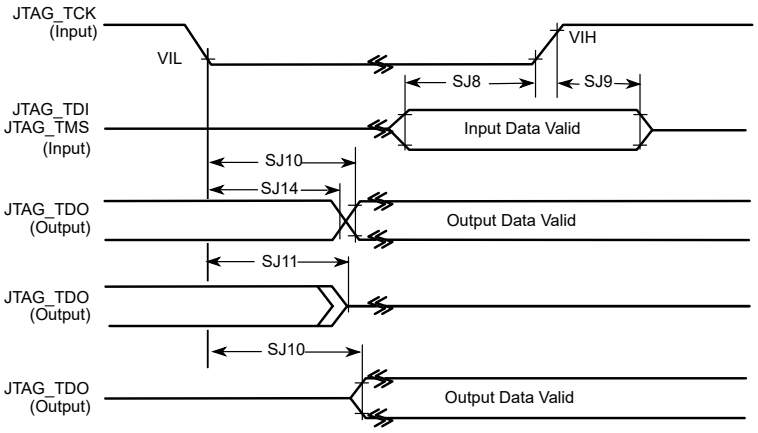


Figure 12. Test Access Port Timing Diagram

Table 31. JTAG Timing[1,2]

ID	Parameter	All Frequencies		Unit
		Min	Max	
SJ0	JTAG_TCK frequency of operation[3,4]	—	50	MHz
SJ1	JTAG_TCK cycle time in crystal mode	20	—	ns
SJ2	JTAG_TCK clock pulse width measured at V_M[5]	10	—	ns
SJ3	JTAG_TCK rise and fall times	—	3	ns
SJ4	Boundary scan input data set-up time	15	—	ns
SJ5	Boundary scan input data hold time	15	—	ns
SJ6	JTAG_TCK low to output data valid	—	600	ns
SJ7	JTAG_TCK low to output high impedance	—	600	ns
SJ8	JTAG_TMS, JTAG_TDI data set-up time	5	—	ns
SJ9	JTAG_TMS, JTAG_TDI data hold time	5	—	ns
SJ10	JTAG_TCK low to JTAG_TDO data valid	—	14	ns
SJ11	JTAG_TCK low to JTAG_TDO high impedance	—	14	ns
SJ14	JTAG_TCK low to JTAG_TDO data invalid	1	—	ns

1. Input timing assumes an input signal slew rate of 3 ns (20%/80%).
2. Output timing valid for maximum external load CL = 25 pF, which is assumed to be a 10 pF load at the end of a 50 Ω, unterminated, 5-inch microstrip trace on standard FR4 (3.3 pF/inch), (25 pF total with margin). For best signal integrity, the series resistance of the transmission line can be equal to the selected RDSON of the I/O pad output driver.
3. T_{DC} = target frequency of JTAG
4. 50 MHz frequency is for the JTAG debug interface. For boundary scan, the maximum TCK frequency is 10 MHz.
5. V_M = mid-point voltage

4.8.4 SWD timing parameters

The DSE[5:0] = 001111 and FSEL1[1:0] = 11 are required drive settings to meet the timing.

Figure 13 depicts the SWD timing.

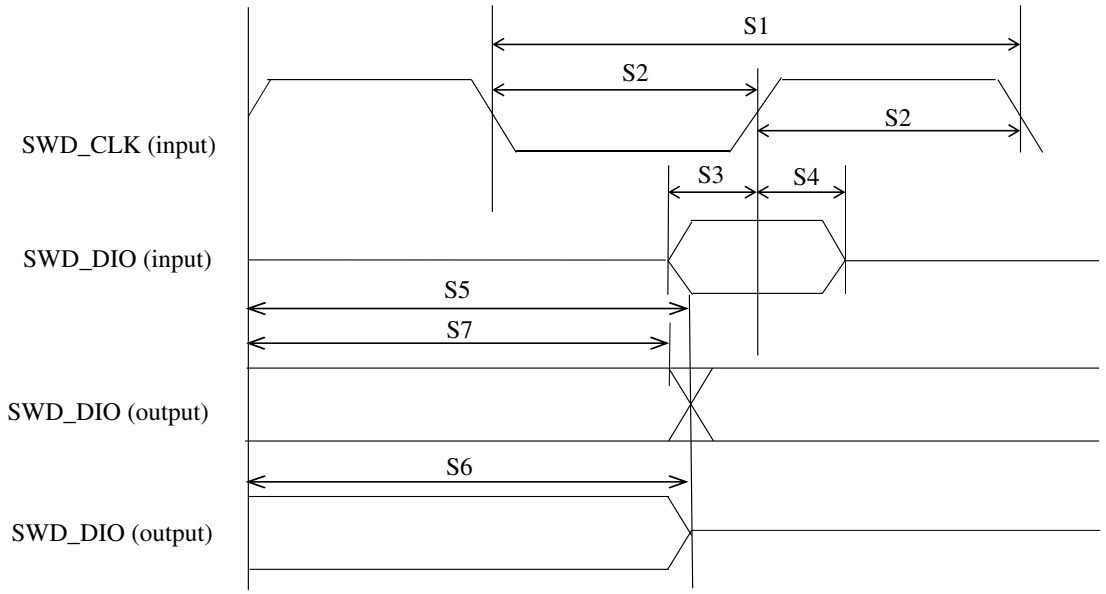


Figure 13. SWD timing

Table 32 lists SWD timing parameters.

Table 32. SWD timing parameters[1,2]

Symbol	Description	Min	Max	Unit
S0	SWD_CLK frequency	—	50	MHz
S1	SWD_CLK cycle time	20	—	ns
S2	SWD_CLK pulse width	10	—	ns
S3	Input data setup time	5	—	ns
S4	Input data hold time	5	—	ns
S5	Output data valid time	—	14	ns
S6	Output high impedance time	—	14	ns
S7	Output data invalid time	0	—	ns

1. Input timing assumes an input signal slew rate of 3 ns (20%/80%).
2. Timing valid for maximum external load CL = 25 pF, which is assumed to be a 10 pF load at the end of a 50 Ω, unterminated, 5-inch microstrip trace on standard FR4 (3.3 pF/inch), (25 pF total with margin). For best signal integrity, the series resistance in the transmission line can be equal to the selected RDSON of the I/O pad output.

4.8.5 DDR SDRAM–specific parameters (LPDDR4/LPDDR4X)

The i.MX 93 Family of processors have been designed and tested to work with JEDEC JESD209—compliant LPDDR4/LPDDR4X memory.

- JEDEC LPDDR4 Specification JESD209-4B, February 2017
- JEDEC LPDDR4X Specification JESD209-4-1, January 2017

Timing diagrams and tolerances required to work with these memories are specified in the respective documents and are not reprinted here.

Meeting the necessary timing requirements for a DDR memory system is highly dependent on the components chosen and the design layout of the system as a whole. NXP cannot cover in this document all the requirements needed to achieve a design that meets full system performance over temperature, voltage, and part variation; PCB trace routing, PCB dielectric material, number of routing layers used, placement of bulk/decoupling capacitors on critical power rails, VIA placement, GND and Supply planes layout, and DDR controller/PHY register settings all are factors affecting the performance of the memory system. Consult the hardware user guide for this device and NXP validated design layouts for information on how to properly design a PCB for best DDR performance. NXP strongly recommends duplicating an NXP validated design as much as possible in the design of critical power rails, placement of bulk/decoupling capacitors and DDR trace routing between the processor and the selected DDR memory. All supporting material is readily available on the device web page on https://www.nxp.com/products/processors-and-microcontrollers/arm-processors/i-mx-applications-processors/i-mx-9-processors:IMX9-PROCESSORS.

Processors that demonstrate full DDR performance on NXP validated designs, but do not function on customer designs, are not considered marginal parts. A report detailing how the returned part behaved on an NXP validated system will be provided to the customer as closure to a customer's reported DDR issue. Customers bear the responsibility of properly designing the Printed Circuit Board, correctly simulating and modeling the designed DDR system, and validating the system under all expected operating conditions (temperatures, voltages) prior to releasing their product to market.

Table 33. i.MX 93 DRAM controller supported SDRAM configurations

Parameter	LPDDR4/LPDDR4X
Number of Controllers	1
Number of Channels	1
Number of Chip Selects	2
Bus Width	16-bit
Maximum supported data rate	
• Low drive mode	1866 MT/s
• Nominal drive mode	2880 MT/s
• Overdrive mode	3733 MT/s[1]

1. For 9 x 9 mm package, the maximum date rate of LPDDR4x/LPDDR4 is 3200 MT/s.

4.8.5.1 Clock/data/command/address pin allocations

These processors uses generic names for clock, data, and command address bus; see Table 103 for details about mapping of clock, data, and command address signals of LPDDR4/LPDDR4X modes.

4.9 Display and graphics

The following sections provide information on display and graphic interfaces.

4.9.1 MIPI D-PHY electrical characteristics

4.9.1.1 MIPI HS-TX specifications

Table 34. MIPI high-speed transmitter DC specifications

Symbol	Parameter	Min	Typ	Max	Unit
V_{CMTX}[1]	High Speed Transmit Static Common Mode Voltage	150	200	250	mV
$\|\Delta V_{CMTX}\|_{(1,0)}$	V_{CMTX} mismatch when Output is Differential-1 or Differential-0	—	—	5	mV
$\|V_{OD}\|$[1]	High Speed Transmit Differential Voltage	140	200	270	mV
$\|\Delta V_{OD}\|$	V_{OD} mismatch when Output is Differential-1 or Differential-0	—	—	14	mV
V_{OHHS}[1]	High Speed Output High Voltage	—	—	360	mV
Z_{OS}	Single Ended Output Impedance	40	50	62.5	Ω
ΔZ_{OS}	Single Ended Output Impedance Mismatch	—	—	10	%

1. Value when driving into load impedance anywhere in the Z_{ID} range.

Table 35. MIPI high-speed transmitter AC specifications

Symbol	Parameter	Min	Typ	Max	Unit
$\Delta V_{CMTX(HF)}$	Common-level variations above 450 MHz	—	—	15	mVRMS
$\Delta V_{CMTX(LF)}$	Common-level variation between 50-450 MHz	—	—	25	mVPEAK
t_R and t_F[1]	Rise Time and Fall Time (20% to 80%)	100	—	0.35 x UI	ps

1. UI is the long-term average unit interval.

4.9.1.2 MIPI HS-RX specifications

Table 36. MIPI high-speed receiver DC specifications

Symbol	Parameter	Min	Typ	Max	Unit
V_{IDTH}	Differential input high voltage threshold	—	—	70	mV
V_{IDTL}	Differential input low voltage threshold	-70	—	—	mV
V_{IHHS}	Single ended input high voltage	—	—	460	mV
V_{ILHS}	Single ended input low voltage	-40	—	—	mV
V_{CMRXDC}	Input common mode voltage	70	—	330	mV
Z_{ID}	Differential input impedance	80	100	125	Ω

Table 37. MIPI high-speed receiver AC specifications

Symbol	Parameter	Min	Typ	Max	Unit
$\Delta V_{CMRX(HF)}$[1]	Common mode interference beyond 450 MHz	—	—	50	mV
$\Delta V_{CMRX(LF)}$	Common mode interference between 50 and 450 MHz	-25	—	25	mV
C_{CM}	Common mode termination	—	—	60	pF

1. $\Delta V_{CMRX(HF)}$ is the peak amplitude of a sine wave superimposed on the receiver inputs.

4.9.1.3 MIPI LP-TX specifications

Table 38. MIPI low-power transmitter DC specifications

Symbol	Parameter	Min	Typ	Max	Unit
V_{OH}[1]	Thevenin Output High Level	1.1	1.2	1.3	V
V_{OL}	Thevenin Output Low Level	–50	—	50	mV
Z_{OLP}[2]	Output Impedance of Low Power Transmitter	110	—	—	Ω

1. This specification can only be met when limiting the core supply variation from 1.1 V till 1.3 V.
2. Although there is no specified maximum for ZOLP, the LP transmitter output impedance ensures the TRLP/TFLP specification is met.

Table 39. MIPI low-power transmitter AC specifications

Symbol	Parameter	Min	Typ	Max	Unit
T_{RLP}/T_{FLP}[1]	15% to 85% Rise Time and Fall Time	—	—	25	ns
T_{REOT}[1,2,3]	30% to 85% Rise Time and Fall Time	—	—	35	ns
$T_{LP\text{-}PULSE\text{-}TX}$[4]	Pulse width of the LP exclusive-OR clock: First LP exclusive-OR clock pulse after Stop state or last pulse before Stop state	40	—	—	ns
	Pulse width of the LP exclusive-OR clock: All other pulses	20	—	—	ns
$T_{LP\text{-}PER\text{-}TX}$	Period of the LP exclusive-OR clock	90	—	—	ns
$\delta V/\delta t_{SR}$[1,5,6,7]	Slew Rate @ CLOAD= 0 pF	25	—	500	mV/ns
	Slew Rate @ CLOAD= 5 pF	25	—	300	mV/ns
	Slew Rate @ CLOAD= 20 pF	25	—	250	mV/ns
	Slew Rate @ CLOAD= 70 pF	25	—	150	mV/ns
C_{LOAD}	Load Capacitance	0	—	70	pF

1. C_{LOAD} includes the low equivalent transmission line capacitance. The capacitance of TX and RX are assumed to always be < 10 pF. The distributed line capacitance can be up to 50 pF for a transmission line with 2 ns delay.
2. The rise-time of TREOT starts from the HS common-level at the moment of the differential amplitude drops below 70 mV, due to stopping the differential drive.

3. With an additional load capacitance CCM between 0 to 60 pF on the termination center tap at RX side of the lane.
4. This parameter value can be lower then TLPX due to differences in rise vs. fall signal slopes and trip levels and mismatches between Dp and Dn LP transmitters. Any LP exclusive-OR pulse observed during HS EoT (transition from HS level to LP-11) is glitch behavior as described in Low-Power Receiver section.
5. When the output voltage is between 15% and below 85% of the fully settled LP signal levels.
6. Measured as average across any 50 mV segment of the output signal transition.
7. This value represents a corner point in a piecewise linear curve.

4.9.1.4 MIPI LP-RX specifications

Table 40. MIPI low power receiver DC specifications

Symbol	Parameter	Min	Typ	Max	Unit
V_{IH}	Logic 1 input voltage	740	—	—	mV
V_{IL}	Logic 0 input voltage, not in ULP state	—	—	550	mV
$V_{IL-ULPS}$	Logic 0 input voltage, ULP state	—	—	300	mV
V_{HYST}	Input hysteresis	25	—	—	mV

Table 41. MIPI low power receiver AC specifications

Symbol	Parameter	Min	Typ	Max	Unit
e_{SPIKE}[1,2]	Input pulse rejection	—	—	300	V.ps
T_{MIN-RX}[3]	Minimum pulse width response	20	—	—	ns
V_{INT}	Peak Interference amplitude	—	—	200	mV
f_{INT}	Interference frequency	450	—	—	MHz

1. Time-voltage integration of a spike above V_{IL} when in LP-0 state or below VIH when in LP-1 state.
2. An impulse below this value will not change the receiver state.
3. An input pulse greater than this value shall toggle the output.

4.9.1.5 MIPI LP-CD specifications

Table 42. MIPI contention detector DC specifications

Symbol	Parameter	Min	Typ	Max	Unit
V_{IHCD}	Logic 1 contention threshold	450	—	—	mV
V_{ILCD}	Logic 0 contention threshold	—	—	200	mV

4.9.2 LCD Controller (LCDIF) timing parameters

The DSE[5:0] = 001111 and FSEL1[1:0] = 11 are required drive settings to meet the timing.

Figure 14 shows the LCDIF timing and Table 43 lists the timing parameters.

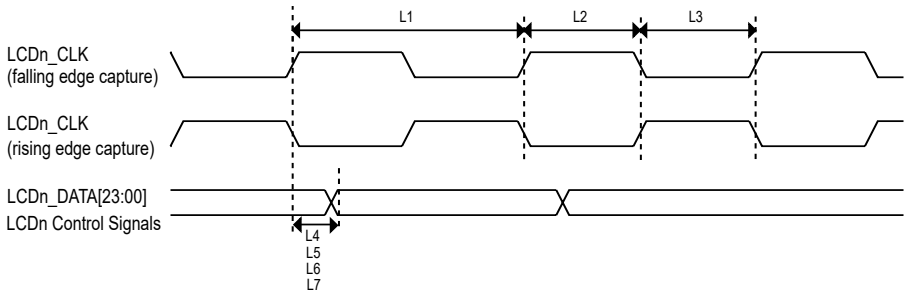


Figure 14. LCD timing

Table 43. LCD timing parameters[1,2]

ID	Parameter	Symbol	Min	Max	Unit
L1	LCD pixel clock frequency[3]	tCLK(LCD)	—	80	MHz
L2	LCD pixel clock high (falling edge capture)	tCLKH(LCD)	5	—	ns
L3	LCD pixel clock low (rising edge capture)	tCLKL(LCD)	5	—	ns
L4	LCD pixel clock high to data valid (falling edge capture)	td(CLKH-DV)	-1.5	1.5	ns
L5	LCD pixel clock low to data valid (rising edge capture)	td(CLKL-DV)	-1.5	1.5	ns
L6	LCD pixel clock high to control signal valid (falling edge capture)	td(CLKH-CTRLV)	-1.5	1.5	ns
L7	LCD pixel clock low to control signal valid (rising edge capture)	td(CLKL-CTRLV)	-1.5	1.5	ns

1. Output timing valid for maximum external load CL = 25 pF, which is assumed to be a 10 pF load at the end of a 50 ohm, unterminated, 5-inch microstrip trace on standard FR4 (3.3 pF/inch), (25 pF total with margin). For best signal integrity, the series resistance in the transmission line should be equal to the selected RDSON of the I/O pad output driver.
2. Input timing assumes an input signal slew rate of 3 ns (20%/80%).
3. The maximum frequency supported is 52 MHz when NVCC_xxxx operating at 3.3 V.

4.10 Audio

This section provides information about audio subsystem.

4.10.1 SAI switching specifications

This section provides the AC timings for the SAI in Controller (clocks driven) and Target (clocks input) modes. All timings are given for non inverted serial clock polarity (SAI_TCR2[BCP] = 0, SAI_RCR2[BCP] = 0) and non inverted frame sync (SAI_TCR4[FSP] = 0, SAI_RCR4[FSP] = 0). If the polarity of the clock and/or the frame sync have been inverted, all the timings remain valid by inverting the clock signal (SAI_BCLK) and/or the frame sync (SAI_FS) shown in the figures below.

The DSE[5:0] = 001111 and FSEL1[1:0] = 11 are required drive settings to meet the timing.

For the 50 MHz BCLK operation, the BCLK and SYNC must always be in the same direction as the data (source synchronous):

- SAI transmitter must be in asynchronous mode with BCLK and SYNC configuration as outputs
- SAI receiver must be:
  - In asynchronous mode with BCLK and SYNC configuration as inputs
  - In synchronous mode with SAI_RCR2[BCI] = 1

Table 44. Controller mode SAI timing (50 MHz)[1,2,3]

Num	Characteristic	Min	Max	Unit
S1	SAI_MCLK cycle time	20	—	ns
S2	SAI_MCLK pulse width high/low	40%	60%	MCLK period
S3	SAI_BCLK cycle time	20	—	ns
S4	SAI_BCLK pulse width high/low	40%	60%	BCLK period
S5	SAI_BCLK to SAI_FS output valid	—	3	ns
S6	SAI_BCLK to SAI_FS output invalid	-2	—	ns
S7	SAI_BCLK to SAI_TXD valid	—	3	ns
S8	SAI_BCLK to SAI_TXD invalid	-2	—	ns
S9	SAI_RXD/SAI_FS input setup before SAI_BCLK	3	—	ns
S10	SAI_RXD/SAI_FS input hold after SAI_BCLK	2	—	ns

1. To achieve 50 MHz for BCLK operation, clock must be set in feedback mode.
2. Input timing assumes an input signal slew rate of 3 ns (20%/80%).
3. Output timing valid for maximum external load CL = 25 pF, which is assumed to be a 10 pF load at the end of a 50 ohm. Unterminated, 5-inch microstrip trace on standard FR4 (3.3 pF/inch), (25 pF total with margin). For best signal integrity, the series resistance in the transmission line should be equal to the selected RDSON of the I/O pad output driver.

Table 45. Controller mode SAI timing (25 MHz)[1,2]

Num	Characteristic	Min	Max	Unit
S1	SAI_MCLK cycle time	40	—	ns
S2	SAI_MCLK pulse width high/low	40%	60%	MCLK period
S3	SAI_BCLK cycle time	40	—	ns
S4	SAI_BCLK pulse width high/low	40%	60%	BCLK period
S5	SAI_BCLK to SAI_FS output valid	—	3	ns
S6	SAI_BCLK to SAI_FS output invalid	-2	—	ns
S7	SAI_BCLK to SAI_TXD valid	—	3	ns
S8	SAI_BCLK to SAI_TXD invalid	-2	—	ns
S9	SAI_RXD/SAI_FS input setup before SAI_BCLK	8	—	ns
S10	SAI_RXD/SAI_FS input hold after SAI_BCLK	0	—	ns

1. Input timing assumes an input signal slew rate of 3 ns (20%/80%).

2. Output timing valid for maximum external load CL = 25 pF, which is assumed to be a 10 pF load at the end of a 50 ohm. Unterminated, 5-inch microstrip trace on standard FR4 (3.3 pF/inch), (25 pF total with margin). For best signal integrity, the series resistance in the transmission line should be equal to the selected RDSON of the I/O pad output driver.

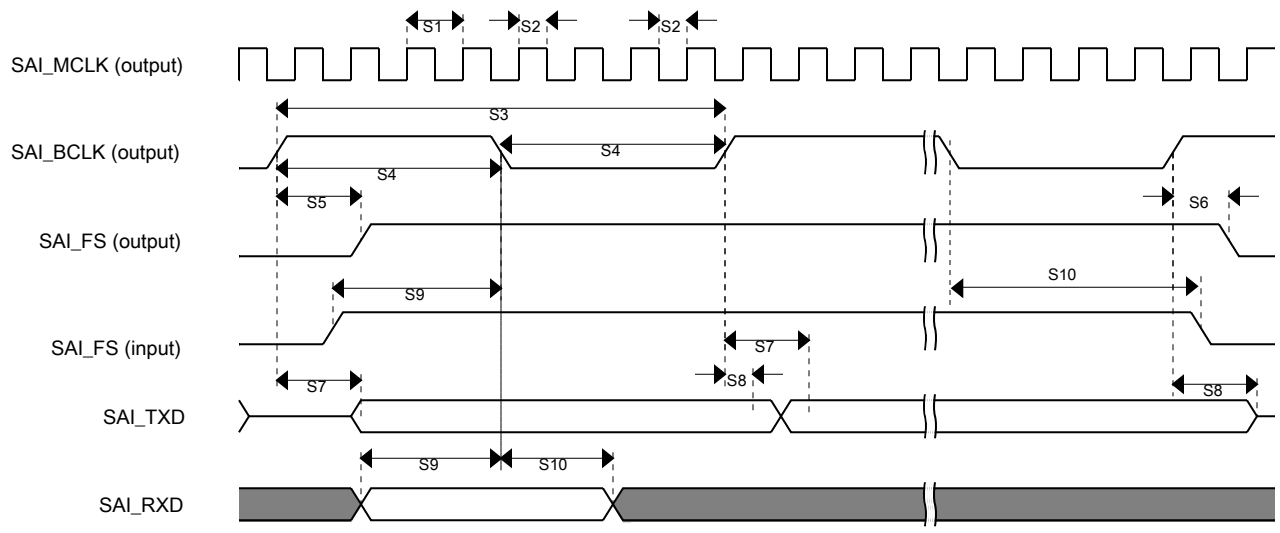


Figure 15. SAI timing—Controller mode

Table 46. Target mode SAI timing (25 MHz)[1,2]

Num	Characteristic	Min	Max	Unit
S11	SAI_BCLK cycle time (input)	40	—	ns
S12	SAI_BCLK pulse width high/low (input)	40%	60%	BCLK period
S13	SAI_FS input setup before SAI_BCLK	3	—	ns
S14	SAI_FS input hold after SAI_BCLK	2	—	ns
S15	SAI_BCLK to SAI_TXD/SAI_FS output valid	—	9	ns
S16	SAI_BCLK to SAI_TXD/SAI_FS output invalid	0	—	ns
S17	SAI_RXD setup before SAI_BCLK	3	—	ns
S18	SAI_RXD hold after SAI_BCLK	2	—	ns
S19	SAI_FS input assertion to SAI_TXD output valid[3]	—	25	ns

1. Input timing assumes an input signal slew rate of 3 ns (20%/80%).
2. Output timing valid for maximum external load CL = 25 pF, which is assumed to be a 10 pF load at the end of a 50 ohm. Unterminated, 5-inch microstrip trace on standard FR4 (3.3 pF/inch), (25 pF total with margin). For best signal integrity, the series resistance in the transmission line should be equal to the selected RDSON of the I/O pad output driver.
3. Applies to first bit in each frame and only if the TCR4[FSE] bit is clear.

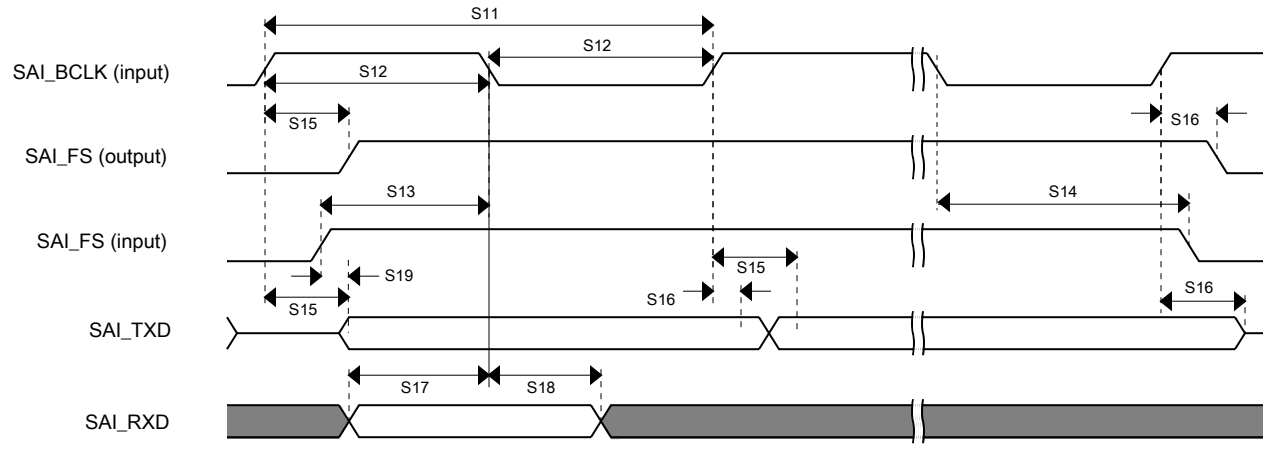


Figure 16. SAI Timing — Target Mode

4.10.2 SPDIF timing parameters

The Sony/Philips Digital Interconnect Format (SPDIF) data is sent using the bi-phase marking code. When encoding, the SPDIF data signal is modulated by a clock that is twice the bit rate of the data signal.

Table 47 and Figure 17 and Figure 18 show SPDIF timing parameters for the Sony/Philips Digital Interconnect Format (SPDIF), including the timing of the modulating Rx clock (SPDIF_SR_CLK) for SPDIF in Rx mode and the timing of the modulating Tx clock (SPDIF_ST_CLK) for SPDIF in Tx mode.

The DSE[5:0] = 001111 and FSEL1[1:0] = 11 are required drive settings to meet the timing.

Table 47. SPDIF timing parameters

Parameter	Symbol	Timing Parameter Range		Unit
		Min	Max	
SPDIF_IN Skew: asynchronous inputs, no specs apply	—	—	0.7	ns
SPDIF_OUT output (Load = 50 pf) • Skew • Transition rising • Transition falling	— — —	— — —	1.5 24.2 31.3	ns
SPDIF_OUT output (Load = 30 pf) • Skew • Transition rising • Transition falling	— — —	— — —	1.5 13.6 18.0	ns
Modulating Rx clock (SPDIF_SR_CLK) period	srckp	40.0	—	ns
SPDIF_SR_CLK high period	srckph	16.0	—	ns

Table continues on the next page...

Table 47. SPDIF timing parameters *...continued*

Parameter	Symbol	Timing Parameter Range		Unit
		Min	Max	
SPDIF_SR_CLK low period	srckpl	16.0	—	ns
Modulating Tx clock (SPDIF_ST_CLK) period	stclkp	40.0	—	ns
SPDIF_ST_CLK high period	stclkph	16.0	—	ns
SPDIF_ST_CLK low period	stclkpl	16.0	—	ns

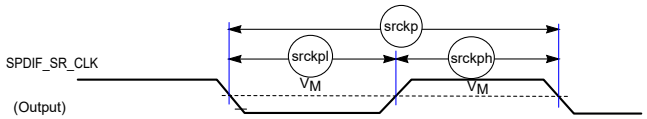


Figure 17. SPDIF_SR_CLK timing diagram

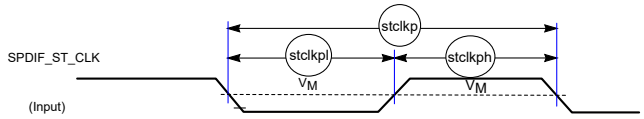


Figure 18. SPDIF_ST_CLK timing diagram

4.10.3 PDM Microphone interface timing parameters

NOTE

These timing requirements apply only if the clock divider is enabled (PDM_CTRL2[CLKDIV] = 0), otherwise there are no special timing requirements.

The PDM microphones must meet the setup and hold timing requirements shown in the following table. The "k" factor value in Table 48 depends on the selected quality mode as shown in Table 49.

Table 48. PDM timing parameters

Parameter	Value
trs, tfs	$<= \frac{\text{floor (kxCLKDIV) - 1}}{@\ \text{(moduleNickname)\_CLK\_ROOTrate}}$ [1]
trh, tfh	≥ 0

1. Depending on K value, user must make sure floor (K x CLKDIV) > 1 to avoid timing problems.

Table 49. K factor value

Quality factor	K factor
High Quality	1/2
Medium Quality, Very Low Quality 0	1
Low Quality, Very Low Quality 1	2
Very Low Quality 2	4

Figure 19 illustrates the timing requirements for the PDM.

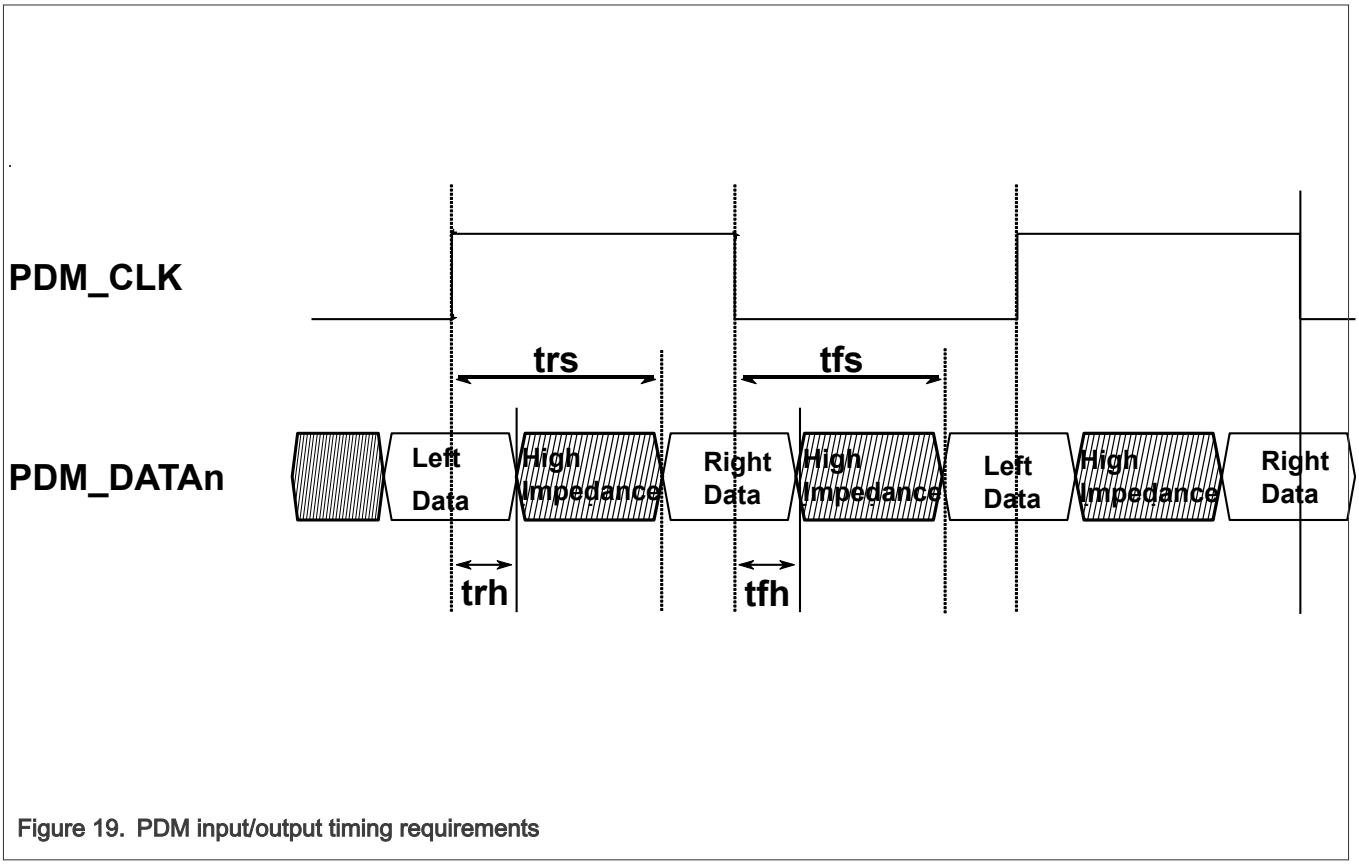


Figure 19. PDM input/output timing requirements

4.10.4 Medium Quality Sound (MQS) electrical specifications

Medium quality sound (MQS) is used to generate medium quality audio via a standard GPIO in the pinmux, allowing the user to connect stereo speakers or headphones to a power amplifier without an additional DAC chip. Two outputs are asynchronous PWM pulses and their maximum frequency is 1/32 x mclk_frequency.

Table 50. MQS specifications

Symbol	Description	Min	Typ	Max	Unit
f_{mclk} [1,2]	Bit clock is used to generate the mclk.	—	24.576	66.5	MHz

1. Frequency of mclk depends on software settings.

Please see General purpose I/O (GPIO) AC parameters for other electrical parameters.

2. The maximum frequency supported is 52 MHz when NVCC_xxxx operating at 3.3 V.

4.11 Analog

The following sections introduce the timing and electrical parameters about analog interfaces of i.MX 93 processors.

4.11.1 12-bit ADC electrical specifications

All ADC channels meet the 12-bit single-ended accuracy specifications.

Table 51. ADC electrical specifications

Symbol	Description	Min	Typ	Max	Unit	Notes
V_{ADIN}	Input voltage	V_{GND}	—	V_{DDA}	V	1
f_{AD_CK}	ADC clock frequency	20	—	80	MHz	—
C_{sample}	Sample cycles	5.5	—	—	Cycle	—
$C_{compare}$	Fixed compare cycles	—	58	—	Cycle	—
$C_{conversion}$	Conversion cycles	$C_{conversion} = C_{sample} + C_{compare}$			Cycle	—
C_{AD_INPUT}	ADC input capacitance	—	—	7	pF	2
R_{AD_INPUT}	ADC input series resistance	—	—	1.25	KΩ	—
DNL	ADC differential nonlinearity	—	±2	—	LSB	3
INL	ADC integral nonlinearity	—	±6	—	LSB	3
R_{AS}	Analog source resistance	—	—	5	KΩ	—
Bandgap	Output voltage ready time for bandgap	—	1	—	µs	4
ENOB	Effective number of bits: Single-ended mode (11 x 11 mm package, PWM)	—	9.8	—	bit	5,6,7,8
	Effective number of bits: Single-ended mode (11 x 11 mm package, PFM)	—	9.4	—		
	Effective number of bits: Single-ended mode (9 x 9 mm package, PWM)	—	9.2	—		
	Effective number of bits: Single-ended mode (9 x 9 mm package, PFM)	—	8.5	—		

Table continues on the next page...

Table 51. ADC electrical specifications *...continued*

Symbol	Description	Min	Typ	Max	Unit	Notes
	Effective number of bits: Single-ended mode (14 x 14 mm package, PWM)	—	10.5	—		
	Effective number of bits: Single-ended mode (14 x 14 mm package, PFM)	—	10.1	—		

1. On or off channels
2. ADC component plus pad capacitance (~ 2 pF)
3. After calibration
4. Based on simulation test
5. Noise on the ADC reference voltage (VDD_ANA1P8) will result in performance loss of the ADC proportional to the noise present.
6. Input data used for test is 1 kHz sine wave.
7. Measured at VREFH = 1.8 V and pwrsel = 2.
8. ENOB can be lower than shown, if an ADC channel corrupts other ADC channels through capacitive coupling. This coupling may be dominated by board parasitics. Care must be taken not to corrupt the desired channel being measured. This coupling becomes worse at higher analog frequencies and with switching waveforms due to the harmonic content.

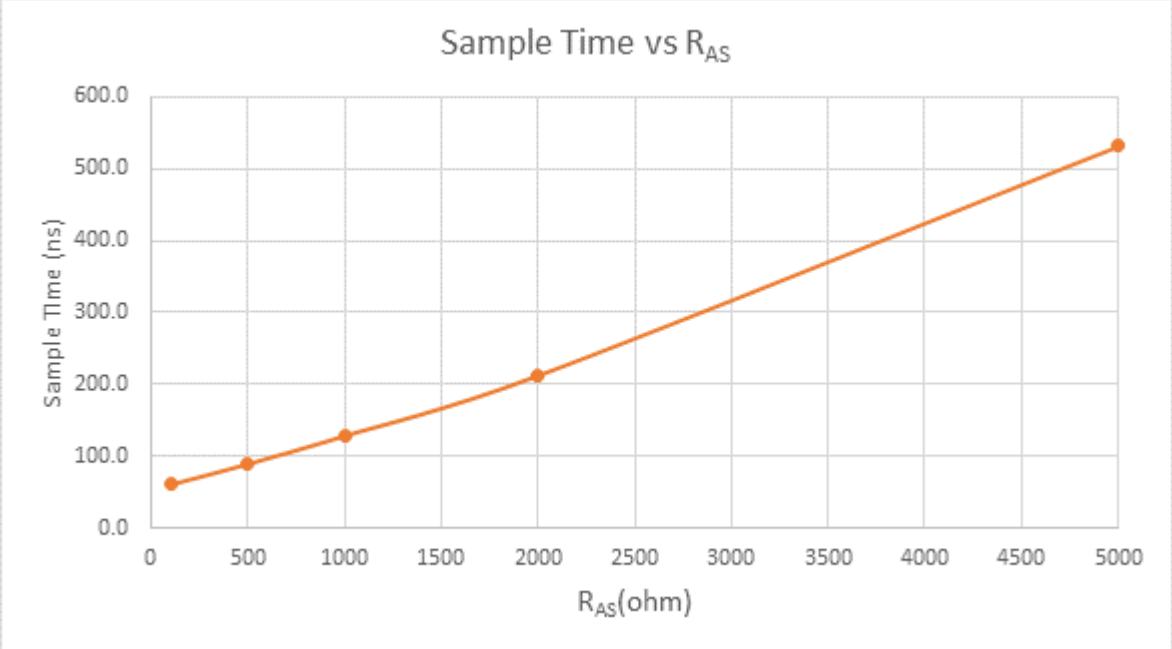


Figure 20. Sample time vs R_{AS}

4.11.2 12-bit ADC input impedance equivalent circuit diagram

There is an additional R_{IOMUX} of 350 Ω (from 295 Ω to 405 Ω) resistance if an input goes through the MUX inside the IO and C_P of 2.5 pF as shown in Figure 21.

To calculate the sample request time, using the following equation where $R_{ADCtotal} = R_{ADIN} + R_{IOMUX}$, R_{IOMUX} = 350 Ω, C_P = 2.5 pF and B = 11 for 1/4 LSB settling.

$T_{smp\_req} = B [R_{AS} (C_{AS} + C_P + C_{ADIN}) + (R_{AS} + R_{ADCtotal}) C_{ADIN}]$

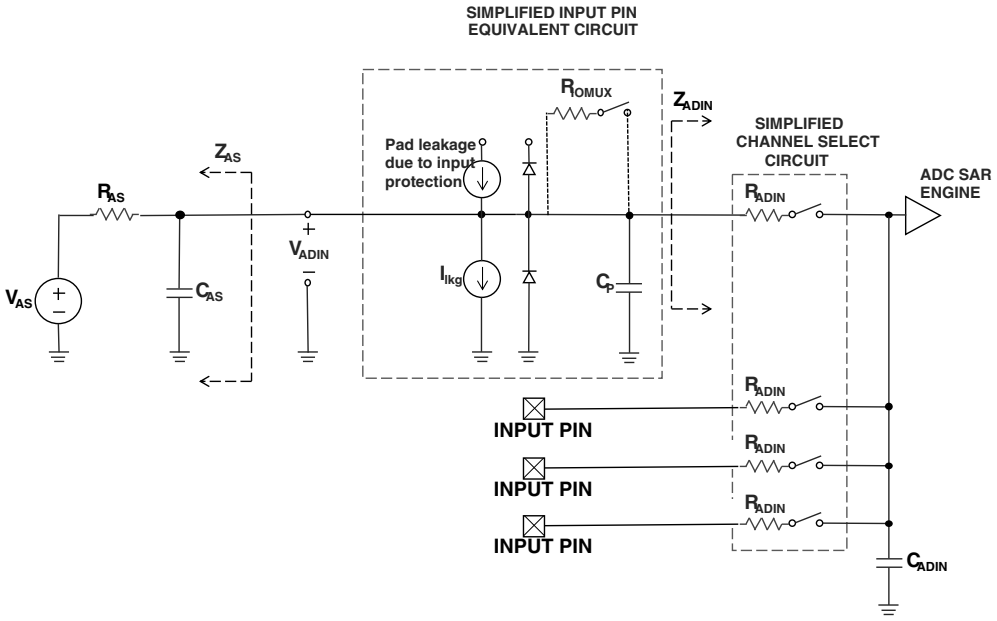


Figure 21. ADC input impedance equivalent circuit diagram

4.12 External peripheral interface parameters

The following subsections provide information on external peripheral interfaces.

4.12.1 Ultra-high-speed SD/SDIO/MMC host interface (uSDHC) AC timing

This section describes the electrical information of the uSDHC, which includes SD/eMMC5.1 (single data rate) timing, eMMC5.1/SD3.0 (dual data rate) timing and SDR50/SDR104 AC timing.

The DSE[5:0] = 001111 and FSEL1[1:0] = 11 are required drive settings to meet the timing.

4.12.1.1 SD3.0/eMMC5.1 (single data rate) AC timing

Figure 22 depicts the timing of SD3.0/eMMC5.1, and Table 52 lists the SD3.0/eMMC5.1 timing characteristics.

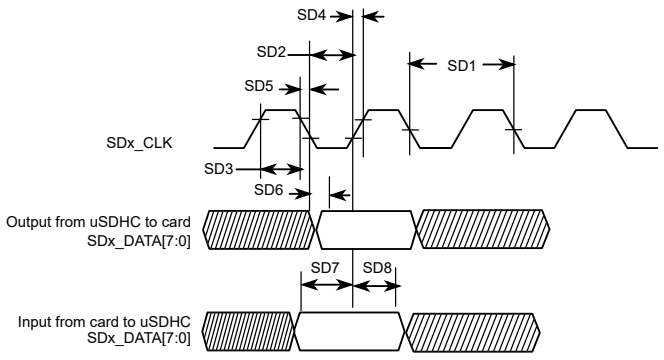


Figure 22. SD3.0/eMMC5.1 (SDR) timing

Table 52. SD3.0/eMMC5.1 (SDR) interface timing specification[1,2]

ID	Parameter	Symbols	Min	Max	Unit
	Card Input Clock				
SD1	Clock Frequency (Low Speed)	f_{PP}[3]	0	400	kHz
	Clock Frequency (SD/SDIO Full Speed/High Speed)	f_{PP}[4]	0	25/50	MHz
	Clock Frequency (MMC Full Speed/High Speed)	f_{PP}[5]	0	20/52	MHz
	Clock Frequency (Identification Mode)	f_{OD}	100	400	kHz
SD2	Clock Low Time	t_{WL}	7	—	ns
SD3	Clock High Time	t_{WH}	7	—	ns
SD4	Clock Rise Time	t_{TLH}	—	3	ns
SD5	Clock Fall Time	t_{THL}	—	3	ns
	uSDHC Output/Card Inputs SD_CMD, SDx_DATAx (Reference to CLK)				
SD6	uSDHC Output Delay	t_{OD}	-6.6	3.6	ns
	uSDHC Input/Card Outputs SD_CMD, SDx_DATAx (Reference to CLK)				
SD7	uSDHC Input Setup Time	t_{ISU}	2.5	—	ns
SD8	uSDHC Input Hold Time[6]	t_{IH}	1.5	—	ns

1. Input timing assumes an input signal slew rate of 3 ns (20%/80%).
2. Output timing valid for maximum external load CL = 25 pF, which is assumed to be a 10 pF load at the end of a 50 ohm, unterminated, 5-inch microstrip trace on standard FR4 (3.3 pF/inch), (25 pF total with margin). For best signal integrity, the series resistance in the transmission line should be equal to the selected RDSON of the I/O pad output driver.
3. In Low-Speed mode, card clock must be lower than 400 kHz, voltage ranges from 2.7 to 3.6 V.
4. In Normal (Full) -Speed mode for SD/SDIO card, clock frequency can be any value between 0 – 25 MHz. In High-speed mode, clock frequency can be any value between 0 – 50 MHz.
5. In Normal (Full) -Speed mode for MMC card, clock frequency can be any value between 0 – 20 MHz. In High-speed mode, clock frequency can be any value between 0 – 52 MHz.

6. To satisfy hold timing, the delay difference between clock input and cmd/data input must not exceed 2 ns.

4.12.1.2 SD3.0/eMMC5.1 (dual data rate) AC timing

Figure 23 depicts the timing of SD3.0/eMMC5.1 (DDR). Table 53 lists the SD3.0/eMMC5.1 (DDR) timing characteristics. Be aware that only DATA is sampled on both edges of the clock (not applicable to CMD).

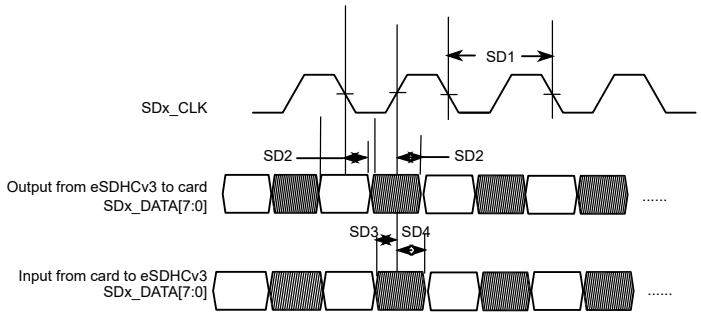


Figure 23. eMMC5.1/SD3.0 (DDR) timing

Table 53. SD3.0/eMMC5.1 (DDR) interface timing specification[1,2]

ID	Parameter	Symbols	Min	Max	Unit
Card Input Clock					
SD1	Clock Frequency (eMMC5.1 DDR)	f_{PP}	0	52	MHz
SD1	Clock Frequency (SD3.0 DDR)	f_{PP}	0	50	MHz
uSDHC Output / Card Inputs SD_CMD, SDx_DATAx (Reference to CLK)					
SD2	uSDHC Output Delay	t_{OD}	2.8	6.8	ns
uSDHC Input / Card Outputs SD_CMD, SDx_DATAx (Reference to CLK)					
SD3	uSDHC Input Setup Time	t_{ISU}	2.4	—	ns
SD4	uSDHC Input Hold Time	t_{IH}	1.5	—	ns

1. Input timing assumes an input signal slew rate of 3 ns (20%/80%).
2. Output timing valid for maximum external load CL = 25 pF, which is assumed to be a 10 pF load at the end of a 50 ohm, unterminated, 5-inch microstrip trace on standard FR4 (3.3 pF/inch), (25 pF total with margin). For best signal integrity, the series resistance in the transmission line should be equal to the selected RDSON of the I/O pad output driver.

4.12.1.3 HS400 DDR AC timing

Figure 24 depicts the timing of HS400 mode, Table 54 and Table 55 list the HS400 timing characteristics. Be aware that only data is sampled on both edges of the clock (not applicable to CMD). The CMD input/output timing for HS400 mode is the same as CMD input/output timing for SDR104 mode. Check SD5, SD6, and SD7 parameters in Table 58 and Table 59 for HS400 mode.

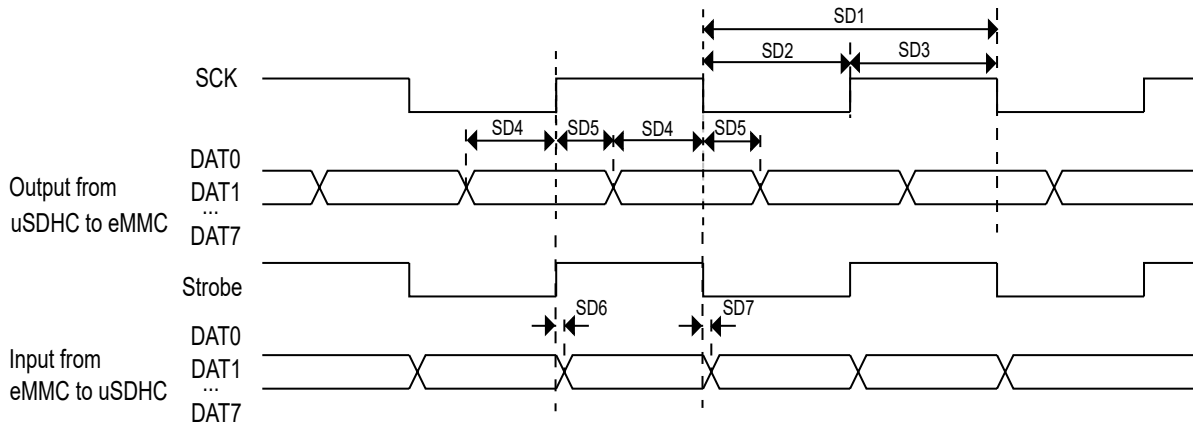


Figure 24. HS400 timing

Table 54. HS400 interface timing specification (Nominal and Overdrive mode)[1,2]

ID	Parameter	Symbols	Min	Max	Unit
Card Input Clock					
SD1	Clock frequency	f_{PP}	0	200	MHz
SD2	Clock low time	t_{CL}	2.2	—	ns
SD3	Clock high time	t_{CH}	2.2	—	ns
uSDHC Output/Card Inputs DAT (Reference to SCK)					
SD4	Output skew from Data of edge of SCK	t_{OSkew1}	0.45	—	ns
SD5	Output skew from SCK to Data of edge	t_{OSkew2}	0.45	—	ns
uSDHC Input/Card Outputs DAT (Reference to Strobe)					
SD6	uSDHC input skew	t_{RQ}	—	0.45	ns
SD7	uSDHC hold skew	t_{RQH}	—	0.45	ns

1. Input timing assumes an input signal slew rate of 1 ns (20%/80%).
2. Output timing valid for maximum external load CL = 15 pF, which is assumed to be a 8 pF load at the end of a 50 ohm, unterminated, 2-inch microstrip trace on standard FR4 (3.3 pF/inch). For best signal integrity, the series resistance of the transmission line should be matched closely to the RDSON of the I/O pad output driver.

Table 55. HS400 interface timing specification (Low drive mode)[1,2]

ID	Parameter	Symbols	Min	Max	Unit
Card Input Clock					
SD1	Clock frequency	f_{PP}	0	133	MHz

Table continues on the next page...

Table 55. HS400 interface timing specification (Low drive mode)[1,2] *...continued*

ID	Parameter	Symbols	Min	Max	Unit
SD2	Clock low time	t_{CL}	3.3	—	ns
SD3	Clock high time	t_{CH}	3.3	—	ns
uSDHC Output/Card Inputs DAT (Reference to SCK)					
SD4	Output skew from data of edge of SCK	t_{OSkew1}	0.45	—	ns
SD5	Output skew from edge of SCk to data	t_{OSkew2}	0.45	—	ns
uSDHC Input/Card Outputs DAT (Reference to Strobe)					
SD6	uSDHC input skew	t_{RQ}	—	0.45	ns
SD7	uSDHC hold skew	t_{RQH}	—	0.45	ns

1. Input timing assumes an input signal slew rate of 1 ns (20%/80%).
2. Output timing valid for maximum external load CL = 15 pF, which is assumed to be a 8 pF load at the end of a 50 ohm, unterminated, 2-inch microstrip trace on standard FR4 (3.3 pF/inch). For best signal integrity, the series resistance of the transmission line should be matched closely to the RDSON of the I/O pad output driver.

4.12.1.4 HS200 Mode AC timing

Figure 25 depicts the timing of HS200 mode, Table 56 and Table 57 list the HS200 timing characteristics.

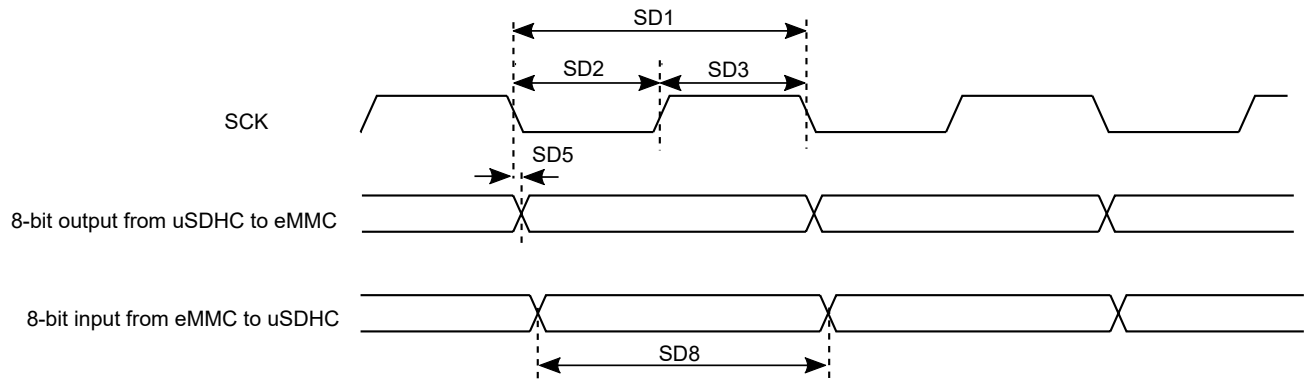


Figure 25. HS200 timing

Table 56. HS200 interface timing specification (Nominal and Overdrive mode)[1,2]

ID	Parameter	Symbols	Min	Max	Unit
Card Input Clock					
SD1	Clock Frequency Period	t_{CLK}	5.0	—	ns
SD2	Clock Low Time	t_{CL}	2.2	—	ns
SD3	Clock High Time	t_{CH}	2.2	—	ns

Table continues on the next page...

Table 56. HS200 interface timing specification (Nominal and Overdrive mode)[1,2] *...continued*

ID	Parameter	Symbols	Min	Max	Unit
uSDHC Output/Card Inputs SD_CMD, SDx_DATAx in HS200 (Reference to CLK)					
SD5	uSDHC Output Delay	t_{OD}	-1.6	1	ns
uSDHC Input/Card Outputs SD_CMD, SDx_DATAx in HS200 (Reference to CLK)[3]					
SD8	uSDHC Input Data Window	t_{ODW}	0.475 x t_{CLK}	—	ns

1. Input timing assumes an input signal slew rate of 1 ns (20%/80%).
2. Output timing valid for maximum external load CL = 15 pF, which is assumed to be a 8 pF load at the end of a 50 ohm, unterminated, 2-inch microstrip trace on standard FR4 (3.3 pF/inch). For best signal integrity, the series resistance of the transmission line should be matched closely to the RDSON of the I/O pad output driver.
3. HS200 is for 8 bits while SDR104 is for 4 bits.

Table 57. HS200 interface timing specification (Low drive mode)[1,2]

ID	Parameter	Symbols	Min	Max	Unit
Card Input Clock					
SD1	Clock Frequency Period	t_{CLK}	7.5	—	ns
SD2	Clock Low Time	t_{CL}	3.3	—	ns
SD3	Clock High Time	t_{CH}	3.3	—	ns
uSDHC Output/Card Inputs SD_CMD, SDx_DATAx in HS200 (Reference to CLK)					
SD5	uSDHC Output Delay	t_{OD}	-1.6	1	ns
uSDHC Input/Card Outputs SD_CMD, SDx_DATAx in HS200 (Reference to CLK)[3]					
SD8	uSDHC Input Data Window	t_{ODW}	0.475 x t_{CLK}	—	ns

1. Input timing assumes an input signal slew rate of 1 ns (20%/80%).
2. Output timing valid for maximum external load CL = 15 pF, which is assumed to be a 8 pF load at the end of a 50 ohm, unterminated, 2-inch microstrip trace on standard FR4 (3.3 pF/inch). For best signal integrity, the series resistance of the transmission line should be matched closely to the RDSON of the I/O pad output driver.
3. HS200 is for 8 bits while SDR104 is for 4 bits.

4.12.1.5 SDR50/SDR104 AC timing

Figure 26 depicts the timing of SDR50/SDR104, Table 58 and Table 59 list the SDR50/SDR104 timing characteristics.

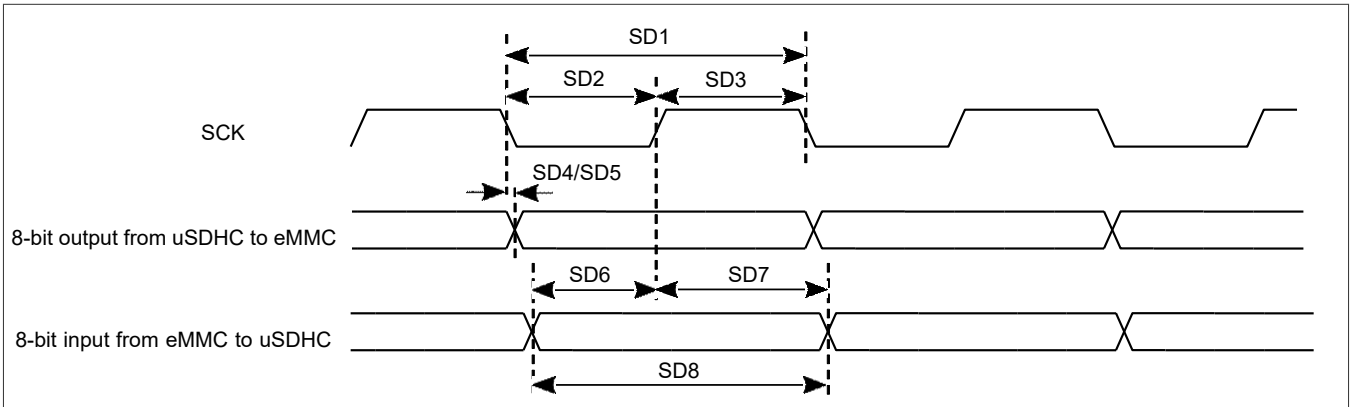


Figure 26. SDR50/SDR104 timing

Table 58. SDR50/SDR104 interface timing specification (Nominal and Overdrive mode)[1,2]

ID	Parameter	Symbols	Min	Max	Unit
Card Input Clock					
SD1	Clock Frequency Period	t_{CLK}	5	—	ns
SD2	Clock Low Time	t_{CL}	2.2	—	ns
SD3	Clock High Time	t_{CH}	2.2	—	ns
uSDHC Output/Card Inputs SD_CMD, SDx_DATAx in SDR50 (Reference to CLK)					
SD4	uSDHC Output Delay	t_{OD}	-3	1	ns
uSDHC Output/Card Inputs SD_CMD, SDx_DATAx in SDR104 (Reference to CLK)					
SD5	uSDHC Output Delay	t_{OD}	-1.6	1	ns
uSDHC Input/Card Outputs SD_CMD, SDx_DATAx in SDR50 (Reference to CLK)					
SD6	uSDHC Input Setup Time	t_{ISU}	2.4	—	ns
SD7	uSDHC Input Hold Time	t_{IH}	1.5	—	ns
uSDHC Input/Card Outputs SD_CMD, SDx_DATAx in SDR104 (Reference to CLK)[3]					
SD8	uSDHC Input Data Window	t_{ODW}	0.5 x t_{CLK}	—	ns

1. Input timing assumes an input signal slew rate of 1 ns (20%/80%).
2. Output timing valid for maximum external load CL = 15 pF, which is assumed to be a 8 pF load at the end of a 50 ohm, unterminated, 2-inch microstrip trace on standard FR4 (3.3 pF/inch). For best signal integrity, the series resistance of the transmission line should be matched closely to the RDSON of the I/O pad output driver.
3. Data window in SDR100 mode is variable.

Table 59. SDR50/SDR104 interface timing specification (Low drive mode)[1,2]

ID	Parameter	Symbols	Min	Max	Unit
Card Input Clock					
SD1	Clock Frequency Period	t_{CLK}	7.5	—	ns
SD2	Clock Low Time	t_{CL}	3.3	—	ns
SD3	Clock High Time	t_{CH}	3.3	—	ns
uSDHC Output/Card Inputs SD_CMD, SDx_DATAx in SDR50 (Reference to CLK)					
SD4	uSDHC Output Delay	t_{OD}	-3	1	ns
uSDHC Output/Card Inputs SD_CMD, SDx_DATAx in SDR104 (Reference to CLK)					
SD5	uSDHC Output Delay	t_{OD}	-1.6	1	ns
uSDHC Input/Card Outputs SD_CMD, SDx_DATAx in SDR50 (Reference to CLK)					
SD6	uSDHC Input Setup Time	t_{ISU}	2.4	—	ns
SD7	uSDHC Input Hold Time	t_{IH}	1.5	—	ns
uSDHC Input/Card Outputs SD_CMD, SDx_DATAx in SDR104 (Reference to CLK)[3]					
SD8	uSDHC Input Data Window	t_{ODW}	0.5 x t_{CLK}	—	ns

1. Input timing assumes an input signal slew rate of 1 ns (20%/80%).
2. Output timing valid for maximum external load CL = 15 pF, which is assumed to be a 8 pF load at the end of a 50 ohm, unterminated, 2-inch microstrip trace on standard FR4 (3.3 pF/inch). For best signal integrity, the series resistance of the transmission line should be matched closely to the RDSON of the I/O pad output driver.
3. Data window in SDR100 mode is variable.

4.12.1.6 Bus operation condition for 3.3 V and 1.8 V signaling

Signaling level of SD/eMMC4.5/5.0/5.1 can be 1.8 V or 3.3 V depending on the working mode. The DC parameters for NVCC_SD2 supplies are identical to those shown in General purpose I/O (GPIO) DC parameters.

4.12.1.7 uSDHC supported modes

For SD:

- All SD 3.0 protocols are supported at full speeds on all three SDHC interfaces. This includes DS, HS, SDR12, SDR25, SDR50, SDR104, and DDR50.
- The maximum supported SDR frequency is 200 MHz which is covered in SDR104 mode, and maximum DDR frequency is 50 MHz as a part of DDR50 mode.

For eMMC:

- eMMC HS400 is only supported on SDHC1 as that is the only one with 8-bit interface.
- eMMC HS200 is supported on all three SDHC interfaces because this protocol supports both 4-bit mode and 8-bit mode, which can work on SDHC2 and SDHC3.
- eMMC High Speed DDR, High Speed SDR, and less than or equal to 26 MHz MMC legacy protocols are also supported on all three SDHC interfaces.

- The maximum supported SDR frequency is 200 MHz which is covered in HS200 mode, and the maximum DDR frequency is 200 MHz as a part of HS400 mode.

uSDHC3 supports up to SDR104 (200 MHz) on primary SD3_* pins, but when it is multiplexing on GPIO_IO[27:22], below are the modes supported:

- eMMC High Speed DDR, High Speed SDR, and less than or equal to 26 MHz MMC legacy protocols are supported.
- SDR50 (100 MHz) and SDR104 (200 MHz) modes are NOT supported.
- eMMC HS400 and HS200 modes are NOT supported
- The maximum supported SDR and DDR frequency is 50 and 52 MHz

If IO is supplied by 3.3 V, the maximum supported SDR/DDR frequency is 50/52 MHz

4.12.2 Ethernet controller (ENET) AC electrical specifications

Ethernet supports the following key features:

- Support ENET AVB
- Support IEEE 1588
- Support Energy Efficient Ethernet (EEE)
- 1.8 V/3.3 V RMII operation, 1.8 V RGMII operation

The following sections introduce the ENET AC electrical specifications.

4.12.2.1 ENET2 signal mapping

The following timing specs are defined at the chip I/O pin and must be translated appropriately to arrive at timing specs/constraints for the physical interface.

Table 60. ENET2 signal mapping[1]

Pad name	RGMII	Alt mode	RMII	Alt mode	Direction
ENET2_MDC	RGMII_MDC	Alt 0	RMII_MDC	Alt 0	O
ENET2_MDIO	RGMII_MDIO	Alt 0	RMII_MDIO	Alt 0	I/O
ENET2_TXC	RGMII_TXC	Alt 0	RMII_TX_ER	Alt 1	O
ENET2_TX_CTL	RGMII_TX_CTL	Alt 0	RMII_TX_EN	Alt 0	O
ENET2_TD0	RGMII_TD0	Alt 0	RMII_TD0	Alt 0	O
ENET2_TD1	RGMII_TD1	Alt 0	RMII_TD1	Alt 0	O
ENET2_TD2	RGMII_TD2	Alt 0	RMII_REF_CLK[2]	Alt 1	I/O
ENET2_TD3	RGMII_TD3	Alt 0	—	Alt 0	O
ENET2_RXC	RGMII_RXC	Alt 0	RMII_RX_ER	Alt 1	I
ENET2_RX_CTL	RGMII_RX_CTL	Alt 0	RMII_CRS_DV	Alt 0	I
ENET2_RD0	RGMII_RD0	Alt 0	RMII_RD0	Alt 0	I

Table continues on the next page...

Table 60. ENET2 signal mapping[1] *...continued*

Pad name	RGMII	Alt mode	RMII	Alt mode	Direction
ENET2_RD1	RGMII_RD1	Alt 0	RMII_RD1	Alt 0	I
ENET2_RD2	RGMII_RD2	Alt 0	—	Alt 0	I
ENET2_RD3	RGMII_RD3	Alt 0	—	Alt 0	I

1. ENET1 is Ethernet QoS with TSN, while ENET2 is Ethernet MAC.
2. The signal can be either input or output.

4.12.2.2 RMII mode timing

In RMII mode, enet1.RMII_CLK is used as the REF_CLK, which is a 50 MHz ± 50 ppm continuous reference clock.

Figure 27 shows RMII mode timings. Table 61 describes the timing parameters (M16–M21) shown in the figure.

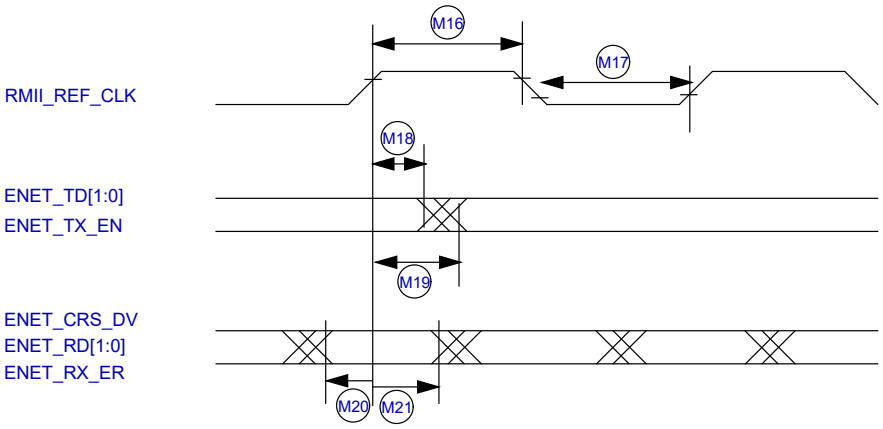


Figure 27. RMII mode signal timing diagram

Table 61. RMII signal timing[1,2,3]

ID	Characteristic	Min.	Max.	Unit
M16	ENET_CLK pulse width high	35%	65%	RMII_REF_CLK period
M17	RMII_REF_CLK pulse width low	35%	65%	RMII_REF_CLK period
M18	RMII_REF_CLK to ENET0_TXD[1:0], ENET_TX_EN invalid	2	—	ns
M19	RMII_REF_CLK to ENET0_TXD[1:0], ENET_TX_EN valid	—	14	ns
M20	ENET_RX_DATA[1:0], ENET_CRS_DV, ENET_RX_ER to RMII_REF_CLK setup	4	—	ns
M21	RMII_REF_CLK to ENET_RX_DATA[1:0], ENET_CRS_DV, ENET_RX_ER hold	2	—	ns

1. The timings assume the following configuration: DSE[5:0] = 001111 and FSEL1[1:0] = 11.

2. Input timing assumes an input signal slew rate of 3 ns (20%/80%).
3. Output timing valid for maximum external load CL = 25 pF, which is assumed to be a 10 pF load at the end of a 50 ohm, unterminated, 5-inch microstrip trace on standard FR4 (3.3 pF/inch), (25 pF total with margin). For best signal integrity, the series resistance in the transmission line should be equal to the selected RDSON of the I/O pad output driver.

4.12.2.3 MII serial management channel timing (ENET_MDIO and ENET_MDC)

The MDC frequency is designed to be equal to or less than 2.5 MHz to be compatible with the IEEE 802.3 MII specification.

Figure 28 shows MII asynchronous input timings. Table 62 describes the timing parameters (M10–M15) shown in the figure.

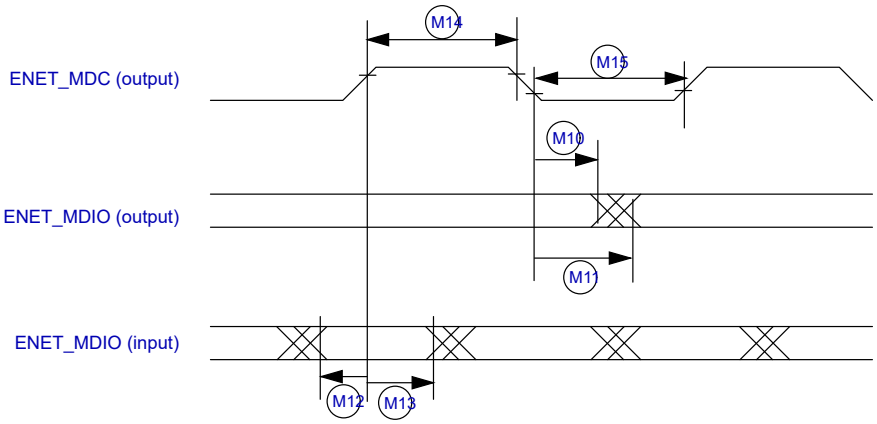


Figure 28. MII serial management channel timing diagram

Table 62. MII serial management channel timing[1,2,3]

ID	Characteristic	Min.	Max.	Unit
M10	ENET_MDC falling edge to ENET_MDIO output invalid (min. propagation delay)	-1.5	—	ns
M11	ENET_MDC falling edge to ENET_MDIO output valid (max. propagation delay)	—	13	ns
M12	ENET_MDIO (input) to ENET_MDC rising edge setup	13	—	ns
M13	ENET_MDIO (input) to ENET_MDC rising edge hold	0	—	ns
M14	ENET_MDC pulse width high	40%	60%	ENET_MDC period
M15	ENET_MDC pulse width low	40%	60%	ENET_MDC period

1. The timings assume the following configuration: DSE[5:0] = 001111 and FSEL1[1:0] = 11.
2. Input timing assumes an input signal slew rate of 3 ns (20%/80%).
3. Output timing valid for maximum external load CL = 25 pF, which is assumed to be a 10 pF load at the end of a 50 ohm. Unterminated, 5-inch microstrip trace on standard FR4 (3.3 pF/inch), (25 pF total with margin). For best signal integrity, the series resistance in the transmission line should be equal to the selected RDSON of the I/O pad output driver.

4.12.2.4 RGMII signal switching specifications

The following timing specifications meet the requirements for RGMII interfaces for a range of transceiver devices.

Table 63. RGMII signal switching specifications[1,2,3,4]

Symbol	Description	Min.	Max.	Unit
T_{cyc}	Clock cycle duration	7.2	8.8	ns
T_{skewT}	Data to clock output skew at transmitter	-500	500	ps
T_{skewR}	Data to clock input skew at receiver	1	2.6	ns
Duty_G	Duty cycle for Gigabit	45	55	%
Duty_T	Duty cycle for 10/100T	40	60	%

1. The timings assume the following configuration: DSE[5:0] = 001111 and FSEL1[1:0] = 11.
2. Measured as defined in *EIA/JESD 8-6 1995* with a timing threshold voltage of VDDQ/2.
3. Output timing valid for maximum external load CL = 15 pF, which is assumed to be a 8 pF load at the end of a 50 ohm, unterminated, 2-inch microstrip trace on standard FR4 (3.3 pF/inch). For best signal integrity, the series resistance in the transmission line should be matched closely to the selected RDSON of the I/O pad output driver.
4. RGMII timing specifications are only valid for 1.8 V nominal I/O pad supply voltage.

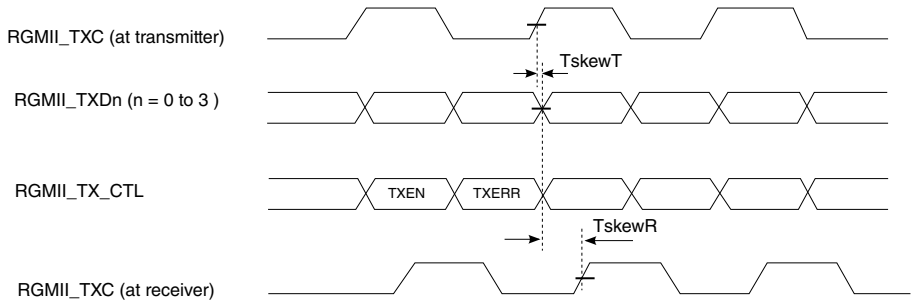


Figure 29. RGMII transmit signal timing diagram original

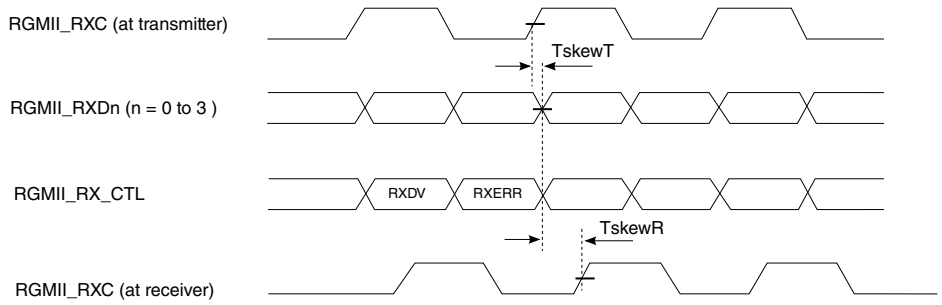


Figure 30. RGMII receive signal timing diagram original

4.12.3 Ethernet Quality-of-Service (QOS) electrical specifications

Ethernet QOS supports the following Time Sensitive Networking (TSN) features:

- 802.1Qbv Enhancements to Scheduling Traffic
- 802.1Qbu Frame preemption
- Time based Scheduling
- 1.8 V/3.3 V RMII operation, 1.8 V RGMII operation

4.12.3.1 Ethernet QOS signal mapping

The following timing specs are defined at the chip I/O pin and must be translated appropriately to arrive at timing specs/constraints for the physical interface.

Table 64. ENET QOS signal mapping[1]

Pad name	RGMII	Alt mode	RMII	Alt mode	Direction
ENET1_MDC	RGMII_MDC	Alt 0	RMII_MDC	Alt 0	O
ENET1_MDIO	RGMII_MDIO	Alt 0	RMII_MDIO	Alt 0	I/O
ENET1_TXC	RGMII_TXC	Alt 0	RMII_TX_ER	Alt 1	O
ENET1_TX_CTL	RGMII_TX_CTL	Alt 0	RMII_TX_EN	Alt 0	O
ENET1_TD0	RGMII_TD0	Alt 0	RMII_TD0	Alt 0	O
ENET1_TD1	RGMII_TD1	Alt 0	RMII_TD1	Alt 0	O
ENET1_TD2	RGMII_TD2	Alt 0	RMII_REF_CLK[2]	Alt 1	I/O
ENET1_TD3	RGMII_TD3	Alt 0	—	Alt 0	O
ENET1_RXC	RGMII_RXC	Alt 0	RMII_RX_ER	Alt 1	I
ENET1_RX_CTL	RGMII_RX_CTL	Alt 0	RMII_CRS_DV	Alt 0	I
ENET1_RD0	RGMII_RD0	Alt 0	RMII_RD0	Alt 0	I
ENET1_RD1	RGMII_RD1	Alt 0	RMII_RD1	Alt 0	I
ENET1_RD2	RGMII_RD2	Alt 0	—	Alt 0	I
ENET1_RD3	RGMII_RD3	Alt 0	—	Alt 0	I

1. ENET1 is Ethernet QoS with TSN, while ENET2 is Ethernet MAC.
2. The signal can be either input or output.

4.12.3.2 RMII mode timing

In RMII mode, enet1.RMII_CLK is used as the REF_CLK, which is a 50 MHz ± 50 ppm continuous reference clock.

Figure 31 shows RMII mode timings. Table 65 describes the timing parameters (M16–M21) shown in the figure.

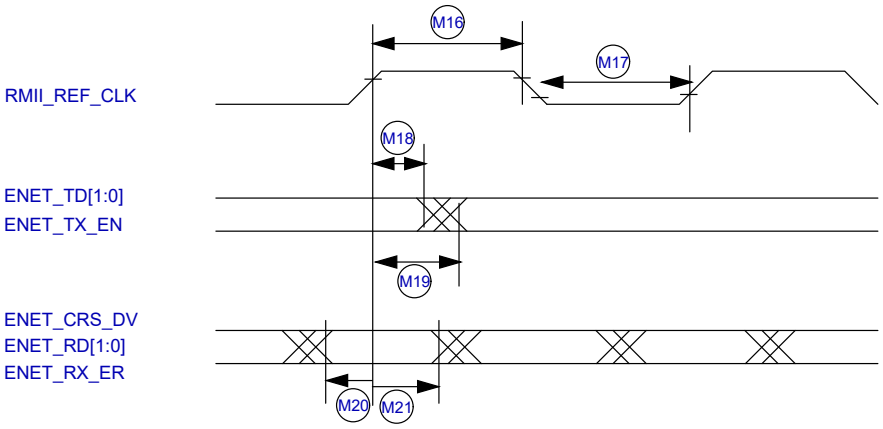


Figure 31. RMII mode signal timing diagram

Table 65. RMII signal timing[1,2,3]

ID	Characteristic	Min.	Max.	Unit
M16	ENET_CLK pulse width high	35%	65%	RMII_REF_CLK period
M17	RMII_REF_CLK pulse width low	35%	65%	RMII_REF_CLK period
M18	RMII_REF_CLK to ENET0_TXD[1:0], ENET_TX_EN invalid	2	—	ns
M19	RMII_REF_CLK to ENET0_TXD[1:0], ENET_TX_EN valid	—	14	ns
M20	ENET_RX_DATA[1:0], ENET_CRS_DV, ENET_RX_ER to RMII_REF_CLK setup	4	—	ns
M21	RMII_REF_CLK to ENET_RX_DATA[1:0], ENET_CRS_DV, ENET_RX_ER hold	2	—	ns

1. The timings assume the following configuration: DSE[5:0] = 001111 and FSEL1[1:0] = 11.
2. Input timing assumes an input signal slew rate of 3 ns (20%/80%).
3. Output timing valid for maximum external load CL = 25 pF, which is assumed to be a 10 pF load at the end of a 50 ohm, unterminated, 5-inch microstrip trace on standard FR4 (3.3 pF/inch), (25 pF total with margin). For best signal integrity, the series resistance in the transmission line should be equal to the selected RDSON of the I/O pad output driver.

4.12.3.3 MII serial management channel timing (ENET_MDIO and ENET_MDC)

The MDC frequency is designed to be equal to or less than 2.5 MHz to be compatible with the IEEE 802.3 MII specification.

Figure 32 shows MII asynchronous input timings. Table 66 describes the timing parameters (M10–M15) shown in the figure.

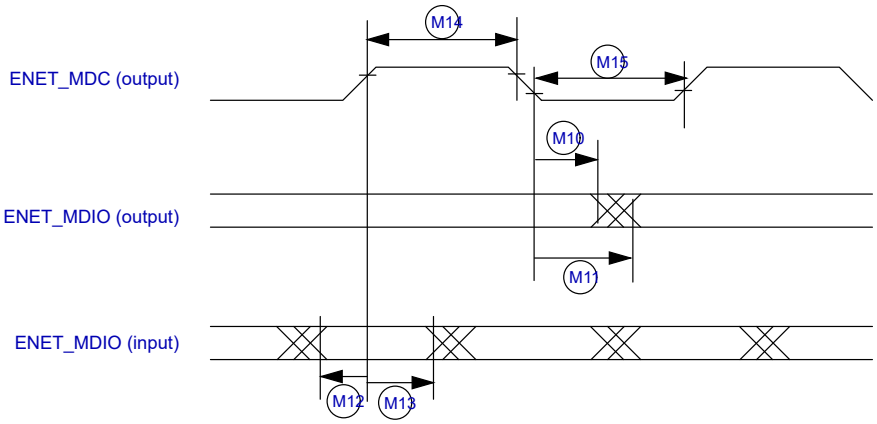


Figure 32. MII serial management channel timing diagram

Table 66. MII serial management channel timing[1,2,3]

ID	Characteristic	Min.	Max.	Unit
M10	ENET_MDC falling edge to ENET_MDIO output invalid (min. propagation delay)	-1.5	—	ns
M11	ENET_MDC falling edge to ENET_MDIO output valid (max. propagation delay)	—	13	ns
M12	ENET_MDIO (input) to ENET_MDC rising edge setup	13	—	ns
M13	ENET_MDIO (input) to ENET_MDC rising edge hold	0	—	ns
M14	ENET_MDC pulse width high	40%	60%	ENET_MDC period
M15	ENET_MDC pulse width low	40%	60%	ENET_MDC period

1. The timings assume the following configuration: DSE[5:0] = 001111 and FSEL1[1:0] = 11.
2. Input timing assumes an input signal slew rate of 3 ns (20%/80%).
3. Output timing valid for maximum external load CL = 25 pF, which is assumed to be a 10 pF load at the end of a 50 ohm. Unterminated, 5-inch microstrip trace on standard FR4 (3.3 pF/inch), (25 pF total with margin). For best signal integrity, the series resistance in the transmission line should be equal to the selected RDSON of the I/O pad output driver.

4.12.3.4 RGMII signal switching specifications

The following timing specifications meet the requirements for RGMII interfaces for a range of transceiver devices.

Table 67. RGMII signal switching specifications[1,2,3,4]

Symbol	Description	Min.	Max.	Unit
T_{cyc}	Clock cycle duration	7.2	8.8	ns
T_{skewT}	Data to clock output skew at transmitter	-500	500	ps
T_{skewR}	Data to clock input skew at receiver	1	2.6	ns

Table continues on the next page...

Table 67. RGMII signal switching specifications[1,2,3,4] *...continued*

Symbol	Description	Min.	Max.	Unit
Duty_G	Duty cycle for Gigabit	45	55	%
Duty_T	Duty cycle for 10/100T	40	60	%

1. The timings assume the following configuration: DSE[5:0] = 001111 and FSEL1[1:0] = 11.
2. Measured as defined in *EIA/JESD 8-6 1995* with a timing threshold voltage of VDDQ/2.
3. Output timing valid for maximum external load CL = 15 pF, which is assumed to be a 8 pF load at the end of a 50 ohm, unterminated, 2-inch microstrip trace on standard FR4 (3.3 pF/inch). For best signal integrity, the series resistance in the transmission line should be matched closely to the selected RDSON of the I/O pad output driver.
4. RGMII timing specifications are only valid for 1.8 V nominal I/O pad supply voltage.

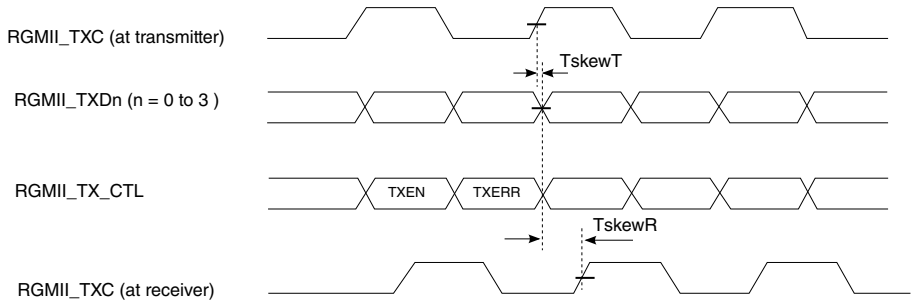


Figure 33. RGMII transmit signal timing diagram original

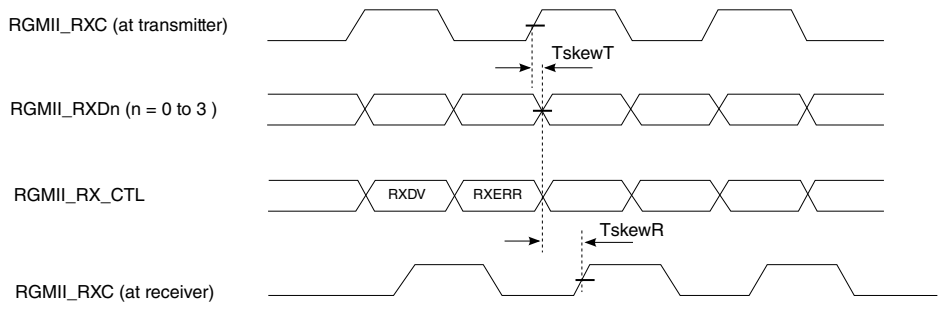


Figure 34. RGMII receive signal timing diagram original

4.12.4 LPSPI timing parameters

The Low Power Serial Peripheral Interface (LPSPI) provides a synchronous serial bus with Controller and Peripheral operations. Many of the transfer attributes are programmable. The following tables provide timing characteristics for classic LPSPI timing modes.

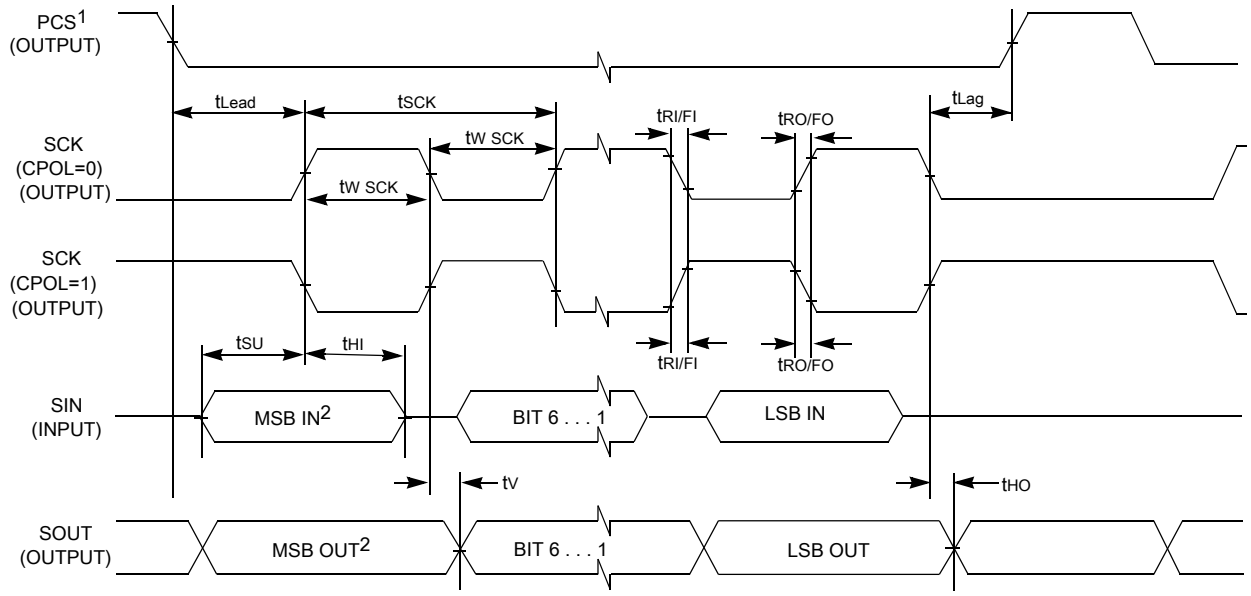
All timing is shown with respect to 20% V_{DD} and 80% V_{DD} thresholds, unless noted, as well as input signal transitions of 3 ns and a 25 pF maximum load on all LPSPI pins.

The DSE[5:0] = 001111 and FSEL1[1:0] = 11 are required drive settings to meet the timing.

Table 68. LPSPI Controller mode timing[1,2]

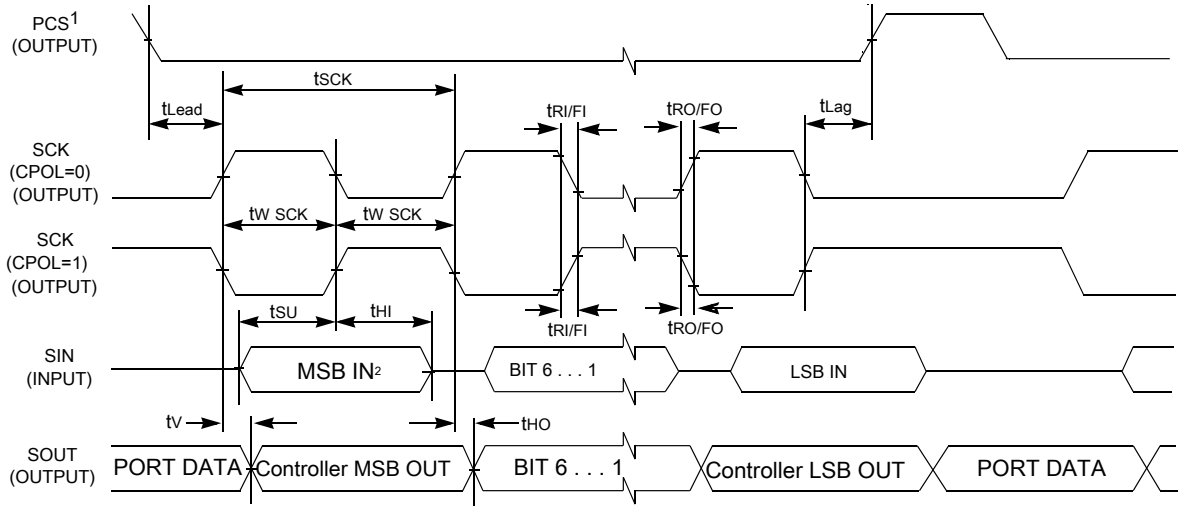
Number	Symbol	Description	Min.	Max.	Units	Note
1	f_{SCK}	Frequency of LPSPI clock[3]	—	30	MHz	4
			—	60	MHz	5
2	t_{SCK}	SCK period	2 x t_{periph}	—	ns	6
3	t_{Lead}	Enable lead time	1	—	t_{periph}	—
4	t_{Lag}	Enable lag time	1	—	t_{periph}	—
5	t_{WSCK}	Clock (SCK) high or low time	t_{SCK} / 2 - 3	t_{SCK} / 2 + 3	ns	—
6	t_{SU}	Data setup time (inputs)	8	—	ns	7,8
7	t_{HI}	Data hold time (inputs)	0	—	ns	7
8	t_V	Data valid (after SCK edge)	—	2.5	ns	—
9	t_{HO}	Data hold time (outputs)	-2.5	—	ns	—

1. Input timing assumes an input signal slew rate of 3 ns (20%/80%).
2. Output timing valid for maximum external load CL = 25 pF, which is assumed to be a 10 pF load at the end of a 50 ohm. Unterminated, 5-inch microstrip trace on standard FR4 (3.3 pF/inch), (25 pF total with margin). For best signal integrity, the series resistance in the transmission line should be equal to the selected RDSON of the I/O pad output driver.
3. The maximum frequency supported is 52 MHz when NVCC_xxxx operating at 3.3 V.
4. The clock driver in the LPSPI module for f_{periph} must guaranteed this limit is not exceeded.
5. In Controller loopback mode when LPSPI_CFGR1[SAMPLE] bit is 1.
6. f_{periph} = Functional clock / (2 ^ PRESCALE) and t_{periph} = 1 / f_{periph}
7. If LPSPI_CFGR1[SAMPLE] bit is 1, the data setup time (inputs) / data hold time (inputs) specifications are same with the one in Peripheral mode.
8. For 3.3 V I/O supply, tSU (Data setup time) parameter value is 9 ns in LPSPI Controller mode.



1. If configured as an output.
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 35. LPSPI Controller mode timing (CPHA = 0)



1.If configured as output
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 36. LPSPI Controller mode timing (CPHA = 1)

Table 69. LPSPI Peripheral mode timing[1,2]

Number	Symbol	Description	Min.	Max.	Units	Note
1	f_{SCK}	Frequency of LPSPI clock	0	30	MHz	—
2	t_{SCK}	SCK period	2 x t_{periph}	—	ns	3
3	t_{Lead}	Enable lead time	1	—	t_{periph}	—

Table continues on the next page...

Table 69. LPSPI Peripheral mode timing[1,2] *...continued*

Number	Symbol	Description	Min.	Max.	Units	Note
4	t_{Lag}	Enable lag time	1	—	t_{periph}	—
5	t_{WSCK}	Clock (SCK) high or low time	t_{SCK} / 2 - 5	t_{SCK} / 2 + 5	ns	—
6	t_{SU}	Data setup time (inputs)	3	—	ns	—
7	t_{HI}	Data hold time (inputs)	3	—	ns	—
8	t_a	Peripheral access time	—	20	ns	4
9	t_{dis}	Peripheral MISO disable time	—	20	ns	5
10	t_V	Data valid (after SCK edge)	—	8	ns	6
11	t_{HO}	Data hold time (outputs)	0	—	ns	—

1. Input timing assumes an input signal slew rate of 3 ns (20%/80%).
2. Output timing valid for maximum external load CL = 25 pF, which is assumed to be a 10 pF load at the end of a 50 ohm. Unterminated, 5-inch microstrip trace on standard FR4 (3.3 pF/inch), (25 pF total with margin). For best signal integrity, the series resistance in the transmission line should be equal to the selected RDSON of the I/O pad output driver.
3. f_{periph} = Functional clock / (2 ^ PRESCALE) and t_{periph} = 1 / f_{periph}
4. Time to data active from high-impedance state
5. Hold time to high-impedance state
6. When operating at 3.3 V I/O supply, this parameter value is 9 ns.

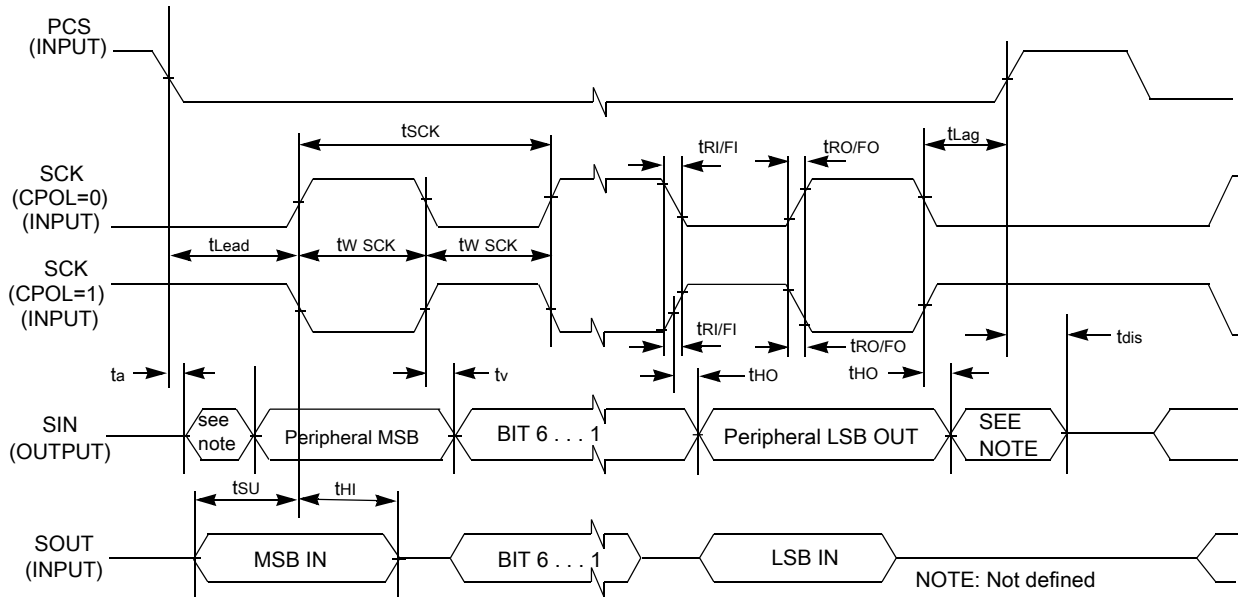


Figure 37. LPSPI Peripheral mode timing (CPHA = 0)

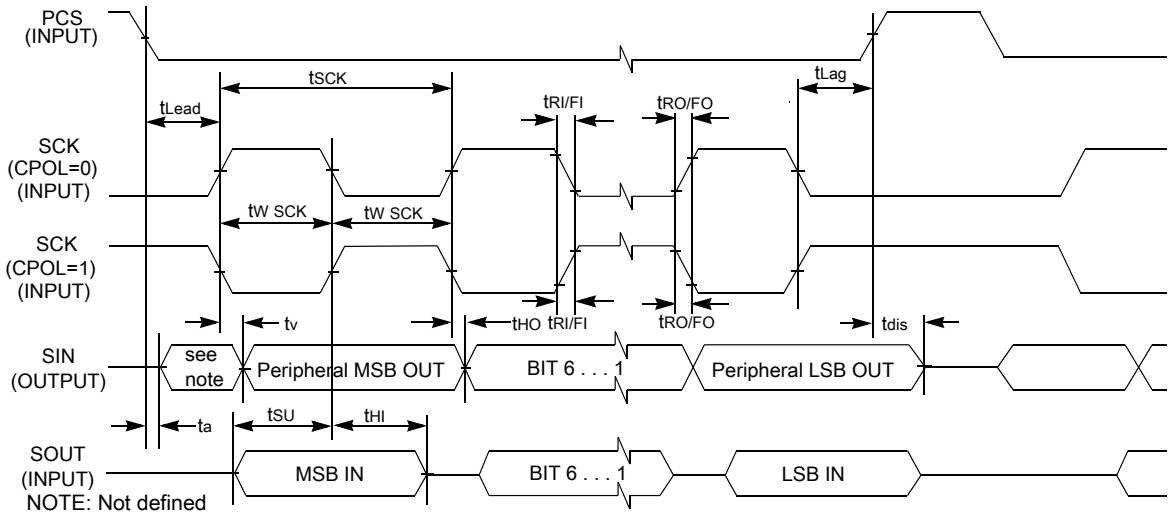


Figure 38. LPSPI Peripheral mode timing (CPHA = 1)

4.12.5 LPI2C timing parameters

LPI2C is a low-power Inter-Integrated Circuit (I2C) module that supports an efficient interface to an I2C bus as a controller and/or as a target.

Table 70. LPI2C module timing parameters[1]

Symbol	Description		Min	Max	Unit	Notes
f_{SCL}	SCL clock frequency	Standard mode (Sm)	0	100	kHz	2
		Fast mode (Fm)	0	400		
		Fast mode Plus (Fm+)	0	1000		
		High speed mode (Hs-mode)	0	3400		
		Ultra Fast mode (UFm)	0	5000		

1. For more details, see *UM10204 I2C-bus specification and user manual*.
2. Standard, Fast, Fast+, and Ultra Fast modes are supported; High speed mode (HS) in target mode.

4.12.6 Improved Inter-Integrated Circuit Interface (I3C) specifications

Unless otherwise specified, I3C specifications are timed to/from the V_{IH} and/or V_{IL} signal points.

The DSE[5:0] = 001111 and FSEL1[1:0] = 11 are required drive settings to meet the timing.

4.12.6.1 I3C Push-Pull Timing Parameters for SDR Mode

I3C interface is not supported on GPIO-Standard-plus pad type for 5 V operation. Measurements are with maximum output load of 30 pf, input transition of 1 ns.

Table 71. I3C Push-Pull Timing Parameters for SDR Mode

Symbol	Description	Min	Typ	Max	Unit	Condition
fSCL	SCL Clock Frequency	0.01	12.5	12.9	MHz	FSCL = 1 / (tDIG_L + tDIG_H)
tDIG_L	SCL Clock Low Period [1,2]	32	—	—	ns	—
tDIG_H	SCL Clock High Period [1]	32	—	—	ns	—
tSCO	Clock in to Data Out for Slave [3,4]	—	—	12	ns	—
tCR	SCL Clock Rise Time [5]	—	—	150e06 * 1 / fSCL (capped at 60)	ns	—
tCF	SCL Clock Fall Time [5]	—	—	150e06 * 1 / fSCL (capped at 60)	ns	—
tHD_PP	SDA Signal Data Hold in Push-Pull Mode, Slave [6]	1	—	—	—	Applicable for slave and master loopback modes
tSU_PP	SDA Signal Data Setup in Push-Pull Mode	3	—	N/A	ns	Applicable for slave and master loopback modes.

1. tDIG_L and tDIG_H are the clock Low and High periods as seen at the receiver end of the I3C Bus using VIL and VIH (see Figure 30)
2. As both edges are used, the hold time needs to be satisfied for the respective edges; i.e., tCF + 3 for falling edge clocks, and tCR + 3 for rising edge clocks.
3. Devices with more than 12ns of tSCO delay shall set the limitation bit in the BCR, and shall support the GETMXDS CCC to allow the Master to read this value and adjust computations accordingly. For purposes of system design and test conformance, this parameter should be considered together with pad delay, bus capacitance, propagation delay, and clock triggering points.
4. Pad delay based on 90 Ω / 4 mA driver and 50 pF load. Note that Master may be a Slave in a multi-Master system, and thus shall also adhere to this requirement
5. The clock maximum rise/fall time is capped at 60 ns. For lower frequency rise and fall the maximum value is limited at 60 ns, and is not dependent upon the clock frequency.
6. tHD_PP is a Hold time parameter for Push-Pull Mode that has a different value for Master mode vs. Slave mode. In SDR Mode the Hold time parameter is referred to as tHD_SDR.

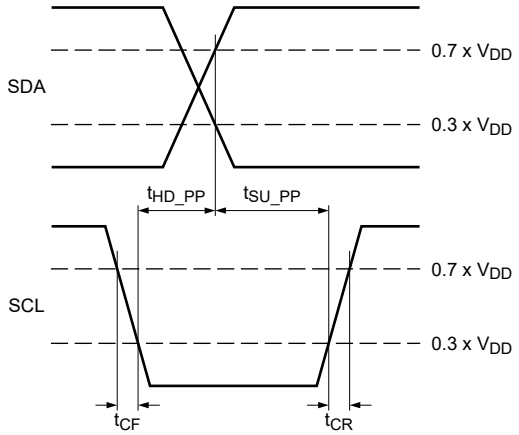


Figure 39. Controller out timing

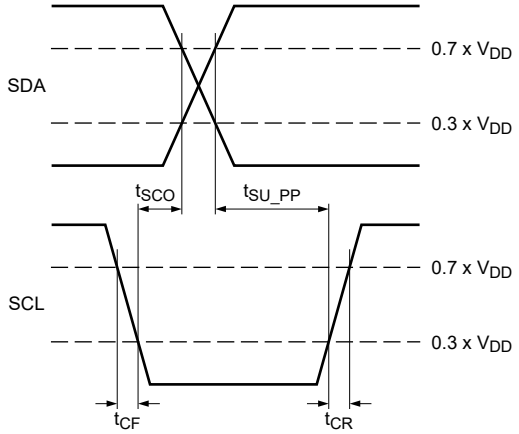


Figure 40. Target out timing

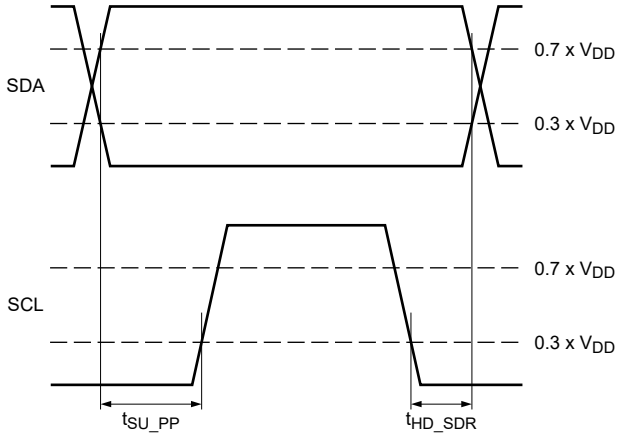


Figure 41. Controller SDR timing

4.12.7 CAN network AC electrical specifications

The Controller Area Network (CAN) module is a communication controller implementing the CAN protocol according to the CAN with Flexible Data rate (CAN FD) protocol and the CAN 2.0B protocol specification. The processor has two CAN modules

available. Tx and Rx ports for both modules are multiplexed with other I/O pins. See the IOMUXC chapter of the device reference manual to see which pins expose Tx and Rx pins; these ports are named CAN_TX and CAN_RX, respectively.

The DSE[5:0] = 001111 and FSEL1[1:0] = 11 are required drive settings to meet the timing.

Please see General purpose I/O (GPIO) AC parameters for timing parameters.

Table 72. CAN-FD electrical specifications

Parameters	FlexCAN (Classical and FD)	Unit
Maximum Baud Rate	8/8	Mbps
TXD Rise time wcs	4/4	ns
TXD Fall time wcs	4/4	ns
RXD Rise time wcs	4/4	ns
RXD Fall time wcs	4/4	ns
TXD	3.3/3.3	V
RXD	3.3/3.3	V
Internal delay wcs	100/50	ns
TX PAD delay wcs	25/25	ns
RX PAD delay wcs	10/10	ns
TX routing delay wcs	5/5	ns
RX routing delay wcs	5/5	ns
Transceiver loop delay wcs	250/250	ns
Total loop delay	395/345	ns

4.12.8 Timer/Pulse width modulator (TPM) timing parameters

This section describes the output timing parameters of the TPM.

The DSE[5:0] = 001111 and FSEL1[1:0] = 11 are required drive settings to meet the timing.

Figure 42 depicts the timing of the PWM, and Table 73 lists the TPM timing parameters.

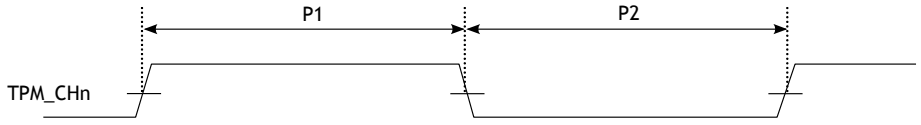


Figure 42. TPM timing

Table 73. TPM output timing parameters

ID	Parameter	Min	Max	Unit
	PWM Module Clock Frequency	0	83.3	MHz
P1	PWM output pulse width high	12	—	ns
P2	PWM output pulse width low	12	—	ns

4.12.9 FlexSPI timing parameters

The FlexSPI interface can work in SDR or DDR modes. FlexSPI*n*_MCR0[RXCLKSRC] = 0 and FlexSPI*n*_MCR0[RXCLKSRC] = 1 configurations are supported when I/O is supplied by 3.3 V and 1.8 V, while FlexSPI*n*_MCR0[RXCLKSRC] = 3 configuration is supported when I/O is supplied by 1.8 Vonly.

Input timing assumes an input signal slew rate of 1 ns (20%/80%) and Output timing valid for maximum external load CL = 15 pF, which is assumed to be a 8 pF load at the end of a 50 ohm, un-terminated, 2-inch microstrip trace on standard FR4 (3.3 pF/inch). For best signal integrity, the series resistance of the transmission line should be matched closely to the selected RDSON of the I/O pad output driver.

The DSE[5:0] = 001111 and FSEL1[1:0] = 11 are required drive settings to meet the timing.

4.12.9.1 FlexSPI input/read timing

There are three sources for the internal sample clock of FlexSPI read data:

- Dummy read strobe generated by FlexSPI controller and looped back internally (FlexSPI*n*_MCR0[RXCLKSRC] = 0x0)
- Dummy read strobe generated by FlexSPI controller and looped back through the DQS pad (FlexSPI*n*_MCR0[RXCLKSRC] = 0x1)
- Read strobe provided by memory device and input from DQS pad (FlexSPI*n*_MCR0[RXCLKSRC] = 0x3)

The following sections describe input signal timing for each of these three internal sample clock sources.

4.12.9.1.1 SDR mode with FlexSPIn_MCR0[RXCLKSRC] = 0x0, 0x1

Table 74. FlexSPI input timing in SDR mode where FlexSPI*n*_MCR0[RXCLKSRC] = 0X0 (Nominal and Overdrive mode)

Symbol	Parameter	Min	Max	Unit
—	Frequency of operation[1]	—	66	MHz
F1	Setup time for incoming data	6	—	ns
F2	Hold time for incoming data	0	—	ns

1. The maximum frequency supported is 52 MHz when NVCC_xxxx operating at 3.3 V.

Table 75. FlexSPI input timing in SDR mode where FlexSPI*n*_MCR0[RXCLKSRC] = 0X0 (Low drive mode)

Symbol	Parameter	Min	Max	Unit
—	Frequency of operation	—	50	MHz
F1	Setup time for incoming data	7	—	ns
F2	Hold time for incoming data	0	—	ns

Table 76. FlexSPI input timing in SDR mode where FlexSPI*n*_MCR0[RXCLKSRC] = 0X1 (Nominal and Overdrive mode)

Symbol	Parameter	Min	Max	Unit
—	Frequency of operation[1]	—	166	MHz
F1	Setup time for incoming data	1	—	ns
F2	Hold time for incoming data	1	—	ns

1. The maximum frequency supported is 52 MHz when NVCC_xxxx operating at 3.3 V.

Table 77. FlexSPI input timing in SDR mode where FlexSPI*n*_MCR0[RXCLKSRC] = 0X1 (Low drive mode)

Symbol	Parameter	Min	Max	Unit
—	Frequency of operation[1]	—	100	MHz
F1	Setup time for incoming data	2	—	ns
F2	Hold time for incoming data	1	—	ns

1. The maximum frequency supported is 52 MHz when NVCC_xxxx operating at 3.3 V.

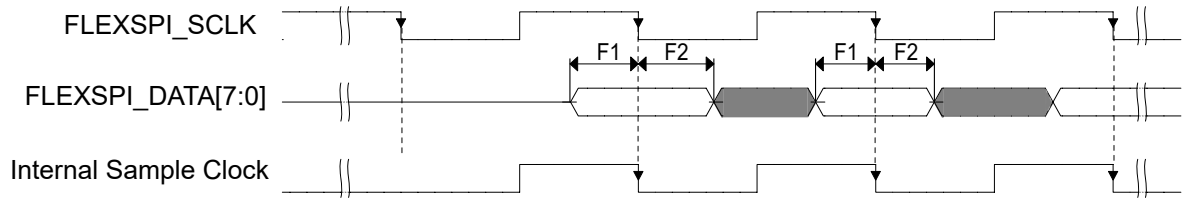


Figure 43. FlexSPI input timing in SDR mode where FlexSPIn_MCR0[RXCLKSRC] = 0X0, 0X1

NOTE

Timing shown is based on the memory generating read data on the SCK falling edge, and FlexSPI controller sampling read data on the falling edge.

4.12.9.1.2 SDR mode with FlexSPIn_MCR0[RXCLKSRC] = 0x3

There are two cases when the memory provides both read data and the read strobe in SDR mode:

- A1—Memory generates both read data and read strobe on SCK rising edge (or falling edge)
- A2—Memory generates read data on SCK falling edge and generates read strobe on SCK rising edge

NOTE

In this mode, it is only working under 1.8 V.

Table 78. FlexSPI input timing in SDR mode where FlexSPIn_MCR0[RXCLKSRC] = 0x3 (case A1) (Nominal and Overdrive mode)

Symbol	Parameter	Min	Max	Unit
—	Frequency of operation	—	200	MHz

Table continues on the next page...

Table 78. FlexSPI input timing in SDR mode where FlexSPIn_MCR0[RXCLKSRC] = 0x3 (case A1) (Nominal and Overdrive mode)*...continued*

Symbol	Parameter	Min	Max	Unit
T_{SCKD}	Time from SCK to data valid	—	—	ns
T_{SCKDQS}	Time from SCK to DQS	—	—	ns
T_{SCKD} - T_{SCKDQS}	Time delta between T_{SCKD} and T_{SCKDQS}	-0.6	0.6	ns

Table 79. FlexSPI input timing in SDR mode where FlexSPI*n*_MCR0[RXCLKSRC] = 0x3 (case A1) (Low drive mode)

Symbol	Parameter	Min	Max	Unit
—	Frequency of operation	—	133	MHz
T_{SCKD}	Time from SCK to data valid	—	—	ns
T_{SCKDQS}	Time from SCK to DQS	—	—	ns
T_{SCKD} - T_{SCKDQS}	Time delta between T_{SCKD} and T_{SCKDQS}	-2	2	ns

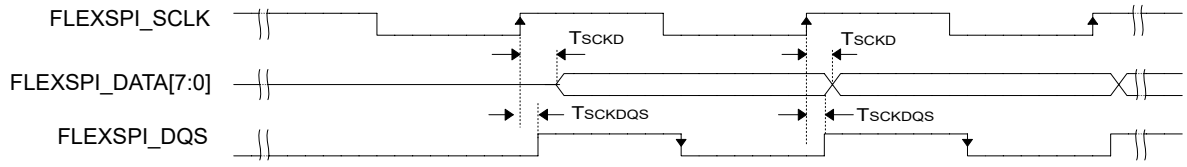


Figure 44. FlexSPI input timing in SDR mode where FlexSPIn_MCR0[RXCLKSRC] = 0X3 (case A1)

NOTE

Timing shown is based on the memory generating read data and read strobe on the SCK rising edge. The FlexSPI controller samples read data on the DQS falling edge.

Table 80. FlexSPI input timing in SDR mode where FlexSPIn_MCR0[RXCLKSRC] = 0x3 (case A2) (Nominal and Overdrive mode)

Symbol	Parameter	Value		Unit
		Min	Max	
—	Frequency of operation	—	200	MHz
T_{SCKD}	Time from SCK to data valid	—	—	ns
T_{SCKDQS}	Time from SCK to DQS	—	—	ns
T_{SCKD} - T_{SCKDQS}	Time delta between T_{SCKD} and T_{SCKDQS}	-0.6	0.6	ns

Table 81. FlexSPI input timing in SDR mode where FlexSPI*n*_MCR0[RXCLKSRC] = 0x3 (case A2) (Low drive mode)

Symbol	Parameter	Value		Unit
		Min	Max	
—	Frequency of operation	—	133	MHz
T_{SCKD}	Time from SCK to data valid	—	—	ns
T_{SCKDQS}	Time from SCK to DQS	—	—	ns
T_{SCKD} - T_{SCKDQS}	Time delta between T_{SCKD} and T_{SCKDQS}	-2	2	ns

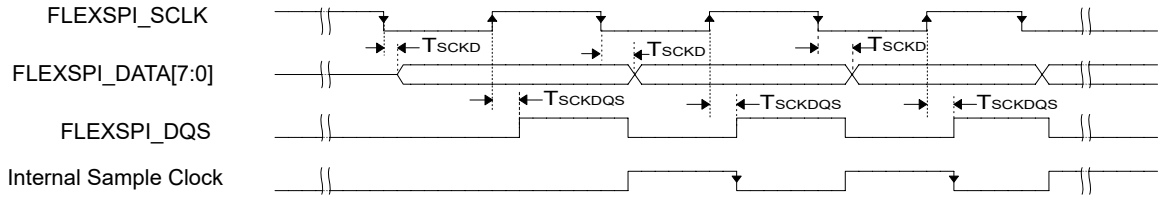


Figure 45. FlexSPI input timing in SDR mode where FlexSPIn_MCR0[RXCLKSRC] = 0X3 (case A2)

NOTE

Timing shown is based on the memory generating read data on the SCK falling edge and read strobe on the SCK rising edge. The FlexSPI controller samples read data on a half cycle delayed DQS falling edge.

4.12.9.1.3 DDR mode with FlexSPIn_MCR0[RXCLKSRC] = 0x0, 0x1

Table 82. FlexSPI input timing in DDR mode where FlexSPI*n*_MCR0[RXCLKSRC] = 0x0 (Nominal, Overdrive, and Low drive mode)

Symbol	Parameter	Min	Max	Unit
—	Frequency of operation	—	33	MHz
F1	Setup time for incoming data	6	—	ns
F2	Hold time for incoming data	0	—	ns

Table 83. FlexSPI input timing in DDR mode where FlexSPI*n*_MCR0[RXCLKSRC] = 0x1 (Nominal and Overdrive mode)

Symbol	Parameter	Min	Max	Unit
—	Frequency of operation[1]	—	83	MHz
F1	Setup time for incoming data	1	—	ns
F2	Hold time for incoming data	1	—	ns

1. The maximum frequency supported is 52 MHz when NVCC_xxxx operating at 3.3 V.

Table 84. FlexSPI input timing in DDR mode where FlexSPI*n*_MCR0[RXCLKSRC] = 0x1 (Low drive mode)

Symbol	Parameter	Min	Max	Unit
—	Frequency of operation[1]	—	66	MHz
F1	Setup time for incoming data	1.5	—	ns
F2	Hold time for incoming data	1	—	ns

1. The maximum frequency supported is 52 MHz when NVCC_xxxx operating at 3.3 V.

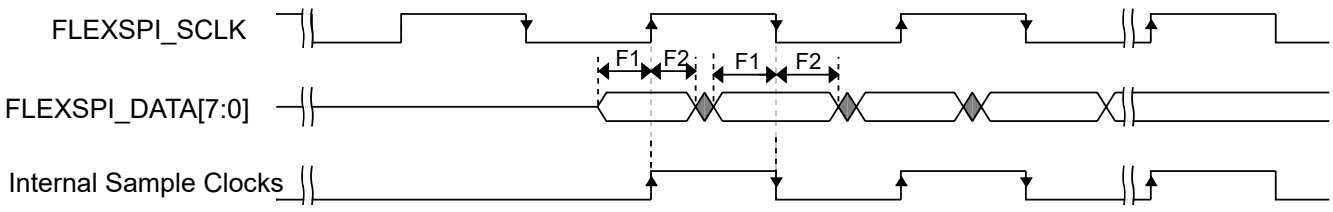


Figure 46. FlexSPI input timing in DDR mode where FlexSPIn_MCR0[RXCLKSRC] = 0x0, 0x1

4.12.9.1.4 DDR mode with FlexSPIn_MCR0[RXCLKSRC] = 0x3

NOTE

In this mode, it is only working under 1.8 V.

Table 85. FlexSPI input timing in DDR mode where FlexSPIn_MCR0[RXCLKSRC] = 0x3 (Nominal and Overdrive mode)[1]

Symbol	Parameter	Min	Max	Unit
—	Frequency of operation	—	200	MHz
T_{SCKD}	Time from SCK to data valid	—	—	ns
T_{SCKDQS}	Time from SCK to DQS	—	—	ns
T_{SCKD} - T_{SCKDQS}	Time delta between T_{SCKD} and T_{SCKDQS}	-0.6	0.6	ns

1. These timing specifications are valid only for 1.8 V nominal I/O pad supply voltage.

Table 86. FlexSPI input timing in DDR mode where FlexSPI*n*_MCR0[RXCLKSRC] = 0x3 (Low drive mode)

Symbol	Parameter	Min	Max	Unit
—	Frequency of operation	—	133	MHz
T_{SCKD}	Time from SCK to data valid	—	—	ns
T_{SCKDQS}	Time from SCK to DQS	—	—	ns
T_{SCKD} - T_{SCKDQS}	Time delta between T_{SCKD} and T_{SCKDQS}	-0.9	0.9	ns

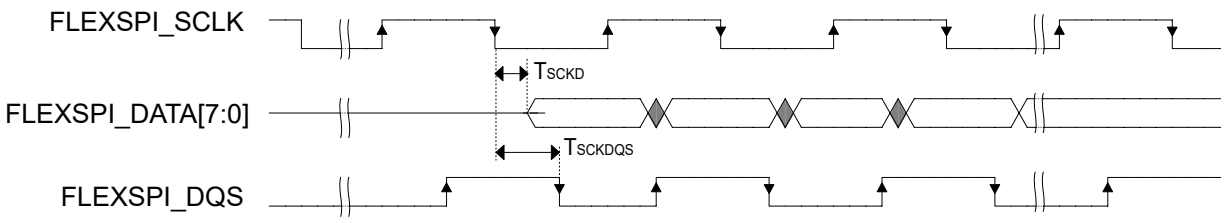


Figure 47. FlexSPI input timing in DDR mode where FlexSPIn_MCR0[RXCLKSRC] = 0x3

4.12.9.2 FlexSPI output/write timing

The following sections describe output signal timing for the FlexSPI controller including control signals and data outputs.

4.12.9.2.1 SDR mode

Table 87. FlexSPI output timing in SDR mode (Nominal and Overdrive mode)[1]

Symbol	Parameter	Min	Max	Unit
—	Frequency of operation[2]	—	200	MHz
T_{ck}	SCK clock period	5	—	ns
T_{DVO}	Output data valid time	—	0.6	ns
T_{DHO}	Output data hold time	-0.6	—	ns
T_{CSS}	Chip select output setup time[3]	(T_{CSS} + 0.5) x T_{ck} - 0.6	—	ns
T_{CSH}	Chip select output hold time[3]	(T_{CSH} x T_{ck}) - 0.6	—	ns

1. These timing specifications are valid only for 1.8 V nominal I/O pad supply voltage.
2. The maximum frequency supported is 52 MHz when NVCC_xxxx operating at 3.3 V.
3. T_{CSS} and T_{CSH} are configured by the FlexSPI*n*_FLSHAxCR1 register. See i.MX 93 Applications Processor Reference Manual (IMX93RM) for more details.

Table 88. FlexSPI output timing in SDR mode (Low drive mode)

Symbol	Parameter	Min	Max	Unit
—	Frequency of operation[1]	—	133[2]	MHz
T_{ck}	SCK clock period	7.5	—	ns
T_{DVO}	Output data valid time	—	2	ns
T_{DHO}	Output data hold time	-2	—	ns

Table continues on the next page...

Table 88. FlexSPI output timing in SDR mode (Low drive mode) *...continued*

Symbol	Parameter	Min	Max	Unit
T_{CSS}	Chip select output setup time	(T_{CSS} + 0.5) x T_{ck} - 2	—	ns
T_{CSH}	Chip select output hold time[3]	(T_{CSH} x T_{ck}) - 2	—	ns

1. The maximum frequency supported is 52 MHz when NVCC_xxxx operating at 3.3 V.
2. The actual maximum frequency supported is limited by the FlexSPI*n*_MCR0[RXCLKSRC] configuration used, see the FlexSPI SDR input timing specifications.
3. T_{CSS} and T_{CSH} are configured by the FlexSPI*n*_FLSHAxCR1 register. See i.MX 93 Applications Processor Reference Manual (IMX93RM) for more details.

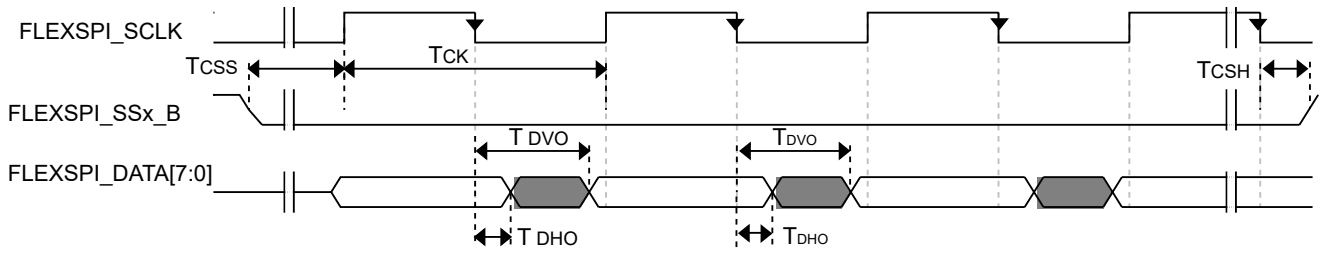


Figure 48. FlexSPI output timing in SDR mode

4.12.9.2.2 DDR mode

Table 89. FlexSPI output timing in DDR mode (Nominal and Overdrive mode)[1]

Symbol	Parameter	Min	Max	Unit
—	Frequency of operation[2]	—	200	MHz
T_{ck}	SCK clock period	5	—	ns
T_{DVO}	Output data valid time	—	1.815	ns
T_{DHO}	Output data hold time	0.615	—	ns
T_{CSS}	Chip select output setup time	(T_{CSS} + 0.5) x T_{ck} - 0.6	—	ns
T_{CSH}	Chip select output hold time[3]	(T_{CSH} + 0.5) x T_{ck} - 0.6	—	ns

1. These timing specifications are valid only for 1.8 V nominal IO pad supply voltage.
2. The maximum frequency supported is 52 MHz when NVCC_xxxx operating at 3.3 V.
3. T_{CSS} and T_{CSH} are configured by the FlexSPI*n*_FLSHAxCR1 register. See i.MX 93 Applications Processor Reference Manual (IMX93RM) for more details.

Table 90. FlexSPI output timing in DDR mode (Low drive mode)

Symbol	Parameter	Min	Max	Unit
—	Frequency of operation[1]	—	133[2]	MHz
T_{ck}	SCK clock period	7.5	—	ns
T_{DVO}	Output data valid time	—	2.75	ns
T_{DHO}	Output data hold time	0.9	—	ns
T_{CSS}	Chip select output setup time[3]	(T_{CSS} + 0.5) x T_{ck} - 0.9	—	ns
T_{CSH}	Chip select output hold time[3]	(T_{CSH} + 0.5) x T_{ck} - 0.9	—	ns

1. The maximum frequency supported is 52 MHz when NVCC_xxxx operating at 3.3 V.
2. The actual maximum frequency supported is limited by the FlexSPI*n*_MCR0[RXCLKSRC] configuration used, see the FlexSPI DDR input timing specifications.
3. T_{CSS} and T_{CSH} are configured by the FlexSPI*n*_FLSHAxCR1 register. See i.MX 93 Applications Processor Reference Manual (IMX93RM) for more details.

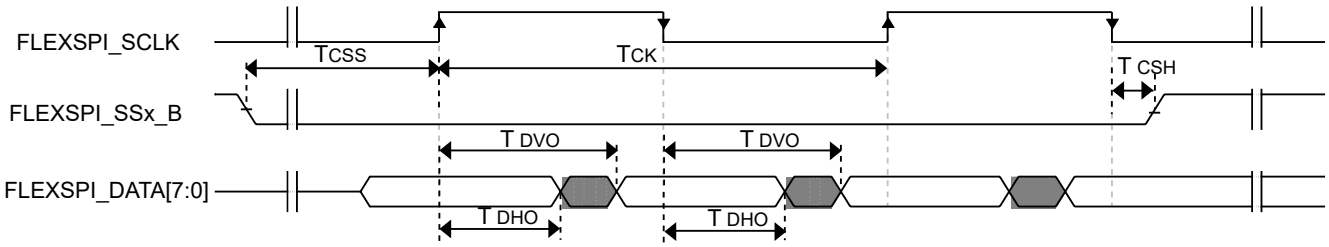


Figure 49. FlexSPI output timing in DDR mode

4.12.10 LPUART I/O configuration and timing parameters

See General purpose I/O (GPIO) AC parameters.

4.12.11 Flexible I/O controller (FlexIO) electrical specifications

The DSE[5:0] = 001111 and FSEL1[1:0] = 11 are required drive settings to meet the timing.

Table 91 shows FlexIO timing specifications.

Table 91. FlexIO timing specifications[1,2]

Symbol	Descriptions	Min	Typ	Max	Unit	Notes
t_{ODS}	Output delay skew between any two FlexIO_Dx pins configured as outputs that toggle on same internal clock cycle	0	—	12	ns	[3]

Table continues on the next page...

Table 91. FlexIO timing specifications[1,2] *...continued*

t_{IDS}	Input delay skew between any two FlexIO_Dx pins configured as inputs that are sampled on the same internal clock cycle	0	—	12	ns	[3]

1. Input timing assumes an input signal slew rate of 3 ns (20%/80%).
2. Output timing valid for maximum external load CL = 25 pF, which is assumed to be a 10 pF load at the end of a 50 ohm. Unterminated, 5-inch microstrip trace on standard FR4 (3.3 pF/inch), (25 pF total with margin). For best signal integrity, the series resistance in the transmission line should be equal to the selected RDSON of the I/O pad output driver.
3. Assume pins muxed on same VDD_IO domain with same load.

4.12.12 USB PHY parameters

The USB PHY parameters meet the electrical compliance requirements listed as following:

- *Universal Serial Bus Revision 2.0 Specification* (including ECNs and errata), *On-The-Go and Embed-ded Host Supplement to the Universal Serial Bus Revision 2.0 Specification* (including ECNs and errata)

4.12.12.1 Pad/Package/Board connections

The USBx_VBUS pin cannot directly connect to the 5 V VBUS voltage on the USB2.0 link.

Each USBx_VBUS pin must be isolated by an external 30 KΩ 1% precision resistor.

The USB 2.0 PHY uses USBx_TXRTUNE and an external resistor to calibrate the USBx_DP/DN 45 Ω source impedance. The external resistor value is 200 Ω 1% precision on each of USBx_TXRTUNE pad to ground.

5 Boot mode configuration

This section provides information on boot mode configuration pins allocation and boot devices interfaces allocation.

i.MX 93 supports three different boot modes:

- Normal Boot Mode
- Boot from Internal Fuse Mode
- Serial Download Boot Mode

Three different boot modes can be either selected via different boot mode pins or overridden by fuses.

i.MX 93 has two kinds of boot type:

- Single Boot: Cortex®-A55 core is in charge of loading all containers and images, while Cortex®-M33 core is doing nothing except waiting Cortex®-M33 firmware is loaded and available during boot.
- Low Power Boot (LPB): only Cortex®-M33 core is running after POR. Cortex®-A55 core cannot be triggered by Cortex®-M33 firmware.

For detailed boot mode configuration, see the "Fuse Map" and the "System Boot" chapter in *i.MX 93 Reference Manual (IMX93RM)*.

5.1 Boot mode configuration pins

There are four boot mode pins used to select boot mode.

Table 92. Fuses and associated pins used for boot

BOOT_MODE[3:0]	Function
x000	Boot from Internal Fuses
0001	Serial Download (USB1)
0010	uSDHC1 8-bit eMMC 5.1
0011	uSDHC2 4-bit SD 3.0
0100	FlexSPI Serial NOR
0101	FlexSPI Serial NAND 2K
0110	Reserved
0111	Reserved
1000	LPB: Boot from Internal Fuses
1001	LPB: Serial Downloader (USB1)
1010	LPB: uSDHC1 8-bit 1.8 V eMMC 5.1
1011	LPB: uSDHC2 4-bit SD 3.0
1100	LPB: FlexSPI Serial NOR
1101	LPB: FlexSPI Serial NAND 2K
1110	Reserved
1111	Reserved

- HW samples the boot CFG pins before ROM starts, these pins should be mapped to Boot CFG pins by default.
- Once HW samples the boot CFG pins and stores the boot CFG in CMC register, the register should be latched. The register value is no more changes and reflecting the pins status.

Additional boot options are also supported for both Normal Boot Mode and Internal Fuse mode:

- All boot modes support for a range of speeds, timings, and protocol formats;
- eMMC and SD boot can be supported from any USDHC instance 1 or 2;
- Serial NOR boot supports for 1-bit, 4-bit, and 8-bit mode;
- Serial NAND boot supports for 1-bit, 4-bit, and 8-bit mode (8-bit Serial NAND)

BOOT_MODE pins are multiplexed over other functional pins. The functional I/O that are multiplexed with these pins must be selected subject to two criteria:

- Functional I/O must not be used if they are inputs to the SoC, which could potentially be constantly driven by external components. Such functional mode driving may interfere with the need for the board to pull these pins a certain way while POR is asserted.
- Functional I/O must not be used if they are outputs of the SoC, which will be connected to components on the board that may misinterpret the signals as valid signals if they are toggled (such as, the board drives them while POR is asserted).

5.2 Boot device interface allocation

i.MX 93 supports three kinds of boot devices:

- Primary Boot Device

  The primary boot device is selected by Boot Config pins if boot mode is the Normal Boot or Internal Fuses Boot. The valid primary boot device options are SD/eMMC/FlexSPI NOR/FlexSPI NAND. The valid options also depend on the Boot Type and other fuses configuration.

- Recovery Boot Device

  After failure of booting from Primary Boot Device, i.MX 93 tries to boot from another boot source. The recovery boot device is only from SPI1/2/3/4.

- Serial Download Boot Device

  Both Cortex®-M33 and Cortex®-A55 support serial download mode via USB1.

The following tables list the interfaces that can be used by the boot process in accordance with the specific boot mode configuration. The tables also describe the interface's specific modes and IOMUXC allocation, which are configured during boot when appropriate.

Table 93. Boot through FlexSPI

Signal name	PAD name	ALT
FlexSPIA_DATA0	SD3_DATA0	ALT1
FlexSPIA_DATA1	SD3_DATA1	ALT1
FlexSPIA_DATA2	SD3_DATA2	ALT1
FlexSPIA_DATA3	SD3_DATA3	ALT1
FlexSPIA_DQS	SD1_STROBE	ALT1
FlexSPIA_SS0_B	SD3_CMD	ALT1
FlexSPIA_SCLK	SD3_CLK	ALT1
FlexSPIA_DATA4	SD1_DATA4	ALT1
FlexSPIA_DATA5	SD1_DATA5	ALT1
FlexSPIA_DATA6	SD1_DATA6	ALT1
FlexSPIA_DATA7	SD1_DATA7	ALT1

Table 94. Boot through uSDHC1

Signal name	PAD name	ALT
USDHC1_CMD	SD1_CMD	ALT0
USDHC1_CLK	SD1_CLK	ALT0
USDHC1_DATA0	SD1_DATA0	ALT0

Table continues on the next page...

Table 94. Boot through uSDHC1*...continued*

USDHC1_DATA1	SD1_DATA1	ALT0
USDHC1_DATA2	SD1_DATA2	ALT0
USDHC1_DATA3	SD1_DATA3	ALT0
USDHC1_DATA4	SD1_DATA4	ALT0
USDHC1_DATA5	SD1_DATA5	ALT0
USDHC1_DATA6	SD1_DATA6	ALT0
USDHC1_DATA7	SD1_DATA7	ALT0
USDHC1_RESET	SD1_DATA5	ALT2

Table 95. Boot through uSDHC2

Signal name	PAD name	ALT
USDHC2_CMD	SD2_CMD	ALT0
USDHC2_CLK	SD2_CLK	ALT0
USDHC2_DATA0	SD2_DATA0	ALT0
USDHC2_DATA1	SD2_DATA1	ALT0
USDHC2_DATA2	SD2_DATA2	ALT0
USDHC2_DATA3	SD2_DATA3	ALT0
USDHC2_RESET	SD2_RESET_B	ALT0
USDHC2_VSELECT	SD2_VSELECT	ALT0

Table 96. Boot through SPI1

Signal name	PAD name	ALT
SPI1_PCS1	PDM_BIT_STREAM0	ALT2
SPI1_SIN	SAI1_TXC	ALT2
SPI1_SOUT	SAI1_RXD0	ALT2
SPI1_SCK	SAI1_TXD0	ALT2
SPI1_PCS0	SAI1_TXFS	ALT2

Table 97. Boot through SPI2

Signal name	PAD name	ALT
SPI2_PCS1	PDM_BIT_STREAM1	ALT2
SPI2_SIN	UART1_RXD	ALT2
SPI2_SOUT	UART2_RXD	ALT2
SPI2_SCK	UART2_TXD	ALT2
SPI2_PCS0	UART1_TXD	ALT2

Table 98. Boot through SPI3

Signal name	PAD name	ALT
SPI3_PCS1	GPIO_IO07	ALT1
SPI3_SIN	GPIO_IO09	ALT1
SPI3_SOUT	GPIO_IO10	ALT1
SPI3_SCK	GPIO_IO11	ALT1
SPI3_PCS0	GPIO_IO08	ALT1

Table 99. Boot through SPI4

Signal name	PAD name	ALT
SPI4_PCS1	GPIO_IO17	ALT5
SPI4_PCS2	GPIO_IO16	ALT5
SPI4_SIN	GPIO_IO19	ALT5
SPI4_SOUT	GPIO_IO20	ALT5
SPI4_SCK	GPIO_IO21	ALT5
SPI4_PCS0	GPIO_IO18	ALT5

USB1 interfaces are dedicated pins, thus no IOMUX options.

6 Package information and contact assignments

This section includes the contact assignment information and mechanical package drawing.

6.1 14 x 14 mm package information

6.1.1 14 x 14 mm, 0.65 mm pitch, ball matrix

Figure 50 shows the top, bottom, and side views of the 14 x 14 mm FCBGA package.

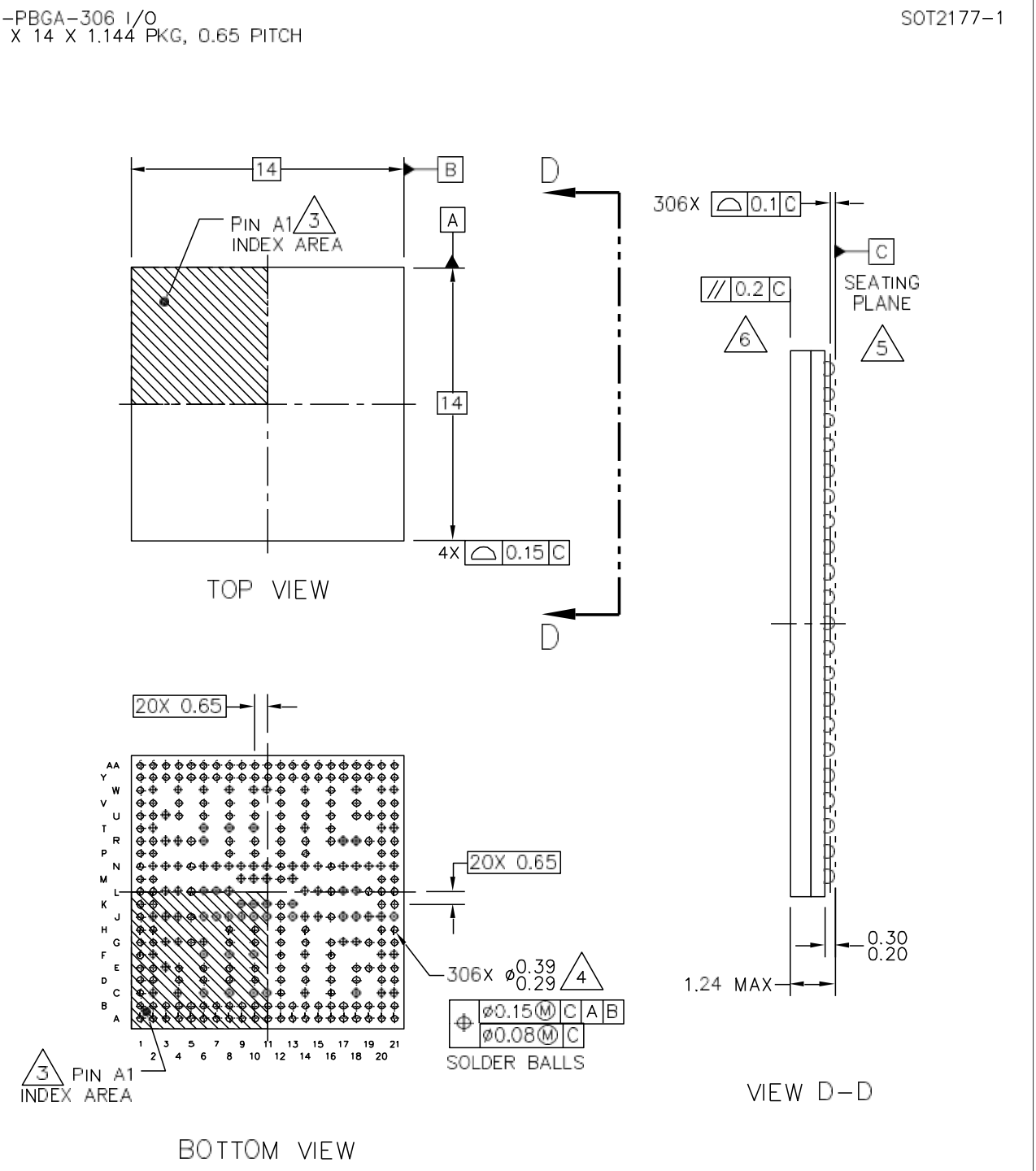


Figure 50. 14 x 14 mm BGA, case x package top, bottom, and side Views

6.1.2 14 x 14 mm supplies contact assignments and functional contact assignments

Table 100 shows the device connection list for ground, sense, and reference contact signals.

Table 100. 14 x 14 mm supplies contact assignment

Supply Rail Name	Ball(s) Position(s)	Remark
NVCC_AON	L16	—
NVCC_BBSM_1P8	G12	—
NVCC_GPIO	N15, N16	—
NVCC_SD2	R16	—
NVCC_WAKEUP	R10, R12, W8	—
VDD_ANA_0P8	J15, J16, R14	—
VDD_ANA0_1P8	F16, G16	—
VDD_ANA1_1P8	R8	—
VDD_ANAVDET_1P8	L15	—
VDD_BBSM_0P8_CAP	G14	—
VDD_LVDS_1P8	F6	—
VDD_MIPI_0P8	G8	—
VDD_MIPI_1P8	F8	—
VDD_SOC	J9, J10, J11, J12, J13, K9, K10, K12, K13, M9, M10, M12, M13, N9, N10, N11, N12, N13	—
VDD_USB_0P8	F10	—
VDD_USB_1P8	E8	—
VDD_USB_3P3	G10	—
VDD2_DDR	L7, N6, N7, R6, T6	—
VDDQ_DDR	G6, J6, J7, L6	—
VSS	A1, A21, C2, C4, C6, C8, C10, C12, C14, C16, C18, E3, E19, G3, G19, H8, H10, H12, H14, J3, J5, J8, J14, J19, K11, L1, L3, L5, L8, L14, L19, M11, N3, N5, N8, N14, N19, P8, P10, P12, P14, R3, R19, T1, U3, U19, W4, W6, W10, W12, W14, W16, W18, AA1, AA21	—

Table 101 shows an alpha-sorted list of functional contact assignments of the 14 x 14 mm package.

Table 101. 14 x 14 mm functional contact assignment

Ball name	14 x 14 ball	Power group	Ball Types	Default setting		
				Default modes	Default function	Status while reset is asserted
ADC_IN0	B19	VDD_ANA_1P8	ANALOG	—	—	Input without PU[1] / PD[2]
ADC_IN1	A20	VDD_ANA_1P8	ANALOG	—	—	Input without PU / PD
ADC_IN2	B20	VDD_ANA_1P8	ANALOG	—	—	Input without PU / PD
ADC_IN3	B21	VDD_ANA_1P8	ANALOG	—	—	Input without PU / PD
CCM_CLKO1	AA2	NVCC_WAKEUP	GPIO	Alt0	CCMSRCGPCMIX.CLK01	Output low
CCM_CLKO2	Y3	NVCC_WAKEUP	GPIO	Alt0	CCMSRCGPCMIX.CLK02	Output low
CCM_CLKO3	U4	NVCC_WAKEUP	GPIO	Alt5	GPIO4.IO[28]	Input with PD
CCM_CLKO4	V4	NVCC_WAKEUP	GPIO	Alt5	GPIO4.IO[29]	Input with PD
CLKIN1	B17	VDD_ANA_1P8	ANALOG	—	—	Input without PU / PD
CLKIN2	A18	VDD_ANA_1P8	ANALOG	—	—	Input without PU / PD
DAP_TCLK_SWCLK	Y1	NVCC_WAKEUP	GPIO	Alt0	DAP.TCLK_SWCLK	Input with PD
DAP_TDI	W1	NVCC_WAKEUP	GPIO	Alt0	DAP.TDI	Input with PU
DAP_TDO_TRACESWO	Y2	NVCC_WAKEUP	GPIO	Alt0	DAP.TDO_TRACESWO	Input without PU/PD
DAP_TMS_SWDIO	W2	NVCC_WAKEUP	GPIO	Alt0	DAP.TMS_SWDIO	Input with PU
DRAM_CA0_A	H2	VDD2_DDR	DDR	—	—	—
DRAM_CA1_A	G1	VDD2_DDR	DDR	—	—	—
DRAM_CA2_A	F2	VDD2_DDR	DDR	—	—	—
DRAM_CA3_A	E1	VDD2_DDR	DDR	—	—	—
DRAM_CA4_A	E2	VDD2_DDR	DDR	—	—	—
DRAM_CA5_A	D1	VDD2_DDR	DDR	—	—	—

Table continues on the next page...

Table 101. 14 x 14 mm functional contact assignment *...continued*

Ball name	14 x 14 ball	Power group	Ball Types	Default setting		
				Default modes	Default function	Status while reset is asserted
DRAM_CK_C_A	G5	VDD2_DDR	DDR	—	—	—
DRAM_CK_T_A	G4	VDD2_DDR	DDR	—	—	—
DRAM_CKE0_A	H1	VDD2_DDR	DDR	—	—	—
DRAM_CKE1_A	J4	VDD2_DDR	DDR	—	—	—
DRAM_CS0_A	F1	VDD2_DDR	DDR	—	—	—
DRAM_CS1_A	G2	VDD2_DDR	DDR	—	—	—
DRAM_DMI0_A	L2	VDDQ_DDR	DDR	—	—	—
DRAM_DMI1_A	T2	VDDQ_DDR	DDR	—	—	—
DRAM_DQ00_A	N1	VDDQ_DDR	DDR	—	—	—
DRAM_DQ01_A	N2	VDDQ_DDR	DDR	—	—	—
DRAM_DQ02_A	M1	VDDQ_DDR	DDR	—	—	—
DRAM_DQ03_A	M2	VDDQ_DDR	DDR	—	—	—
DRAM_DQ04_A	K1	VDDQ_DDR	DDR	—	—	—
DRAM_DQ05_A	K2	VDDQ_DDR	DDR	—	—	—
DRAM_DQ06_A	J1	VDDQ_DDR	DDR	—	—	—
DRAM_DQ07_A	J2	VDDQ_DDR	DDR	—	—	—
DRAM_DQ08_A	V1	VDDQ_DDR	DDR	—	—	—
DRAM_DQ09_A	V2	VDDQ_DDR	DDR	—	—	—
DRAM_DQ10_A	U2	VDDQ_DDR	DDR	—	—	—
DRAM_DQ11_A	U1	VDDQ_DDR	DDR	—	—	—
DRAM_DQ12_A	R1	VDDQ_DDR	DDR	—	—	—
DRAM_DQ13_A	R2	VDDQ_DDR	DDR	—	—	—
DRAM_DQ14_A	P2	VDDQ_DDR	DDR	—	—	—

Table continues on the next page...

Table 101. 14 x 14 mm functional contact assignment *...continued*

Ball name	14 x 14 ball	Power group	Ball Types	Default setting		
				Default modes	Default function	Status while reset is asserted
DRAM_DQ15_A	P1	VDDQ_DDR	DDR	—	—	—
DRAM_DQS0_C_A	L4	VDDQ_DDR	—	—	—	—
DRAM_DQS0_T_A	N4	VDDQ_DDR	DDRCLK	—	—	—
DRAM_DQS1_C_A	R5	VDDQ_DDR	—	—	—	—
DRAM_DQS1_T_A	R4	VDDQ_DDR	DDRCLK	—	—	—
DRAM_MTEST1	D4	VDD2_DDR	DDR	—	—	—
DRAM_RESET_N	D2	VDD2_DDR	DDR	—	—	—
DRAM_ZQ	E4	VDDQ_DDR	DDR	—	—	—
ENET1_MDC	AA11	NVCC_WAKEUP	GPIO	Alt5	GPIO4.IO[0]	Input with PD
ENET1_MDIO	AA10	NVCC_WAKEUP	GPIO	Alt5	GPIO4.IO[1]	Input with PD
ENET1_RD0	AA8	NVCC_WAKEUP	GPIO	Alt5	GPIO4.IO[10]	Input with PD
ENET1_RD1	Y9	NVCC_WAKEUP	GPIO	Alt5	GPIO4.IO[11]	Input with PD
ENET1_RD2	AA9	NVCC_WAKEUP	GPIO	Alt5	GPIO4.IO[12]	Input with PD
ENET1_RD3	Y10	NVCC_WAKEUP	GPIO	Alt5	GPIO4.IO[13]	Input with PD
ENET1_RX_CTL	Y8	NVCC_WAKEUP	GPIO	Alt5	GPIO4.IO[8]	Input with PD
ENET1_RXC	AA7	NVCC_WAKEUP	GPIO	Alt5	GPIO4.IO[9]	Input with PD
ENET1_TD0	W11	NVCC_WAKEUP	GPIO	Alt5	GPIO4.IO[5]	Input with PD
ENET1_TD1	T12	NVCC_WAKEUP	GPIO	Alt5	GPIO4.IO[4]	Input with PD
ENET1_TD2	U12	NVCC_WAKEUP	GPIO	Alt5	GPIO4.IO[3]	Input with PD
ENET1_TD3	V12	NVCC_WAKEUP	GPIO	Alt5	GPIO4.IO[2]	Input with PD
ENET1_TX_CTL	V10	NVCC_WAKEUP	GPIO	Alt5	GPIO4.IO[6]	Input with PD
ENET1_TXC	U10	NVCC_WAKEUP	GPIO	Alt5	GPIO4.IO[7]	Input with PD
ENET2_MDC	Y7	NVCC_WAKEUP	GPIO	Alt5	GPIO4.IO[14]	Input with PD

Table continues on the next page...

Table 101. 14 x 14 mm functional contact assignment *...continued*

Ball name	14 x 14 ball	Power group	Ball Types	Default setting		
				Default modes	Default function	Status while reset is asserted
ENET2_MDIO	AA6	NVCC_WAKEUP	GPIO	Alt5	GPIO4.IO[15]	Input with PD
ENET2_RD0	AA4	NVCC_WAKEUP	GPIO	Alt5	GPIO4.IO[24]	Input with PD
ENET2_RD1	Y5	NVCC_WAKEUP	GPIO	Alt5	GPIO4.IO[25]	Input with PD
ENET2_RD2	AA5	NVCC_WAKEUP	GPIO	Alt5	GPIO4.IO[26]	Input with PD
ENET2_RD3	Y6	NVCC_WAKEUP	GPIO	Alt5	GPIO4.IO[27]	Input with PD
ENET2_RX_CTL	Y4	NVCC_WAKEUP	GPIO	Alt5	GPIO4.IO[22]	Input with PD
ENET2_RXC	AA3	NVCC_WAKEUP	GPIO	Alt5	GPIO4.IO[23]	Input with PD
ENET2_TD0	T8	NVCC_WAKEUP	GPIO	Alt5	GPIO4.IO[19]	Input with PD
ENET2_TD1	U8	NVCC_WAKEUP	GPIO	Alt5	GPIO4.IO[18]	Input with PD
ENET2_TD2	V8	NVCC_WAKEUP	GPIO	Alt5	GPIO4.IO[17]	Input with PD
ENET2_TD3	T10	NVCC_WAKEUP	GPIO	Alt5	GPIO4.IO[16]	Input with PD
ENET2_TX_CTL	V6	NVCC_WAKEUP	GPIO	Alt5	GPIO4.IO[20]	Input with PD
ENET2_TXC	U6	NVCC_WAKEUP	GPIO	Alt5	GPIO4.IO[21]	Input with PD
GPIO_IO00	J21	NVCC_GPIO	GPIO	Alt0	GPIO2.IO[0]	Input with PD
GPIO_IO01	J20	NVCC_GPIO	GPIO	Alt0	GPIO2.IO[1]	Input with PD
GPIO_IO02	K20	NVCC_GPIO	GPIO	Alt0	GPIO2.IO[2]	Input with PD
GPIO_IO03	K21	NVCC_GPIO	GPIO	Alt0	GPIO2.IO[3]	Input with PD
GPIO_IO04	L17	NVCC_GPIO	GPIO	Alt0	GPIO2.IO[4]	Input with PD
GPIO_IO05	L18	NVCC_GPIO	GPIO	Alt0	GPIO2.IO[5]	Input with PD
GPIO_IO06	L20	NVCC_GPIO	GPIO	Alt0	GPIO2.IO[6]	Input with PD
GPIO_IO07	L21	NVCC_GPIO	GPIO	Alt0	GPIO2.IO[7]	Input with PD
GPIO_IO08	M20	NVCC_GPIO	GPIO	Alt0	GPIO2.IO[8]	Input with PD
GPIO_IO09	M21	NVCC_GPIO	GPIO	Alt0	GPIO2.IO[9]	Input with PD

Table continues on the next page...

Table 101. 14 x 14 mm functional contact assignment *...continued*

Ball name	14 x 14 ball	Power group	Ball Types	Default setting		
				Default modes	Default function	Status while reset is asserted
GPIO_IO10	N17	NVCC_GPIO	GPIO	Alt0	GPIO2.IO[10]	Input with PD
GPIO_IO11	N18	NVCC_GPIO	GPIO	Alt0	GPIO2.IO[11]	Input with PD
GPIO_IO12	N20	NVCC_GPIO	GPIO	Alt0	GPIO2.IO[12]	Input with PD
GPIO_IO13	N21	NVCC_GPIO	GPIO	Alt0	GPIO2.IO[13]	Input with PD
GPIO_IO14	P20	NVCC_GPIO	GPIO	Alt0	GPIO2.IO[14]	Input with PD
GPIO_IO15	P21	NVCC_GPIO	GPIO	Alt0	GPIO2.IO[15]	Input with PD
GPIO_IO16	R21	NVCC_GPIO	GPIO	Alt0	GPIO2.IO[16]	Input with PD
GPIO_IO17	R20	NVCC_GPIO	GPIO	Alt0	GPIO2.IO[17]	Input with PD
GPIO_IO18	R18	NVCC_GPIO	GPIO	Alt0	GPIO2.IO[18]	Input with PD
GPIO_IO19	R17	NVCC_GPIO	GPIO	Alt0	GPIO2.IO[19]	Input with PD
GPIO_IO20	T20	NVCC_GPIO	GPIO	Alt0	GPIO2.IO[20]	Input with PD
GPIO_IO21	T21	NVCC_GPIO	GPIO	Alt0	GPIO2.IO[21]	Input with PD
GPIO_IO22	U18	NVCC_GPIO	GPIO	Alt0	GPIO2.IO[22]	Input with PD
GPIO_IO23	U20	NVCC_GPIO	GPIO	Alt0	GPIO2.IO[23]	Input with PD
GPIO_IO24	U21	NVCC_GPIO	GPIO	Alt0	GPIO2.IO[24]	Input with PD
GPIO_IO25	V21	NVCC_GPIO	GPIO	Alt0	GPIO2.IO[25]	Input with PD
GPIO_IO26	V20	NVCC_GPIO	GPIO	Alt0	GPIO2.IO[26]	Input with PD
GPIO_IO27	W21	NVCC_GPIO	GPIO	Alt0	GPIO2.IO[27]	Input with PD
GPIO_IO28	W20	NVCC_GPIO	GPIO	Alt0	GPIO2.IO[28]	Input with PD
GPIO_IO29	Y21	NVCC_GPIO	GPIO	Alt0	GPIO2.IO[29]	Input with PD
I2C1_SCL	C20	NVCC_AON	GPIO	Alt5	GPIO1.IO[0]	Input with PD
I2C1_SDA	C21	NVCC_AON	GPIO	Alt5	GPIO1.IO[1]	Input with PD
I2C2_SCL	D20	NVCC_AON	GPIO	Alt5	GPIO1.IO[2]	Input with PD

Table continues on the next page...

Table 101. 14 x 14 mm functional contact assignment *...continued*

Ball name	14 x 14 ball	Power group	Ball Types	Default setting		
				Default modes	Default function	Status while reset is asserted
I2C2_SDA	D21	NVCC_AON	GPIO	Alt5	GPIO1.IO[3]	Input with PD
LVDS_D0_P	B5	VDD_LVDS_1P8	PHY	—	—	—
LVDS_D0_N	A5	VDD_LVDS_1P8	PHY	—	—	—
LVDS_D1_P	B4	VDD_LVDS_1P8	PHY	—	—	—
LVDS_D1_N	A4	VDD_LVDS_1P8	PHY	—	—	—
LVDS_D2_P	B2	VDD_LVDS_1P8	PHY	—	—	—
LVDS_D2_N	A2	VDD_LVDS_1P8	PHY	—	—	—
LVDS_D3_P	C1	VDD_LVDS_1P8	PHY	—	—	—
LVDS_D3_N	B1	VDD_LVDS_1P8	PHY	—	—	—
LVDS_CLK_P	B3	VDD_LVDS_1P8	PHY	—	—	—
LVDS_CLK_N	A3	VDD_LVDS_1P8	PHY	—	—	—
MIPI_CSI1_CLK_N	D10	MIPI_CSI1_VPH	PHY	—	—	—
MIPI_CSI1_CLK_P	E10	MIPI_CSI1_VPH	PHY	—	—	—
MIPI_CSI1_D0_N	A11	MIPI_CSI1_VPH	PHY	—	—	—
MIPI_CSI1_D0_P	B11	MIPI_CSI1_VPH	PHY	—	—	—
MIPI_CSI1_D1_N	A10	MIPI_CSI1_VPH	PHY	—	—	—
MIPI_CSI1_D1_P	B10	MIPI_CSI1_VPH	PHY	—	—	—
MIPI_DSI1_CLK_N	D6	MIPI_DSI1_VPH	PHY	—	—	—
MIPI_DSI1_CLK_P	E6	MIPI_DSI1_VPH	PHY	—	—	—
MIPI_DSI1_D0_N	A6	MIPI_DSI1_VPH	PHY	—	—	—
MIPI_DSI1_D0_P	B6	MIPI_DSI1_VPH	PHY	—	—	—
MIPI_DSI1_D1_N	A7	MIPI_DSI1_VPH	PHY	—	—	—
MIPI_DSI1_D1_P	B7	MIPI_DSI1_VPH	PHY	—	—	—

Table continues on the next page...

Table 101. 14 x 14 mm functional contact assignment *...continued*

Ball name	14 x 14 ball	Power group	Ball Types	Default setting		
				Default modes	Default function	Status while reset is asserted
MIPI_DSI1_D2_N	A8	MIPI_DSI1_VPH	PHY	—	—	—
MIPI_DSI1_D2_P	B8	MIPI_DSI1_VPH	PHY	—	—	—
MIPI_DSI1_D3_N	A9	MIPI_DSI1_VPH	PHY	—	—	—
MIPI_DSI1_D3_P	B9	MIPI_DSI1_VPH	PHY	—	—	—
MIPI_REXT	D8	MIPI_DSI1_VPH	PHY	—	—	—
ONOFF	A19	NVCC_BBSM_1P8	GPIO	Alt0	BBSMMIX.ONOFF	Input without PU / PD
PDM_BIT_STREAM0	J17	NVCC_AON	GPIO	Alt5	GPIO1.IO[9]	Input with PD
PDM_BIT_STREAM1	G18	NVCC_AON	GPIO	Alt5	GPIO1.IO[10]	Input with PD
PDM_CLK	G17	NVCC_AON	GPIO	Alt5	GPIO1.IO[8]	Input with PD
PMIC_ON_REQ	A17	NVCC_BBSM_1P8	GPIO	Alt0	BBSMMIX.PMIC_ON_REQ	Output high without PU / PD
PMIC_STBY_REQ	B18	NVCC_BBSM_1P8	GPIO	Alt0	BBSMMIX.PMIC_STBY_REQ	Output low without PU / PD
POR_B	A16	NVCC_BBSM_1P8	GPIO	Alt0	BBSMMIX.POR_B	Input without PU / PD
RTC_XTALI	E16	NVCC_BBSM_1P8	ANALOG	Alt0	BBSMMIX.RTC	—
RTC_XTALO	D16	NVCC_BBSM_1P8	ANALOG	—	—	—
SAI1_RXD0	H20	NVCC_AON	GPIO	Alt5	GPIO1.IO[14]	Input with PD
SAI1_TXC	G20	NVCC_AON	GPIO	Alt5	GPIO1.IO[12]	Input with PD
SAI1_TXD0	H21	NVCC_AON	GPIO	Alt5	GPIO1.IO[13] CCMSRCGPCMIX.BOOT_MODE[3]	Input with PD
SAI1_TXFS	G21	NVCC_AON	GPIO	Alt5	GPIO1.IO[11] CCMSRCGPCMIX.BOOT_MODE[2]	Input with PD

Table continues on the next page...

Table 101. 14 x 14 mm functional contact assignment *...continued*

Ball name	14 x 14 ball	Power group	Ball Types	Default setting		
				Default modes	Default function	Status while reset is asserted
SD1_CLK	Y11	NVCC_WAKEUP	GPIO	Alt5	GPIO3.IO[8]	Input with PD
SD1_CMD	AA12	NVCC_WAKEUP	GPIO	Alt5	GPIO3.IO[9]	Input with PD
SD1_DATA0	AA14	NVCC_WAKEUP	GPIO	Alt5	GPIO3.IO[10]	Input with PD
SD1_DATA1	AA15	NVCC_WAKEUP	GPIO	Alt5	GPIO3.IO[11]	Input with PD
SD1_DATA2	AA16	NVCC_WAKEUP	GPIO	Alt5	GPIO3.IO[12]	Input with PD
SD1_DATA3	AA13	NVCC_WAKEUP	GPIO	Alt5	GPIO3.IO[13]	Input with PD
SD1_DATA4	Y13	NVCC_WAKEUP	GPIO	Alt5	GPIO3.IO[14]	Input with PD
SD1_DATA5	Y14	NVCC_WAKEUP	GPIO	Alt5	GPIO3.IO[15]	Input with PD
SD1_DATA6	Y15	NVCC_WAKEUP	GPIO	Alt5	GPIO3.IO[16]	Input with PD
SD1_DATA7	Y16	NVCC_WAKEUP	GPIO	Alt5	GPIO3.IO[17]	Input with PD
SD1_STROBE	Y12	NVCC_WAKEUP	GPIO	Alt5	GPIO3.IO[18]	Input without PU / PD
SD2_CD_B	Y17	NVCC_SD2	GPIO	Alt5	GPIO3.IO[0]	Input with PD
SD2_CLK	AA19	NVCC_SD2	GPIO	Alt5	GPIO3.IO[1]	Input with PD
SD2_CMD	Y19	NVCC_SD2	GPIO	Alt5	GPIO3.IO[2]	Input with PD
SD2_DATA0	Y18	NVCC_SD2	GPIO	Alt5	GPIO3.IO[3]	Input with PD
SD2_DATA1	AA18	NVCC_SD2	GPIO	Alt5	GPIO3.IO[4]	Input with PD
SD2_DATA2	Y20	NVCC_SD2	GPIO	Alt5	GPIO3.IO[5]	Input with PD
SD2_DATA3	AA20	NVCC_SD2	GPIO	Alt5	GPIO3.IO[6]	Input with PD
SD2_RESET_B	AA17	NVCC_SD2	GPIO	Alt5	GPIO3.IO[7]	Input with PD
SD2_VSELECT	V18	NVCC_WAKEUP	GPIO	Alt5	GPIO3.IO[19]	Input with PD
SD3_CLK	V16	NVCC_WAKEUP	GPIO	Alt5	GPIO3.IO[20]	Input with PD
SD3_CMD	U16	NVCC_WAKEUP	GPIO	Alt5	GPIO3.IO[21]	Input with PD
SD3_DATA0	T16	NVCC_WAKEUP	GPIO	Alt5	GPIO3.IO[22]	Input with PD

Table continues on the next page...

Table 101. 14 x 14 mm functional contact assignment *...continued*

Ball name	14 x 14 ball	Power group	Ball Types	Default setting		
				Default modes	Default function	Status while reset is asserted
SD3_DATA1	V14	NVCC_WAKEUP	GPIO	Alt5	GPIO3.IO[23]	Input with PD
SD3_DATA2	U14	NVCC_WAKEUP	GPIO	Alt5	GPIO3.IO[24]	Input with PD
SD3_DATA3	T14	NVCC_WAKEUP	GPIO	Alt5	GPIO3.IO[25]	Input with PD
TAMPER0	B16	NVCC_BBSM_1P8	GPIO	Alt0	BBSMMIX.TAMPER0	Input with PD
TAMPER1	F14	NVCC_BBSM_1P8	GPIO	Alt0	BBSMMIX.TAMPER1	Input with PD
UART1_RXD	E20	NVCC_AON	GPIO	Alt5	GPIO1.IO[4]	Input with PD
UART1_TXD	E21	NVCC_AON	GPIO	Alt5	GPIO1.IO[5] CCMSRCGPCMIX.BOOT_MODE[0]	Input with PD
UART2_RXD	F20	NVCC_AON	GPIO	Alt5	GPIO1.IO[6]	Input with PD
UART2_TXD	F21	NVCC_AON	GPIO	Alt5	GPIO1.IO[7] CCMSRCGPCMIX.BOOT_MODE[1]	Input with PD
USB1_D_N	A14	VDD_USB_3P3	PHY	—	—	—
USB1_D_P	B14	VDD_USB_3P3	PHY	—	—	—
USB1_ID	C11	VDD_USB_1P8	PHY	—	—	—
USB1_TXRTUNE	D12	VDD_USB_1P8	PHY	—	—	—
USB1_VBUS	F12	VDD_USB_3P3	PHY	—	—	—
USB2_D_N	A15	VDD_USB_3P3	PHY	—	—	—
USB2_D_P	B15	VDD_USB_3P3	PHY	—	—	—
USB2_ID	E12	VDD_USB_1P8	PHY	—	—	—
USB2_TXRTUNE	D14	VDD_USB_1P8	PHY	—	—	—
USB2_VBUS	E14	VDD_USB_3P3	PHY	—	—	—
WDOG_ANY	J18	NVCC_AON	GPIO	Alt0	WDOG1.WDOG_ANY	Input with PU
XTALI_24M	D18	VDD_ANA_1P8	ANALOG	—	—	—

Table continues on the next page...

Table 101. 14 x 14 mm functional contact assignment *...continued*

Ball name	14 x 14 ball	Power group	Ball Types	Default setting		
				Default modes	Default function	Status while reset is asserted
XTALO_24M	E18	VDD_ANA_1P8	ANALOG	—	—	—

1. Pull Up
2. Pull Down

6.1.3 14 x 14 mm, 0.65 mm pitch, ball map

Table 102 shows the 14 x 14 mm, 0.65 mm pitch ball map for the i.MX 93.

Table 102. 14 x 14 mm, 0.65 mm pitch, ball map

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	
A	VSS	LVDS_D2_N	LVDS_CLK_N	LVDS_D1_N	LVDS_D0_N	MIPI_DSI1_D0_N	MIPI_DSI1_D1_N	MIPI_DSI1_D2_N	MIPI_DSI1_D3_N	MIPI_CSI1_D1_N	MIPI_CSI1_D0_N	NC_A12	NC_A13	USB1_D_N	USB2_D_N	POR_B	PMIC_ON_REQ	CLKIN2	ONOFF	ADC_IN1	VSS	A
B	LVDS_D3_N	LVDS_D2_P	LVDS_CLK_P	LVDS_D1_P	LVDS_D0_P	MIPI_DSI1_D0_P	MIPI_DSI1_D1_P	MIPI_DSI1_D2_P	MIPI_DSI1_D3_P	MIPI_CSI1_D1_P	MIPI_CSI1_D0_P	NC_B12	NC_B13	USB1_D_P	USB2_D_P	TAMPER0	CLKIN1	PMIC_STBY_REQ	ADC_IN0	ADC_IN2	ADC_IN3	B
C	LVDS_D3_P	VSS		VSS		VSS		VSS		VSS	USB1_ID	VSS		VSS		VSS		VSS		I2C1_SCL	I2C1_SDA	C
D	DRAM_CA5_A	DRAM_RESET_N		DRAM_MTEST1		MIPI_DSI1_CLK_N		MIPI_REXT		MIPI_CSI1_CLK_N		USB1_TXRTUNE		USB2_TXRTUNE		RXC_XTALO		XTALI_24M		I2C2_SCL	I2C2_SDA	D
E	DRAM_CA3_A	DRAM_CA4_A	VSS	DRAM_ZQ		MIPI_DSI1_CLK_P		VDD_USB_1P8		MIPI_CSI1_CLK_P		USB2_ID		USB2_VBUS		RTC_XTALI		XTALO_24M	VSS	UART1_RXD	UART1_TXD	E
F	DRAM_CS0_A	DRAM_CA2_A				VDD_LVDS_1P8		VDD_MIPI_1P8		VDD_USB_0P8		USB1_VBUS		TAMPER1		VDD_ANA0_1P8				UART2_RXD	UART2_TXD	F
G	DRAM_CA1_A	DRAM_CS1_A	VSS	DRAM_CK_T_A	DRAM_CK_C_A	VDDQ_DDR		VDD_MIPI_0P8		VDD_USB_3P3		NVCC_BBSM_1P8		VDD_BBSM_0P8_CAP		VDD_ANA0_1P8	PDM_CLK	PDM_BIT_STREAM1	VSS	SAI1_TXC	SAI1_TXF	G

Table continues on the next page...

Table 102. 14 x 14 mm, 0.65 mm pitch, ball map *...continued*

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	
H	DRAM_CKE0_A	DRAM_CA0_A						VSS		VSS		VSS		VSS						SAI1_RXD0	SAI1_TXD0	**H**
J	DRAM_DQ06_A	DRAM_DQ07_A	VSS	DRAM_CKE1_A	VSS	VDDQ_DDR	VDDQ_DDR	VSS	VDD_SOC	VDD_SOC	VDD_SOC	VDD_SOC	VDD_SOC	VSS	VDD_ANA_0P8	VDD_ANA_0P8	PDM_BIT_STREAM0	WDOG_ANY	VSS	GPIO_IO01	GPIO_IO00	**J**
K	DRAM_DQ04_A	DRAM_DQ05_A							VDD_SOC	VDD_SOC	VSS	VDD_SOC	VDD_SOC							GPIO_IO02	GPIO_IO03	**K**
L	VSS	DRAM_DMI0_A	VSS	DRAM_DQS0_C_A	VSS	VDDQ_DDR	VDD2_DDR	VSS						VSS	VDD_ANAVDET_1P8	NVCC_AON	GPIO_IO04	GPIO_IO05	VSS	GPIO_IO06	GPIO_IO07	**L**
M	DRAM_DQ02_A	DRAM_DQ03_A							VDD_SOC	VDD_SOC	VSS	VDD_SOC	VDD_SOC							GPIO_IO08	GPIO_IO09	**M**
N	DRAM_DQ00_A	DRAM_DQ01_A	VSS	DRAM_DQS0_T_A	VSS	VDD2_DDR	VDD2_DDR	VSS	VDD_SOC	VDD_SOC	VDD_SOC	VDD_SOC	VDD_SOC	VSS	NVCC_GPIO	NVCC_GPIO	GPIO_IO10	GPIO_IO11	VSS	GPIO_IO12	GPIO_IO13	**N**

Table continues on the next page...

Table 102. 14 x 14 mm, 0.65 mm pitch, ball map *...continued*

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	
P	DRAM_DQ15_A	DRAM_DQ14_A						VSS		VSS		VSS		VSS						GPIO_IO14	GPIO_IO15	P
R	DRAM_DQ12_A	DRAM_DQ13_A	VSS	DRAM_DQS1_T_A	DRAM_DQS1_C_A	VDD2_DDR		VDD_ANA1_1P8		NVCC_WAKEUP		NVCC_WAKEUP		VDD_ANA_0P8		NVCC_SD2	GPIO_IO19	GPIO_IO18	VSS	GPIO_IO17	GPIO_IO16	R
T	VSS	DRAM_DMI1_A				VDD2_DDR		ENET2_TD0		ENET2_TD3		ENET1_TD1		SD3_DATA3		SD3_DATA0				GPIO_IO20	GPIO_IO21	T
U	DRAM_DQ11_A	DRAM_DQ10_A	VSS	CCM_CLKO3		ENET2_TXC		ENET2_TD1		ENET1_TXC		ENET1_TD2		SD3_DATA2		SD3_CMD		GPIO_IO22	VSS	GPIO_IO23	GPIO_IO24	U
V	DRAM_DQ08_A	DRAM_DQ09_A		CCM_CLKO4		ENET2_TX_CTL		ENET2_TD2		ENET1_TX_CTL		ENET1_TD3		SD3_DATA1		SD3_CLK		SD2_VSELECT		GPIO_IO26	GPIO_IO25	V
W	DAP_TDI	DAP_TMS_SWDIO		VSS		VSS		NVCC_WAKEUP		VSS	ENET1_TD0	VSS		VSS		VSS		VSS		GPIO_IO28	GPIO_IO27	W
Y	DAP_TCLK_S	DAP_TDO_T	CCM_CLKO2	ENET2_R	ENET2_RD1	ENET2_RD3	ENET2_MDC	ENET1_R	ENET1_RD1	ENET1_RD3	SD1_CLK	SD1_STROBE	SD1_DATA4	SD1_DATA5	SD1_DATA6	SD1_DATA7	SD2_CD_B	SD2_DATA0	SD2_CMD	SD2_DATA2	GPIO_IO29	Y

Table continues on the next page...

Table 102. 14 x 14 mm, 0.65 mm pitch, ball map *...continued*

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	
	WCLK	RACESWO		X_CTL				X_CTL														
AA	VSS	CCM_CLKO1	ENET2_RXC	ENET2_RD0	ENET2_RD2	ENET2_MDIO	ENET1_RXC	ENET1_RD0	ENET1_RD2	ENET1_MDIO	ENET1_MDC	SD1_CMD	SD1_DATA3	SD1_DATA0	SD1_DATA1	SD1_DATA2	SD2_RESET_B	SD2_DATA1	SD2_CLK	SD2_DATA3	VSS	AA
	1	2		3	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	

6.2 DDR pin function list

Table 103 shows the DDR pin function list.

Table 103. DDR pin function list

Ball name	LPDDR4/LPDDR4x
DRAM_DQS0_T_A	DQSA_T[0]
DRAM_DQS0_C_A	DQSA_C[0]
DRAM_DMI0_A	DM/DBIA[0]
DRAM_DQ00_A	DQA[0]
DRAM_DQ01_A	DQA[1]
DRAM_DQ02_A	DQA[2]
DRAM_DQ03_A	DQA[3]
DRAM_DQ04_A	DQA[4]
DRAM_DQ05_A	DQA[5]
DRAM_DQ06_A	DQA[6]
DRAM_DQ07_A	DQA[7]
DRAM_DQS1_T_A	DQSA_T[1]
DRAM_DQS1_C_A	DQSA_C[1]
DRAM_DMI1_A	DM/DBIA[1]
DRAM_DQ08_A	DQA[8]
DRAM_DQ09_A	DQA[9]
DRAM_DQ10_A	DQA[10]
DRAM_DQ11_A	DQA[11]
DRAM_DQ12_A	DQA[12]
DRAM_DQ13_A	DQA[13]
DRAM_DQ14_A	DQA[14]
DRAM_DQ15_A	DQA[15]
DRAM_RESET_N	RESET_N

Table continues on the next page...

Table 103. DDR pin function list *...continued*

DRAM_MTRST1	—
DRAM_CKE0_A	CKEA[0]
DRAM_CKE1_A	CKEA[1]
DRAM_CS0_A	CSA[0]
DRAM_CS1_A	CSA[1]
DRAM_CK_T_A	CLKA_T
DRAM_CK_C_A	CLKA_C
DRAM_CA0_C	CAA[0]
DRAM_CA1_C	CAA[1]
DRAM_CA2_C	CAA[2]
DRAM_CA3_C	CAA[3]
DRAM_CA4_C	CAA[4]
DRAM_CA5_C	CAA[5]
DRAM_ZQ[1]	—

1. DRAM_ZQ can be connected with a 120 Ω ±1% resistor to GND.

7 Revision history

Table 104 provides a revision history for this data sheet.

Table 104. i.MX 93 Data Sheet document revision history

Rev. Number	Date	Substantive Change(s)
IMX93AEC v.6.1	07 July 2025	• Removed the I/O pin information from Ordering information • Updated the Package type in Figure 1 • Removed Section 9 x 9 mm package information
IMX93AEC v.6.0	04 June 2025	• Updated Ordering information • Updated Figure 1 • Updated the descriptions about DRAM and LPUART, and ADC in Table 1; Removed FlexIO from Table 1 • Added LPDDR4 in Figure 2; updated ADC and LPUART in Figure 2

Table continues on the next page...

Table 104. i.MX 93 Data Sheet document revision history...*continued*

Rev. Number	Date	Substantive Change(s)
		• Updated the description about ONOFF and XTALI_24/XTALO_24M in Table 3 • Added Table 11 • Updated Table 15 • Updated Table 27 • Updated the description of DDR SDRAM–specific parameters (LPDDR4/LPDDR4X) and Clock/data/command/address pin allocations • Added a footnote in Table 43 • Added a footnote in Table 50 • Updated the unit of C_{sample}, $C_{compare}$, and $C_{conversion}$ to cycle in Table 51; removed the maximum value of $C_{compare}$ and second ADC clock in Table 51; added ENOB lavues in Table 51 • Removed Table. ADC electrical specifications (VREFH = VDD_ANAx_1p8 and $VADIN_{max}$ ≤ VREFH) • Added a footnote in Table 68 • Updated Table 71 • Removed BCAN, BCANXL, and minimum operating frequency from Table 72 • Added the maximum frequency footnotes in FlexSPI timing parameters • Updated LPB descriptions in Boot mode configuration
Rev. 5	01/2025	• Added new part number in Table 2 • Updated the definition of special fuse in Figure 1 • Removed Module list • Updated the descriptions of External clock sources • Updated the NVCC_BBSM_1P8 in Figure 4 • Updated the footnote of Table 29 • Updated the values of V_{IDTH}, V_{IDTL}, V_{IHHS}, and V_{IHHS} in Table 36 • Updated Figure 50 • Updated the default function of SAI1_RXD0 in Table 101
Rev. 4	08/2024	• Updated Table 2 • Updated Figure 1 • Updated Clock sources • Added a footnote in Figure 4 • Updated Table 24 and Table 25 • Updated Table 26 and Table 28

Table continues on the next page...

Table 104. i.MX 93 Data Sheet document revision history...*continued*

Rev. Number	Date	Substantive Change(s)
		• Updated JTAG timing parameters • Updated descriptions and a table footnote in SWD timing parameters • Updated descriptions and a footnote in LCD Controller (LCDIF) timing parameters • Updated descriptions and footnotes in SAI switching specifications • Updated descriptions of SPDIF timing parameters • Updated footnotes, descriptions, and Figure 25 in Ultra-high-speed SD/SDIO/MMC host interface (uSDHC) AC timing • Updated descriptions and footnotes in Table 60, Table 61, Table 62, Table 63, and Table 64 • Updated descriptions and footnotes in Table 61, Table 62, • Updated descriptions and footnotes in LPSPI timing parameters • Updated Improved Inter-Integrated Circuit Interface (I3C) specifications • Updated descriptions of CAN network AC electrical specifications • Updated descriptions of Timer/Pulse width modulator (TPM) timing parameters • Updated descriptions in FlexSPI timing parameters • Updated descriptions and a footnote in Flexible I/O controller (FlexIO) electrical specifications • Updated Table 92
Rev. 3	12/2023	• Updated Table 2. Ordering information • Added information about FlexIO in Table i.MX 93 modules list • Updated Figure 1, "Part number nomenclature—i.MX 93" • Updated Figure 2 • Updated Table 4. Special signal considerations • Updated Table 9. Absolute maximum ratings • Updated Table 10. Electrostatic discharge and latch up ratings • Added Section 4.1.2.3, 14 x 14 mm FCBGA package thermal characteristics • Updated Table 14. Operating ranges • Added Table 17. External clock frequency • Updated the current values in Table 21. Maximum supply currents • Added a note in Section 4.2.1, Power mode definition • Updated Table 22. The power supply states • Added footnotes in Table 23. Low power mode definition • Added Table 24. Chip power in different LP modes

Table continues on the next page...

Table 104. i.MX 93 Data Sheet document revision history...*continued*

Rev. Number	Date	Substantive Change(s)
		• Updated Table 26. GPIO DC parameters, Table 27. Additional leakage parameters, and Table 27 • Updated the operating frequency in Table 30. LVDS AC parameters • Updated ENOB values in Table 54. ADC electrical specificatins (VREFTH = VDDA_ANAx_1P8 and $VADIN_{max}$ ≤VREFH • Updated Section 4.12.9, FlexSPI timing parameters • Update the signal name of RMII_RX_ER in Table 63. ENET2 signal mapping and Table 67. ENET QOS signal mapping • Updated the naming of ENET_CLK to RMII_REF_CLK, ENET_TD, and ENET_RD in Section 4.12.2.2, RMII mode timing • Removed USB 3.0 information from Section 4.12.12, USB PHY parameters • Added 14 x 14 mm package information
Rev. 2	08/2023	• Updated the term "Consumer" to "Commercial" • Updated JTAG pin description in Table 1 • Updated Table 2. Ordering information • Updated remarks in Table 4. Special signal considerations • Added ADC and TAMPER pin information in Table 5. Unused function strapping recommendations • Updated NVCC_BBSM_1P8 description in Section 4.1.3, Power architecture • Updated descriptions in Section 4.1.6.1, External clock sources • Updated Figure 7, "Output transition time waveform" • Updated Table 26. GPIO DC parameters and Table 27. Additional leakage parameters • Removed JTAG_TRST information from Section 4.8.3, JTAG timing parameters • Updated Table 63. ENET2 signal mapping and Table 67. ENET QOS signal mapping • Updated footnotes of Table 68 and Table 69 • Updated Table 98. Fuses and associated pins used for boot
Rev. 1	04/2023	• Initial version

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Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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