AN11801

TEA19161 and TEA19162 controller ICs

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Document information

Information	Content
Keywords	TEA19161, TEA19162, PFC, burst mode operation, low-power mode, cycle-by-cycle control, V_{cap} control, resonant power converter
Abstract	The TEA19161T and TEA19162T are a set of controller ICs for resonant power supplies that include a PFC. To reach a high efficiency at all power levels, the TEA19161T(LLC) introduces a new operating mode: low-power mode. This mode operates in the power region between continuous switching (now called high-power mode) and burst mode. Most LLC resonant converter controllers regulate the output power by adjusting the operating frequency. The TEA19161T regulates the output power by adjusting the voltage across the primary resonant capacitor for accurate state control and a linear power control. External presets can define operation modes and protections. This feature provides flexibility and ease of design for optimizing controller properties to application-specific requirements.

1 Introduction

The TEA1916 is a fully digital controller for high-efficiency resonant power supplies. It is a 2-chip combo, which includes the TEA19161 resonant/LLC controller and the TEA19162 PFC controller. Together with the TEA1995T dual SR controller, a complete resonant power supply can be built, which is easy to design and has a very low component count. This power supply meets the efficiency regulations of Energy Star, the Department of Energy (DoE), the Eco-design directive of the European Union, the European Code of Conduct, and other guidelines. So, an additional power supply for the standby supply is not required.

This application note describes the TEA19161 and TEA19162 functions for different applications. It covers the functionality of the standard IC versions TEA19161T, TEA19162T, and the safe-restart versions TEA19161CT and TEA19162CT. Because the combination of two controllers provides extensive functionality, many topics are discussed.

This document is set up in such a way that a chapter or paragraph of a specific topic can be read as a standalone explanation. A minimum number of cross-references to other document parts of the TEA19161T or TEA19162T data sheets is used. This document setup leads to repetition of some information within the application note and to descriptions or figures that are similar to the ones published in the data sheets. To enhance readability, only typical values are given.

The TEA19161T and TEA19162T can be considered as one PFC + HBC system controller. In this document, the one system controller is called TEA1916. Only in specific cases, the TEA19161T and TEA19162T names are used.

1.1 Related documents

For more information and tools, see the various other TEA1916 documents such as:

- Data sheets TEA19161T (Ref. 1), TEA19161CT (Ref. 3), TEA19162T (Ref. 2), and TEA19162CT (Ref. 4)
- Excel calculation sheet (available on request)
- Online calculation tool
- Demo board user manuals

1.2 Related products

NXP Semiconductors products that are related to the TEA1916 ones are:

- TEA1716:
  This product provides a PFC + LLC controller in an SO24 IC package. It allows low-power consumption burst mode operation.
- TEA1713:
  This product provides a PFC + LLC controller in one SO24 IC package. It is more suitable for applications that do not have stringent requirements on burst mode operation.

Other NXP Semiconductors products for resonant power conversion are:

- TEA1795:
  Synchronous rectification controller for resonant converters with dual gate drivers in SO8.
- TEA1995:
  Synchronous rectification controller for resonant converters with dual gate drivers in an SO8 package. This product is optimized for the TEA1916 operating modes.
- TEA1708:
  X-capacitor discharge IC.

2 TEA1916 highlights and features

2.1 Resonant conversion

The market of today demands high-quality, reliable, small, lightweight, and efficient power supplies.

A resonant DC-to-DC converter produces sinusoidal currents with low switching losses. It provides the possibility of operating at higher frequencies with excellent efficiency at high power levels.

In recent years, LLC resonant converters have become more popular because of the high efficiency at medium and high output load. The latest generation of resonant controllers that support burst-mode operation have enabled good efficiency, even at low output load, a low power consumption in standby, or no-load operation.

The TEA19161 offers a next step in low-load operation. Reducing the converter power losses further and providing programmable operation behavior to make the best fit for each application.

2.2 Power factor correction conversion

Basic switch-mode power supplies represent a non-linear impedance (load characteristic) to the mains input. The current taken from the mains supply occurs only at the highest voltage peaks and is stored in a large capacitor. The energy is taken from this capacitor in accordance with the switch-mode power supply operation characteristics.

Government regulations dictate special requirements for the load characteristics of certain applications.

Two main requirements can be distinguished:

- Mains harmonics requirements EN61000-3-2
- Power factor (real power/apparent power)

The requirements impose a more resistive characteristic of the mains load.

To fulfill these requirements, measures must be taken regarding the input circuit of the power supply. To modify the mains load characteristics, passive (typically a series coil) or active (typically a boost converter) circuits can be used.

An additional market requirement for the added mains input circuit is that it works with a good efficiency and that the cost is low.

To meet these requirements, using a boost converter with a resonant converter provides the benefit of a fixed DC input voltage. The fixed input voltage ensures an easier design of the resonant converter (especially for wide mains input voltage range applications) and makes reaching a higher efficiency possible.

To implement optimal burst-mode operation and complementary protection functions, the TEA19162 provides a PFC controller that operates in close cooperation with the TEA19161.

2.3 TEA19161 and TEA19162 controller combination

The TEA19161T and TEA19162T form a control combo-IC. The combo-IC incorporates a half-bridge controller for a resonant LLC tank and a PFC controller. It provides high efficiency at all power levels. Together with the TEA1995T dual LLC resonant SR controller, a high-performance cost-effective resonant power supply can be designed. The design can meet the efficiency requirements of Energy Star, the Department of Energy (DoE), the Eco-design Directive of the European Union, the European Code of Conduct, and other guidelines.

Generally, resonant converters show an excellent efficiency at high power levels, while at lower levels the efficiency reduces because of the relatively high magnetizing current and switching losses. To reach a high efficiency at all power level, the TEA19161T (LLC) introduces a new operating mode, low-power mode. This

mode allows operation in the power region between continuous switching (now called high-power mode) and burst mode.

Most LLC resonant converter controllers regulate the output power by adjusting the operating frequency. The TEA19161T regulates the output power by adjusting the voltage across the primary resonant capacitor. The result is accurate state control and a linear power control.

Using a voltage divider, the primary resonant capacitor voltage provides accurate information about the output power to the controller. The voltage divider sets the output power levels. It determines when the system switches from the high-power mode to low-power mode and when it switches from low-power mode to burst mode.

External presets define the operating modes and protections. At start-up, the IC measures the applied resistor value on a pin and sets the mode or protection parameters accordingly. This feature provides flexibility and ease of design to optimize controller properties to application-specific requirements.

The following protections are implemented using the communication between the two controllers:

- Overcurrent protection (OCP)
- Overvoltage protection (OVP)
- Overpower protection (OPP)
- Brownin
- Brownout
- Capacitive mode regulation (CMR)
- Overtemperature protection (OTP)
- Open-loop protection (OLP)

2.4 Features and benefits

2.4.1 Distinctive features

- Complete combo functionality combining TEA19161 and TEA19162
- Integrated X-capacitor discharge without additional external components
- Universal mains supply operation (70 V (AC) to 276 V (AC))
- Integrated PFC soft start and soft stop
- Integrated high-voltage start-up
- V_{CC} regulation via HV source allowing small VCC capacitor
- Fast system start-up (< 0.5 s)
- Integrated high-voltage level shifter
- Maximized range of operation on switching frequencies outside the audible area
- Integrated LLC soft start
- Power good signal
- Up to 500 kHz half-bridge switching frequency
- Ease of design because control and operation parameters can be preset

2.4.2 Green features

- PFC valley/zero voltage switching for minimum switching losses
- PFC frequency limitation for best efficiency at reduced switching losses
- Very high system efficiency at all load conditions
- Compliant with Energy using Product directive (EuP) lot 6
- Excellent no-load system input power (< 75 mW)
- Regulated low feedback optocoupler current, enabling low no-load power consumption
- Very low supply current during non-switching state in burst mode
- Transitions between modes and power levels are adjustable with external presets
- LLC adaptive non-overlap time

2.4.3 Protection features

- Safe restart mode for system fault conditions
- PFC continuous-mode protection using demagnetization detection
- Accurate overvoltage protection (OVP)
- Open-loop protection (OLP)
- Internal and external IC overtemperature protection (OTP)
- Low and adjustable PFC overcurrent protection (OCP) trip level
- Adjustable brownin/brownout protection
- Supply undervoltage protection (UVP)
- Overpower protection (OPP)
- Integrated presettable overpower timeout
- Presettable latch or restart function for system fault conditions (CT-versions are safe start versions)
- Capacitive mode protection (CMP)
- Maximum low-side and high-side LLC on-time protection
- Overcurrent protection (OCP)
- Disable input

2.5 Typical areas of application

- High-power adapters
- Low-power adapters
- Slim notebook adapters
- Computer power supplies
- LCD television
- Office equipment
- Server supplies
- Professional lighting

3 Pinning

3.1 TEA19161T (HBC) pin overview

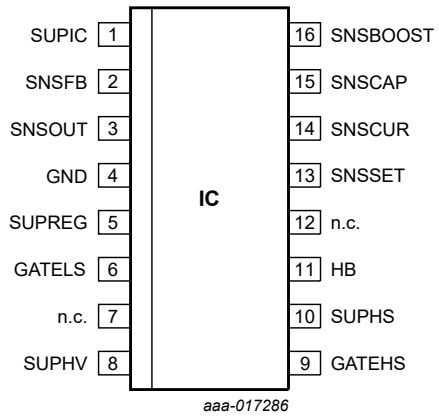


Figure 1. TEA19161T pinning diagram

Table 1. TEA19161T (PFC) pins

Pin	Pin name	Functional description summary
1	SUPIC	IC voltage supply input and output of the HV start-up source All internal circuits are directly or indirectly (via SUPREG) supplied from this pin. The exception is the high-voltage circuit. The SUPIC can be connected to the SUPIC function of the TEA19162 PFC controller. The buffer capacitor on SUPIC can be charged or supplied in several ways: • High-voltage (HV) start-up source • Auxiliary winding from HBC transformer or capacitive supply from switching half-bridge node • External DC supply, for example a standby supply When the SUPIC voltage has reached the start level of 19.1 V, the IC enables operation. If supplied by the HV source, the voltage is regulated with a hysteresis of 0.7 V. When the voltage drops to below 13.2 V, the IC stops operating. A system reset is activated at 3.5 V. During the non-switching period in burst mode, the HV source is activated when the SUPIC voltage drops to 14 V. To avoid that the system stops during a long period of non-switching, the HV source regulates the SUPIC voltage with a hysteresis of 0.9 V. In this way, a voltage drop on the SUPIC pin to below 14 V is avoided.
2	SNSFB	Sense input for HBC output regulation feedback because of current Normally, the pin is connected to ground via an optocoupler. Pulling current from SNSFB regulates the feedback. The IC measures the regulation current. For measuring the current during engineering work, an additional 100 Ω or 1 kΩ series resistor to GND can be useful. To minimize power consumption, the internal source slowly regulates the SNSFB to an average low current level (optobias regulation): • HP and LP mode: 80 µA • Burst mode: 100 µA The SNSFB current and voltage levels are now independent of the output power. Changes in the required power level drive the SNSFB regulation.

Table 1. TEA19161T (PFC) pins*...continued*

Pin	Pin name	Functional description summary
3	SNSOUT	Input for indirect sensing the output voltage of the resonant converter cycle-by-cycle To set the burst repetition frequency, the resistor value to GND (R_{SNSOUT}) is measured and stored at start-up. When R_{SNSOUT} < 1.5 kΩ, start-up is disabled. The peak voltage is measured during each positive half cycle. When SNSOUT exceeds 3.5 V during 11 cycles with a minimum time of 75 µs, a latched overvoltage protection is triggered. The CT-versions are safe restart versions. This pin contains a small current source of 50 nA for open-pin detection that pulls the voltage to OVP in this fault condition.
4	GND	Ground Reference for GATELS driver and measurement inputs.
5	SUPREG	Output of the internal voltage regulator: 11 V SUPREG can provide a minimum current of 30 mA. The supply made with this function is used for: • GATELS • SUPHS with bootstrap • Reference voltage for optional external circuit SUPREG is charged along with SUPIC. UVP: If the voltage on the SUPREG pin drops to below 9 V, the IC stops operating.
6	GATELS	Gate driver output for low-side MOSFET of the HBC
7	n.c.	Do not connect; high-voltage spacer
8	SUPHV	High-voltage supply input for the HV start-up source A series resistor (24 kΩ typical) must be connected as part of the HV source function. The HV source charges the SUPIC pin to the start level of 19.1 V. It regulates the SUPIC pin with a hysteresis of 0.7 V. When the voltage on the SUPIC pin drops to below 3.5 V, the current is limited to 0.75 mA to limit the power if there is a SUPIC short circuit. During the non-switching period in burst mode, the HV source is activated when the SUPIC voltage drops to 14 V. To avoid that the system stops during a long period of non-switching, the HV source regulates the voltage on the SUPIC pin with a hysteresis of 0.9 V when it drops to below 14 V.
9	GATEHS	Gate driver output for high-side MOSFET of HBC
10	SUPHS	High-side driver supply connected to an external bootstrap capacitor between HB and SUPHS The supply is obtained using an external diode between the SUPREG and SUPHS pins.
11	HB	Reference for the high-side driver GATEHS HB is externally connected to a half-bridge node between the MOSFETs of HBC. It is an input for the internal half-bridge slope dV/dt detection circuit for adaptive non-overlap regulation and top switching in LP mode.
12	n.c.	Do not connect; high-voltage spacer
13	SNSSET	Pin for settings and power good (PG) signal Two resistor values are measured and stored at start-up. They provide settings for: • Transition levels HP/LP mode • LP/BM • OPP level • OPP timeout • Restart or latched protection After measuring the settings, the pin provides an output for a PG signal. This signal shows the status of stable operation after start-up. It provides a warning that the supply is about to shut down.

Table 1. TEA19161T (PFC) pins*...continued*

Pin	Pin name	Functional description summary
14	SNSCUR	Sense input for the momentary primary current of the HBC using a voltage across and external measurement resistor. To avoid disturbance, a series capacitor placed very close to the pin applies the voltage signal. The IC biases the DC voltage on the pin to 2.5 V. Internal voltage levels are: • If $V_{SNSCUR} - V_{BIAS} > \pm 1.5$ V, the gate driver is switched off to limit the power to the OCP level. After 8 OCP cycles, a latched protection is activated. The CT-version are safe restart versions. • $V_{SNSCUR} - V_{BIAS} = \pm 100$ mV level for detecting the (almost) zero current level. To prevent capacitive mode switching, the driver switches off at this level. • $V_{SNSCUR} - V_{BIAS} = \pm 13$ mV for detecting the current polarity. Used as a parameter in the internal switching logic.
15	SNSCAP	Senses the voltage on the HBC capacitor for driving the correct output power The SNSCAP pin is externally connected to a resistive and a capacitive divider to the voltage on the resonant capacitor. An internal bias circuit generates a 2.5 V DC level on SNSCAP. The divider scales the voltage levels on the resonant capacitor for the power level control range from 0 % to 200 % to the maximum SNSCAP voltage range of 1 V to 4 V. The scaling includes input voltage compensation. The scaling sets the correct levels for: • Transition level HP/LP • Minimum energy per cycle (ECmin) • OPP level • 200 % power level For each half cycle, the internal power control sets a new target SNSCAP voltage level for switching off the HBC MOSFET to reach the required power. It is based on: • SNSFB current (feedback regulation) • SNSBOOST voltage (input voltage compensation) • Mode transition control • Slope compensation (power reduction during start-up and protection) • HB symmetry regulation
16	SNSBOOST	This pin combines three functions. The boost voltage is sensed for: • Brownin and brownout of the HBC • HBC input voltage compensation Adapting the V_{cap} levels to keep a constant output power level at varying input voltages. • Communication between the TEA19161 and TEA19162 via internal current sources The SNSBOOST pin is externally connected to a resistive divided boost voltage. The resistor from SNSBOOST to GND must be 100 kΩ. To ensure the intended functionality, the parallel capacitor must be ≤ 4.7 nF. The pin uses three voltage levels: • Fast latch reset level: 2 V: For generating a fast latch reset in the TEA19161, the TEA19162 pulls high the pin level using a −210 µA current source. • At 2.3 V: The HBC starts operation because the boost voltage is high enough (brownin). • At 1.6 V: The HBC stops operation because the boost voltage is too low (brownout) The voltage levels on SNSBOOST are operated by: • External resistive divider of the boost voltage • Current sources in the TEA19162: +200 µA and −100 µA • Current sources in the TEA19161: +5 µA, +30 µA, and −100 µA

3.2 TEA19162T (PFC) pin overview

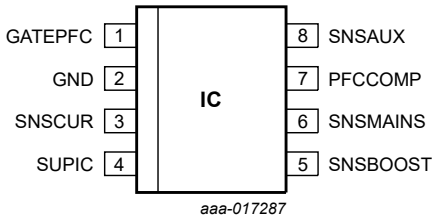


Figure 2. TEA19162T pinning diagram

Table 2. TEA19162T (PFC) pins

Pin	Pin name	Functional description summary
1	GATEPFC	Gate driver output for PFC MOSFET
2	GND	Ground Reference for PFC driver and measurement points.
3	SNSCUR	Current sense input for PFC This input is used to limit the maximum peak current in the PFC core. The current sense input is a cycle-by-cycle protection. When the SNSCUR level reaches 500 mV, the PFC MOSFET is switched off. The external sense resistor value determines the current value. Internally, a soft start function limits the peak current to 135 mV at the first cycle. During the soft start time, the peak current limit is gradually increased. It reaches the nominal value of 500 mV after 3.75 ms. For the X-capacitor discharge function there are two detection levels: • 10 mV: Maximum level of the discharge current pulse during X-capacitor discharge. • 50 mV: Detection level for ending the X-capacitor discharge function (mains voltage reconnected)
4	SUPIC	IC voltage supply input Connected to the SUPIC pin (pin 1) of the TEA19161. For start-up, the SUPIC pin can be charged or supplied in several ways: • High-voltage (HV) start-up source in the TEA19161 • Auxiliary winding from the HBC transformer or capacitive supply from the switching half-bridge node • External DC supply, for example, a standby supply When the SUPIC voltage reaches the start level of 13 V, the IC is activated. During system start-up, the TEA19161 pulls down the SNSBOOST pin of the TEA19162. In this way, the start of both controllers is synchronized. When the voltage on the SUPIC pin drops to below 9 V, the IC stops operation. A SUPIC system latch reset function is supported on the TEA19161.

Table 2. TEA19162T (PFC) pins*...continued*

Pin	Pin name	Functional description summary
5	SNSBOOST	This pin combines two functions: • It senses the boost voltage for regulation (output voltage of the PFC stage). • It is used for communication between the TEA19161 and TEA19162 via internal current sources. The SNSBOOST pin is externally connected to a resistive divided boost voltage. The resistor from SNSBOOST to GND must be 100 kΩ. To ensure the intended functionality, the parallel capacitor must be ≤ 4.7 nF. The SNSBOOST pin uses seven voltage levels: • Short-pin or open-pin detection using an internal −35 nA current source: $V_{scp(stop)}$ = 0.4 V and $V_{scp(start)}$ = 0.5 V. If a protection is triggered or before start-up, the TEA19161 also uses this function is to disable the IC. • Fast latch reset level: 2 V: To generate a fast latch reset in the TEA19161, the pin level is pulled high by a 200 µA internal current source of the TEA19162. • Regulation of the PFC output voltage in burst mode by the TEA19161: Soft start at 2.4 V and soft stop at 2.5 V. • Control of the burst mode by TEA19161: Soft start at 2.4 V; soft stop at 2.5 V. • Regulation of the PFC output voltage in normal operation: $V_{reg(SNSBOOST)}$ = 2.5 V • The pin voltage varies between 2.8 V and 3.23 V in the burst stop state of the burst mode operation of the TEA19161. • PFC OVP (cycle-by-cycle): $V_{OVP(SNSBOOST)}$ ≥ 2.63 V (after a delay of 100 µs) The voltage levels on the SNSBOOST pin are influenced by: • External resistive divider connected to the boost voltage • Current sources in the TEA19162: −210 µA; +35 nA; +100 µA • Current sources in the TEA19161: −6.4 µA; +30 µA; +110 µA
6	SNSMAINS	This pin combines two functions. The functions are alternately active in time during the same half-mains voltage cycle. **Mains voltage sensing** During the mains voltage sensing, the SNSMAINS pin is clamped to 0.25 V. The clamping of the SNSMAINS pin prevents that current leaks through the OTP network. There is no interference of the mains voltage measurement. For mains sensing, the current flowing in the SNSMAINS pin is measured. The current depends on the external resistor value (typical 20 MΩ). The mains voltage determines the amount of current. During a half-mains voltage cycle, the peak current value is determined and stored. The value is used as an input for: • The mains compensation function of the PFC regulation loop • The brownin and brownout functions The SNSMAINS current level is sensed continuously until the current level drops below 2.5 µA. Then, the external temperature measurement starts. At a current level of 5.75 µA, the brownin level is reached and the IC starts switching. When the current drops again to below 5 µA, the brownout level is reached and the IC switching stops. When, after brownout, the brownin level is reached again, the latched protection state is reset. If during 120 ms no positive dV/dt is detected, the X-capacitor discharge function is triggered. To reconnect the mains, the current on the SNSMAINS pin is monitored during the X-capacitor discharge mode.

Table 2. TEA19162T (PFC) pins*...continued*

Pin	Pin name	Functional description summary
6 (continued)	SNSMAINS	**External NTC overtemperature protection (OTP)** The OTP measurement lasts maximum 1 ms. During this time, a 200 µA current flows from the pin through the external diode and NTC to ground. The resulting voltage on the pin is measured. When the voltage on the pin < 2 V at four consecutive measurement half-cycles, the OTP protection is activated.
7	PFCCOMP	Frequency compensation for the PFC control-loop. Externally connected filter with typical values: 150 nF // (33 kΩ + 470 nF). The voltage on PFCCOMP is used to generate a soft stop behavior.
8	SNSAUX	Sense input from an auxiliary winding of the PFC coil for: • Demagnetization timing • Valley detection to control the PFC switching It is a −90 mV level with a timeout of 44.5 µs. To prevent damage of the input during surges (for example, lightning), the auxiliary winding must be connected to the pin via an impedance (recommended is a 5.1 kΩ series resistor). The open-pin detection uses an internal pull-up current source.

4 Application diagram

4.1 TEA19162

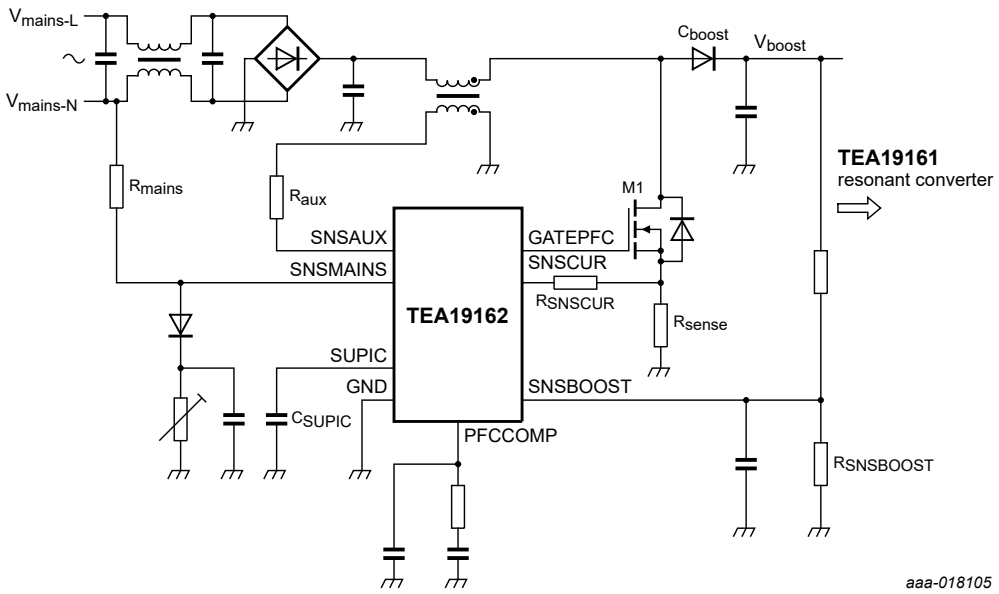


Figure 3. TEA19162 application diagram

4.2 TEA19161T

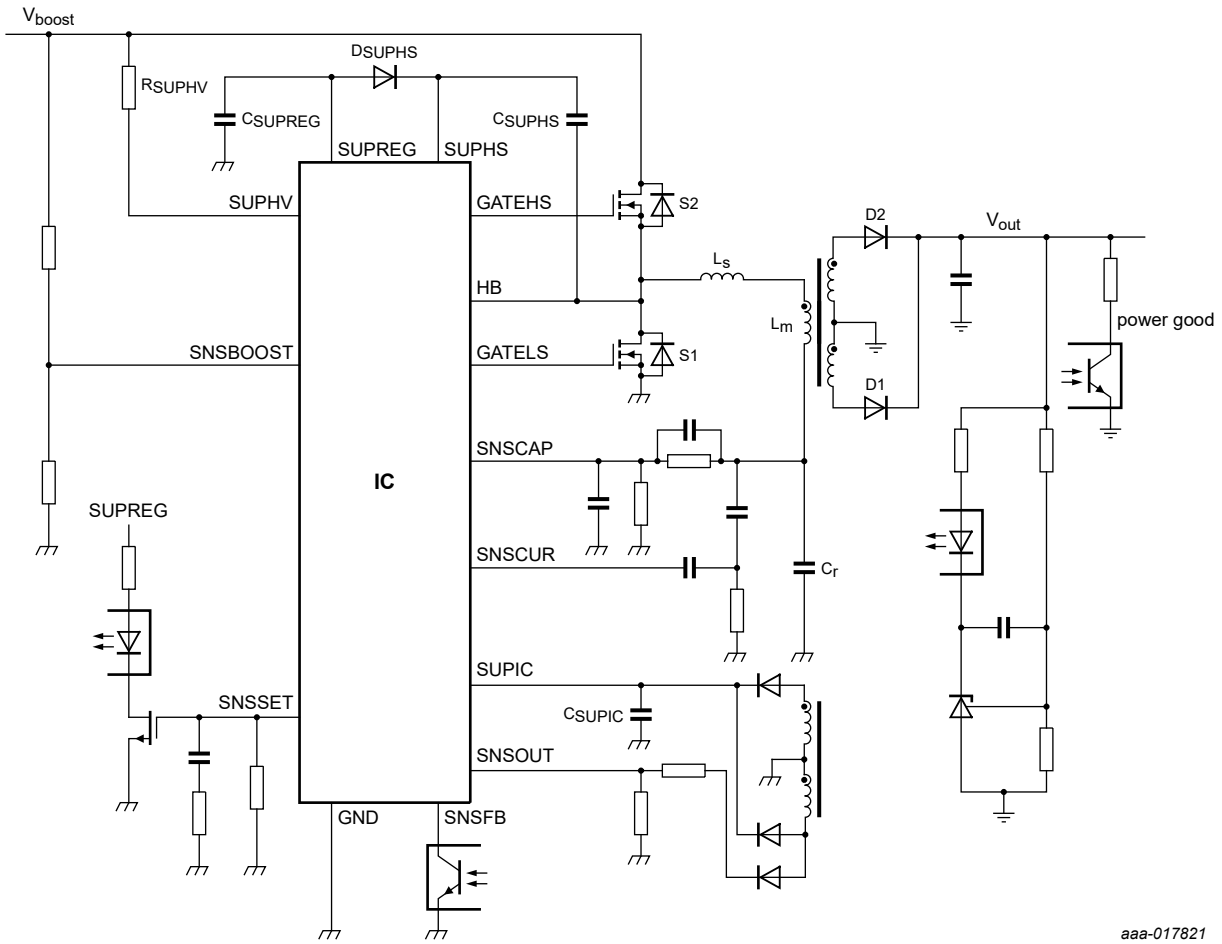


Figure 4. TEA19161T application diagram

5 Block diagram

5.1 TEA19162T

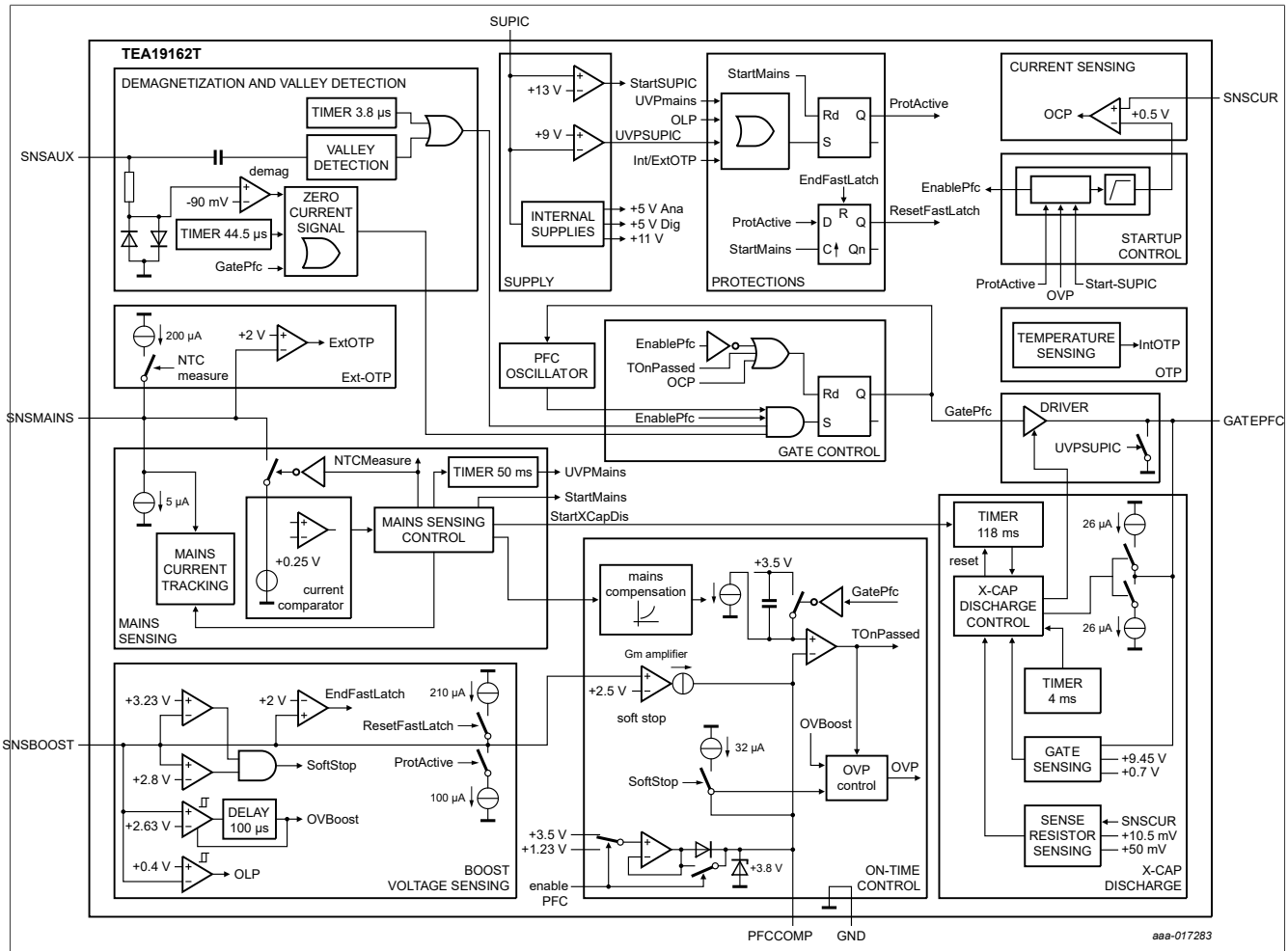


Figure 5. TEA19162T block diagram

5.2 TEA19161T

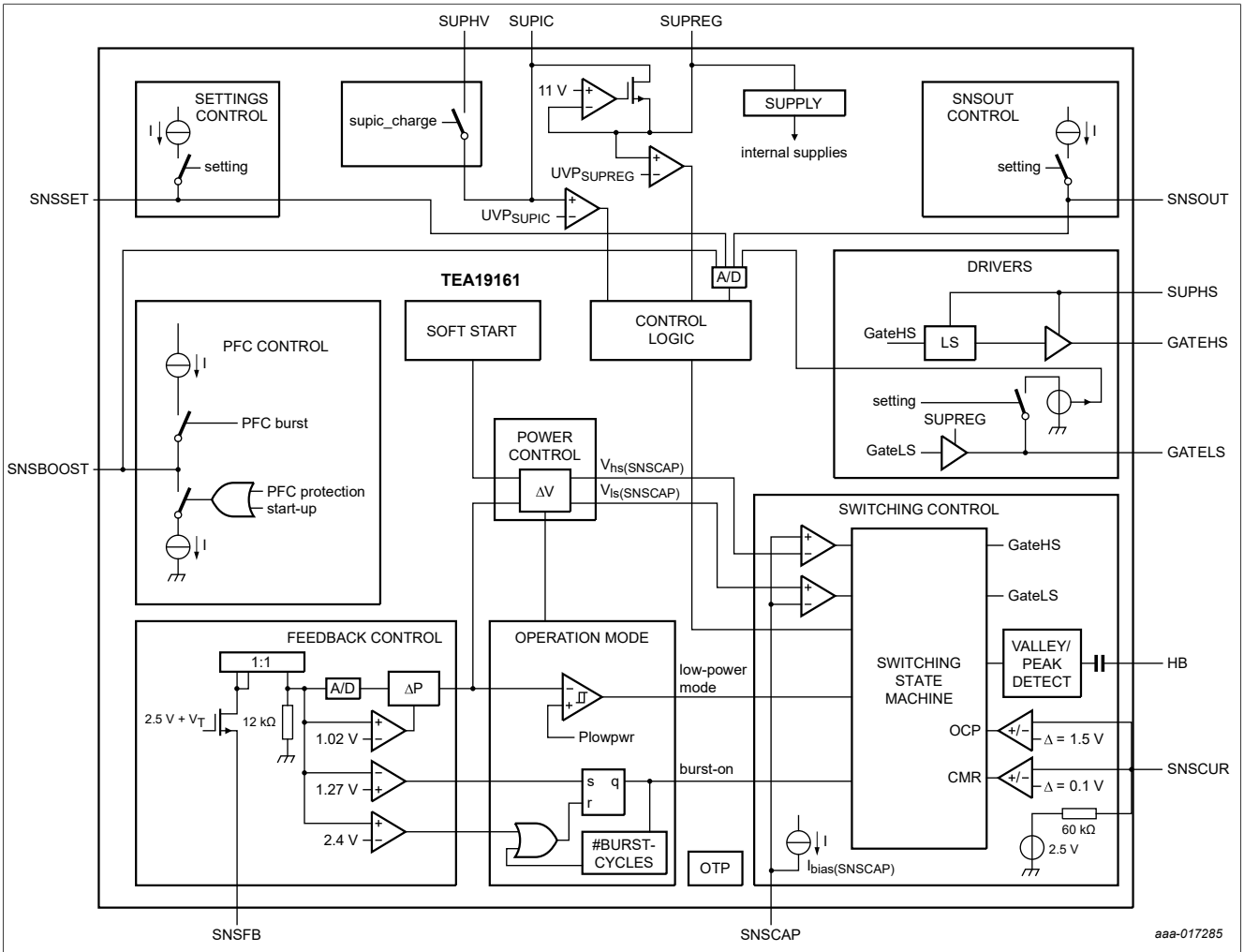


Figure 6. TEA19161T block diagram

6 Supply functions and start-up

6.1 Basic supply system overview

The TEA19161 has a high-voltage supply pin for start-up (SUPHV), a general supply (SUPIC), and an accurate regulated voltage output (SUPREG).

The SUPIC function can be used to supply the TEA19162 PFC controller IC. Start-up and protection levels are optimized to work as one system.

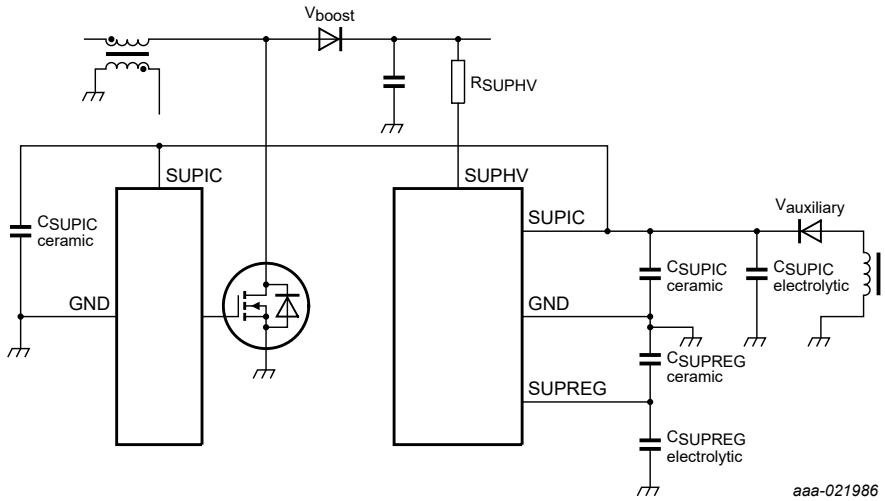


Figure 7. TEA1916 basic IC supply application

6.2 SUPHV high-voltage supply

To provide the SUPHV start-up source, the TEA19161 uses an external resistor. In this way, a high start-up current can be provided without too much power dissipation in the IC. It reduces the size of the IC die for low-cost design. Most of the power during start-up is located in the external resistor. To provide a start-up of approximately 0.5 s and generate sufficient MOSFET drive current during start-up, R_{SUPHV} is typical 24 kΩ. The value of the mains voltage influences the behavior.

To handle the power during start-up and potential fault conditions, the external resistor R_{SUPHV} must be selected. To handle the high voltage level in most applications, R_{SUPHV} can include several SMD resistors in series.

If there is a latched protection and an off-state, the SUPHV pin also provides the IC supply.

6.2.1 Start-up via the SUPHV pin

Initially, the SUPHV source charges the capacitors on the SUPIC and SUPREG pins. The SUPHV pin is connected to V_{boost}. In the TEA19161, a high-voltage series switch is located between the SUPHV and SUPIC pins. From the SUPIC pin, an internal linear regulator supplies the SUPREG pin.

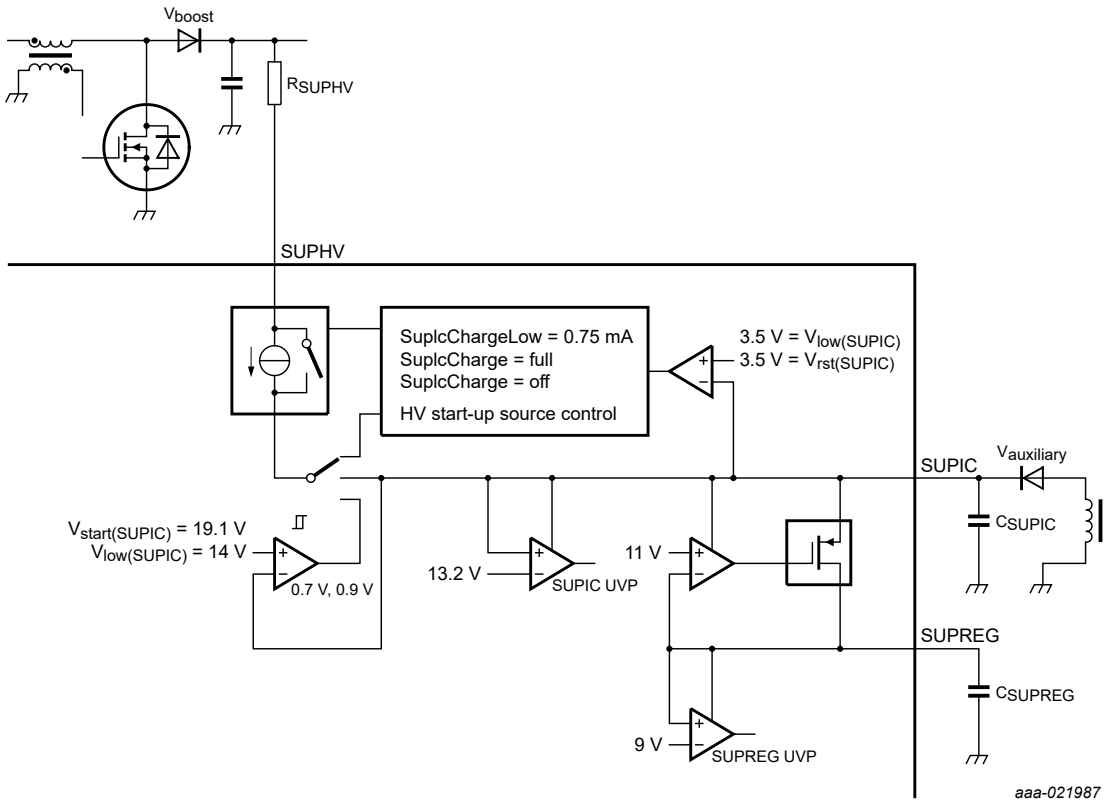


Figure 8. TEA19161 SUPHV, SUPIC, and SUPREG supply system

The SUPIC pin charge current is limited to 0.75 mA until the voltage on the SUPIC pin reaches 3.5 V. When the voltage on the SUPIC pin exceeds 3.5 V, the V_{boost} voltage and the external resistor R_{SUPHV} determine the charge current. However, to handle the power dissipation in the IC, the value of external resistor R_{SUPHV} must limit the current to < 20 mA.

When the SUPIC reaches the 19.1 V start-up level, it is continuously regulated to this level with a hysteresis of 0.7 V. When the voltage on the SUPIC pin drops to below 19.1 V − 0.7 V = 18.4 V, the switch between the SUPHV and SUPIC pins is activated.

When start-up is completed, regulation of the voltage on the SUPIC pin is ended. When the current taken from the SNSFB pin exceeds 63 µA, it ends the start-up operation.

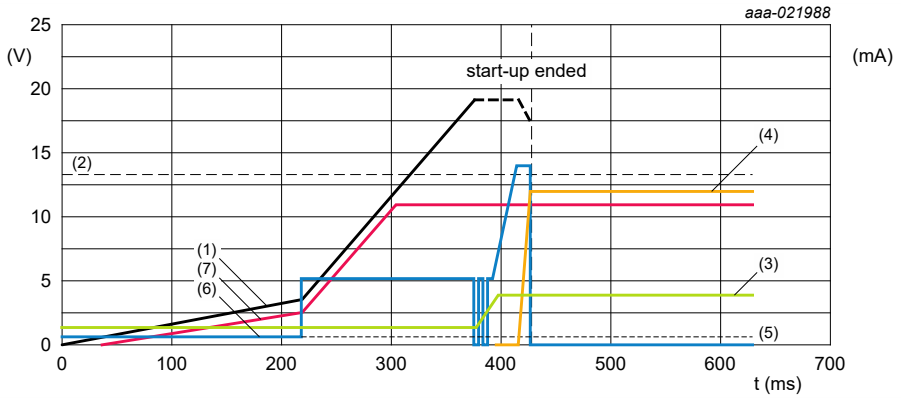
During start-up, several other tasks are done:

- To ensure that the TEA19162 does not start operating before the complete system is ready for start-up, TEA19161 pulls low the voltage on the SNSBOOST pin.
- When the voltage on the SUPIC pin has reached the 19.1 V start-up level, the TEA19161 first reads all settings on the SNSOUT, GATELS, and SNSSET pins. When the reading of the settings is done, the voltage on the SNSBOOST pin is no longer pulled low. It is released.
- Before start-up is enabled, several signal levels are checked:
  - The bias voltage on the SNSCUR and SNSCAP pins
  - The voltage on the SNSBOOST pin must exceed 2.3 V
  - Other protection levels

When the SUPIC voltage is very low, the IC current consumption is zero. At about 1.5 V, some internal circuits become active and, when the voltage increases, the current increases.

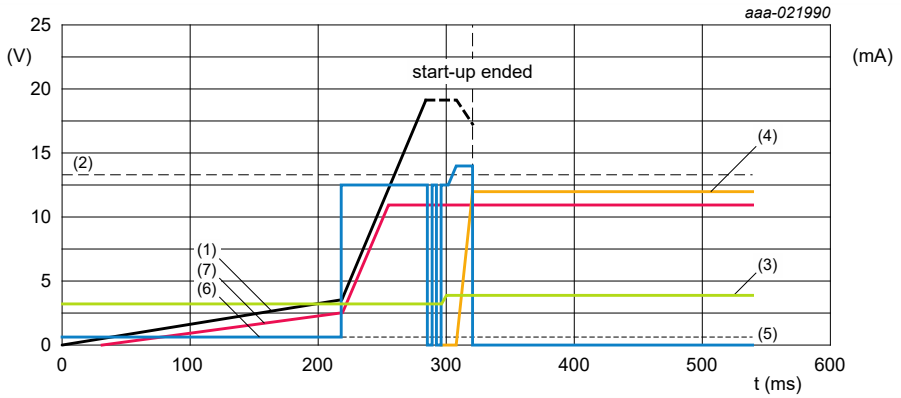
On average, when the SUPIC voltage is stable, the SUPIC current is approximately 3 mA for the TEA19161 and the TEA19162 ICs.

During SUPHV charging, approximately 3 mA flows into the IC circuits. The rest of the SUPHV current charges the SUPIC capacitors and the SUPREG capacitors up to 11 V.



- (1) SUPIC voltage
- (2) SUPIC UVP (V)
- (3) PFC output / 100 (V)
- (4) HBC output voltage
- (5) Low start-up current
- (6) HV source (mA)
- (7) SUPREG voltage

Figure 9. Typical start-up sequence (V_{mains} = 100 V (AC))



- (1) SUPIC voltage
- (2) SUPIC UVP (V)
- (3) PFC output / 100 (V)
- (4) HBC output voltage
- (5) Low start-up current
- (6) HV source (mA)
- (7) SUPREG voltage

Figure 10. Typical start-up sequence (V_{mains} = 230 V (AC))

6.2.2 SUPHV pin during burst mode operation

When the SUPIC voltage temporarily drops to a low value during burst mode, the SUPHV source can be activated. The voltage drop can happen, for example, when there is a long period of non-switching after a load step. In this situation, the supply from the auxiliary winding does not generate energy for a long time, while the IC still takes a low amount of current.

When the SUPIC voltage drops to 14 V during the non-switching period of the burst mode, the HV source is activated. The SUPHV source regulates the SUPIC voltage between 14 V and 15 V. This emergency function prevents that the system stops and restarts because of an accidental condition. It triggers the SUPIC UVP level at 13.2 V.

6.2.3 R_{SUPHV} value for protection mode

The resistance value of R_{SUPHV} must not be too high because the IC requires 3.7 mA (worse case for TEA19161) + 0.2 mA (worse case for TEA19162) during a latched protection condition. To prevent that SUPIC drops and causes a latch reset, the SUPHV source must be able to deliver it.

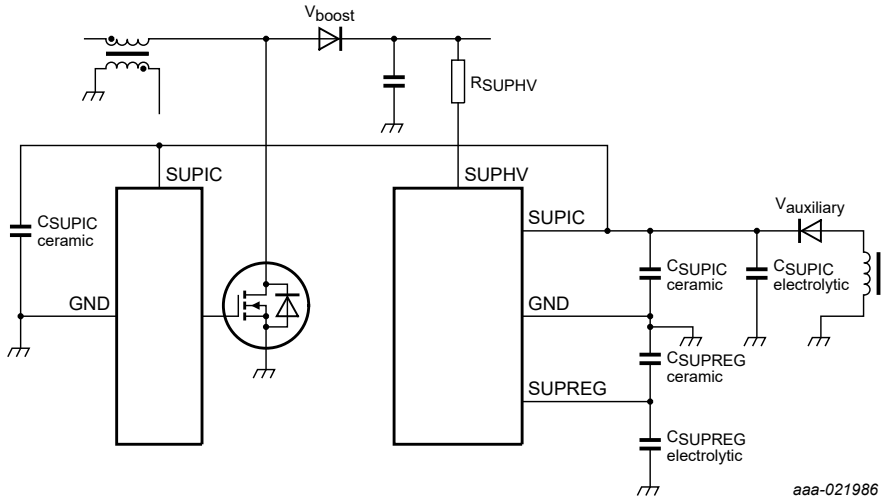


Figure 11. TEA1916 basic IC supply application

Estimation of power in R_{SUPHV} during protection with example values:

- $I_{prot(SUPIC)}$ = 3.7 mA (TEA19161) + 0.2 mA (TEA19162) = 3.9 mA
- V_{boost} = 120 V (rectified mains voltage at 85 V (AC))
- V_{SUPIC} = 19 V
- $R_{SUPHV,max}$ = (120 V − 19 V) / 3.9 mA = 25.9 kΩ

6.2.4 SUPHV during protection

SUPHV supplies SUPIC during a latched protection state or a safe restart state. It regulates SUPIC between 19.1 V and 18.4 V by switching on/off the SUPHV supply.

During this state, resistor R_{SUPHV} dissipates the power that can be calculated with the voltage drop and the average amount of current that is used by the TEA1916 ICs during that state. Figure 115 shows that four 1206-type SMD resistors are used for the R_{SUPHV} function to handle the voltage and the power during protection.

Estimation of power in R_{SUPHV} during protection with example values:

- $I_{prot(SUPIC)}$ = 3.7 mA (TEA19161) + 0.2 mA (TEA19162) = 3.9 mA
- V_{boost} = 380 V
- V_{SUPIC} = 19 V
- P_{RSUPHV} = (380 V − 19 V) × 3.9 mA = 1.4 W

6.3 SUPIC supply using HBC transformer auxiliary winding

To obtain a supply voltage for the SUPIC pin during operation, an auxiliary winding on the HBC transformer can be used. As the SUPIC pin has a wide operational voltage range (13.2 V to 36 V), it is not a critical parameter.

However:

- To minimize power consumption, the voltage on the SUPIC pin must be low.
- During burst mode operation and because of the low current consumption of the supply, the repetition frequency of the burst can become very low (for example, at no output load). This behavior can cause an imbalance in the half-bridge switching, leading to a serious drop in the auxiliary supply for the SUPIC pin. To maintain the HBC load balance and avoid the extra SUPIC pin voltage drop, replace a single-side rectified auxiliary supply with a center-tapped construction. The center-tapped construction consists of two windings and two diodes.
- To use the auxiliary winding voltage for the IC supply and for HBC output voltage measurement (using SNSOUT), the auxiliary winding supply must be an accurate representation of V_O. To ensure a good coupling, place the transformer auxiliary winding physically on the secondary output side. When the transformer contains separate sections for primary and secondary winding (see Figure 12 and Figure 13), this aspect is more critical than on transformers that have all windings in one section.
- When mains insulation is included in the transformer, it can affect the auxiliary winding construction. When the transformer auxiliary winding is placed on the transformer construction secondary area, triple insulated wire is required.

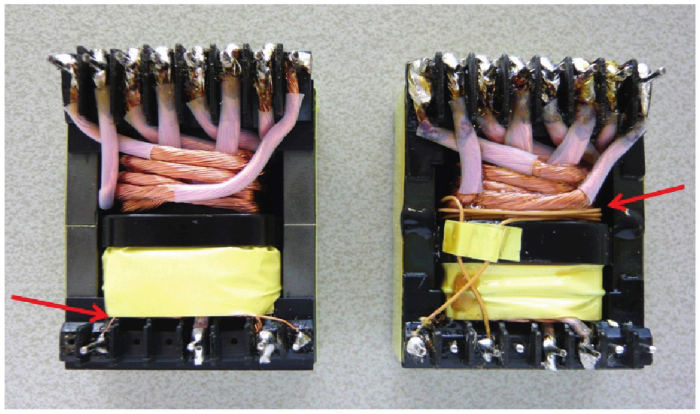


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Figure 12. Transformer auxiliary winding on primary side (left, not preferred) and secondary side (right)

In a combined SUPIC and SNSOUT function using a transformer auxiliary winding, a good representation of the output voltage for SNSOUT measurement can only be obtained after addressing several issues.

The advantage of a good coupling/representation of the auxiliary winding with the output windings is that a stable auxiliary voltage is obtained for the SUPIC pin. A low voltage on the SUPIC pin can be designed more easily for the lowest power consumption.

6.3.1 Auxiliary winding on the HBC transformer

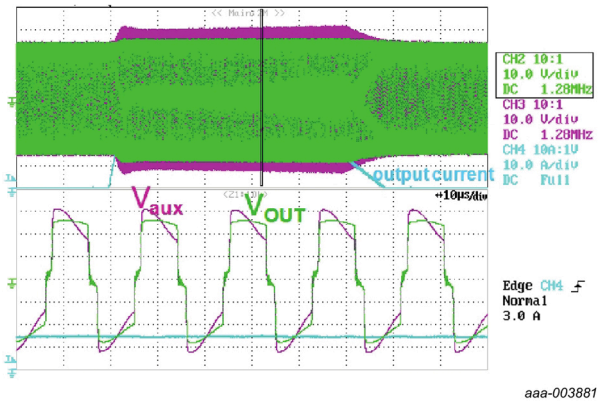
The HBC output causes variation on an auxiliary winding supply. At peak current loads, the regulation compensates the voltage drop across the series components in the HBC output stage (resistance and diodes). The result is a higher voltage on the windings at higher output currents, because the higher currents cause a greater voltage drop across the series components.

In burst mode operation near no load, the number of pulses in time that charge the SUPIC pin in time is limited. To prevent that the voltage drop severely, the rectifiers used in the auxiliary supply must be able to handle the high currents.

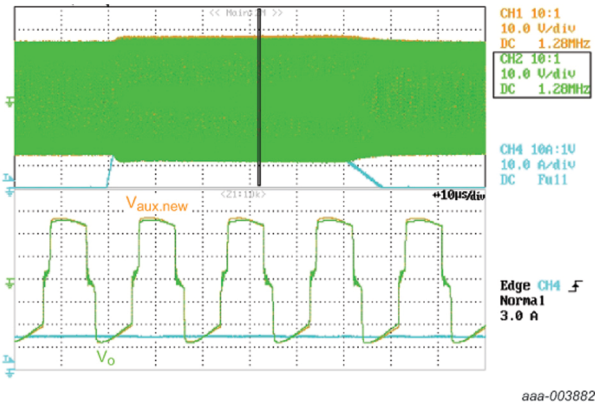
6.3.2 Voltage variations depending on auxiliary winding position: Primary side component

V_{SNSOUT} and/or V_{SUPIC} can contain unwanted primary voltage because of the less optimal position of the auxiliary winding. When the transformer contains separate sections for primary and secondary winding (see type in Figure 12 and Figure 13), this aspect is more critical than on transformers that have all windings in one section. This deviation can seriously endanger the feasibility of the SNSOUT sensing function. It can also have a serious effect on the SUPIC voltage.

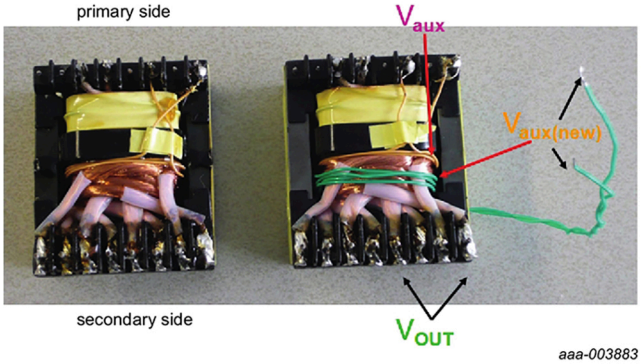
To avoid a primary voltage component on the auxiliary voltage, the coupling of the auxiliary winding with the primary winding must be as small as possible. Place the auxiliary winding on the secondary windings and physically as remote as possible from the primary winding. Figure 13 shows the differences in results using comparison of the secondary side position.



a. Bad coupling V_{aux} to V_{out} at high output current



b. Correct coupling V_{aux} to V_{out} at high output current



c. Example photograph

Figure 13. Example of a (new) position of the auxiliary winding for a better coupling to the output voltage

6.4 SUPIC pin supply using external voltage

When the SUPIC pin is supplied using another (standby) power supply, the SUPHV pin can be left unconnected. The SUPIC start-up level remains 19.1 V. The UVP level is 13.2 V.

6.5 SUPREG pin

The SUPIC pin has a wide voltage range for easy application. However, it cannot be used to supply the internal MOSFET drivers directly because the allowed gate voltage of many external MOSFETs is exceeded.

To avoid this issue and to create a few other benefits, the TEA1916 incorporates an integrated series stabilizer. The series stabilizer generates an accurately regulated voltage on the external buffer capacitor of the SUPREG pin.

The stabilized SUPREG voltage is used for:

- Supply of the internal low-side HBC driver
- Supply of the internal high-side driver using external components
- Supply for several internal circuits
- Reference voltage for optional external circuits
- Supply voltage for optional external circuits

The series stabilizer for the SUPREG pin is charged along with the SUPIC pin. To enable HBC operation, the SUPREG voltage must reach the regulation level of 11 V.

The SUPREG pin can provide a maximum total current of at least 30 mA.

It is important to realize that the SUPREG pin can only source current.

The drivers of GATELS and GATEPFC are supplied using the SUPREG pin. Depending on the operating condition, they draw current from it during operation. Depending on current load and temperature, small changes in value can be expected.

6.5.1 SUPREG supply for external circuit

The stabilized voltage source, SUPREG, can be used to supply an external circuit or as a reference voltage for external circuits.

The SUPREG function can deliver at least 30 mA. However, a part of this current is used for internal functions, like the GATELS driver. It is also used for the bootstrap function to supply SUPHS.

Usually, an external circuit on SUPREG only requires a few mA. If the current needed for SUPREG is substantial, the thermal condition of the IC can become critical and must be checked.

To check the thermal aspects, the power dissipation in the IC must be estimated.

Example: GATELS and GATEHS (driving a total of two MOSFETs):

$$\Delta I_{SUPREG\_MOSFETS} = 2 \times Q_{gate} \times f_{bridge} \quad (1)$$

- Q_{gate} = 40 nC
- f_{bridge} = 100 kHz

$$\Delta I_{SUPREG\_MOSFETS} = 2 \times 40\,nC \times 100\,\text{kHz} = 8\,mA$$

Note: *Generally, The calculated value is higher than the practical value, because the switching operation deviates from the MOSFET specification for Q_{gate}.*

The total current available from SUPREG is a minimum of 30 mA. To determine how much current is available for an external circuit, it must be known how much the IC is using.

$$I_{SUPREG\_external\_max} = 30\ mA\ - I_{SUPREG\_IC} \quad (2)$$

Regarding the IC, the MOSFET drivers GATELS and GATEHS consume most current from SUPREG by far. Other circuit parts in the IC consume approximately 3 mA during normal mode operation.

$$I_{SUPREG\_IC} = I_{SUPREG\_MOSFETS} + I_{SUPREG\_for\_other\_IC\text{-}circuits} \quad (3)$$

$$I_{SUPREG\_IC} = I_{SUPREG\_MOSFETS} + 3\ mA$$

$I_{SUPREG\_MOSFETS}$ can be estimated by the method provided. Using the example value:

$$I_{SUPREG\_IC} = 8\ mA + 3\ mA = 11\ mA$$

$$I_{SUPREG\_external\_max} = 30\ mA\ - 11\ mA = 19\ mA$$

6.6 SUPHS pin

An external bootstrap buffer capacitor supplies the high-side driver. The bootstrap capacitor is connected between the high-side reference the HB pin and the high-side driver supply input the SUPHS pin. When HB is low, an external diode from the SUPREG pin charges this capacitor.

Selecting a suitable external diode can minimize the voltage drop between the SUPREG and SUPHS pins. Minimizing the voltage drop is important when using a MOSFET that requires a large amount of gate charge and/or when switching at high frequencies.

Note: *The current drawn from the SUPREG pin to charge C_{SUPHS}, differs (in time and shape) from the current that the GATEPFC and GATELS drivers draw for each cycle.*

6.6.1 Initial charging of the SUPHS pin

To charge C_{SUPHS} using the bootstrap function, the GATELS switches on the low-side MOSFET at start-up.

The current taken from the SUPHS pin consists of two parts:

- Internal MOSFET driver GATEHS
- Internal circuit to control the GATEHS pin

6.6.2 A lower voltage SUPHS pin

Each time the half-bridge node (HB) is switched to ground level during normal operation, the bootstrap function charges C_{SUPHS}. The voltage value between the HB and SUPHS pins is normally lower than the voltage on the SUPREG pin (or other bootstrap supply input) because of the voltage drop across the bootstrap diode.

The voltage drop across the bootstrap diode is directly related to the amount of current that is required to charge C_{SUPHS}. The resulting voltage between the SUPHS and HB pins also depends on the available charge time.

When an external MOSFET with a large gate capacitance must be switched at high frequency (high current + short time), a large voltage drop occurs.

During burst mode operation, voltages that are low or even too low can occur on the SUPHS pin. In burst mode, there are (long) periods of not switching. So, long periods during which the SUPHS pin is not charged can occur. During this time, the circuit C_{SUPHS} slowly discharges the supply voltage capacitor. When a new burst starts, the voltage on the SUPHS pin is lower than during normal operation. During the first switching cycles, C_{SUPHS} is recharged to its normal level. At low output power during burst mode, the switching frequency is usually relatively high. The high switching frequency limits fast recovery of the voltage between the SUPHS and HB pins.

Although in most applications the voltage drop is limited, it is an important issue for evaluation. The voltage drop can influence the selection of the best diode type for the bootstrap function. It can also influence the value of the SUPHS pin buffer capacitor.

When the voltage across C_{SUPHS} drops to below 7 V, the driver stops operation to prevent unreliable switching.

6.7 Capacitor values on the SUPIC, SUPREG, and SUPHS pins

Section 15 gives an example of a practical application (240 W power supply).

6.7.1 SUPIC pin

Because the TEA19161 and TEA19162 are combined, the SUPIC functions are also combined.

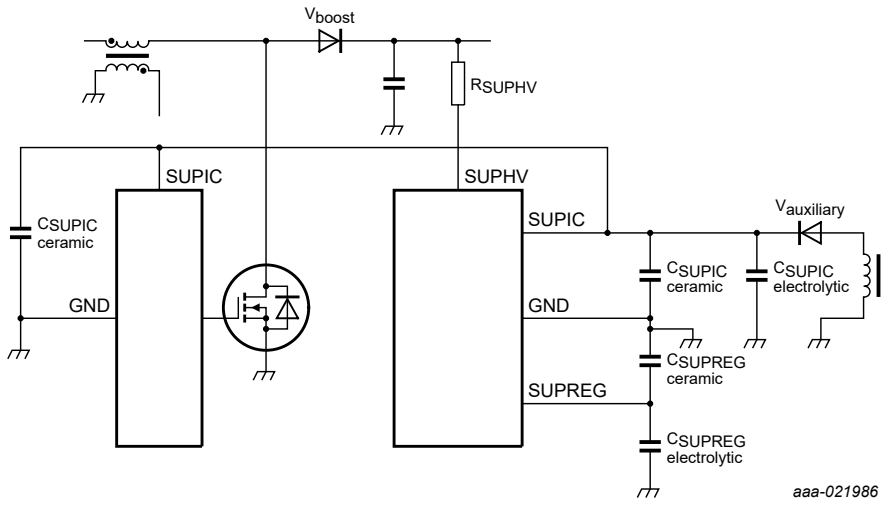


Figure 14. TEA1916 basic IC supply application

6.7.1.1 General

Use two types of capacitors on the SUPIC pin. An SMD ceramic type with a smaller value located close to both ICs and an electrolytic type incorporating the major part of the capacitance.

Typical values are:

- Electrolytic: C_{SUPIC} = 47 µF
- Ceramic capacitor near pin 1 of the TEA19161: C_{SUPIC} = 470 nF
- Ceramic capacitor near pin 4 of the TEA19162: C_{SUPIC} = 100 nF

6.7.1.2 Start-up

When an HV source provides the start-up energy, the SUPIC capacitor value can be small. However, it must be sufficient to handle the start-up during the 12 ms period between the start of the HBC pin and the auxiliary winding taking over the supply of the SUPIC pin.

Example of the basic value estimation:

- $I_{SUPIC\_start\_HBC}$ = 25 mA
- $\Delta V_{SUPIC(startup)} = V_{start(SUPIC)} - V_{uvp(SUPIC)}$ = 19.1 V − 13 V = 5.9 V
- Δt_{vaux} > 13 V = 12 ms
  12 ms is the time it takes for V_{aux} to exceed 13 V.
- $V_{boost(nom)}$ = 390 V
- R_{SUPHV} = 24 kΩ

$$I_{SUPHV\_start\_HBC} = \frac{V_{boost(nom)} - V_{SUPIC(startup)}}{R_{SUPHV}} \quad (4)$$

Example:

$$I_{SUPHV\_start\_HBC} = \frac{390\ V - 19.2\ V}{24\ k\Omega} = 15.45\ mA$$

$$C_{SUPIC} = \left(I_{SUPC\_start\_HBC} - I_{SUPHV\_start\_HBC}\right) \times \frac{\Delta t_{vaux}}{\Delta V_{SUPIC(startup)}} \quad (5)$$

Example:

$$C_{SUPIC} = \left(25\ mA - 15.45\ mA\right) \times \frac{12\ ms}{5.9\ V} = 20\ \mu F$$

6.7.1.3 Normal operation

The main purpose of the capacitors on the SUPIC pin is to keep the current load variations (for example, gate drive currents) local at normal operation.

6.7.1.4 Burst mode operation

When burst mode operation is applied, the supply construction often uses an auxiliary winding and start-up from the HV source. While in the burst mode, there is a long period during which the auxiliary winding is not able to charge C_{SUPIC}. There is no HBC switching time between two bursts. The capacitor value on SUPIC must be high enough to keep the voltage above 13.2 V to prevent activating the SUPIC undervoltage stop level.

For efficiency reasons, it must also prevent that the SUPHV source is activated at 14 V.

Example of a value estimation:

$$I_{SUPIC\_between\_2\_burst} = 1\ mA \quad (6)$$

$$\Delta V_{SUPIC\_between\_2\_bursts} = V_{aux(burst)} + V_{low(SUPIC)} = 19\ V - 14\ V = 5\ V$$

$$\Delta t_{between\_2\_bursts} = 40\ ms \quad (7)$$

$$C_{SUPIC} > I_{SUPIC\_between\_2\_bursts} \times \frac{\Delta t_{between\_2\_bursts}}{\Delta V_{SUPIC(burst)}} = 1\ mA \times \frac{40\ ms}{5\ V} = 8\ \mu F$$

6.7.2 Value of the capacitor for the SUPREG pin

SUPREG is the supply for the current of the HBC MOSFET drivers. Keeping current peaks local can be achieved using an SMD ceramic capacitor supported by an electrolytic capacitor. Keeping current peaks local is necessary to provide sufficient capacitance to prevent voltage drop during high current loads. To prevent significant voltage drop, the value of the capacitor on the SUPREG pin must be much higher than the (total) capacitance of the MOSFETs that must be driven. The total capacitance of the MOSFETs includes the SUPHS parallel load and capacitor bootstrap construction.

When considering the proper internal voltage regulator operation, the value of the capacitance on the SUPREG pin must be ≥ 1 µF.

6.7.3 Value of the capacitor for the SUPHS pin

To support the charging of the gate of the high-side MOSFET, the value of the capacitor for the SUPHS pin must be much higher than the gate capacitance. The higher capacitance prevents that a significant voltage drop occurs on the SUPHS pin because of the gate charge. When burst mode is applied, a small leakage current during the time between two bursts discharges the SUPHS pin.

7 MOSFET drivers (GATELS, GATEHS, and GATEPFC)

The TEA1916 provides three outputs for driving external high-voltage power MOSFETs:

- GATEPFC for driving the PFC MOSFET (TEA19162)
- GATELS for driving the low side of the HBC MOSFET (TEA19161)
- GATEHS for driving the low side of the HBC MOSFET (TEA19161)

7.1 GATEPFC

To drive a high-voltage power MOSFET, the TEA19162 includes a strong output stage for PFC. The SUPIC pin supplies this output stage.

7.2 GATELS and GATEHS

Both TEA19161 drivers have identical driving capabilities for the gate of an external high-voltage power MOSFET. The low-side driver is referenced to the GND pin and is supplied from the SUPREG pin. The high-side driver has a floating connection to the midpoint of the external half-bridge. It is referenced to HB. The high-side driver is supplied using a capacitor on the SUPHS pin. The capacitor is supplied using an external bootstrap function of the SUPREG pin. When the low-side MOSFET is on, the bootstrap diode charges C_{SUPHS}.

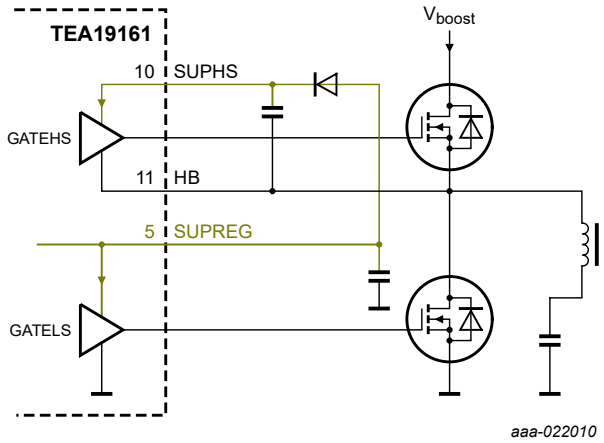


Figure 15. Supply system for GATELS and GATEHS

Both HBC drivers have a strong current source capability and an extra strong current sink capability. In general HBC operation, fast switch-on of the external MOSFET is not critical, as the HB node swings automatically to the correct state after switch-off. Fast switch-off, however, is important to limit switching losses and to prevent that a delay occurs, especially at high operating frequency.

7.3 MOSFET drivers - General information

7.3.1 Switch-on

The time to switch on depends on:

- The supply voltage for the internal driver
- The characteristic of the internal driver
- Charging the gate capacitance
- The gate threshold voltage for the MOSFET that switches on
- The external circuit to the gate

7.3.2 Switch-off

The time to switch off depends on:

- The characteristic of the internal driver
- Discharging the gate capacitance
- The voltage on the gate just before discharge
- The gate threshold voltage for the MOSFET that switches off
- The external circuit to the gate

The internal driver can sink more current than it can source, because the timing for switching off the MOSFET is more critical than the time for switching it on. At higher frequencies and/or short on-time, timing becomes more critical for correct switching. Sometimes, a compromise must be made between fast switching and EMI effects. To optimize the switching behavior, a gate circuit between the driver output and the gate can be used.

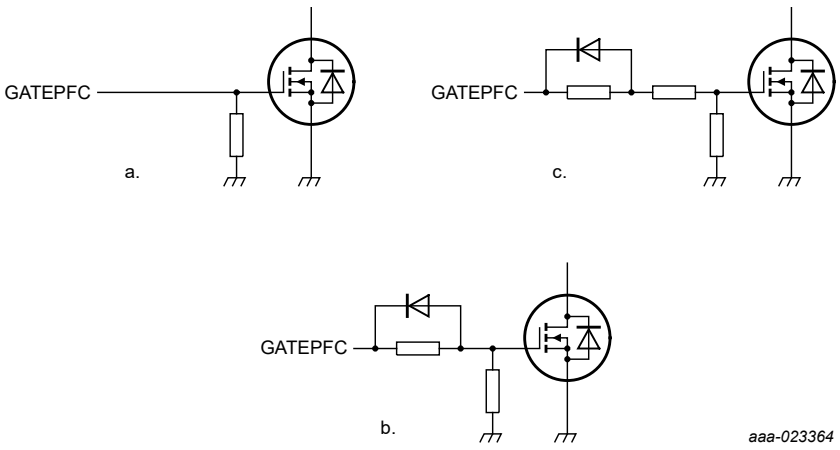


Figure 16. Examples of three different gate circuits

The switching on/off of the MOSFETs with the drivers is approximated by alternating the charge and discharge of a MOSFET gate-source capacitance using a resistor (R_{DSon} of the internal driver MOSFET and connections). The resistor value for discharging the gate is lower than for charging the gate.

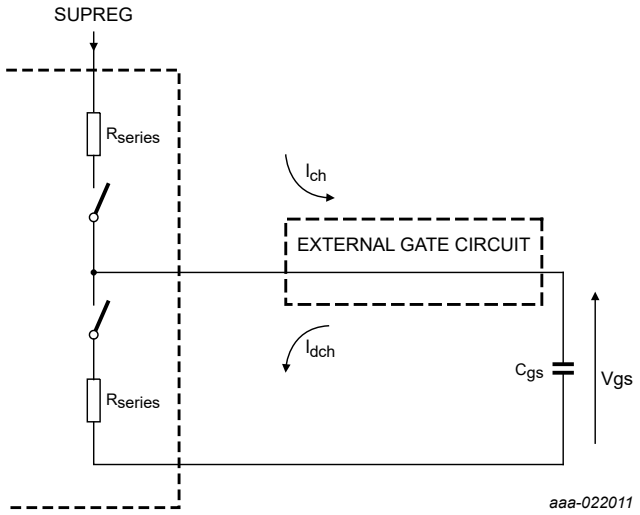


Figure 17. Simplified model of a MOSFET drive

7.4 Specification of the gate drivers

The main function of the internal MOSFET drivers is to source and sink current to switch on/switch off the external MOSFET. To show the capability of the internal driver, the amount of sink current and source current is specified.

The simplified model in Figure 17 demonstrates that the charge and discharge current values depend on the supply and gate voltage conditions. When the supply voltage is highest and the gate voltage 0 V, the source current value is highest. When the gate voltage is highest, the sink current value is highest.

Table 3. HBC and PFC driver specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
GATELS and GATEHS pins						
$I_{source(GATEHS)}$	source current on pin GATEHS	$V_{GATEHS} - V_{HB} = 4$ V	-	−340	-	mA
$I_{source(GATELS)}$	source current on pin GATELS	$V_{GATELS} - V_{GND} = 4$ V	-	−340	-	mA
$I_{sink(GATEHS)}$	sink current on pin GATEHS	$V_{GATEHS} - V_{HB} = 2$ V	-	580	-	mA
		$V_{GATEHS} - V_{HB} = 11$ V	-	2	-	A
$I_{sink(GATELS)}$	sink current on pin GATELS	$V_{GATELS} - V_{GND} = 2$ V	-	580	-	mA
		$V_{GATELS} - V_{GND} = 11$ V	-	2	-	A
Gate driver output (GATEPFC)						
$I_{source(GATEPFC)}$	source current on pin GATEPFC	$V_{GATEPFC} = 2$ V; $V_{SUPIC} \geq 13$ V	-	−0.6	-	A
$I_{sink(GATEPFC)}$	sink current on pin GATEPFC	$V_{GATEPFC} = 2$ V; $V_{SUPIC} \geq 13$ V	-	0.6	-	A
		$V_{GATEPFC} = 10$ V; $V_{SUPIC} \geq 13$ V	-	1.4	-	A

7.5 Active gate drive during IC supply start-up

Internal active pull-up and pull-down circuits provide a well-defined state of the external MOSFETs during start-up.

GATELS is pulled up with the charging of SUPREG. It switches on the low-side switch of the half-bridge and enables that the bootstrap charges SUPHS. SUPHS supplies the high-side gate driver GATEHS. When SUPHS (voltage between SUPHS and HB) reaches 2.5 V, GATEHS is actively pulled low. Normally, GATEHS is immediately pulled low when the low-side MOSFET switches on.

When SUPIC on the TEA19162 reaches 0.6 V, GATEPFC is actively pulled low to prevent an unintended switch-on.

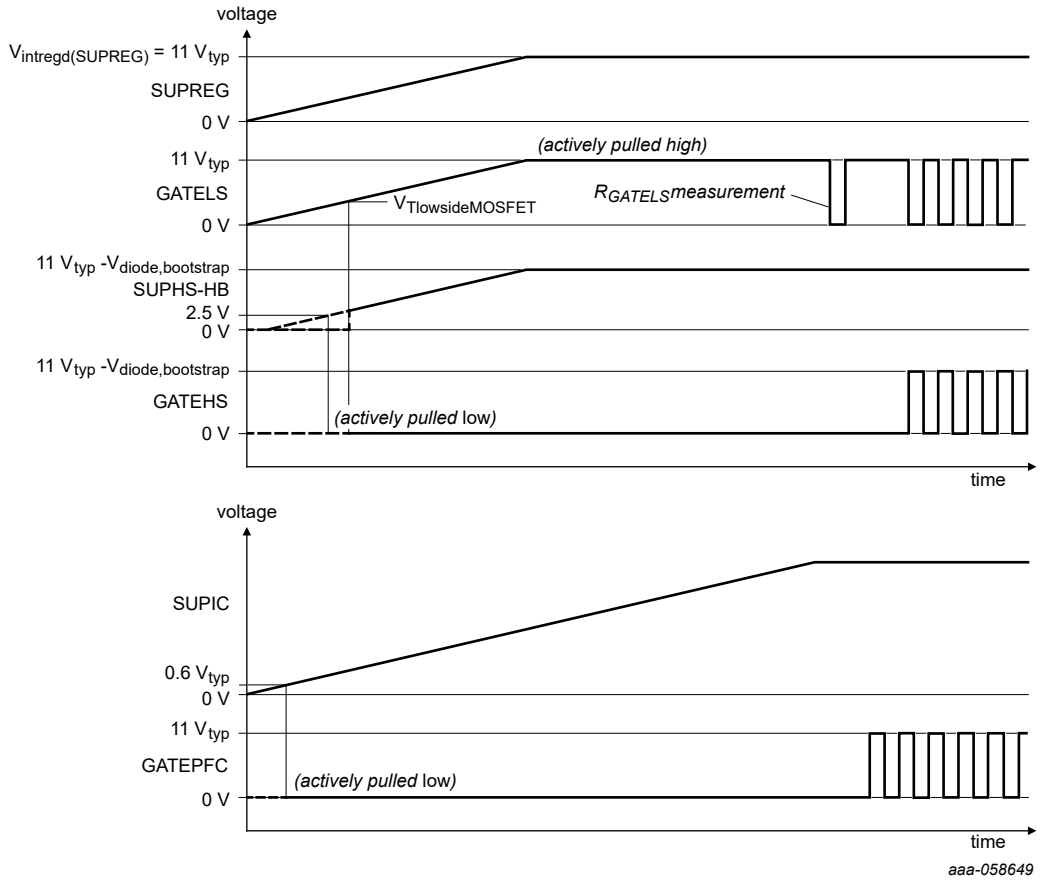


Figure 18. Active gate drive during IC supply start-up

7.6 Limiting values for the high-side drivers GATEHS, SUPHS, and HB

The high-side MOSFET driver for a half-bridge MOSFET stage has some specific behavior aspects. The reason is that a circuit that is supplied by a floating supply drives it. A bootstrap circuit supplies this floating voltage on the SUPHS pin. The high-side MOSFET and the driver are referenced to the HB voltage node. Regarding the circuit ground level, the HB node continuously switches between (approximately) 0 V and the input voltage (V_{boost}).

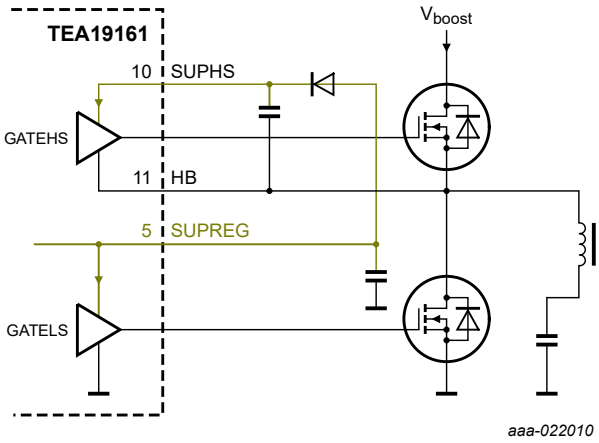


Figure 19. Supply system for GATEHS and GATELS

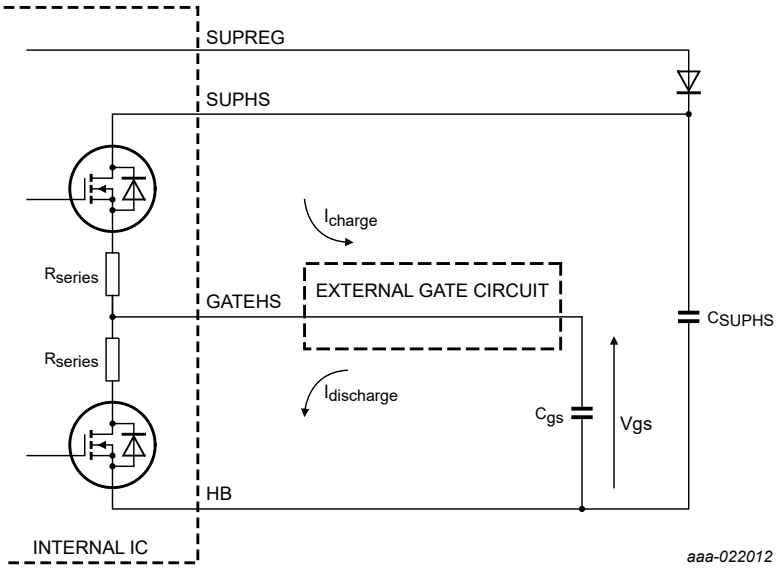


Figure 20. Simplified model of charging/discharging the gate of the high-side MOSFET

7.6.1 Supply voltage for the GATEHS output driver (SUPHS pin)

An external bootstrap buffer capacitor supplies the high-side driver. The bootstrap capacitor is connected between the high-side reference (the HB pin) and the high-side driver supply input (the SUPHS pin). Each time HB is low, an external diode from the SUPREG pin charges this capacitor.

Instead of using the SUPREG pin as the power source for charging the SUPHS pin, another supply source can be used. In such a construction, it is important to check for correct start/stop sequences and to prevent that the SUPHS voltage exceeds 14 V (referenced to HB).

7.6.2 GATEHS switching

Figure 21 shows that current is taken from SUPHS when the external high-side MOSFET is switched on. Switching on the internal high-side MOSFET, charges the gate of the external MOSFET (that can be represented as a capacitor C_{gs}) to a high voltage (V_{gs}). When the external MOSFET is switched off, the internal low-side MOSFET discharges C_{gs}.

The shape of the current is related to:

- The supply voltage for the internal driver (V_{SUPHS})
- The characteristic of the internal driver
- The gate capacitance to be charged
- The gate threshold voltage for the MOSFET
- The external circuit to the gate
- External parasitics

7.6.3 HBC circuit behavior and the GATEHS pin

In Figure 21, the behavior of GATEHS has been split into six events.

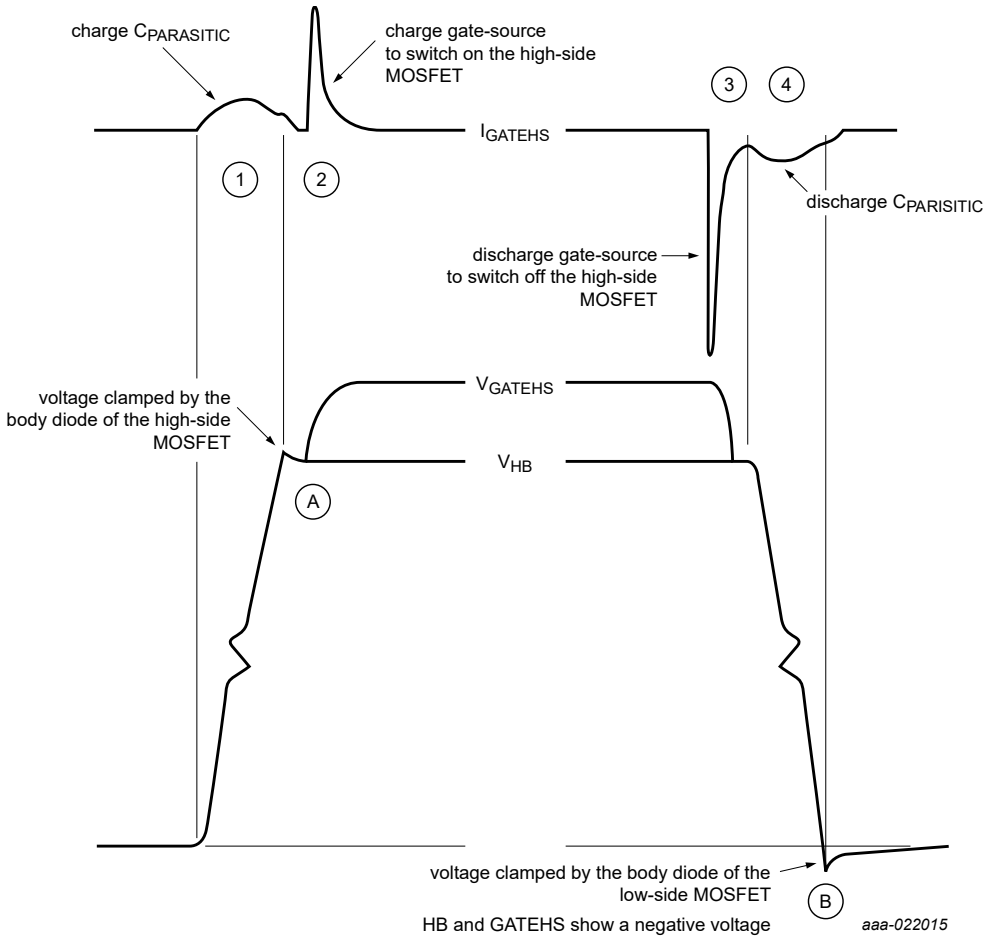


Figure 21. GATEHS current and voltage

Figure 22 and Figure 23 show the corresponding action in circuit diagrams that include the parasitic capacitance between GATEHS and ground.

- (1) During the positive HB slope, the internal lower MOSFET of GATEHS charges the parasitic capacitance.
- (2) During the switch-on of the high-side HBC MOSFET, the charge current flows from the SUPHS pin to the gate of the high-side HBC MOSFET through the internal upper MOSFET of GATEHS.
- (3) During the switch-off of the high-side HBC MOSFET, the discharge current flows from the gate of the high-side HBC MOSFET to the HB pin through the internal lower MOSFET of GATEHS.
- (4) During the negative HB slope, the conducting internal lower MOSFET of GATEHS discharges the parasitic capacitance.
- (A) At the end of the positive HB slope, the voltage on HB exceeds V_{boost}. The body diode of the high-side MOSFET clamps the voltage.
- (B) At the end of the negative HB slope, the voltage on the HB pin becomes negative. The body diode of the low-side MOSFET clamps the voltage to the ground level.

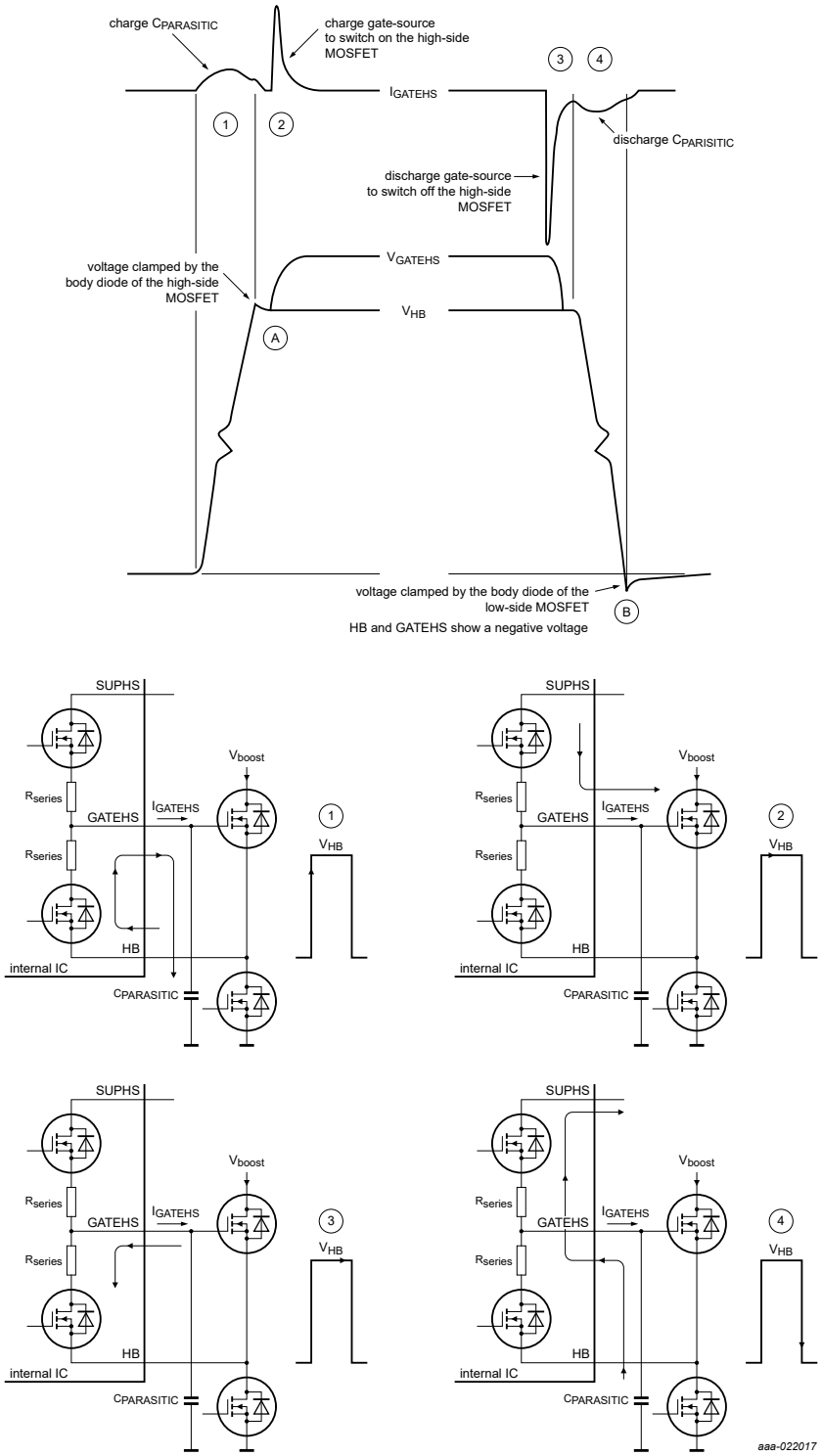


Figure 22. Current in GATEHS

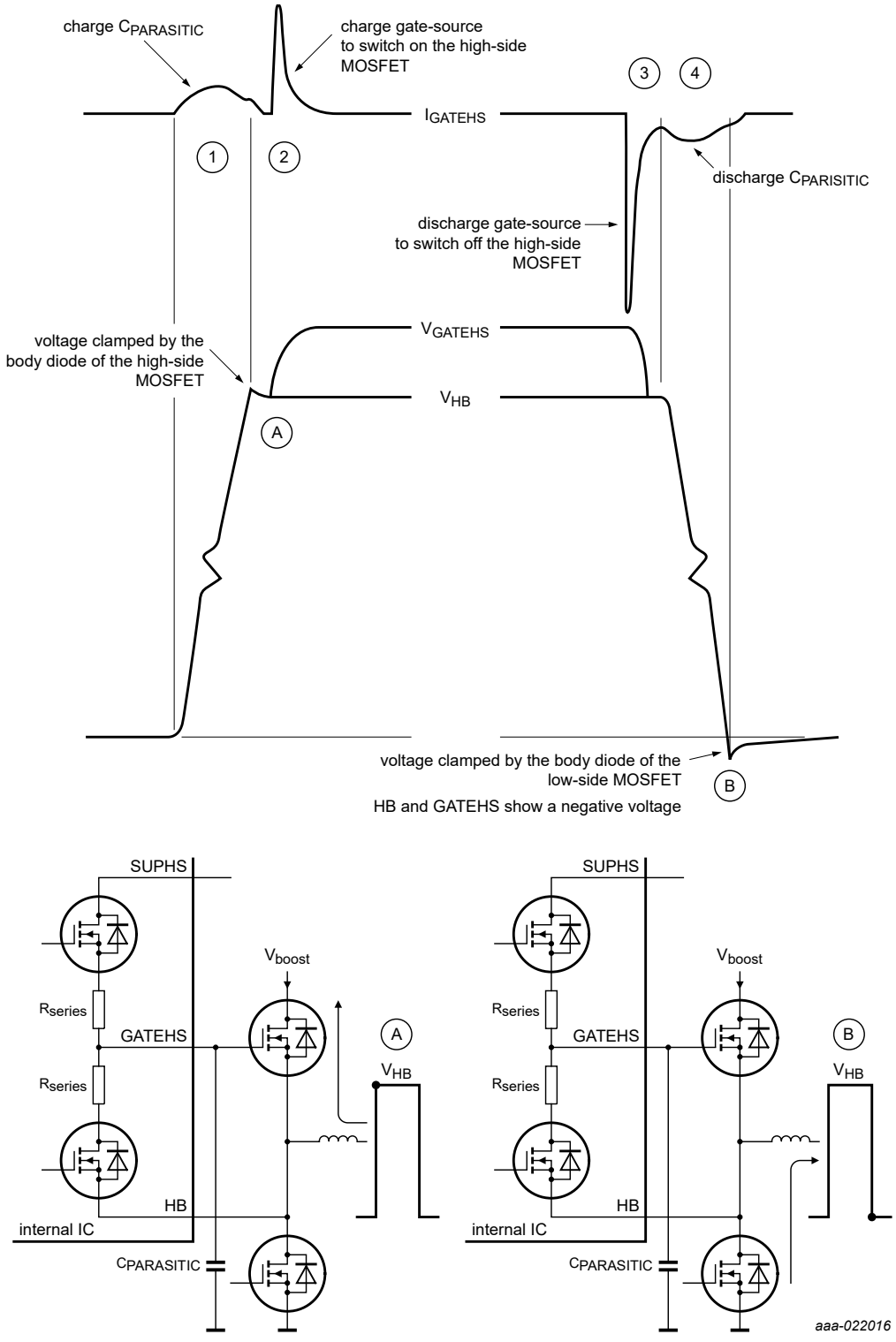


Figure 23. Voltage on GATEHS and HB

7.6.4 Limiting values of SUPHS and HB

The HB node and the SUPHS node are closely related because the internal high-voltage circuit is supplied with the voltage between these nodes. The voltage restrictions on the SUPHS pin are related to the limits for the voltage on the HB pin.

The values for HB can be derived from the voltage limits specified for the SUPHS pin using the practical voltage between both nodes: V_{SUPHS} to V_{HB}.

Table 4. Limiting values defined for V_{SUPHS}, V_{HB}, and V_{GATEHS}

Symbol	Parameter	Conditions	Min	Max	Unit
Voltages					
V_{SUPHS}	voltage on pin SUPHS		V_{HB}	V_{HB} + 14	V
V_{HB}	voltage on pin HB	maximum during mains surge; not repetitive	−3	+700	V
		t < 1 µs	−14	-	V
V_{GATEHS}	voltage on pin GATEHS		V_{HB} − 0.4	V_{SUPHS} + 0.4	V

7.6.5 GATEHS limits

7.6.5.1 GATEHS voltage

The GATEHS voltage remains approximately within the voltage between the SUPHS and HB pins. In situation 1 (see Figure 22), the voltage on the GATEHS pin can become a little lower than the voltage on the HB pin, because of the conducting body diode. And at GATEHS switch-off, the voltage can become lower because of a ringing effect (see Section 7.7 and Table 4).

7.6.5.2 GATEHS current

Measurement setup

The behavior of the current in the GATEHS of a certain application can be checked. Because charging/discharging the parasitic capacitance causes the GATEHS current during the HB slopes, do not increase the parasitic capacitance too much at measurement setup.

Do not connect a voltage probe because it adds a relatively large capacitance (for example, on GATEHS).

A current probe is suitable for measurement because it only adds a small amount of extra capacitance to the application circuit. Because of the small amount of extra capacitance added by a current probe, the measurement results show higher currents than in the original circuit.

The extra current can be measured by (temporarily) adding a second current probe. The additional current caused by one probe can be found by measuring the difference in current values between one probe connected and two probes connected. Subtracting this probe-related current from the measurement result can provide more accurate values.

Current values

The SUPHS internal driver itself drives the currents in situations 2 and 3.

Another source causes the currents in situations 1 and 4. These currents must not become excessive. In situation 4, the GATEHS conducts to HB via the internal lower MOSFET of GATEHS. The peak current value can become similar to the discharge current without a problem. In situation 1, the GATEHS does not actively conduct, but the current flows through the body diode of the internal lower MOSFET of GATEHS. Normally, the peak current level in situation 1 is much lower than the discharge current of the same lower MOSFET in situation 3.

The expected value as a rule of thumb:

$$I_{peak\_in\_1} \approx -0.25 \times I_{peak\_in\_3} \quad (8)$$

At switch-off after situation 3, some parasitic ringing may occur. To check this condition for the gate drivers in general, see Section 7.7.

7.7 Gate driver switch-off and limiting values

Parasitic inductance in the IC-to-MOSFET connections leads to a ringing effect after switch-off. A negative voltage and current occur in the gate driver pin. When designing the PBC layout, avoid long tracks. To prevent switching problems and stay within the specification of the IC function, the resulting behavior must be checked.

The limiting voltage values in the TEA19161T data sheet (Ref. 1) only provide a safe minimum DC level of −0.4 V. However, if the level is not high and the duration is short, the internal driver circuit can handle some extra reverse current.

7.7.1 Determining if switch-off reverse current is still safe

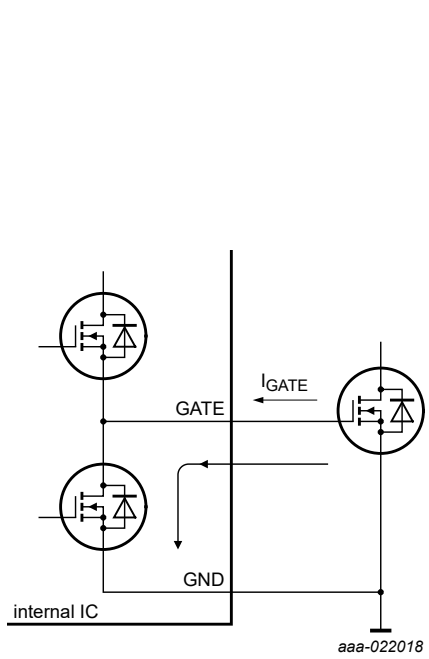
When a voltage measurement on the gate pin shows that the level is below −0.4 V, the current in the pin can be checked. In this way, how much energy the IC gate drive circuit contains can be seen. Because of several parasitic elements in the gate drive circuit (application) and the IC, a voltage measurement is often not conclusive.

The gate current must be checked using a DC current probe and an oscilloscope. Make sure that adding the current probe measurement does not (significantly) change the behavior of the circuit.

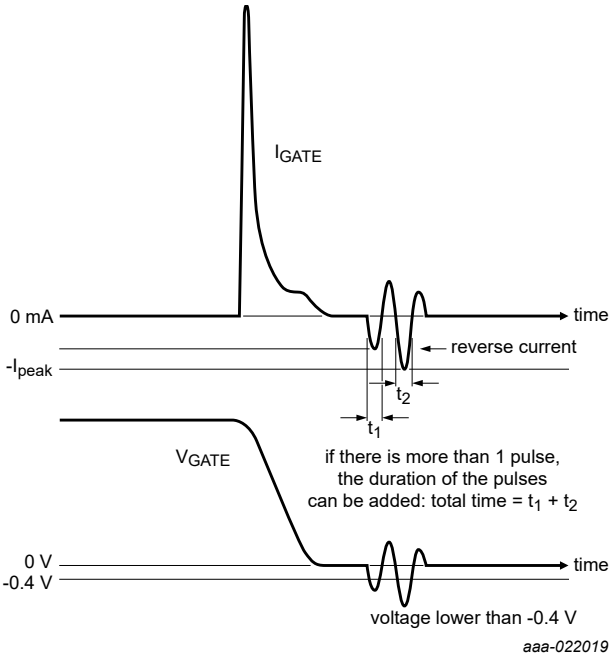
When all three conditions below are met, the reverse current is still safe:

- The reverse current does not exceed −300 mA (peak)
- The duration of pulses is shorter than 500 ns during each event
- The repetition rate of the events is lower than 200 kHz

This rule is valid for the GATELS and GATEHS pins (TEA1916) and for the GATEPFC pin (TEA19162).



a. Circuit



b. Measurement example

Figure 24. Ringing after GATE driver switch-off

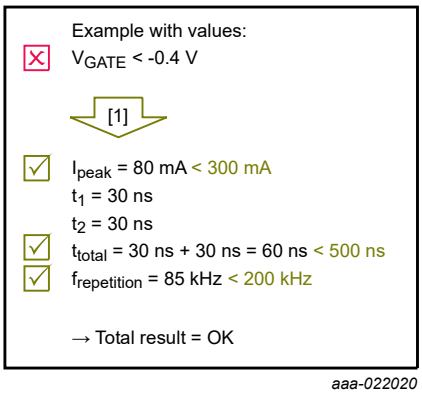


Figure 25. Example of checking if the gate driver reverse current is OK at switch-off

7.8 Avoiding high dV/dt slopes

Steep HB slopes (high dV/dt) can give disturbances on measurement signals, adding voltage spikes through capacitive coupling. These unwanted disturbances can be limited in two ways:

- Immunize the (measurement) circuits by filtering or low impedance.
- To reduce the disturbance source, lower dV/dt HB slopes.

To reduce disturbances, measurement circuits are often filtered or use a low impedance. The circuits in the IC are also designed to provide robustness against HB dV/dt disturbances.

Because new MOSFET technology, like GaN, provides switching devices with lower capacitance, an additional risk of HB slopes becoming very steep exists. To minimize the disturbances and risk of bad operation, steep HB slopes must be avoided.

Two operation conditions must be checked for HB dV/dt:

- Normal operation
- Start-up and output short

During normal operation, the HB slopes are not very steep, usually below 10 V/ns. Because in this condition most performance requirements are tested, disturbances must be limited to ensure good operation.

During start-up and output short, the primary current is much higher, leading to very steep dV/dt. Sometimes, HB dV/dt values of 40 V/ns or higher can be observed. These slopes can give big disturbances and cause the operation to become unreliable. Because these slopes are special and temporary conditions, there are usually no severe performance requirements.

If problems occur because of a high HB dV/dt, the steepness of the slopes can be reduced by adding a capacitor between the HB and the GND pins (for example 47 pF or 100 pF).

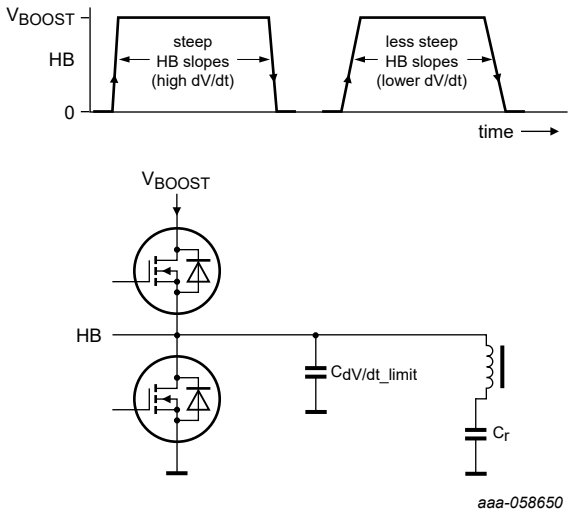


Figure 26. Additional capacitor on HB to help reduce steep HB dV/dt slopes

8 TEA19162 PFC functions

8.1 Mains voltage sensing and OTP (SNSMAINS pin)

The SNSMAINS pin combines two functions:

- The mains voltage sensing
- The sensing of an external NTC for detecting an OTP

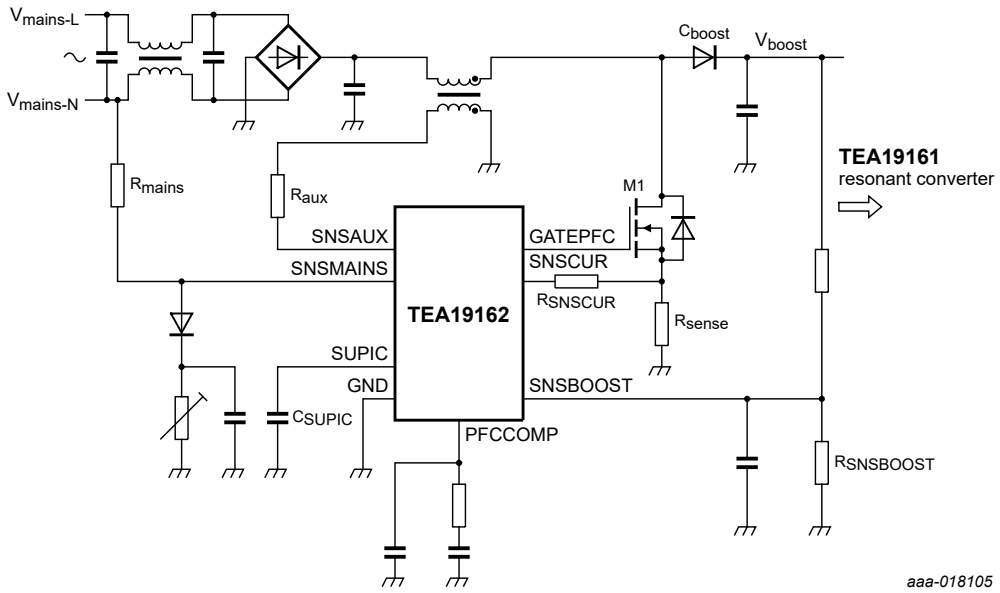


Figure 27. Mains voltage sensing and OTP (SNSMAINS pin)

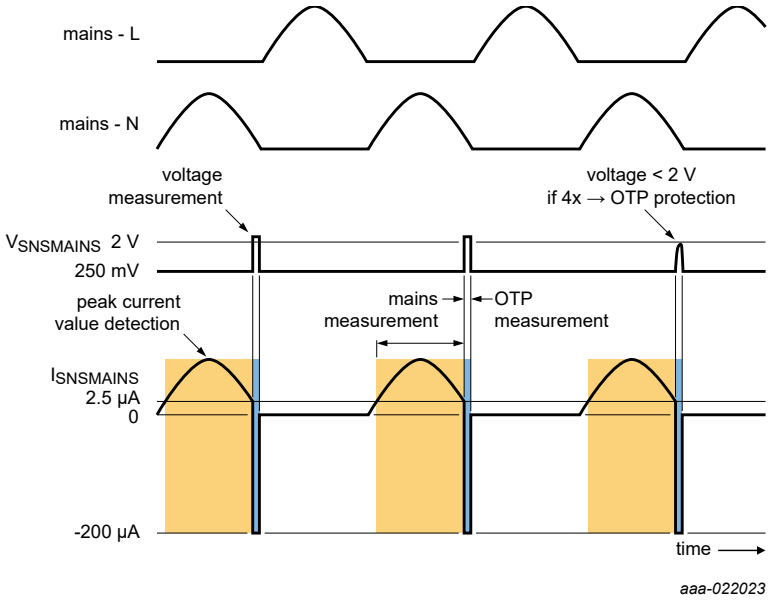


Figure 28. Mains voltage sensing and OTP sensing alternating in time (SNSMAINS pin)

8.2 Mains voltage sensing (SNSMAINS pin)

A resistor of typically 20 MΩ connects one pole of the mains to the SNSMAINS pin. It allows the mains voltage measurement by sensing the current flowing into the SNSMAINS pin. During the mains measurement, an internal source clamps the SNSMAINS pin to 250 mV.

The mains current is tracked continuously. When the peak level is detected, the measured value is stored internally. The peak value is updated every half-mains measurement cycle (so, effectively every second half-mains cycle).

When the current value drops to below 2.5 µA, the OTP measurement is activated. The mains current measurement is not active until the next half-mains half measurement cycle.

The measured current level is used for the brownout/brownin detection. The peak current level is used for the mains compensation in the PFC control loop.

The mains information is also used for starting and stopping the X-capacitor discharge and the latch reset functions.

8.3 Brownin and brownout (SNSMAINS pin)

At the SNSMAINS current level of 5.75 µA, the PFC brownin level is detected and the PFC switching is started. At the 5 µA current level, the brownout is detected and PFC stops switching.

When the current level drops to below the 5 µA UVP level during operation, an internal timer of 50 ms is started. The current level must remain below 5 µA for 50 ms before the UVP protection (brownout) is triggered.

This 50 ms time filter is intended to prevent false triggering or accidental switch on-off-on sequences.

- $V_{mains(peak)} = 1.41 \times V_{mains(rms)}$
- $V_{SNSMAINS} = 0.25\ V$
- $I_{bi} = 5.75\ \mu A$
- $I_{bo} = 5\ \mu A$

Requirement example: $V_{bi(rms)} = 82\ V$

$$R_{SNSMAINS} = \frac{V_{mains(peak)} - V_{SNSMAINS}}{I_{bi}} = \frac{(1.41 \times 82\ V - 0.25\ V)}{5.75\ \mu A} = 20\ M\Omega \quad (9)$$

$$V_{bo(rms)} = \frac{1}{1.41} \times (0.25\ V + I_{bo} \times R_{SNSMAINS})$$

$$= \frac{1}{1.41} \times (0.25\ V + 5\ \mu A \times 20\ M\Omega) = 71\ V$$

8.4 NTC measurement for external OTP (SNSMAINS pin)

During the external OTP sensing period, the activated internal current source causes a 200 µA flow out of the SNSMAINS pin, through the external diode, and NTC to ground. The resulting voltage on the pin is measured. When the voltage on the pin is below 2 V for four consecutive measurement cycles, the OTP protection is activated.

Figure 29 shows a typical application circuit.

The protection value of the NTC can be calculated with Equation 7:

$$R_{NTC} = \frac{V_{det(SNSMAINS)} - V_{Fd}}{I_{o(SNSMAINS)}} - R_{series} = \frac{2\ V - 0.6\ V}{200\ \mu A} - 3.3\ k\Omega = 3.8\ k\Omega \quad (10)$$

With the required temperature level and the calculated NTC value, a suitable device can be selected. To optimize the protection function with the selected NTC type, the value of resistor R_{series} can be modified.

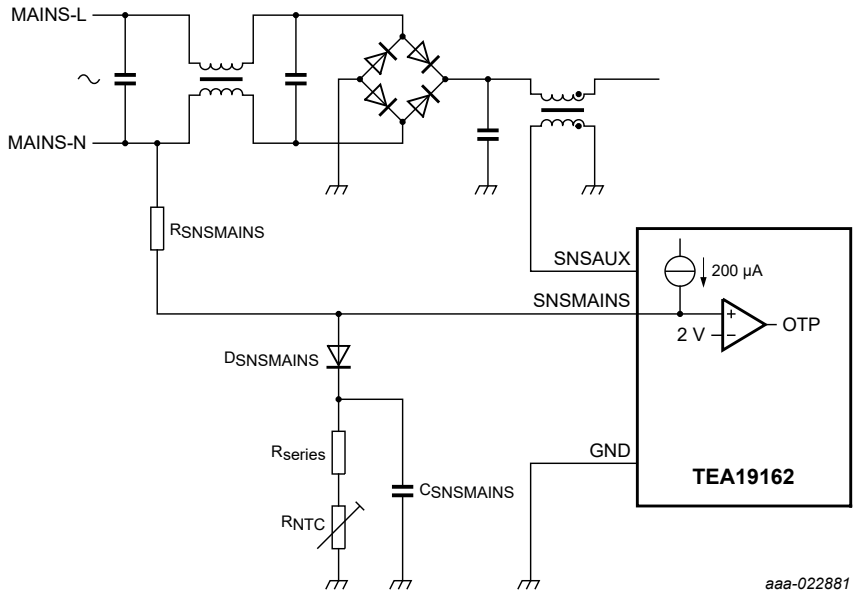


Figure 29. Typical external OTP function implementation on SNSMAINS with NTC

8.5 PFC operation

The PFC operates in quasi-resonant (QR) or discontinuous conduction mode (DCM) using valley detection to reduce the switch-on losses. The maximum switching frequency of the PFC is limited to 134 kHz. This limitation reduces switching losses because of valley skipping. The reduction of switching losses is mainly near the zero voltage crossings of the mains voltage. It is very effective at low mains input voltages and medium/low output load conditions.

The PFC is designed as a boost converter with a fixed output voltage. An advantage of a fixed boost converter is that the HBC can be designed to a high input voltage, making the HBC design easier. Another advantage of the fixed boost converter is the option to use a smaller boost capacitor value or to have a significantly longer hold-up time.

In the TEA1916 system, the PFC is always active. When the mains voltage is present, the PFC is switched on first. After the boost capacitor is charged to approximately 90 % ($V_{SNSBOOST}$ = 2.3 V) of its normal value, the HBC is switched on.

For improved efficiency at low output loads, the system can be operated in burst mode. Based on the output power and the voltage on the SNSBOOST pin, the HBC controller controls the PFC operation by stopping and starting the PFC during burst mode.

8.6 PFC output power and peak current

The PFC of the TEA19162 is time controlled. So, measuring the mains phase angle is not required. To obtain a good power factor (PF) and mains harmonics reduction (MHR), the on-time is kept constant during the half sine wave for a given mains voltage and load condition.

When the on-time is constant, the PFC input peak current level follows the shape of the mains voltage.

The highest peak current is an essential parameter for the PFC coil design. This current occurs at the lowest input voltage and maximum power.

The maximum peak current $I_{p(max)}$ for a PFC operating in critical conduction mode can be calculated with Equation 8.

$$I_{p(max)} = \frac{2\sqrt{2} \times P_{i(max)}}{V_{min(AC)}} = \frac{2\sqrt{2} \times \frac{P_{o(nameplate)}}{\eta}}{V_{min(AC)}} \quad (11)$$

Example:

- Efficiency (η) = 0.9
- $P_{o(nameplate)}$ = 250 W
- $V_{min\ (AC)}$ = 90 V

$$I_{p(max)} = \frac{2\sqrt{2} \times P_{i(max)}}{V_{min(AC)}} = \frac{2\sqrt{2} \times \frac{P_{o(nameplate)}}{\eta}}{V_{min(AC)}} = \frac{2\sqrt{2} \times \frac{250\ W}{0.9}}{90\ V} = 8.73\ A$$

$$I_{p(max)} + 10\ \% = 9.60\ A$$

The TEA1916 PFC operates in quasi-resonant (QR) mode with valley detection, providing good efficiency. Valley detection requires additional ringing time within every switching cycle. This ringing time adds short periods of no power transfer to the output capacitor. The system must compensate for these periods using a higher peak current. A rule of thumb is that the peak current in QR mode is maximum 10 % higher than the calculated peak current in critical conduction mode.

8.7 PFC output voltage regulation (SNSBOOST pin)

A resistive divider between the PFC output voltage, the SNSBOOST pin, and GND sets the boost output voltage value. When in regulation, the voltage on the SNSBOOST pine is kept at 2.5 V.

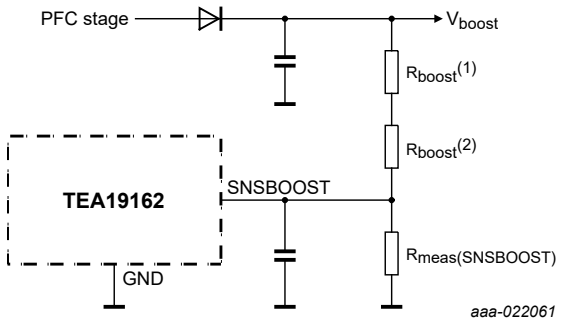


Figure 30. PFC output regulation using the SNSBOOST pin

To support correct functioning for communication and burst mode operation, the resistor between the SNSBOOST and the GND pins must be 100 kΩ. The TEA19161 and TEA19162 share the SNSBOOST pin. Section 8.19 discusses the shared functions. Section 13 provides important PCB layout design information.

The value of the resistors between the PFC output voltage and the SNSBOOST pin can be calculated with Equation 9:

$$R_{boost} = R_{boost}(1) + R_{boost}(2) \quad (12)$$

$$R_{boost} = R_{meas(SNSBOOST)} \times \frac{V_{boost} - V_{reg(SNSBOOST)}}{V_{reg(SNSBOOST)}}$$

Typical system values are:

- $R_{meas(SNSBOOST)}$ = 100 kΩ
- $V_{reg(SNSBOOST)}$ = 2.5 V

For example, To obtain a nominal PFC output voltage of V_{boost} = 390 V, R_{boost} must be 15.6 MΩ.

8.8 PFC gate driver (GATEPFC pin)

The circuit that drives the gate of the power MOSFET has a high-current sourcing capability ($I_{source(GATEPFC)}$) of 0.6 A. It also has a high-current sink capability ($I_{sink(GATEPFC)}$) of 1.4 A. To ensure efficient operation, the source and sink capabilities enable fast switch-on and switch-off of the external power MOSFET. To ensure a drive voltage of 11 V, the driver is supplied from the SUPIC pin via an internal voltage regulator.

Do not use active components like transistors to enhance switching behavior. They introduce the risk of bad switching behavior in special conditions.

8.9 PFC on-time control

The PFC operates under on-time control. The PFC MOSFET on-time is determined by:

- The error amplifier and the loop compensation using the voltage on the PFCCOMP pin. At 3.5 V, the on-time is reduced to zero. At 1.93 V, the on-time is at the maximum.
- Mains compensation using the voltage on the SNSMAINS pin.

In the TEA19162, the on-time is related to the voltage on the PFCCOMP and SNSMAINS pins. The relationship can be calculated with Equation 10:

$$t_{on}\,(\mu s) = 460 \times \frac{3.5\ V - V_{PFCCOMP}(V)}{\left(I_{SNSMAINS}(\mu A)\right)^2} \quad (13)$$

8.10 PFC soft start and soft stop (SNSCUR and PFCCOM pins)

The PFC controller features a soft start function. The function slowly increases the primary peak current during start-up. The soft stop function slowly decreases the PFC peak current before operation is halted. These functions prevent audible noise of the PFC components (mainly the PFC coil) at start-up and during burst mode operation.

The soft start is included in the SNSCUR function (see Section 8.17) and the soft stop is included in the PFCCOMP function (see Section 8.11.4).

8.11 PFCCOMP in the PFC voltage control loop

8.11.1 SNSBOOST error amplifier

The PFC output voltage is set and controlled using the SNSBOOST pin. The internal error amplifier senses the voltage on the SNSBOOST pin using a reference voltage of 2.5 V.

The amplifier converts the input error voltage to its output with a transconductance (g_m = 75 µA/V). The regulation level is 2.5 V. When the voltage on the SNSBOOST pin exceeds 2.6 V, the transconductance of the error amplifier is increased. The increase allows that the voltage on the SNSBOOST pin is corrected to the regulation level faster. Figure 30 shows the amplifier characteristic.

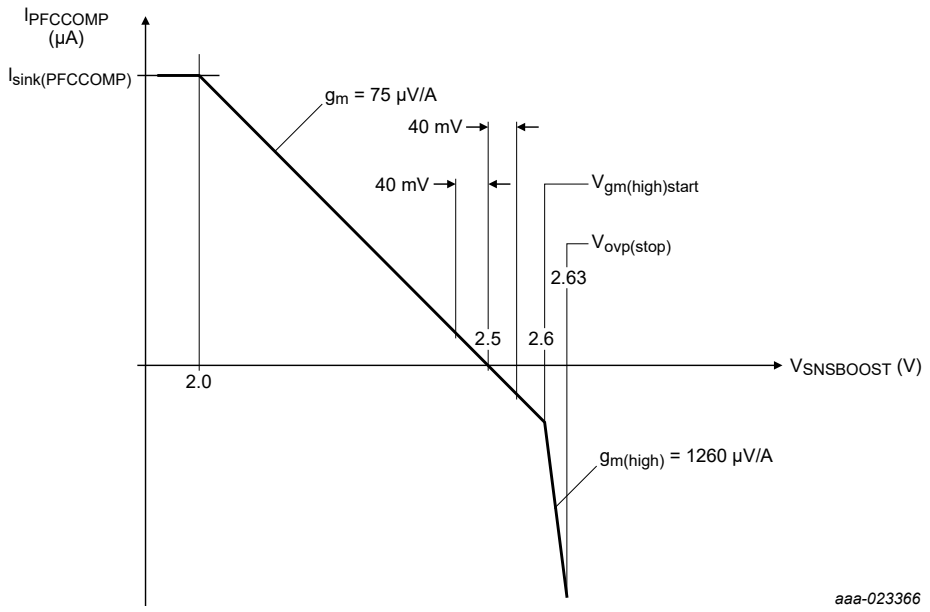


Figure 31. SNSBOOST-PFCCOMP amplifier characteristic

8.11.2 PFCCOMP voltage

The transconductance amplifier output is available at the PFCCOMP pin. It can be used to add an external loop compensation network. The current from the error amplifier results in a voltage on the PFCCOMP pin. The PFCCOMP voltage and the voltage on the SNSMAINS pin determine the PFC switch-on time.

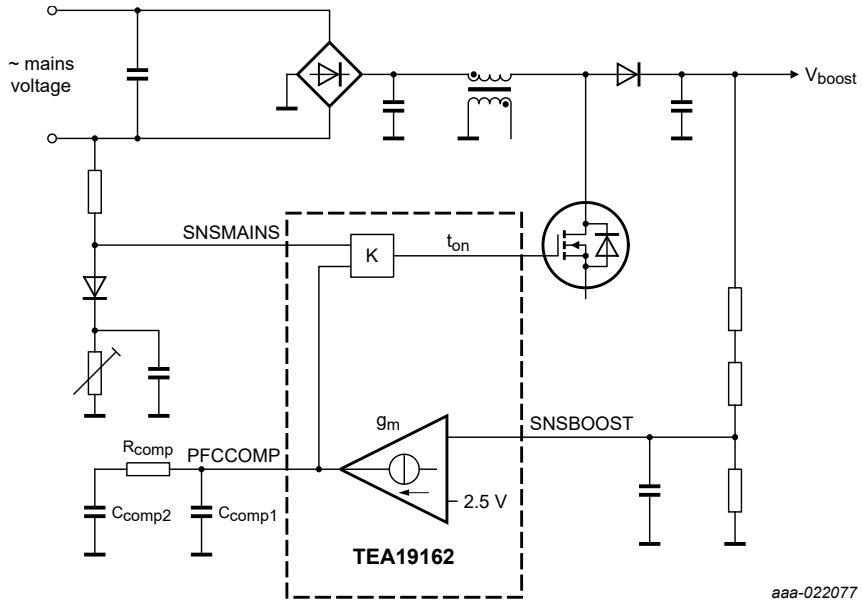


Figure 32. Basic PFC control loop with PFCCOMP

8.11.3 PFCCOMP network

To stabilize the PFC control loop, a compensation network, typically consisting of one resistor and two capacitors at the PFCCOMP pin, is used.

The transfer function has a pole at 0 Hz, a zero at R_{comp}/C_{comp2}, and a pole again at C_{comp1}/C_{comp2}. Set the zero frequency to 10 Hz while the next pole frequency is at 40 Hz. The zero point and pole frequencies of the compensation network can be calculated with Equation 11 and Equation 12.

$$f_{zero} = \frac{1}{2\pi \times R_{comp} \times C_{comp2}} \quad (14)$$

$$f_{pole} = \frac{C_{comp1} + C_{comp2}}{2\pi \times R_{comp} \times C_{comp2} \times C_{comp1}} \quad (15)$$

A trade-off between the power factor performance and the transient behavior must be made. A lower regulation bandwidth leads to a better power factor but poorer transient behavior. A higher regulation bandwidth leads to a better transient response but a poorer power factor.

8.11.4 Soft stop

The PFCCOMP function also includes a soft-stop mode. When the PFC switching has stopped, the soft-stop mode is used. This function is important to reduce audible noise of the intermitting PFC operation during burst mode operation.

During soft stop, an additional internal circuit sets the PFCCOMP voltage. The output voltage of the SNSBOOST transconductance amplifier is disconnected. To reduce the PFC on-time, an internal current source of 30 µA charges the PFCCOMP network to a higher voltage. When the PFCCOMP voltage has reached 3.5 V, the soft stop ends (zero on-time).

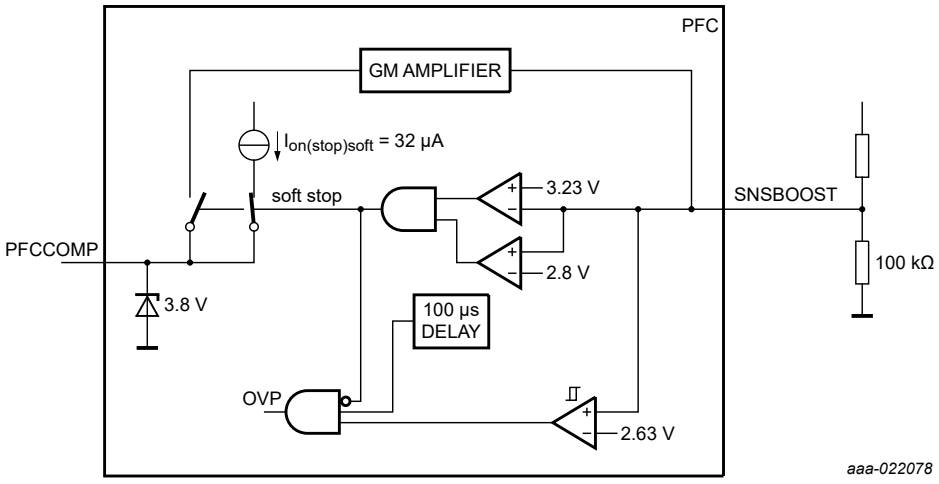


Figure 33. Soft stop function on PFCCOMP

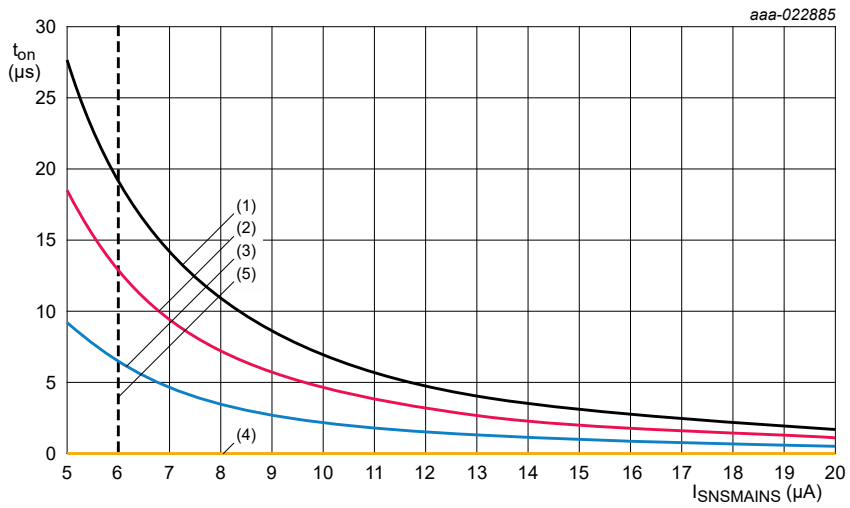
8.12 Mains compensation in the PFC voltage control loop

The PFC transfer function, from which the PFC on-time can be derived, is inversely proportional to the squared mains input voltage (see Figure 32).

$$K_{(Vmains)} = \frac{A}{V_{mains}^2} \quad (16)$$

In a typical application, the result is a low bandwidth for low mains input voltages. At high mains input voltages, the MHR requirements can be hard to meet.

To compensate for the mains input voltage influence, the TEA19162 contains a correction circuit. The peak mains voltage is measured at the SNSMAINS pin. It is used for the internal compensation. Figure 34 shows the relationship between the SNSMAINS voltage, the PFCCOMP voltage and the on-time according to Equation 10 in Section 8.9.



- (1) $V_{PFCCOMP}$ = 2 V
- (2) $V_{PFCCOMP}$ = 2.5 V
- (3) $V_{PFCCOMP}$ = 3 V
- (4) $V_{PFCCOMP}$ = 3.5 V
- (5) Minimum $I_{SNSMAINS}$ for normal operation

Figure 34. On-time at different voltages on the PFCCOMP pin

8.13 PFC demagnetization sensing (SNSAUX pin)

The voltage on the SNSAUX pin is used to detect transformer demagnetization. During the secondary stroke, the transformer is magnetized and current flows to the boost output. During this time, the SNSAUX voltage is lower than −90 mV and the PFC MOSFET remains switched off.

When the transformer is demagnetized and the current stops flowing to the boost output, the SNSAUX voltage exceeds −90 mV and valley detection is started. The MOSFET remains off until a valley is detected.

To ensure that switching continues under all circumstances, the MOSFET is forced to switch on if the magnetization of the transformer is not detected within 44.5 µs after the GATEPFC pin goes LOW.

8.14 PFC valley sensing (SNSAUX pin)

If the voltage at the MOSFET drain is at its minimum (valley switching), the PFC MOSFET is switched on for the next stroke. This action reduces switching losses and EMI (see Figure 35).

The valley sensing on the SNSAUX pin detects the valleys. It measures the voltage on the auxiliary winding of the PFC coil. This signal is a scaled and inverted copy of the MOSFET drain voltage. When a valley of the drain voltage (= top of the SNSAUX voltage) is detected, the MOSFET is switched on for the next cycle.

If no valley is detected within 44.5 µs after demagnetization, the MOSFET is forced to switch on.

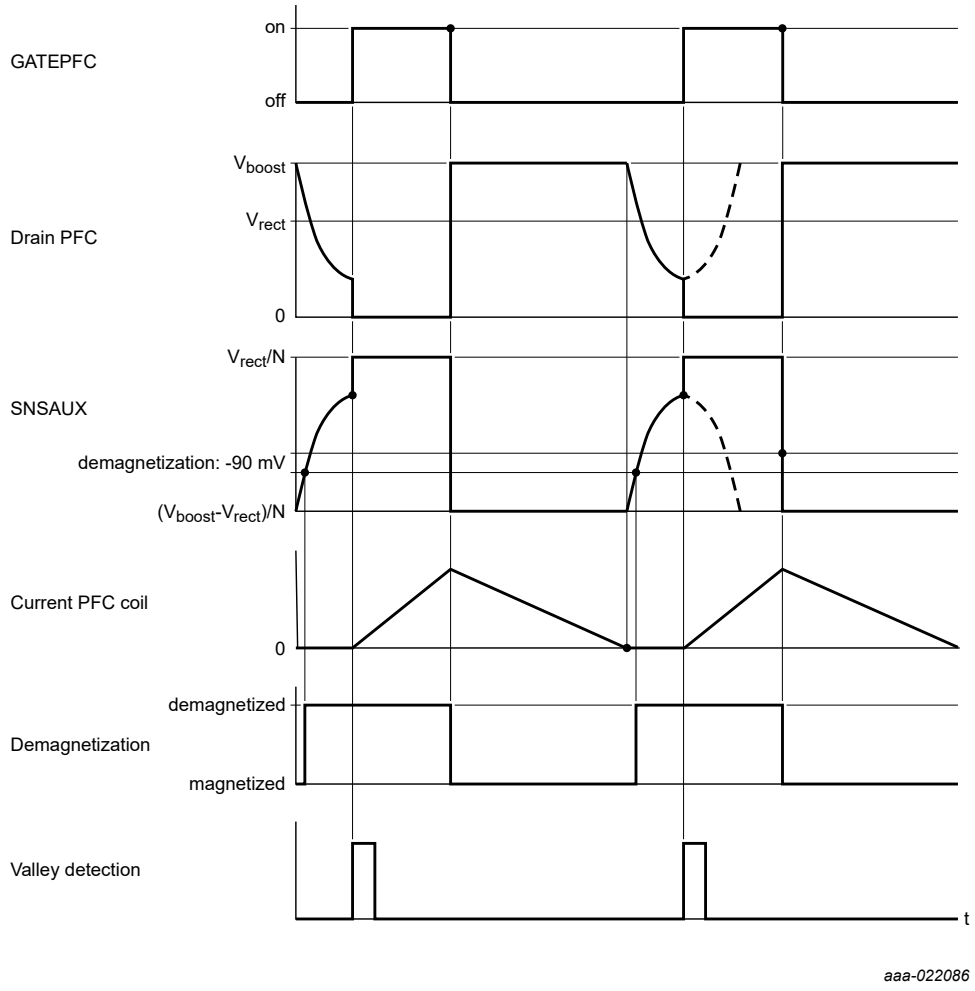


Figure 35. PFC demagnetization and valley detection

8.15 PFC auxiliary sensing circuit

Adding a 5.1 kΩ series resistor to the SNSAUX pin protects the internal IC circuit against excessive voltage, for example, during lightning surges. To prevent disturbances causing incorrect switching, place this resistor close to the IC.

Maintain valley detection even at low ringing amplitudes. Set the voltage on the SNSAUX pin as high as possible, while considering its absolute maximum rating of ±25 V.

The maximum number of turns of the auxiliary winding on the PFC coil can be calculated with Equation 15.

The boost output voltage at the overvoltage protection (OVP) determines the maximum voltage across the PFC primary winding. It can be calculated with Equation 14.

Both calculations are made with example values:

- V_{boost} (nominal) = 394 V

- Numbers of turns of PFC coil design = 52

$$V_{boost\_max} = \frac{V_{ovp(SNSBOOST)}}{V_{reg(SNSBOOST}} \times V_{boost} = \frac{2.63\ V\ (typical)}{2.5\ V\ (typical)} \times 394\ V = 415\ V \quad (17)$$

$$N_{aux\_max} = \frac{V_{aux(PFC)}}{V_{boost\_max}} \times N_p = \frac{25\ V}{415\ V} \times 52 = 3.13 \rightarrow 3\ turns \quad (18)$$

When a PFC coil with a higher number of auxiliary turns is used, place a resistor voltage divider between the auxiliary winding and the SNSAUX pin. To prevent a delay of the valley detection combined with parasitic capacitances, the total resistive value of the divider must not be too high. To judge if the delay is short or acceptable, compare the original PFC MOSFET drain voltage shape with the signal on the SNSAUX pin.

8.16 PFC frequency and off-time limiting

For the PFC coil value design and electromagnetic interference (EMI) and to minimize switching losses, the switching frequency is limited to 134 kHz. If the frequency for QR operation exceeds 134 kHz, the system switches to DCM operation. When the drain-source voltage is at a minimum (valley switching) at one of the next valleys, the PFC MOSFET is switched on. This feature is called valley skipping.

To ensure good switching control of the PFC MOSFET under all circumstances, the minimum off-time is limited at 1.55 µs.

8.17 PFC overcurrent regulation, OCR-PFC, and soft start (SNSCUR pin)

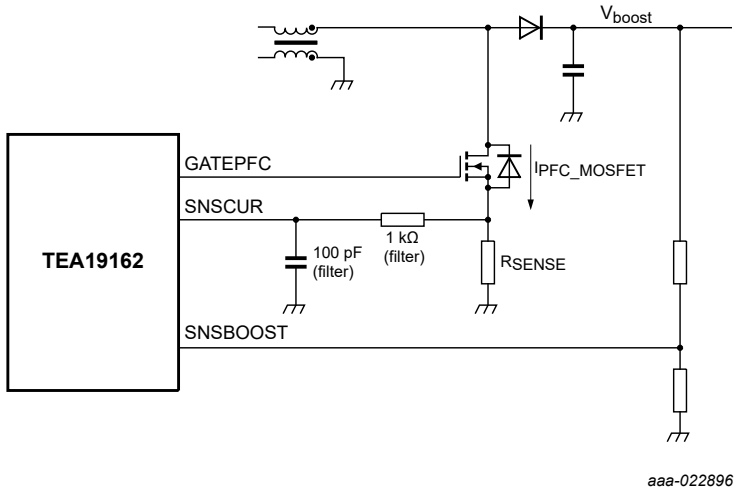


Figure 36. SNSCUR senses the PFC MOSFET current

The maximum PFC peak current is limited cycle-by-cycle by sensing the voltage across an external sense resistor in series with the source of the PFC MOSFET. The voltage is measured via the SNSCUR pin of the TEA19162. It is limited to 0.5 V. When the voltage on the SNSCUR pin reaches 0.5 V, the MOSFET is switched off.

For design purposes, include a margin of approximately 100 mV for the value of the measurement resistor. In this way, practical deviations are compensated.

Example:

$$R_{sense(PFC)} = \frac{V_{ocr(SNSCUR)} - 100\ mV}{I_{p(max)}} = \frac{500\ mV - 100\ mV}{8.73\ A_p} = 46\ m\Omega \quad (19)$$

Because of the discharging of the MOSFET drain capacitance, a voltage peak appears on the SNSCUR pin when the PFC MOSFET is switched on during a switching cycle. The 300 ns leading-edge blanking time ensures that the overcurrent sensing function does not react to this transitory peak.

To minimize audible noise at start-up or restart, a soft-start function is included in the SNSCUR pin. The OCR level is modified for this soft-start function, starting with 135 mV. This level is gradually increased to the regular 500 mV within 3.75 ms. The PFC on-time increases accordingly.

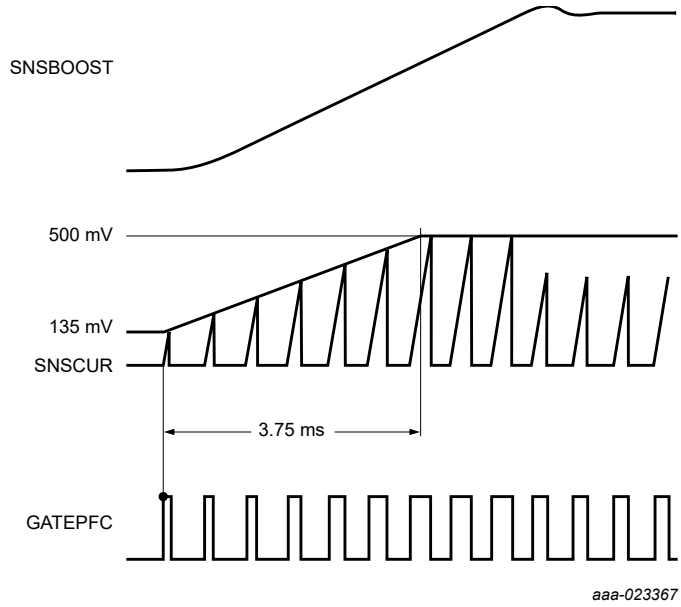


Figure 37. Soft start SNSCUR pin

8.18 Active X-capacitor discharge

The TEA19162T provides an active X-capacitor discharge function with a special PFC MOSFET operation mode.

To suppress electromagnetic interference in most applications, a filter is required on the mains input. In addition to an inductance, EMI filters typically include one or more X-capacitors connected between the mains input terminals.

The active X-capacitor discharge function reduces the voltage between the device mains terminals to a safe value within a certain time period after the device is disconnected from the mains. In some regulatory regimes, this reduction is mandatory. If the voltage is not reduced, contacting the terminals of the plug can cause an electrical shock.

In most applications, resistors between the mains connections provide the discharge function. This resistive path always takes some power from the mains during operation. In the TEA1916 concept, these resistors are not required. To limit circuit current consumption during operation, the TEA19162 only activates the discharge function when required. It improves the no-load and low-load power consumption performance.

The SNSMAINS mains sensing function monitors the input voltage every cycle. When mains disconnection is detected, a special operation mode for the PFC MOSFET discharges the X-capacitors and the output capacitor of the bridge rectifier.

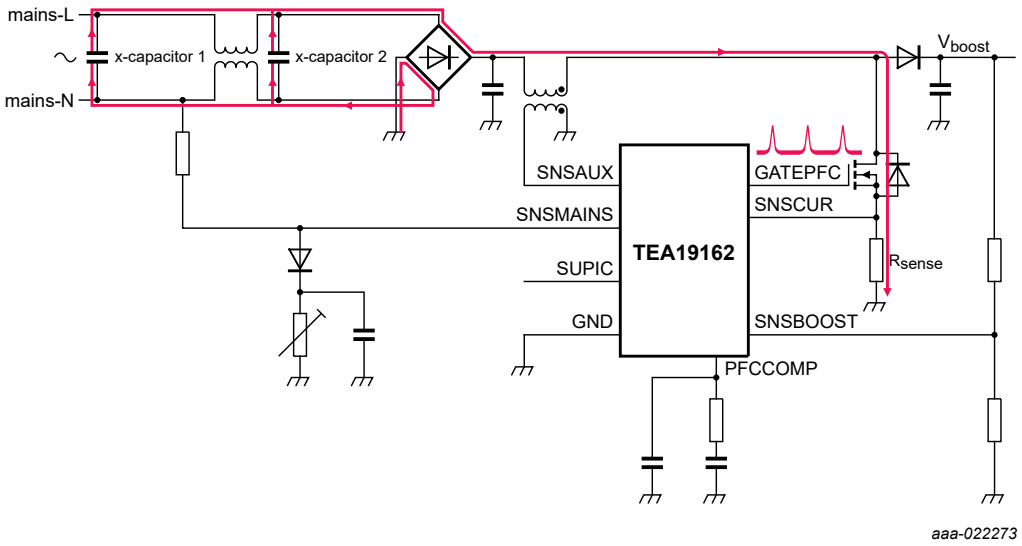


Figure 38. X-capacitor discharge with a PFC MOSFET discharge mode

8.18.1 Start active X-capacitor discharge

After the mains voltage is disconnected, the active X-capacitor discharge function is activated.

When the mains input voltage (and so also the measured current into the SNSMAINS pin) increases during the mains measurement, the system assumes the presence of a mains voltage. When the mains voltage does not increase (no positive dV/dt) for a minimum period of 120 ms, the X-capacitor discharge function is activated. The minimum period of 120 ms is measured starting from the time when the mains peak is reached.

When the active X-capacitor discharge function is activated, the X-capacitor is discharged in a special operating mode of an external PFC MOSFET (see Figure 38 and Figure 39).

8.18.2 X-capacitor discharge via a PFC MOSFET operation

During the PFC MOSFET operation for discharging the X-capacitor, several internal functions are used:

- SNSMAINS to detect when the mains voltage is interrupted or switched on again
- SNSCUR to measure the discharge current during each cycle
- GATEPFC to charge and discharge the gate of the external PFC MOSFET and to measure the resulting voltage on the GATEPFC pin

To avoid that the PFC output (boost) capacitor is charged, the X-capacitor discharge is not done continuously but in small discharge pulses. The external PFC MOSFET is slowly turned on until a small current is detected via a sense resistor. A slow increase of the voltage on the GATEPFC pin is achieved using an internal 26 µA current source that slowly charges the gate-source capacitance of the external MOSFET.

When 10 mV is measured on the SNSCUR pin, the internal current source of 26 µA is disabled and another internal current source of −26 µA is activated. As a result, the gate-source capacitance of the external MOSFET is discharged and the MOSFET is slowly turned off.

After the off-time discharge period ($t_{off(dch)}$), that can vary between 1.88 ms and 6.4 ms, the external MOSFET capacitance charge and discharge cycle is repeated. The duration of the charge and discharge pulses depends on the external MOSFET type used (different gate-source capacitance). For typical external MOSFETs, the pulse duration is shorter than 2 ms. So, the pulse period ($t_{rep(pulse)}$) is typically 4 ms (see Figure 39).

When the voltage on the GATEPFC pin exceeds 10 V, while the voltage on SNSCUR pin is still below 10 mV, a full discharge of the X-capacitor is assumed. The X-capacitor discharge operation is terminated. Unless the mains is reconnected or the system stops, the X-capacitor discharge function is activated again after 118 ms.

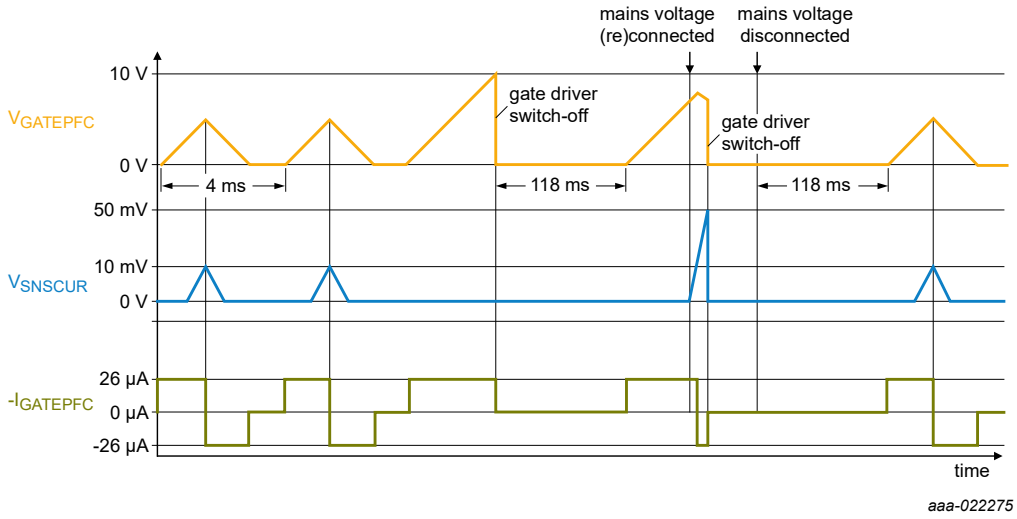


Figure 39. X-capacitor discharge operation

8.18.3 X-capacitor discharge calculations

The X-capacitors on the mains input circuit and the filter capacitors on the output of the mains rectifier are discharged. The total capacitance must be considered for calculation.

$$C_{total} = C_{xcap1} + C_{xcap2} + C_{filter1} + C_{filter2} \quad (20)$$

$$= 470\ nF + 470\ nF + 1000\ nF + 470\ nF = 2410\ nF$$

The time it takes to discharge C_{total} must be calculated starting from the worse case maximum mains voltage $V_{mains(max)}$ to the voltage level that is considered safe $V_{mains(safe)}$.

- $V_{mains(safe)}$ = 138 V
- $V_{mains(max)}$ = 373 V

There is a time delay between the moment that the mains disconnection is detected and the moment that the X-capacitor discharge starts.

- $t_{d(dch)xcap}$ = 118 ms

The average discharge current can be estimated as given in Section 8.18.3.1.

- $I_{dch(AV)}$ = 1.43 mA

The time to discharge can be calculated as given in Section 8.18.3.1

$$\Delta t_{dch} = t_{dch(xcap)} + \frac{C_{total} \times \left(V_{mains(max)} - V_{mains(safe)}\right)}{I_{dch(AV)}} \quad (21)$$

$$= 118\ ms + \frac{2410\ nF \times (373\ V - 138\ V)}{143\ mA} = 516\ ms$$

8.18.3.1 Estimation of average discharge current

The peak current during discharge can be calculated with the charge stop level on the SNSCUR pin and the value of the SNSCUR sense resistor.

$$I_{dch(peak)} = \frac{V_{stop(ch)SNSCUR}}{R_m} = \frac{10\ mV}{40\ m\Omega} = 250\ mA \quad (22)$$

The properties of the PFC MOSFET must be used to determine the duration of one discharge pulse. Here MOSFET example characteristics are used:

- Gate capacitance: C_{iss} = 1750 pF
- Gate threshold for conducting: V_{th} = 4.0 V
- Gate voltage for reaching $I_{dch(peak)}$: V_{peak} = 4.5 V
  This voltage is often not accurately specified. So, a best estimation must be used. The estimation value can be checked in the application.

With these values, a MOSFET constant for conduction can be defined.

$$K_{Idch\text{-}Vgs} = \frac{I_{dch(peak)}}{\left(V_{peak} - V_{th}\right)^2} = \frac{250\ mA}{(4.5\ V - 4\ V)^2} = 1\ A/V^2 \quad (23)$$

The time for charging and discharging the MOSFET gate is the same: $I_{ch(GATEPFC)} = I_{dch(GATEPFC)}$ = 26 µA.

$$t_{Vth} = \frac{C_{iss} \times V_{th}}{I_{ch(GATEPFC)}} = \frac{1750\ pF \times 4\ V}{26\ \mu A} = 269\ \mu s \quad (24)$$

$$t_{Vpeak} = \frac{C_{iss} \times V_{peak}}{I_{ch(GATEPFC)}} = \frac{1750\ pF \times 4\ V}{26\ \mu A} = 303\ \mu s$$

The average current during one pulse can be calculated with Equation 22:

$$I_{pulse(AV)} = \frac{1}{3} \times \left(\frac{V_{peak}}{t_{Vpeak}}\right)^2 \times \left(t_{Vpeak} - t_{Vth}\right)^2 \times K_{Idch\text{-}Vgs} \quad (25)$$

$$= \frac{1}{3} \times \left(\frac{4.5\ V}{303\ \mu s}\right)^2 \times \left(303\ \mu s - 269\ \mu s\right)^2 \times 1\ A/V^2 = 83.3\ mA$$

The average current during the complete discharge period includes the off-time.

- $t_{rep(pulse)}$ = 4 ms

$$t_{dch(AV)} = \frac{I_{pulse(AV)} \times 2 \times \left(t_{Vpeak} - t_{Vth}\right)}{t_{rep(pulse)}} \quad (26)$$

$$= \frac{83.3\ mA \times 2 \times (303\ \mu s - 269\ \mu s)}{4\ ms} = 142\ mA$$

8.18.4 Reconnecting the mains voltage while discharging

A positive dV/dt on the SNSMAINS pin detects the reconnected mains. If the mains is reconnected while the GATEPFC pin discharges the X-capacitor, the current through the external MOSFET rapidly increases to exceed 10 mV. When the voltage on SNSCUR exceeds 50 mV, the X-capacitor discharge function is terminated. At the same time, the internal driver for an external MOSFET is brought from the high-impedance mode to a normal operation mode. So, the external MOSFET is turned off like it is during normal operation.

8.18.5 HB disturbances during X-capacitor discharge

The X-capacitor discharge function is especially important at low output-load conditions. In this situation, the X-capacitor discharge because of converter switching, is small.

It is important to check and prevent disturbances of HB switching on the measured SNSCUR signal for X-capacitor discharge. Usually, the HB is switching in burst mode operation and the disturbances can happen when the HB switching is at the same time as the X-capacitor discharge. The disturbances can increase the discharge time.

8.18.6 Disabling X-capacitor discharge function

The X-capacitor discharge function can be disabled by adding a DC offset that exceeds 10 mV on the SNSCUR pin. Adding a DC offset can be done using a resistor connected to the SUPREG pin (see Figure 39). This small offset has a minor effect on the regular current sensing during operation and soft start.

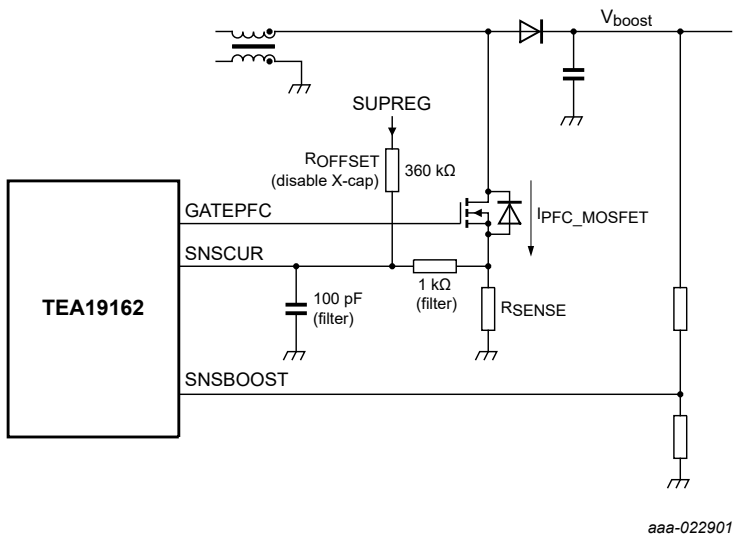


Figure 40. Disabling the X-capacitor discharge function

8.18.7 GATEPFC gate-source resistor value

In some applications, it is preferred to add a resistor between the gate and the source of the PFC MOSFET. The main reason is to prevent voltage drift on the gate that can cause an accidental switch-on.

The TEA19162 provides an active pull-down function that prevents false switch-on.

If a resistor is applied between GATEPFC to GND, the value must be 470 kΩ or higher to ensure full X-capacitor discharge functionality.

During X-capacitor discharge, the gate is charged with a small current of 26 µA. Current leakage of a parallel resistor must be limited. It prevents that the gate cannot be switched on anymore or that the GATEPFC voltage cannot reach the 10 V level to end the discharge procedure.

8.19 PFC burst mode

Based on the output power and the feedback level of the HBC converter, the HBC controller decides when the PFC enters the burst mode. Based on the SNSBOOST voltage level and the power requirement on the output, the HBC controller decides when the PFC starts switching and stops switching.

To provide the correct communication levels, the resistor from the SNSBOOST pin to GND must be 100 kΩ. In parallel, a noise suppression capacitor can be applied. The value of this capacitor must not affect the dynamic behavior too much. A few nanofarads are recommended.

8.19.1 PFC start and stop

8.19.1.1 Stop PFC

An internal current source of 6.4 µA in the TEA19161 HBC controller controls the PFC burst mode operation. When the current source is active, it lifts the voltage on the SNSBOOST pin and the PFC controller stops switching. Because the resistor on SNSBOOST is 100 kΩ, the voltage increases by 100 kΩ × 5 µA = 500 mV. Initially, the level increases from 2.5 V (normal regulation level) to 3 V. In burst mode, the voltage levels on the SNSBOOST pin slightly deviate because of the dynamic behavior.

8.19.1.2 Start PFC

While the PFC is not switching, the PFC output voltage decreases. The voltage on the SNSBOOST pin also decreases. When the SNSBOOST voltage decreases 100 mV, the HBC controller switches off the internal current source. So, the voltage on the SNSBOOST pin drops to below 2.8 V and PFC starts switching again.

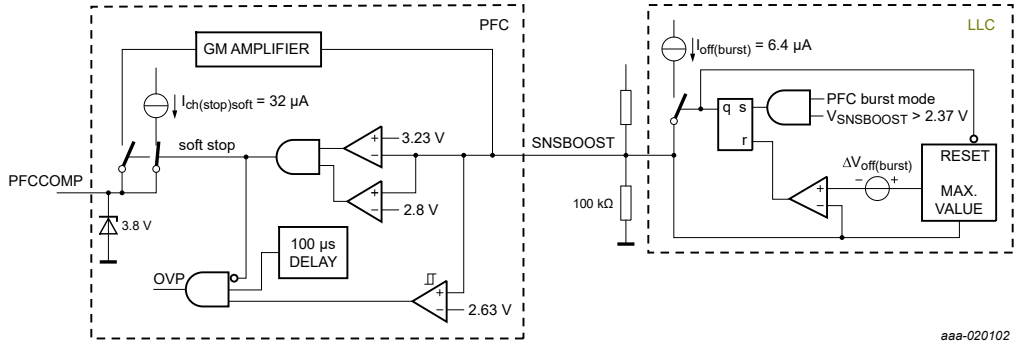
8.19.1.3 Stop PFC (burst mode)

During the PFC switching in burst mode, the PFC output voltage increases again. When the SNSBOOST voltage reaches 2.37 V, the HBC controller switches on the current source to pull up the voltage on the SNSBOOST pin. The PFC stops switching. To minimize audible noise, the PFC starts and stops using a soft-start and soft-stop procedure.

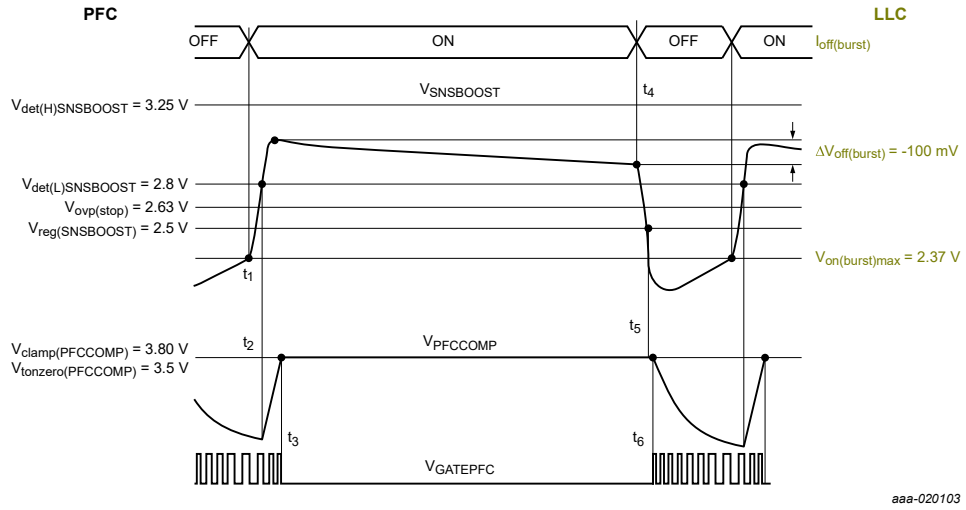
8.19.2 SNSBOOST levels

- **3.25 V**
  Overvoltage protection level in burst mode after the burst switching has ended with a soft stop.
- **2.8 V to 3.25 V**
  The voltage range in PFC burst mode when the HBC current source is active. The PFC does not switch and the PFC output voltage and the HBC current source set the voltage on the SNSBOOST pin.
- **2.8 V**
  Start PFC switching in burst mode. The HBC controller disables the current source to start PFC burst mode switching with a soft start.
- **2.63 V**
  PFC overvoltage protection. When the SNSBOOST reaches the OVP level during operation (PFC switching), the switching is stopped. The OVP function has a delay of 100 µs for general purposes and to prevent interference in burst mode during the transition from switching to not switching.
- **2.5 V**
  Regulation level of the internal error amplifier during PFC operation.
- **2.37 V**
  PFC stops switching in burst mode. The HBC controller enables the internal current source to stop PFC switching with a soft stop.

- **2.0 V**
  Latched protection reset level.
- **0.4 V**
  PFC open-loop protection.



a. Block diagram



b. Timing diagram

Figure 41. PFC burst mode control using the SNSBOOST pin

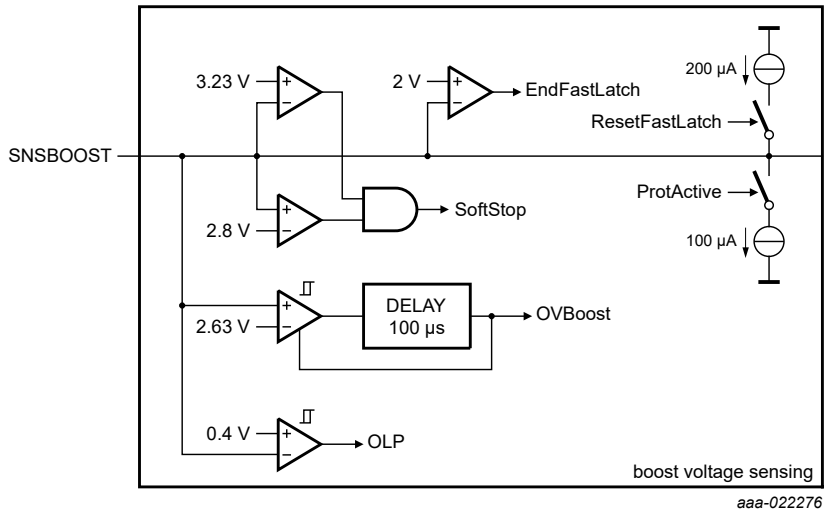


Figure 42. Internal block diagram SNSBOOST function

9 TEA19161 HBC functions

9.1 HBC start and SNSBOOST UVP

To ensure proper working of the HBC, the TEA19161T starts operating when the input voltage is higher than approximately 90 % of the nominal boost voltage ($V_{SNSBOOST(nom)}$ = 2.3 V). For the TEA19161T to start operating, the SUPIC start level must also be reached and the initial procedures completed.

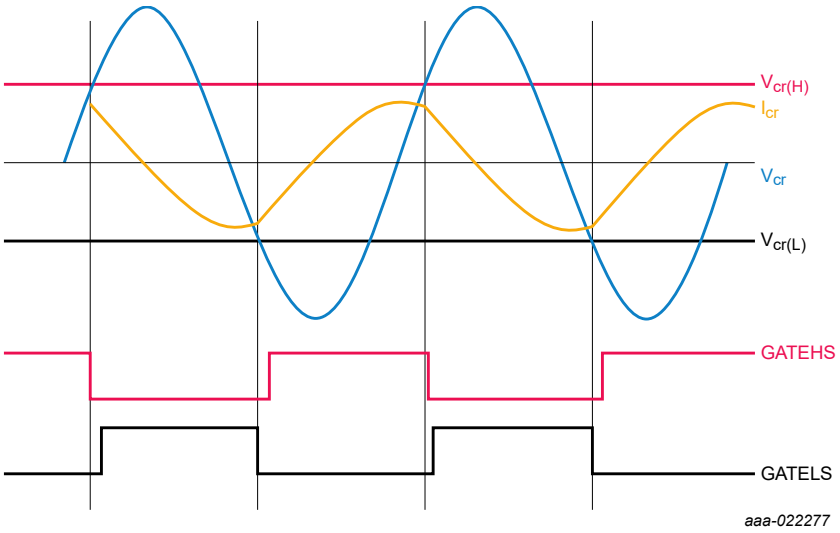
The voltage on the SNSBOOST pin is sensed continuously. When the voltage on the SNSBOOST pin drops to below 1.6 V and the low-side MOSFET is on, HBC switching is stopped. When the SNSBOOST voltage exceeds the start level of 2.3 V, the HBC starts/restarts.

9.2 Power regulation using V_{cap} control

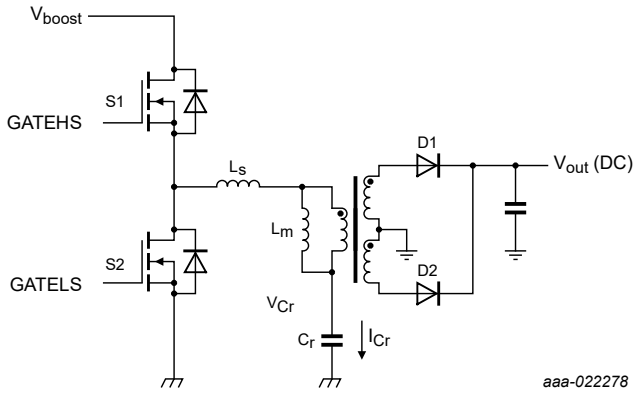
The TEA19161 uses the voltage across the resonant capacitor (V_{SNSCAP}) to control the output power. V_{SNSCAP} has a linear relationship with the output power. The voltage changes on the resonant capacitor are a result of the primary current that drives the power conversion.

The power can be controlled by switching off the gate drive at a certain V_{SNSCAP}. The adaptive non-overlap function drives the gate drive switch-on.

For higher power or lower power, the system feedback drives the V_{SNSCAP} levels.



a. Curve



b. Circuit

Figure 43. V_{cap} power control: switch-off at the required V_{SNSCAP} voltage level ($V_{hs(SNSCAP)}$ and $V_{ls(SNSCAP)}$)

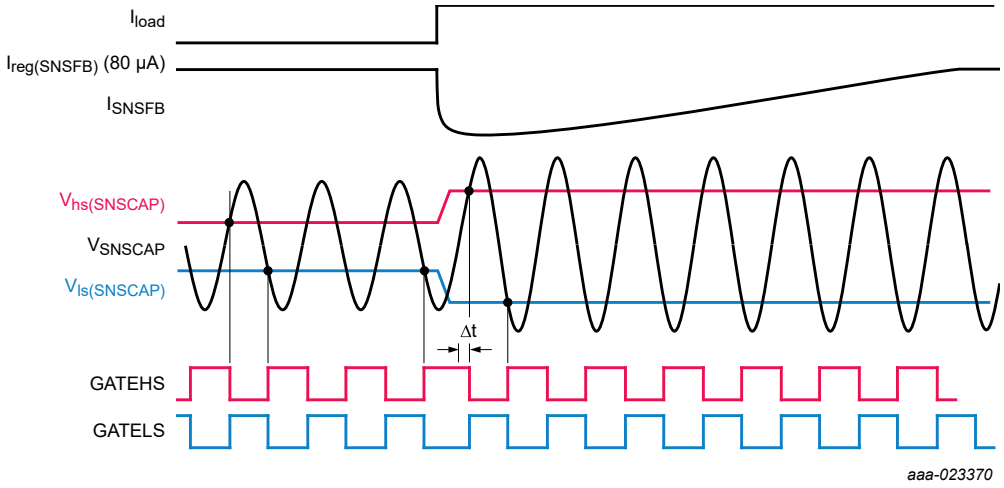


Figure 44. Example of changing V_{SNSCAP} levels ($V_{hs(SNSCAP)}$ and $V_{ls(SNSCAP)}$ at increasing output power)

9.2.1 Sensing V_{SNSCAP} with resistive and capacitive divider

A resistive and capacitive divider on the SNSCAP pin senses the voltage on the resonant capacitor. In parallel, a resistive divider provides DC information. The shape of the signal must not be distorted.

9.2.2 Scaling the V_{SNSCAP} range to the SNSCAP pin

The values of the divider must scale the voltage range for the output power to the available 3 V range on the SNSCAP pin. Because the SNSCAP pin is internally biased to 2.5 V, the minimum voltage on the pin is 1 V. The maximum voltage on the SNSCAP pin is 4 V.

The range used during normal operation is much smaller because V_{cap} control uses input voltage compensation and a power range of 200 %.

At nominal input voltage ($V_{SNSBOOST}$ = 2.5 V) and nominal (100 %) output power, $V_{hs(SNSCAP)}$ = 3 V and $V_{ls(SNSCAP)}$ = 2 V.

$$V_{hs(SNSCAP)} = 2.5 + \left(\frac{1.6\ V}{V_{SNSBOOST}} \times 0.0075\ V \times P_{out(\%)}\right) \quad (27)$$

$$V_{ls(SNSCAP)} = 2.5 - \left(\frac{1.6\ V}{V_{SNSBOOST}} \times 0.0075\ V \times P_{out(\%)}\right) \quad (28)$$

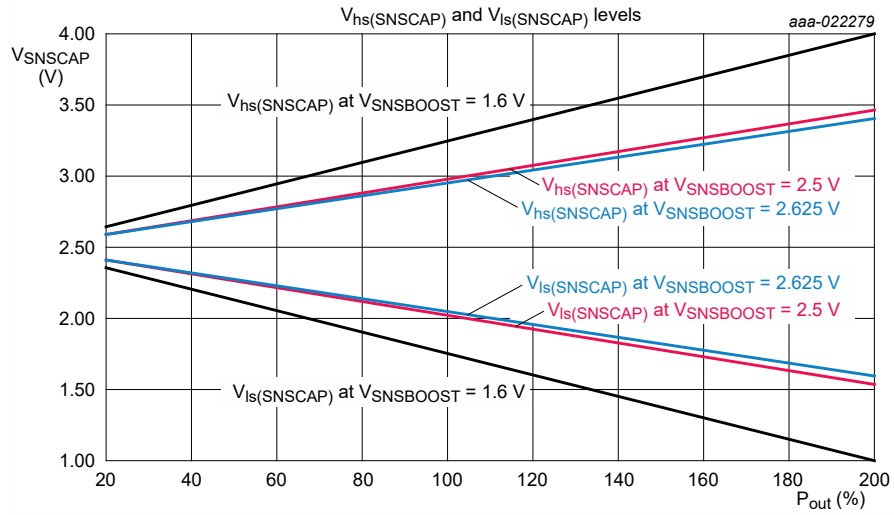


Figure 45. V_{cap} control: $V_{hs(SNSCAP)}$ and $V_{ls(SNSCAP)}$ levels on V_{SNSCAP}

The converter regulation of the SNSFB pin corrects any deviations in the regulation chain. The actual $V_{hs(SNSCAP)}$ and $V_{ls(SNSCAP)}$ levels can therefore deviate from the ideal values that are used for the nominal design.

These levels are valid for the HP mode. Below a preset power level, the LP mode is entered and the levels are recalculated to fit the correct $V_{hs(SNSCAP)}$ and $V_{ls(SNSCAP)}$ LP levels for operation.

9.2.3 Calculation of the SNSCAP divider value: $C_{SNSCAP(low)}$ and $C_{SNSCAP(high)}$

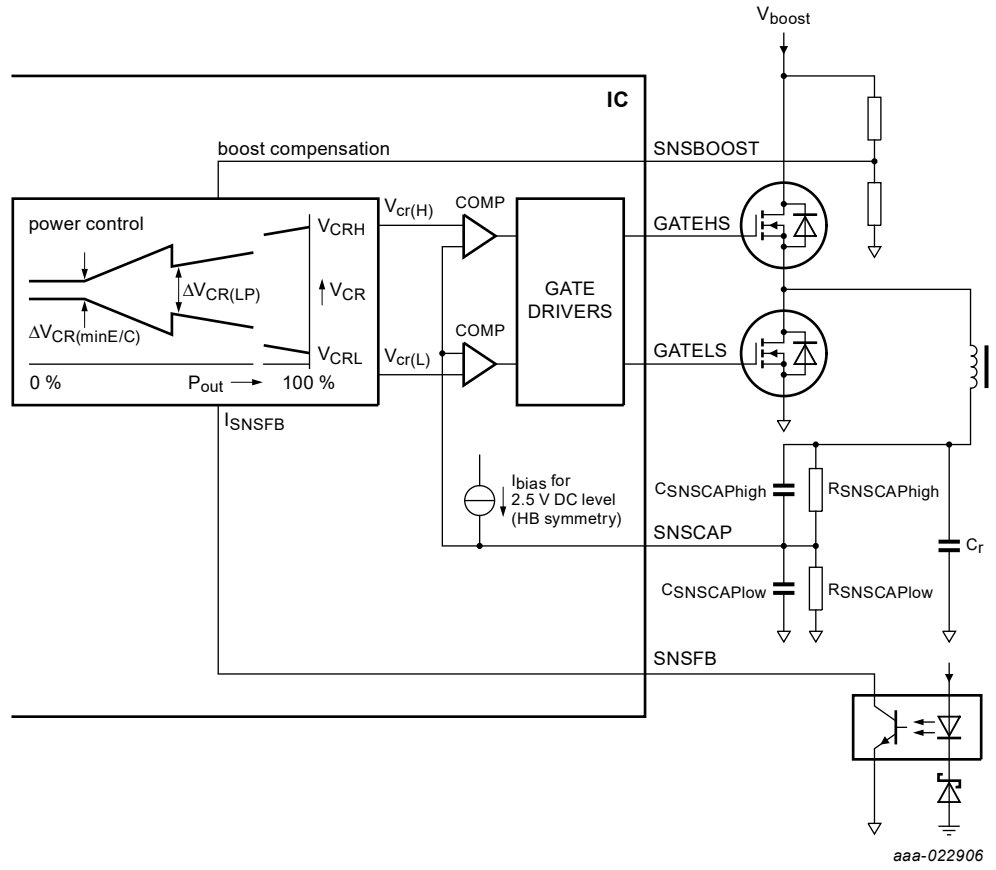


Figure 46. V_{SNSCAP} power control and SNSCAP sensing

The SNSCAP divider scales the voltage range on C_r down to the voltage range of the TEA19161. The capacitors provide the divider and the resistors contribute to the DC information to the SNSCAP pin.

The voltage on C_r depends on the output power and can be calculated with Equation 29.

$$V_{Cr(ideal)} = \frac{P_{out}}{V_{boost} \times C_r \times f_{HB}} \quad (29)$$

Because of a time delay between detecting a target power level and really switching polarity for the next half cycle, the voltage on C_r is slightly higher than in the basic calculation (see Section 10.7). When assuming the system is switching near the transition of DCM-CCM, the difference can be calculated with the primary magnetization current.

$$\Delta V_{Cr(d)} = \frac{I_{mag(peak)} \times \Delta t_d}{C_r} \quad (30)$$

For estimating the SNSCAP divider, a certain power level must be calculated with the voltage that the delay causes.

$$\Delta V_{Cr} = \Delta V_{Cr(ideal)} - \Delta V_{Cr(d)} \quad (31)$$

In practice, the C_r resonant capacitor consists of two capacitors in parallel. The main resonant capacitor and a capacitor in parallel to measure the resonant current. $C_{r\_total} = C_r + C_{r(par)}$. Because the value of the

measurement resistor R_m is small, its influence can be neglected and $C_{r(par)}$ can be considered a current source of the current divided by the two capacitors in parallel.

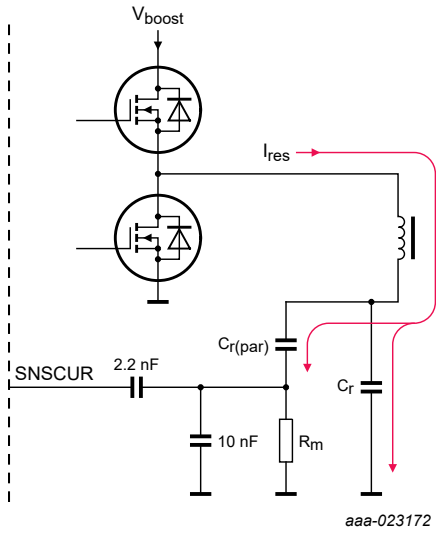


Figure 47. $C_{r\_total} = C_{r(par)} + C_r$

ΔV_{Cr} must match with the correct ΔV_{SNSCAP}.

For a 100 % power level at a nominal $V_{SNSBOOST}$ value (2.5 V), the voltage on the SNSCAP pin can be calculated with the equations in Section 10.7.

$$\Delta V_{SNSCAP} = 2 \times \frac{1.67\ V}{2.5\ V} \times 0.0075 \times 100 = 0.96\ V \quad (32)$$

The SNSCAP divider must match the 100 % power V_{Cr} with V_{SNSCAP} = 0.96 V.

Example for V_{Cr}:

$$\Delta V_{Cr} = \Delta V_{Cr(ideal)} - \Delta V_{Cr(d)} = \frac{240\ W}{390\ V \times 47\ nF \times 70\ Hz} - \frac{1.3\ A \times 450\ ns}{47\ nF} = 185\ V \quad (33)$$

According to this ratio, $C_{SNSCAP(low)}$ must be higher than the $C_{SNSCAP(high)}$.

$$C_{SNSCAP(low)} = \frac{\Delta V_{Cr} - \Delta V_{SNSCAP}}{\Delta V_{SNSCAP}} \times C_{SNSCAP(high)} \quad (34)$$

$$= \frac{185\ V - 0.96\ V}{0.96\ V} \times C_{SNSCAP(high)} = 192 \times C_{SNSCAP(high)}$$

9.2.4 Practical restrictions for SNSCAP divider

For the SNSCAP to function correctly, there are a few practical restrictions for designing the SNSCAP divider.

- Because the internal SNSCAP 2.5 V bias source can only source current, the divider must not cause the voltage on SNSCAP to exceed the DC-level of 2.5 V. The resistive divider ($R_{SNSCAP(low)}$ and $R_{SNSCAP(high)}$) part must ensure that the DC-level is not exceeded.
- For the bias source of SNSCAP to operate correctly, the resistor value of the $R_{SNSCAP(low)}$ between the SNSCAP and GND pins must be higher than 15 kΩ.
- During operation, the resistive part of the divider causes constant losses. It also causes constant losses during burst mode operation. To limit power losses, the total impedance must be high, for example, $R_{SNSCAP(low)} + R_{SNSCAP(high)}$ = 5 MΩ.

After implementing the estimated values, check the result to the OPP reference level in the real application. The power level for triggering OPP must be correct. If it is not, the divider values must be corrected to achieve a better result.

When the SNSCAP divider is correct, the mode transition levels can be modified with specific settings as given in Section 9.3.

9.2.5 HB symmetry regulation

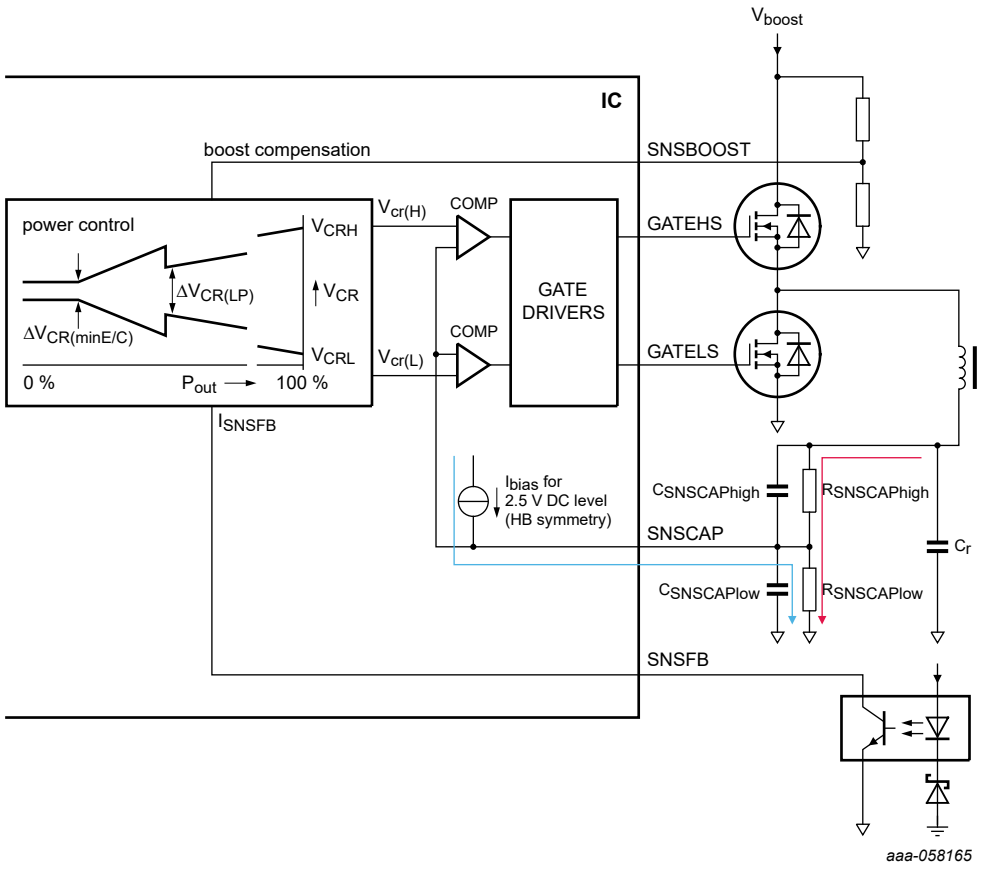


Figure 48. VSNSCAP power control and SNSCAP sensing

SNSCAP provides the symmetry regulation for a 50 % duty cycle switching. The regulation compares and equalizes the internal driver on-time periods. To make the internal on time periods equal, the system changes the bias current value (higher/lower) on the SNSCAP pin. This regulation works slower than the converter switching frequency for a correction within a few milliseconds.

The resistive divider and an internal current source that the HB symmetry regulation controlls determine the average (DC) bias voltage on the SNSCAP pin.Figure 48 shows the current flows for it.

The modified bias current for SNSCAP results in a small voltage offset in the switch-off target SNSCAP levels, which make one half-cycle shorter and the other half-cycle longer. Figure 49 shows the principle of how the SNSCAP bias voltage modifies the on-time of GATEHS and GATELS.

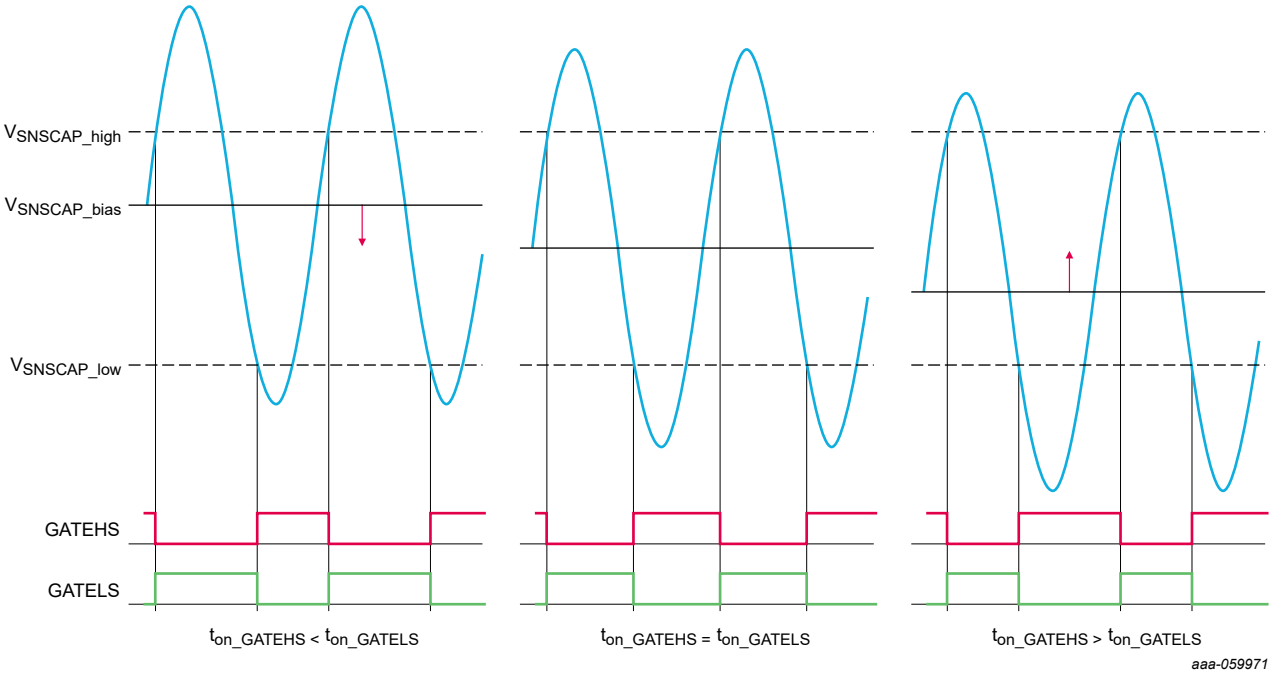


Figure 49. The principle of modifying the SNSCAP bias voltage to obtain HB symmetry

When $T_{GATEHS} > T_{GATELS}$, the SNSCAP bias voltage is increased by increasing I_{bias}. When $T_{GATEHS} < T_{GATELS}$, the SNSCAP bias voltage is decreased by decreasing I_{bias}. In this way, the HB duty cycle is regulated toward 50 %.

A changing bias voltage can be observed on the SNSCAP pin. A greater and smaller amplitude for SNSCAP compensates the usual voltage ripple on Vboost to keep the output power stable. These immediate changes can lead to some asymmetry, which the symmetry regulation corrects again. Because the symmetry regulation is working slower, a temporary asymmetry can be observed during the correction.

9.2.6 SNSFB regulation

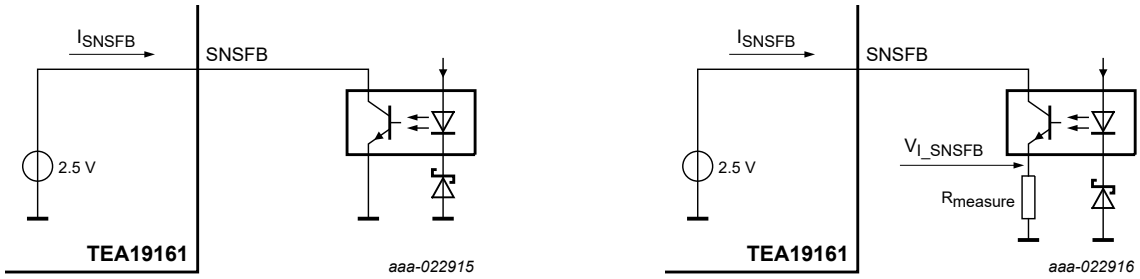
In the TEA19161, a special circuit is used to have a low current flowing in the feedback circuit continuously. The continuous low current helps to reach a very low power consumption of the converter at no-load or low-load conditions.

During LP and HP mode, an internal bias regulation slowly regulates the average current level in the SNSFB pin at 80 µA. During burst mode, the current varies but remains close to the burst start level of 100 µA.

The voltage on the SNSFB pin or the current in the pin does not directly show the power level of the converter. A method to monitor the regulation is to measure the current in the SNSFB pin by adding a measurement resistor for engineering purposes.

The voltage across the measurement resistor shows the regulation at transients or when changes occur. When running at a constant power level, the current in the SNSFB pin is always 80 µA in LP and HP mode. Because BM operation is based on periods of switching and not switching, there are transients continuously. So, the SNSBF current varies according to the output regulation with a burst start level at 100 µA in BM.

Figure 44, Figure 53, and Figure 54 show examples of the behavior of the current in the SNSFB pin.



a. Feedback circuit without $R_{measure}$

b. Feedback circuit with $R_{measure}$

Note: *For engineering work, a series resistor can be added to observe the SNSFB current behavior. 100 Ω or 1 kΩ are typical values for $R_{measure}$. Make sure that the measurement setup does not introduce any disturbances.*

Figure 50. SNSFB regulation

9.3 Operation modes

To reach a high efficiency at all power levels, the TEA19161 introduces a new operating mode: Low-Power (LP) mode. This mode operates in the power region between continuous High-Power (HP) mode switching and Burst Mode (BM) operation.

The LP mode itself has two power control modes, energy-per-cycle control and repetition frequency control. In total, the normal output power range is split into four operation modes.

- HP-mode (traditional continuous switching)
- LP-mode with energy-per-cycle control
- LP-mode with repetition frequency control
- Burst mode

To optimize the modes for application requirements, several parameters can be preset. Figure 51 shows an overview of the modes and the modifications that can be made using presets.

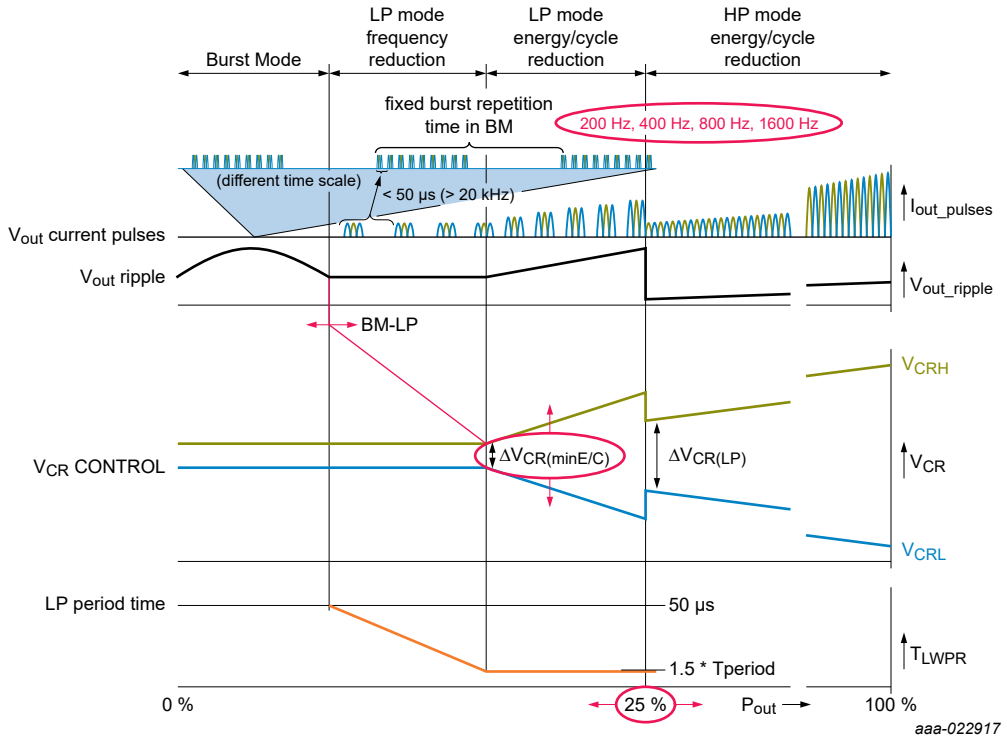


Figure 51. Operation modes and levels that can be modified with presets (in red)

9.3.1 High-power (HP) mode

The HP-mode operates in continuous HBC switching with a 50 % duty cycle, which is similar to the traditional LLC operation via frequency control. The TEA1916, however, obtains the result by V_{SNSCAP} control driving for voltage levels on the resonant capacitor instead of switching by time/frequency.

In all operation modes, the V_{SNSCAP} level determines when the gate drive is switched off. When the correct V_{SNSCAP} level for the required output power is reached, the gate drive is switched off.

The adaptive non-overlap function based on the HB end-of-slope detection switches on the gate drive.

9.3.2 Low-power (LP) mode

The low-power mode is a kind of burst mode at high repetition frequency. In this mode, the energy in each pulse is kept relatively high to provide a better conversion efficiency. During the not-switching period, the losses are low. To avoid audible noise, the repetition frequency of the complete LP cycle is higher than 23 kHz. The transition from HP-mode to LP-mode can be set at a certain power level with presets. To define the lower power part in the LP mode and the EC that it uses in BM, a minimum energy-per-cycle (ECmin) can be set. When using an ECmin, the efficiency over the complete power range can be kept at a high level. A higher ECmin provides a higher efficiency in the low-power range. So, the output ripple voltage becomes higher.

9.3.2.1 LP-mode switching

Each LP switching cycle consists of one conversion cycle and a period of no switching. To optimize transitions between switching and waiting, four extra events are added. These extra stages of the LP sequence minimize the losses in the converter transition from energy conversion to a period of waiting.

LP sequence:

1. First half of energy conversion
2. Second half of energy conversion
3. Energy dump preparation (also generates output power)
4. Energy dump
5. Waiting period
6. Energy restore

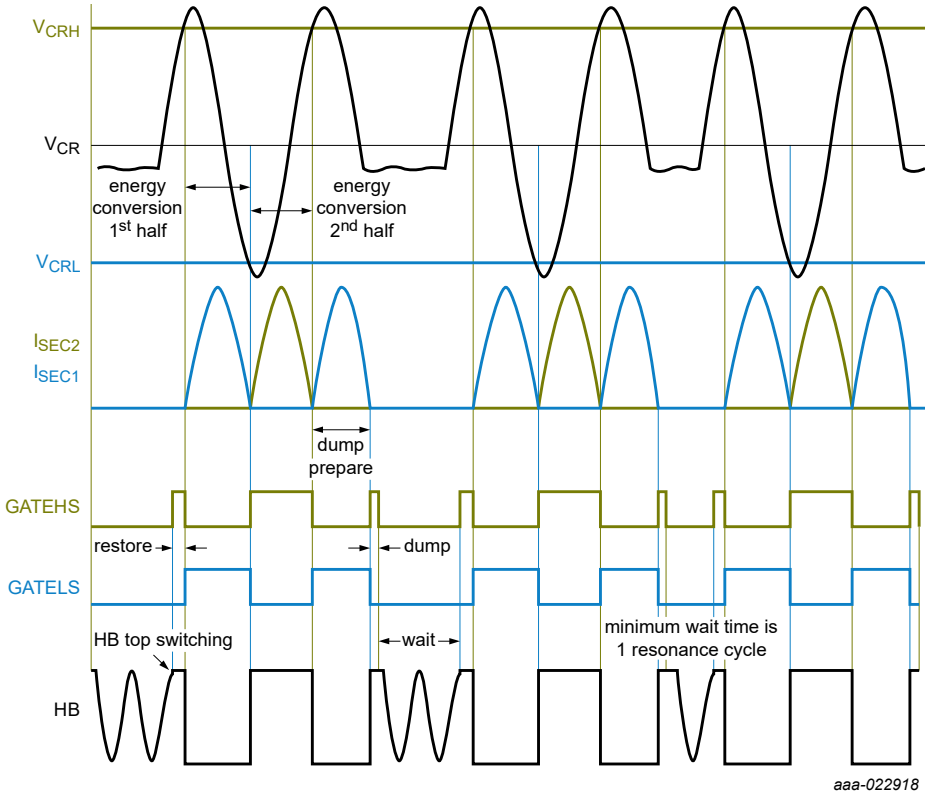


Figure 52. Low-Power (LP) mode switching

The energy conversion state

This stage is like normal conversion switching. The power level is in accordance with the required level in EC control or on ECmin during LP-RF control.

Energy dump preparation

The controller holds the energy in the primary resonant capacitor at a level that leads to a minimum primary current flowing after switch-off. In this way, losses during the waiting stage are minimized.

This stage is similar to the first half of the normal energy conversion state (GATELS on). However, the switch-off level is different. It is earlier than normal and leads to minor CCM switching on the output current. It is an important difference.

Energy dump

The energy dump and the energy dump preparation cause the primary capacitor to hold energy at a level where a minimum primary current flows after switch-off. The minimum current minimizes losses during the waiting stage. The energy dump consists of a short on-time for GATEHS.

Waiting period

The waiting period is the period of no switching where energy losses are minimal. This period reduces the average magnetization losses because there are no losses during the waiting period.

To minimize switching losses at the end of a waiting period, the restore stage starts when the voltage on the HB node is at the maximum level (top switching). The duration of the waiting period depends on the resonance behavior of the LLC. The minimum time of a waiting period is 1 resonance cycle. The duration can increase during the repetition frequency mode of LP, which leads to a waiting period of several resonance cycles.

Restore

To start the energy conversion after a waiting period, the resonant capacitor must be charged again to the correct V_{SNSCAP} level. The charging is done using a shorter GATEHS switch-on/off action. Top switching on the GATEHS shows hard switching of the HB.

Hard switching in LP

Two switching events include hard switching:

- The start of the restore using top switching
- The end of the dump preparation because of output CCM switching

Top switching causes the TEA1916 to optimize the switching for the start restore state. To prevent extra losses or voltage overshoot, CCM switching requires some application attention on the secondary switch (diode or SR).

Timeout for top switching

The internal HB dV/dt detection system is used during the waiting period to find the peak for starting a next LP cycle. If no peak is detected within 5 µs after the last peak was detected, a timeout switches on the high side to start the next LP cycle.

9.3.2.2 LP-mode with energy-per-cycle control

In the higher output power region of the LP mode, the energy control mechanism changes the power level via the amplitude of the 3 current pulses to the output.

9.3.2.3 LP mode with repetition frequency control

In the lower power part of the LP mode, modifying the duration of the waiting time controls the average energy. The energy in each LP cycle is according to the preset ECmin. A longer waiting time reduces the output power. This time can only be changed in discrete steps of 1 resonance cycle, because to achieve the best efficiency, the top switching must be ensured. At some power levels, the discrete number of LP cycles leads to constantly varying waiting times between two adjacent numbers of resonance cycles. For example, 2 and 3 resonance cycles, or 4 and 5 resonance cycles.

9.3.2.4 Audible noise in LP mode

In general, audible noise can occur when the power regulation is not stable. The result can be power variations, which occur in the audible frequency range.

In the LP frequency reduction mode, audible noise can happen when the output power is constantly changing, causing the LP cycles to switch between a different number of ringing cycles. No hysteresis is included for changing the number of ringing cycles in each LP cycle.

To minimize/prevent the risk of audible noise in this operation, extra attention must be given to regulation stability in this operation power range.

9.3.3 Burst mode operation

In burst mode, each burst consists of a series of LP cycles. The burst mode is a period of LP switching. Each LP cycle contains energy. The presets of the ECmin determine the level of this energy in burst mode (ECmin). The wait time of the LP cycle is now fixed as in the transition from RF/LP mode to burst mode.

Presetting of the resistor value on the SNSOUT pin fixes the repetition frequency or time for the bursts. The preset values are 200 Hz, 400 Hz, 800 Hz, or 1600 Hz (see Table 5 and Table 6).

To control the average output power, the number of LP cycles in a burst mode is variable. An internal algorithm that targets the fixed repetition frequency for a burst determines the required number of LP cycles in the burst mode.

When the output power drops to below the power level corresponding to 1 LP cycle with the target burst repetition frequency, the time between 2 LP pulses is further increased. The result is a lower BM repetition frequency than preset.

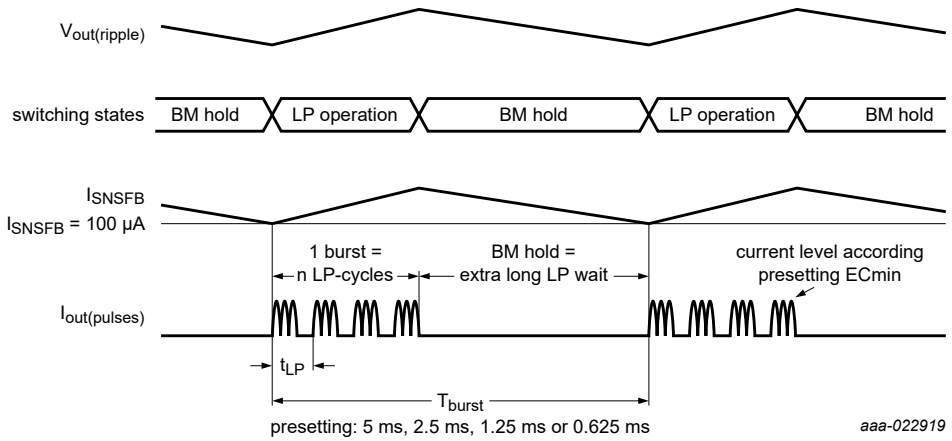


Figure 53. The burst mode system consists of LP switching and BM hold time

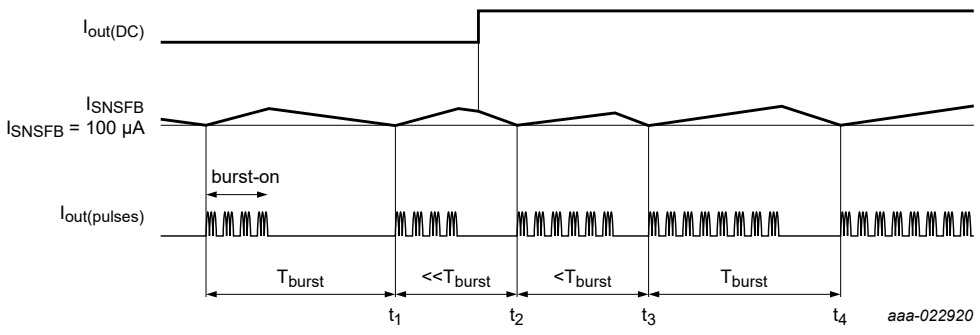


Figure 54. Regulating the number of LP cycles in a burst to adapt to a new output load for the same T_{burst}

9.3.4 Mode presetting

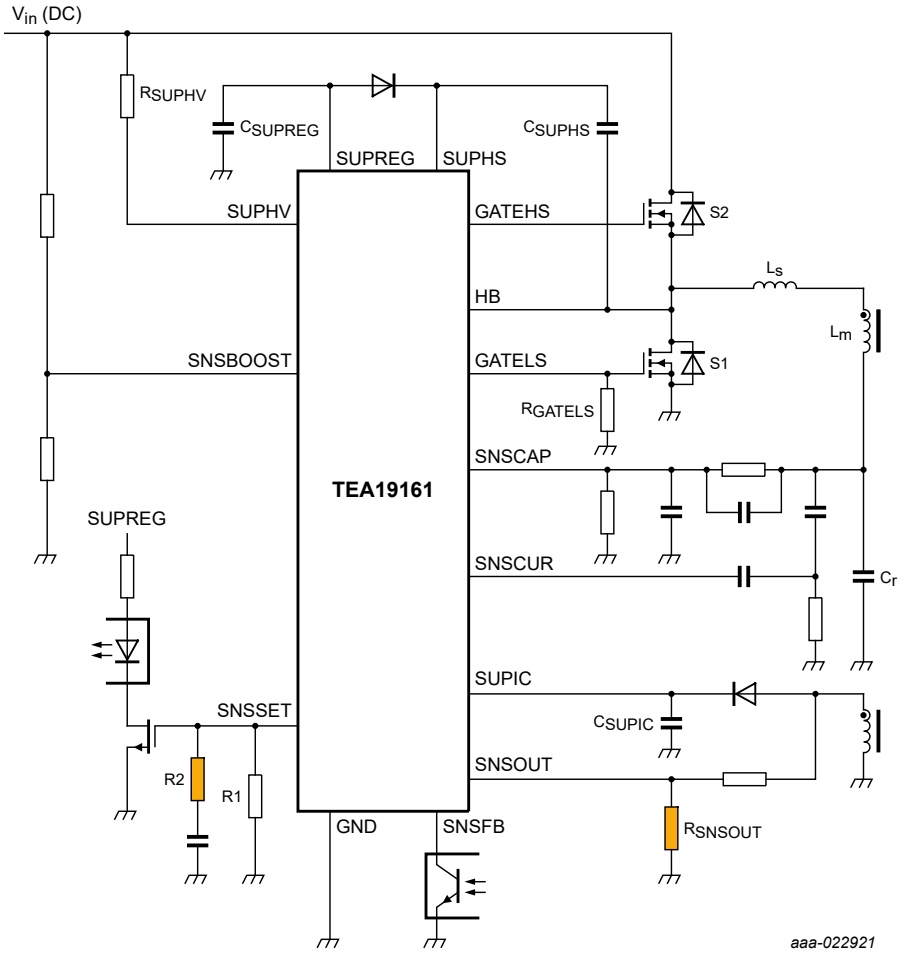


Figure 55. Mode presetting with the values of SNSSET R2 and R_{SNSOUT}

Table 5. Presetting for HP to LP transition and BM to LP transition

R2 (kΩ)	Burst repetition frequency [1]	200 Hz	400 Hz	800 Hz	1600 Hz
	R_{SNSOUT}	22 kΩ	15 kΩ	10 kΩ	6.8 kΩ
	HP to LP transition (% of nominal power) [2]	BM to LP transition (% of nominal power) [3]			
1	25	9	9	9	9
6.8	25	12	12	12	12
15	37.5	9	9	9	10
27	37.5	12	12	12	13
47	50	9	10	11	12
82	50	12	13	15	17
180	62.5	9	10	12	14
open	62.5	12	15	17.5	20

[1] Resistor R_{SNSOUT} can set the burst repetition frequency: 4 values.
[2] HP to LP transition can be set by the R2 value on the SNSSET pin: 4 values.
[3] ECmin level or BM level can be set by the R2 value on SNSSET: 2 values depending on the value of R_{SNSOUT}.

Table 6. Presetting for HP to LP transition and ECmin

R2 (kΩ)	Burst repetition frequency [1]	200 Hz	400 Hz	800 Hz	1600 Hz
	R_{SNSOUT}	22 kΩ	15 kΩ	10 kΩ	6.8 kΩ
	HP to LP transition (% of nominal power) [2]	ECmin (% of nominal power) [3]			
1	25	5	5	5	5
6.8	25	9	9	9	9
15	37.5	5	5	5	6
27	37.5	9	9	9	11
47	50	5	6	7	9
82	50	9	10	14	17
180	62.5	5	7	9	11
open	62.5	9	14	18	23

[1] Resistor R_{SNSOUT} can set the burst repetition frequency: 4 values.
[2] HP to LP transition can be set by the R2 value on the SNSSET pin: 4 values.
[3] ECmin level or BM level can be set by the R2 value on SNSSET: 2 values depending on the value of R_{SNSOUT}.

The values in Table 5 and Table 6 include the additional shift due to a fixed internal time delay (150 ns) and a typical application delay (300 ns). With an external resistor and capacitor, these transition levels can be modified to a new table of values.

9.3.5 Mode transitions

9.3.5.1 HP to LP transition

The value of resistor R2 on the SNSSET pin presets the HP to LP transition. 25 %, 37.5 %, 50 %, or 62.5 % of the nominal converter power can be chosen.

At the HP to LP transition point, the energy-per-cycle in LP-mode is compensated (more energy) for the same average power level in HP-mode. The compensation provides a smooth regulation transition between the modes.

9.3.5.2 LP to EC/RF transition

In the LP-mode two submodes are used:

- LP-mode with energy-per-cycle control
- LP-mode with repetition frequency control

The transition between both submodes can be influenced by presetting the minimum energy per cycle (ECmin). A combination of the resistor R2 value on the SNSSET pin and the resistor value on the SNSOUT pin sets the ECmin. It is expressed in a percentage of the total SNSCAP voltage range that represents the output power.

Extra:

If the presetting is made for ECmin = 9 % in a 200 W converter, the transition between the two LP modes is an output power of approximately 200 W × 9 / 100 = 18 W.

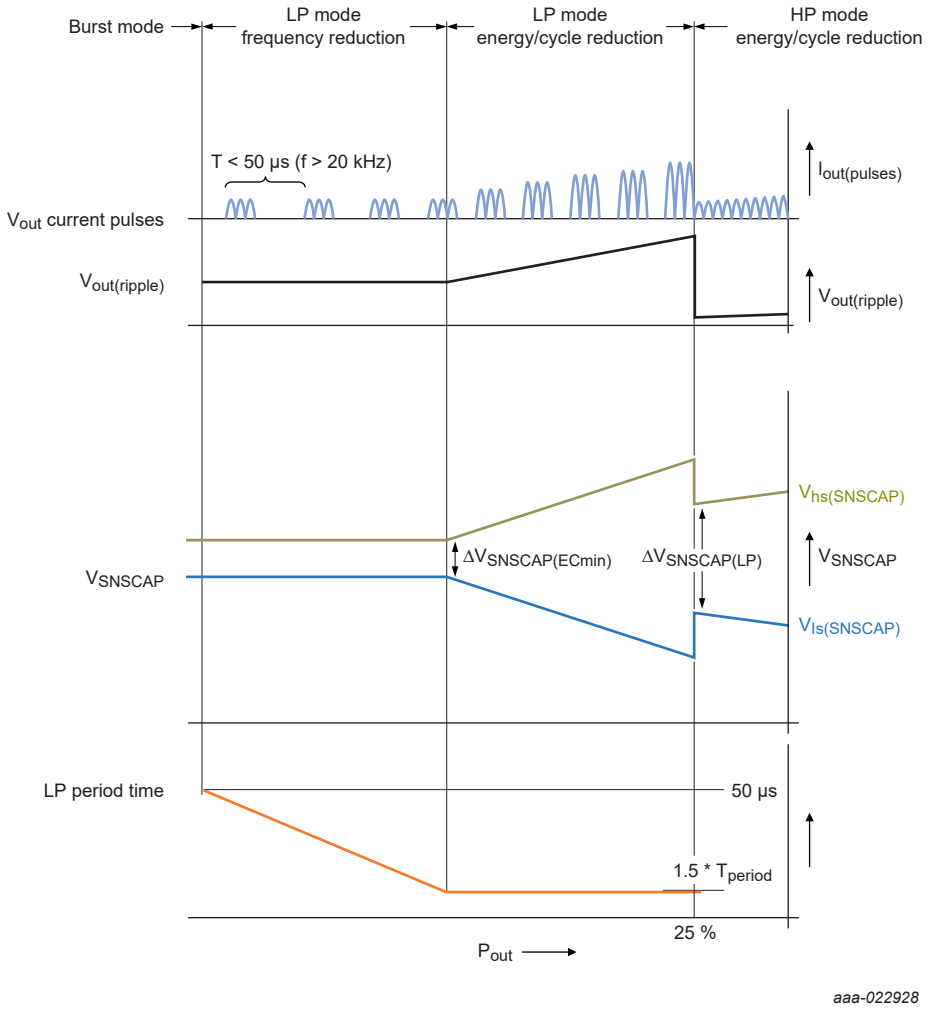


Figure 56. LP modes: regulation and transitions

9.3.6 LP to BM transition

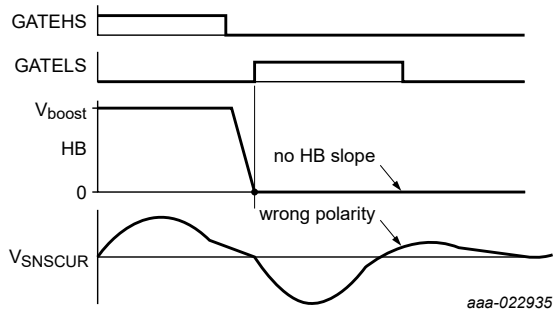
The choice for ECmin also slightly influences at which power level LP mode switches over to BM operation. At a low ECmin, the LP to BM transition is at a lower output power level.

To enter BM, the LP repetition frequency reaches 23 kHz. To make sure that with some tolerance the repetition rate in LP remains above 20 kHz, 23 kHz is the typical value for this parameter.

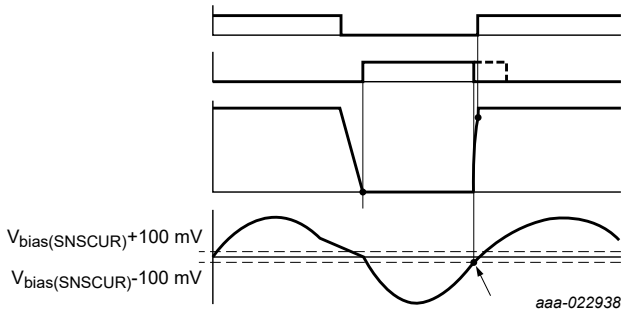
The output power level at which the LP to BM transition takes place (reaching 23 kHz) also depends on other system timings, like the resonance frequency and the HBC operating frequency.

9.3.7 Capacitive mode prevention using the SNSCUR pin

The primary current is measured accurately, cycle-by-cycle, for the internal switching logic. Two comparators of 100 mV above and below the 2.5 V bias voltage detect when the primary current is approaching capacitive mode operation. When this level is reached before V_{SNSCAP} control switches off the gate, the capacitive mode prevention forces a switch-off. This switch-off prevents capacitive mode switching.



a. Signals when running into capacitive mode operation



b. Capacitive mode prevention. When ±100 mV level is detected, GATEHS/LS is switched off.

Figure 57. Capacitive mode protection/prevention

9.3.7.1 Practical application of CMR switching

Normally, design choices can prevent capacitive mode switching. But for some applications, performance parameters like system efficiency, can only be met if switching near capacitive mode is allowed when the input voltage V_{boost} decreases. The CMR function in the TEA19161 supports operation near capacitive mode by keeping the switching inductive at the border of the capacitive mode region. When the CMR is active, the output power is limited. The result is often a decrease of the voltage on the output.

9.3.7.2 Measuring the voltage on the SNSCUR pin

The voltage on the SNSCUR pin is difficult to measure because attaching a probe seriously disturbs operation. An internal bias source puts the input signal on a 2.5 V DC voltage level. A 2.2 nF capacitor connects the AC voltage that represents the resonant current signal to this pin. The AC voltage part can best be checked on the measurement resistor R_m.

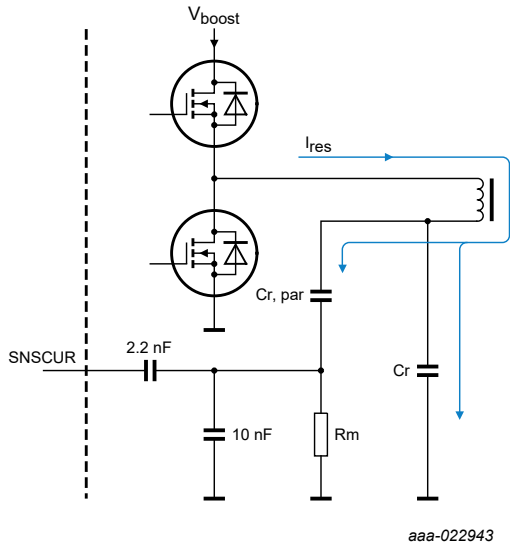


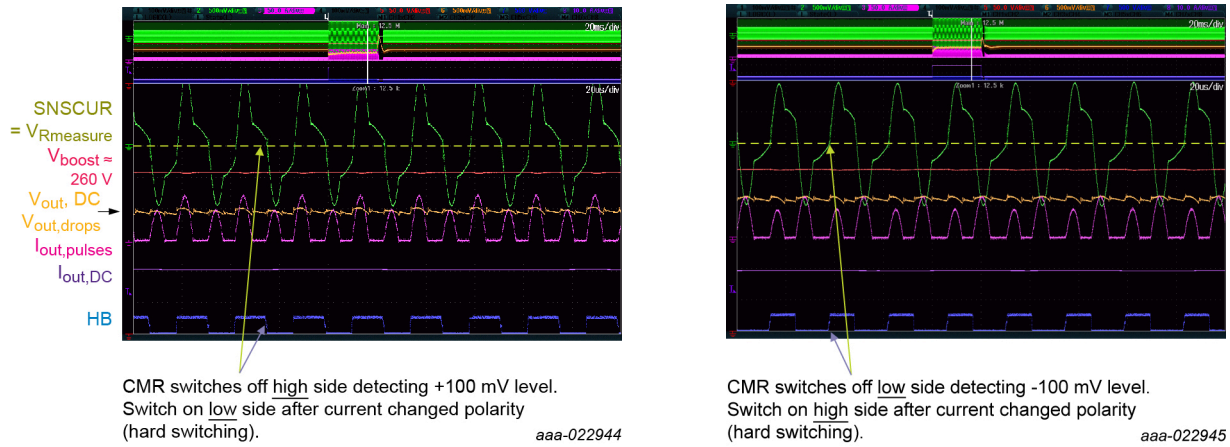
Figure 58. Typical current sensing circuit for SNSCUR

9.3.7.3 Example of CMR switching in a test condition

To observe the switching behavior during CMR, the input voltage of the HBC, V_{boost} is supplied by a DC source of a very low operating voltage of approximately 260 V ($V_{boost(nom)}$ = 390 V). In this way, the converter cannot deliver more than nominal output power. When a higher peak load occurs, the system starts running in CMR.

The CMR GATEHS or GATELS switch-off moment is close to the zero current level. The result is a small asymmetry and a deviation from the 50 % duty cycle target. Because the system regulates switching to a 50 % duty cycle operation, it gradually changes the switching timing to achieve it, causing the CMR timings to change over time.

Figure 58 shows a steady state CMR switching when +100 mV is detected and when −100 mV is detected.



a. Detection +100 mV level

b. Detection −100 mV level

Figure 59. Example of running in CMR during a test condition when V_{boost} is very low

To set the CMR to the best level in an application, the value of the resistor R_m can be modified. The value of R_m also determines the OCP level. Normally, both levels are not critical. A good value can be chosen. If a conflict remains, the option given in Section 14.3.8 can be considered.

10 Presetting TEA1916 functionality and power good

Before the system starts operation, it reads the external settings. Several internal settings can be defined with specific values for resistors at GATELS, SNSSET, and SNSOUT. These settings cannot be changed during operation. They are refreshed at each start or restart. The resistors are:

- GATELS resistor R_{GATELS}
- SNSSET resistor R1
- SNSSET resistor R2
- SNSOUT resistor R_{SNSOUT}

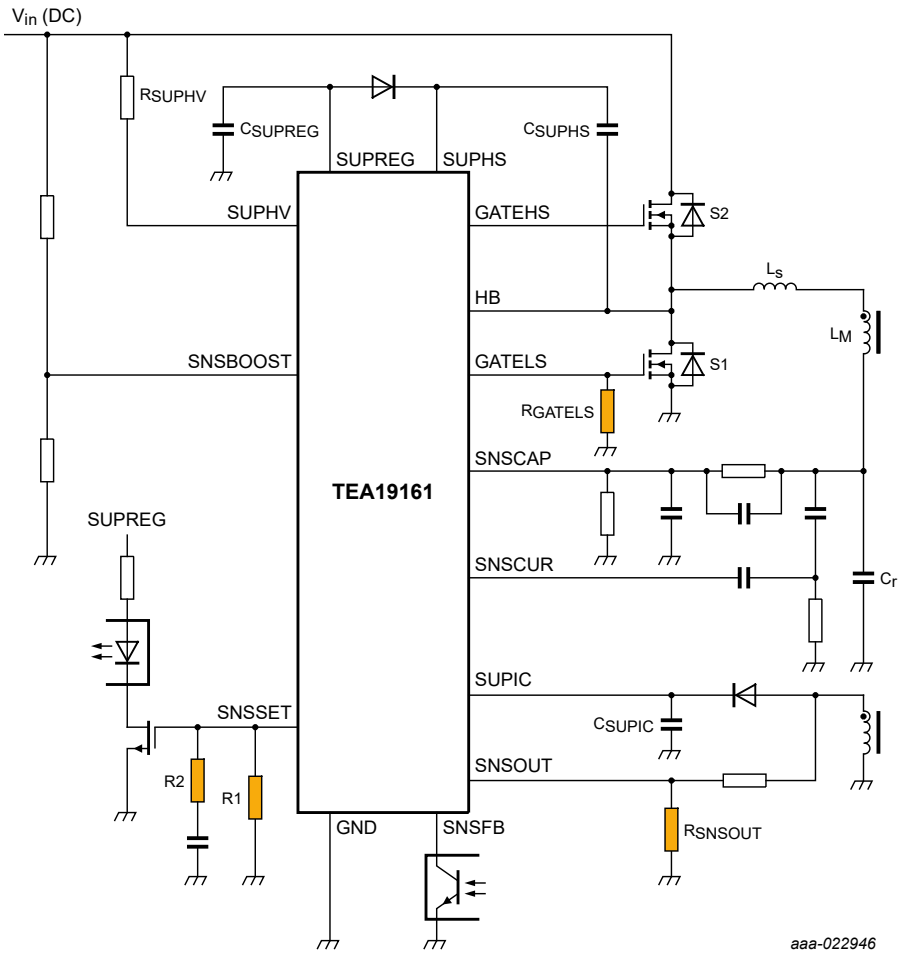


Figure 60. Presetting TEA1916 using values of four resistors

10.1 Setting the soft start power level (R_{GATELS})

To limit the power in each cycle at start-up, the VSNSCAP control switching levels are given an offset.

During start-up, the slope compensation makes a sweep of 12 ms. The maximum start-up time is 12 ms. However, under normal conditions the start-up time is much shorter.

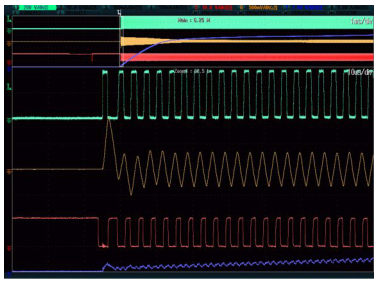
The level of compensation that is used at start-up can be optimized with the value of resistor R_{GATELS}. The range of values for resistor R_{GATELS} is: $100\ k\Omega \leq R_{GATELS} \leq 300\ k\Omega$

Any value within this range can be applied. The value is sampled in 255 steps accuracy which approaches an analog setting. At 100 kΩ, the amount of energy in the first cycle is smallest and at 300 kΩ it is highest.

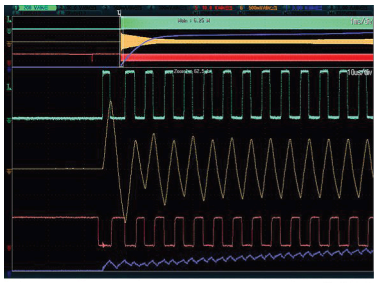
This optimization function depends strongly on the application converter properties and behavior. So, when the behavior of the primary current and the output voltage increase are monitored, experimenting must determine the value. A typical value is 180 kΩ.

During the start-up slope, functions that are also active during normal operation can influence the behavior.

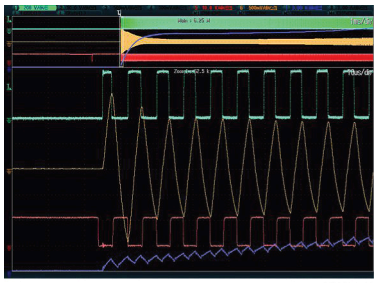
- SNSBOOST pin: compensation for lower input voltage
- Symmetry regulation to keep the duty cycle close to 50 %
- SNSFB: start regulation when the nominal output voltage is reached



a. R_{GATELS} = 120 kΩ



b. R_{GATELS} = 180 kΩ



c. R_{GATELS} = 240 kΩ

- (1) HB (light blue signal)
- (2) SNSCUR ($V_{Rmeasure}$; orange signal)
- (3) GATELS (red signal)
- (4) V_{out} (purple curve)

Figure 61. Start-up behavior at different values for resistor R_{GATELS}

10.1.1 Soft-start sweep

The soft start results in gradually increasing the target SNSCAP levels at which the drivers switch off. It provides a linear increase of output power until the feedback regulation takes over when the output voltage is reached.

If the feedback regulation or protections do not intercept, the soft start ends in a 200 % power level after 12 ms. The starting power level depends on the setting of R_{GATELS}.

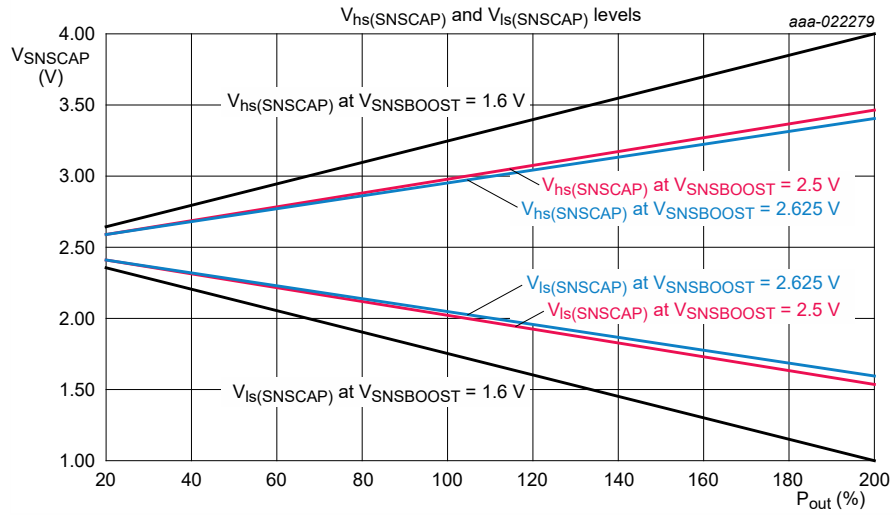


Figure 62. V_{cap} control: $V_{hs(SNSCAP)}$ and $V_{ls(SNSCAP)}$ levels on V_{SNSCAP}

During the soft-start sweep, the boost voltage compensation and the symmetry regulation are active to help increase the power in a linear way.

Note: *During the soft start, the resulting switching frequency depends strongly on the converter design. Because the relationship between the output power and the frequency is not linear, the soft start of the TEA19161 does not provide a linear frequency sweep.*

10.2 Protection mode and OPP setting (SNSSET resistor R1)

Table 7. Protection mode and OPP setting (SNSSET resistor R1)

SNSSET R1	Power limit	Start OPP timer	Start OPP timer at start-up	OPP time to protection	Protection mode	End of power good timer
< 10 kΩ	no start-up					
46.4 kΩ	200 %	no OPP (only 200 % power limit)				
53.6 kΩ	200 %	175 %	170 %	200 ms	1 s restart	190 ms
61.9 kΩ	200 %	175 %	170 %	50 ms	1 s restart	45 ms
71.5 kΩ	150 %	125 %	120 %	200 ms	1 s restart	190 ms
82.5 kΩ	150 %	125 %	120 %	50 ms	1 s restart	45 ms
95.3 kΩ	200 %	175 %	170 %	200 ms	latched	190 ms
110 kΩ	200 %	175 %	170 %	50 ms	latched	45 ms
127 kΩ	150 %	125 %	120 %	200 ms	latched	190 ms
147 kΩ	150 %	125 %	120 %	50 ms	latched	45 ms

The SNSSET resistor R1 settings consist of two major categories:

- Safe restart protection mode
- Latched protection mode (also available in the CT-versions)

Each category has four basic subcategories:

- OPP just above nominal power with 50 ms timer
- OPP just above nominal power with 200 ms timer
- OPP at a high power level with 50 ms timer
- OPP at a high power level with 200 ms timer

In addition to the main categories there are two special modes:

- No OPP function and power limited at 200 %
- Start-up disabled

To ensure that the OPP level is in accordance with the chosen setting, the external capacitive/resistive divider on the SNSCAP pin must be designed and optimized. The chosen setting can be a 125 % or a 175 % power level. The OPP level must be used as the main reference for the SNSCAP divider design.

When the V_{SNSCAP} ($V_{hs(SNSCAP)}$ − $V_{ls(SNSCAP)}$) exceeds the $V_{opp(SNSCAP)}$ voltage difference, an internal counter is started. When this counter exceeds the chosen value of 50 ms or 200 ms, the system enters a latched/safe restart protection as defined by the external settings.

The voltage difference between $V_{hs(SNSCAP)}$ and $V_{ls(SNSCAP)}$ is also limited to the preset maximum power level of 150 % or 200 %. If the output load of the LLC converter exceeds the maximum power level, the output voltage decreases because the power delivered by the LLC converter is limited.

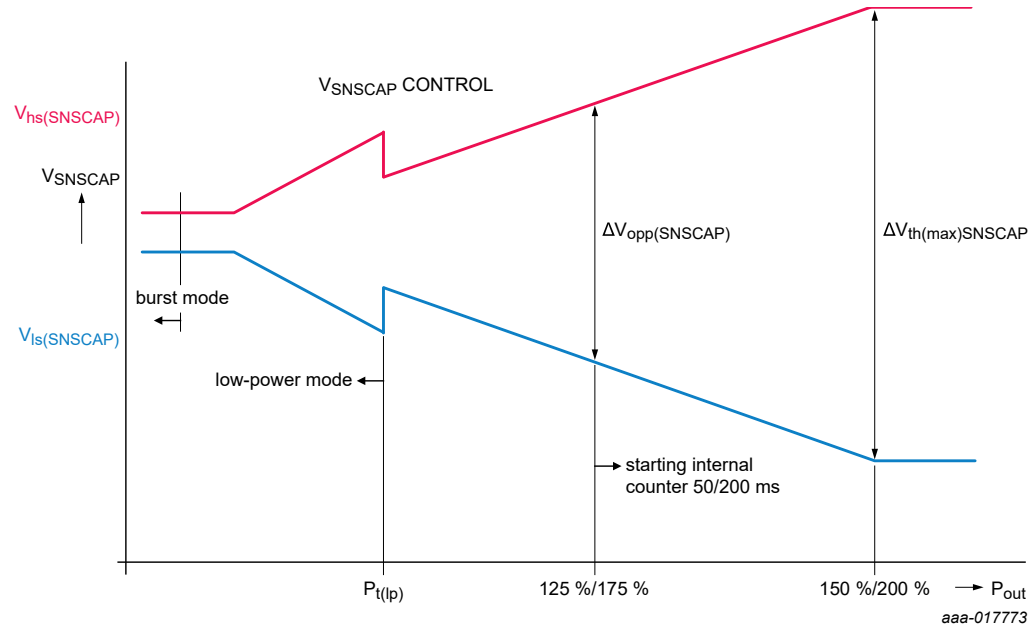


Figure 63. V_{SNSCAP} control range and OPP

10.3 Power good (PG) function

For housekeeping the total system, a power good signal can be used to communicate a basic message to the application that is supplied by the power supply.

- Power delivery is stable after start-up; power supply is OK.
- Power delivery (soon) goes down; power supply is (soon) not OK.

The TEA1916 supports the PG function by making the SNSSET output pin high or low, depending on the state of the power supply. The SENSSET pin is also used for settings during a short moment at start-up.

The SNSSET output is made active high after the settings are measured. This condition shows that the output is not yet OK because the output is at start-up.

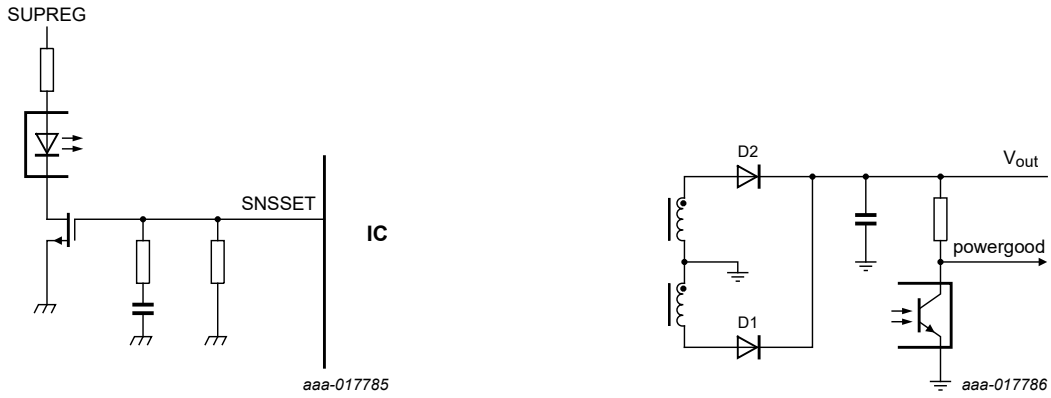
To show that the output is OK, the SNSSET output is pulled low when the system enters the operating state.

To provide a warning that the power delivery soon stops, the SNSSET output becomes active high when:

- The voltage on the SNSBOOST pin drops to below 1.95 V.
- The OPP timer is 5 ms or 10 ms before its end value.

When the system enters another protection mode (OVP, OCP, UVP, or OTP), the SNSSET pin is also pulled high. However, switching is stopped immediately.

Figure 64 shows a typical PG circuit. A pull-up circuit on the primary and the secondary sides, connected using an optocoupler, provides the PG signal to the application that is supplied by the power supply.



a. Primary side

b. Secondary side

Figure 64. Typical power good circuit

10.4 SNSSET R2: Power level for HP-LP transition

Presetting the HP/LP transition is done with the value of resistor R2 on SNSSET. The possible options are: 25 %, 37.5 %, 50 %, and 62.5 % of the nominal converter power.

At the HP/LP transition point, the energy-per-cycle in LP mode is compensated (higher) for the same average power level in HP mode. It provides a smooth regulation transition between the modes.

Table 8. Power level settings HP-LP transition

SNSSET R2	HP-LP transition level
1 kΩ	25 %
6.8 kΩ	25 %
15 kΩ	37.5 %
27 kΩ	37.5 %
47 kΩ	50 %
82 kΩ	50 %
180 kΩ	62.5 %
open	62.5 %

Two resistor values give the same transition level. The difference between the values is that they set a different minimum energy-per-cycle level for the LP mode (see Section 10.7).

The values in Table 8 include the additional shift due to a fixed internal time delay (150 ns) and a typical application delay (300 ns). These transition levels can be modified to a new table of values using an external resistor and capacitor.

10.5 Capacitor value for the SNSSET pin

To measure the values for resistors R1 and R2 on the SNSSET pin, a capacitor is used in series with resistor R2. For reliable measurement, the value of this capacitor must be according to Table 9.

Table 9. SNSSET capacitor (C_{SNSSET} (nF)) value versus resistor values

	1	6.8	15	27.0	47	82.0	180	open	R2 (kΩ)
46.4	33	33	33	33	33	22	12		
53.6	33	33	33	33	33	22	12		
61.9	33	33	33	33	33	22	12		
71.5	33	33	33	33	22	22	12		
82.5	33	33	33	22	22	22	12		
95.3	33	33	22	22	22	12	12		
110	22	22	22	22	22	12	12		
127	22	22	22	22	12	12	12		
147	22	22	22	12	12	12	12		
R1 (kΩ)									

10.6 R_{SNSOUT}: Burst repetition frequency

The fixed burst repetition frequency can be set with the resistor value on the SNSOUT pin.

A lower repetition frequency reduces the risk of audible noise. However, it gives a higher output voltage ripple in burst mode. Determining the best resistor value on the SNSOUT pin depends on the requirements for the power supply.

Table 10. Burst repetition frequency settings

R_{SNSOUT}	Burst repetition frequency
22 kΩ	200 Hz
15 kΩ	400 Hz
10 kΩ	800 Hz
6.8 kΩ	1600 Hz
< 1.5 kΩ	start-up disabled

The minimum energy-per-cycle (ECmin) also influences the burst mode operation sequences. For each burst repetition frequency, there is a choice for two ECmin values that can be set with resistor R2 of the SNSSET pin.

The SNSOUT pin also includes a disable function. When the pin is actively pulled to GND, start-up of the HBC is disabled (R_{SNSOUT} < 1.5 kΩ).

10.7 Burst mode transition level: SNSSET R2 and R_{SNSOUT}

For each burst repetition frequency (R_{SNSOUT} value) and HP-to-LP transition level, one of two BM-to-LP transition levels can be selected. These BM-to-LP transition levels can be set with resistor R2 of the SNSSET pin. Table 11 shows the possible combinations.

Table 11. HP-to-LP transition, BM-to-LP transition, and burst repetition frequency presets

	Burst repetition frequency [1]	200 Hz	400 Hz	800 Hz	1600 Hz
	R_{SNSOUT}	22 kΩ	15 kΩ	10 kΩ	6.8 kΩ
SNSSET R2	HP → LP (% of nominal power) [2]	BM → LP (% of nominal power) [3]			
1 kΩ	25	9	9	9	9
6.8 kΩ	25	12	12	12	12
15 kΩ	37.5	9	9	9	10
27 kΩ	37.5	12	12	12	13
47 kΩ	50	9	10	11	12
82 kΩ	50	12	13	15	17
180 kΩ	62.5	9	10	12	14
open	62.5	12	15	17.5	20

[1] Burst repetition frequency can be set with resistor R_{SNSOUT}: 4 values.
[2] HP-to-LP transition can be set with resistor R2 on the SNSSET pin: 4 values.
[3] BM-to-LP transition can be set with resistor R2 on the SNSSET pin and with R_{SNSOUT}.

The values in Table 11 include the additional shift due to a fixed internal time delay (150 ns) and a typical application delay (300 ns). These transition levels can be modified to a new table of values using an external resistor and capacitor.

10.7.1 Time delay V_{SNSCAP}-to-HB transition

The mode transition levels are the expected levels in an application. When the SNSCAP divider scales the power correctly (in alignment with the power supply requirements), the transition levels are given as a percentage of the nominal output power.

The level of transition depends on an internal SNSCAP target level and a time delay until the HB transition. The time delay includes:

- Time between the moment that SNSCAP reaches the target level (A) and the moment that the GATE switches off (B). This time is internally fixed: 150 ns.
- Time between the moment that the GATE switches off (B) and the moment that HB reaches half of its maximum value (C). This time depends on the application properties. In this document, 300 ns is assumed.

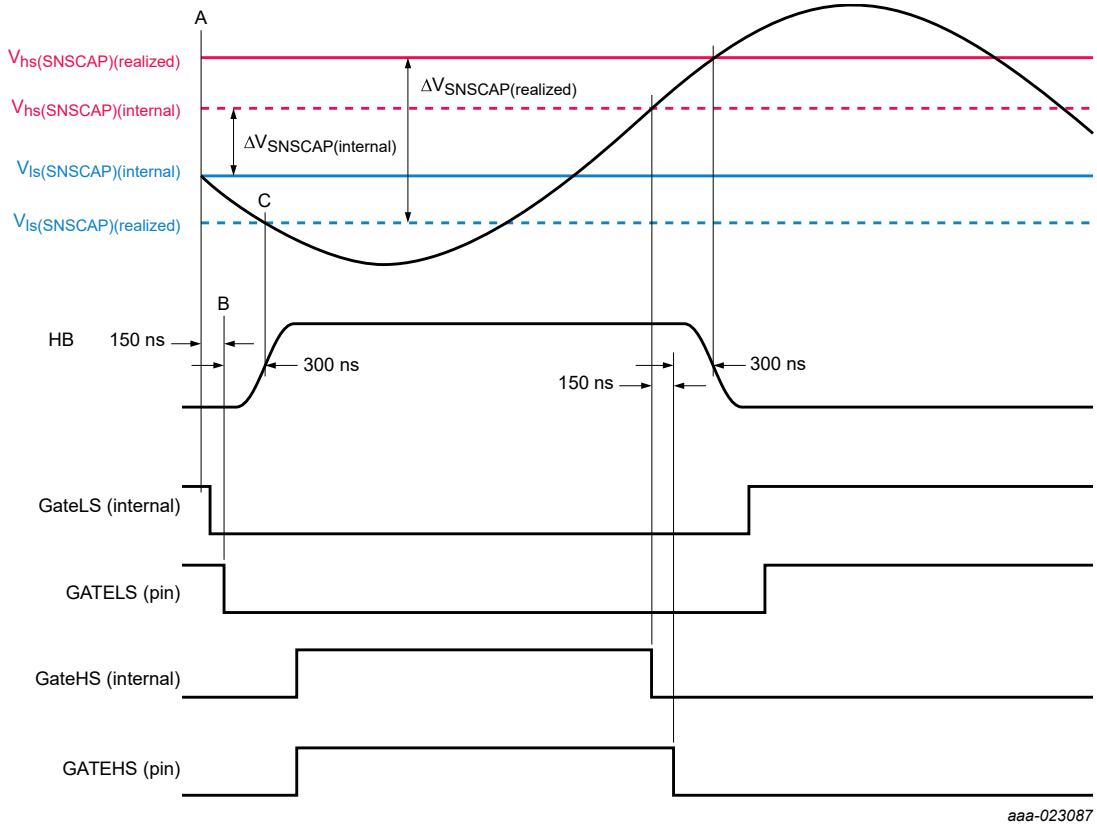


Figure 65. Time delay V_{SNSCAP}-to-HB transition

The time delay leads to a difference in power level between the control and reality. This difference can lead to a substantial difference in (mode transition) power levels. When the application-depending delay (B-C) is different from the 300 ns used in this document, the estimated power levels are different as well.

10.7.2 Accuracy of mode transition levels

Several component values and circuit properties contribute to the resulting mode transition level. Table 12 and Table 13 gives the list of contributions, including the specified or estimated example tolerances.

Table 12. Spread calculation example for burst-mode transition

Contributing item	Tolerance	Comment
resonant capacitor	10 %	specification
capacitive divider SNSCAP	10 %	specification
SNSCAP comparator levels	15 %	specification
time delay	14 %	estimation
SNSBOOST	3 %	estimation; boost compensation
23 kHz timing spread	15 %	estimation; BM transition only
total estimated spread	30 %	root of squares (valid for normal distribution)

Table 13. Spread calculation example for OPP protection level

Contributing item	Tolerance	Comment
resonant capacitor	5 %	specification
capacitive divider SNSCAP	10 %	specification
SNSCAP comparator levels	3 %	specification
time delay	1 %	estimation
SNSBOOST	3 %	estimation; boost compensation
total estimated spread	12 %	root of squares (valid for normal distribution)

The excel calculation sheet included in the Ringo software shows more details and can help with the estimation for a specific design.

Example regarding Table 12 for the burst-mode transition:

When the nominal burst mode transition level is set for 1 A output current, the transition level is between 0.7 A and 1.3 A output current at normal distribution. Using capacitor values with less spread can slightly improve the total tolerance.

10.8 Modify power levels for HP-to-LP and burst mode transition

Normally, the value resistor R2 of the SNSSET pin is chosen to set the mode transition levels. However, sometimes, the options in the table do not meet the requirements, for example, when transitions must be set at a very low power level.

When a voltage offset is added to SNSCAP, the values in the Table 11 can be changed to meet the requirements. This offset has a similar effect as the time delay discussed in Section 10.7.1. The delay or offset shifts the total power range. However, it has a greater effect on the lower power region (near LP-to-BM transition) than on the higher power region (100 % level).

When the offset is added and the SNSCAP is modified to obtain the correct OPP level again, the transition table changes.

10.8.1 Adding an offset to the SNSCAP signal to modify (transition) power levels

The SNSCAP pin can be connected to the voltage on the auxiliary winding using resistor R_{offset} and capacitor C_{offset}. It adds a voltage to the SNSCAP signal for both polarities of the SNSCAP signal. The winding direction of the auxiliary winding determines whether an offset is added or subtracted.

This offset changes the power range defined by the SNSCAP divider.

Because it is important that the OPP level remains as required, the SNSCAP divider must be corrected.

When this offset circuit is added and the SNSCAP divider is modified, the values in the mode transition table are changed. Using this method, table values can be created that are best suited for the application to be designed.

The value of the auxiliary voltage and the value of R_{offset} determine the amount of offset on SNSCAP. Capacitor C_{offset} provides the AC coupling of the offset signal. The value of C_{offset} must allow correct timing for the function.

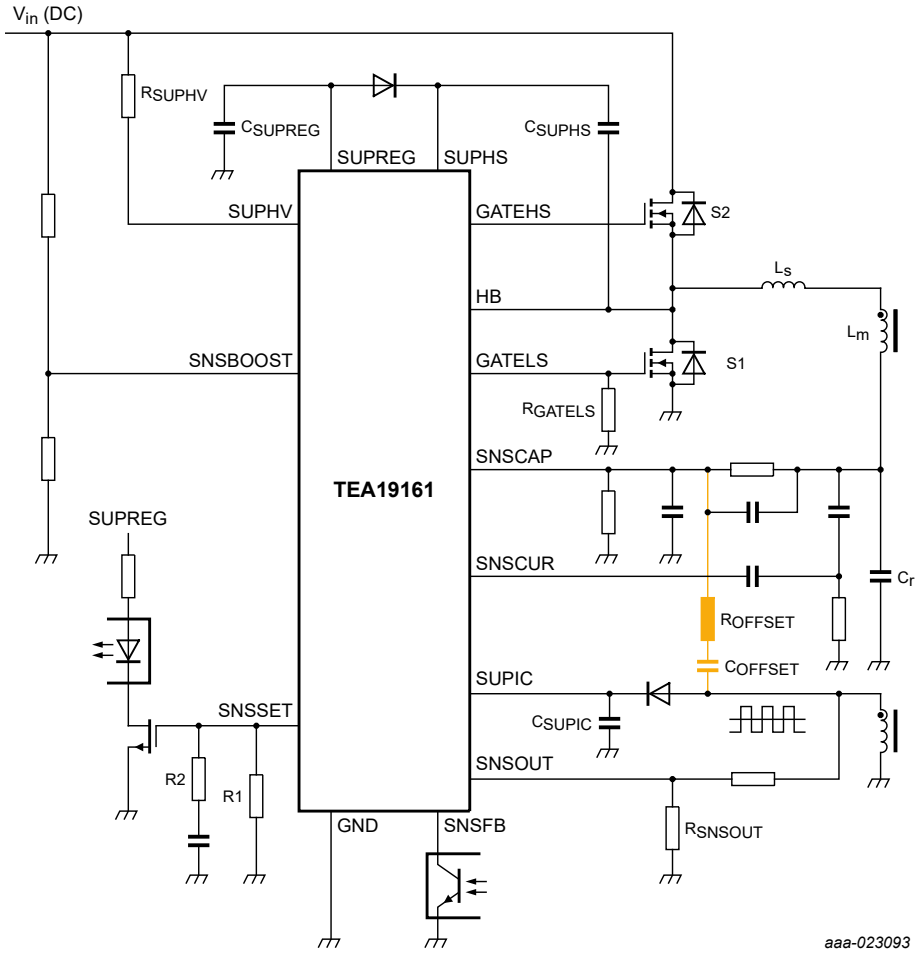


Figure 66. Adding an offset on SNSCAP to modify mode transition power levels

10.8.2 Example of changed mode transition power levels

In most applications, the auxiliary winding is chosen to generate approximately 18 V to supply the SUPIC pin. Given this auxiliary voltage value, typical values for the offset components are:

- R_{offset} = 180 kΩ
- C_{offset} = 120 pF

Using this offset in the TEA1916 240 W demo board results in a new SNSSET R2 table (see Table 12). Compare the values with the values in Table 11.

Table 14. Mode transition power levels modified by adding an offset to SNSCAP

	Burst repetition frequency	200 Hz	400 Hz	800 Hz	1600 Hz
	R_{SNSOUT}	22 kΩ	15 kΩ	10 kΩ	6.8 kΩ
SNSSET R2	HP → LP (% of nominal power)	BM → LP (% of nominal power)			
1 kΩ	15	2.5	2.5	2.5	2.5
6.8 kΩ	15	5	5	5	5
15 kΩ	30	2.5	2.5	2.5	3
27 kΩ	30	5	5	5	6
47 kΩ	42.5	2.5	3	4	5
82 kΩ	42.5	5	6	8	10
180 kΩ	55	2.5	4	5	7
open	55	6	9	12	15

10.9 Settings measurements timing sequence

The measurements are made sequentially:

1. SNSOUT
2. SNSSET
3. GATELS

The sequence starts when SUPIC reaches the start level.

10.9.1 SNSOUT

The duration of the SNSOUT measurement is typical 500 µs and maximum 1000 µs.

The resistor value on SNSOUT must have a value of high accuracy: 1 % or less. The IC system uses the measured voltage value for the calibration of internal references.

10.9.2 SNSSET

The duration of the SNSSET discharge is 7 ms typical. The maximum duration 8.4 ms.

The duration of this measurement is 15 ms typical. The maximum duration is 25 ms.

To ensure that the measurements during charging provide the correct information to extract the resistor values of R1 and R2, the SNSSET measurement starts with a discharge of SNSSET.

10.9.3 GATELS

The duration of the SNSOUT measurement is 650 µs typical. The maximum duration is 800 µs.

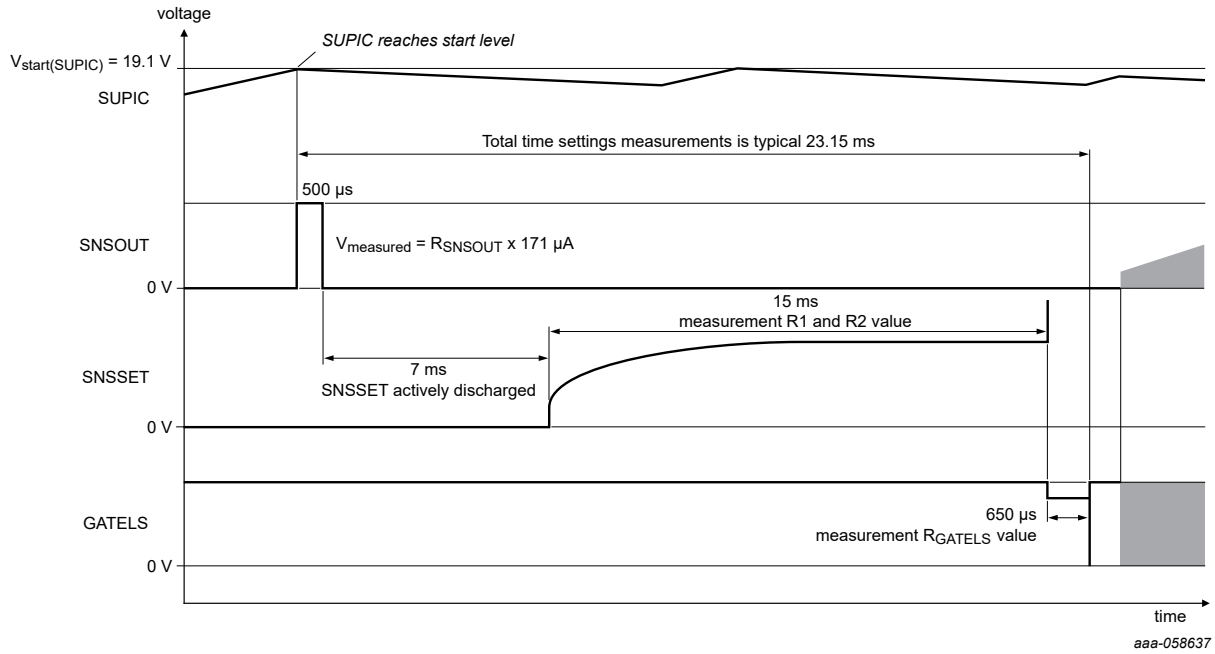


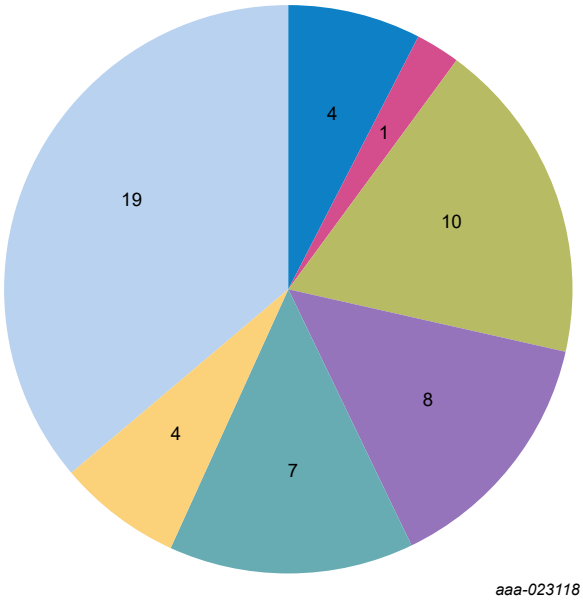
Figure 67. Settings measurements typical timing sequence

11 Standby or no-load condition in burst mode operation

11.1 No-load power consumption

The currents that flow continuously in time mainly determine the power consumption during no-load operation. The energy used for power conversion in a burst is practically negligible because the bursts happen during a relatively short time. Figure 68 shows the main contributors to power consumption during no-load burst mode operation.

Converted power generates some currents. To obtain the power taken from the mains, these currents must be calculated using the conversion efficiency.



No-load power consumption power in mW

- 1. Blue: Mains input filter = 4 mW
- 2. Pink: Mains input measurement = 1 mW
- 3. Light green: PFC output resistive divider = 10 mW
- 4. Purple: Power in SNSCAP divider = 8 mW
- 5. Green: Feedback circuit = 7 mW
- 6. Orange: HBC output resistive divider = 4 mW
- 7. Light blue: TEA1916 = 19 mW

Figure 68. Typical TEA1916 power consumption distribution in no-load condition

11.1.1 Power consumption of feedback circuit and output resistive divider

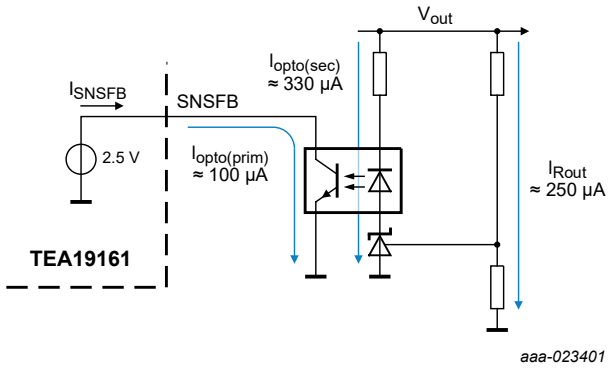


Figure 69. Typical current in the feedback circuit during burst mode operation

The TEA1916 regulates the SNSFB current to approximately 100 µA during burst mode. The secondary current depends on the CTR value of the optocoupler. It can be calculated. The chosen resistor values determine the current through the output resistive divider.

Example for power consumption of an optocoupler circuit:

$$P_{opto(prim)} = V_{SUPIC} \times I_{opto(prim)} = 18\ V \times 100\ \mu A = 1.8\ mW \quad (35)$$

$$P_{opto(sec)} = V_{out} \times \frac{I_{opto(prim)}}{CTR} = 12\ V \times \frac{100\ \mu A}{30\ \%} = 4\ mW \quad (36)$$

$$P_{opto(mains)} = \frac{\left(P_{opto(prim)} + P_{opto(sec)}\right)}{\eta} = \frac{(1.8\ mW + 4\ mW)}{0.8} = 7.25\ mW \quad (37)$$

Example for power consumption of output resistive divider:

$$P_{Rout(mains)} = \frac{V_{out} \times I_{Rout}}{\mu} = \frac{12\ V \times 250\ \mu A}{0.8} = 3.75\ mW \quad (38)$$

11.1.2 Power consumption of TEA19161 and TEA19162 SUPIC

To minimize power consumption during burst mode operation, the TEA19161 IC includes a power save state. With this specified current value, the energy consumption can be calculated.

Example:

- TEA19161: $I_{CC(burst)SUPIC}$ = 0.7 mA
- TEA19162: $I_{CC(ps)typ}$ = 0.15 mA

$$P_{ICs} = V_{SUPIC} \times \left(I_{CC(burst)SUPIC} + I_{CC(ps)}\right) \quad (39)$$

$$= 18\ V \times (0.7\ mA + 0.15\ mA) = 15.3\ mW$$

$$P_{ICs(mains)} = \frac{P_{ICs}}{\eta} = \frac{15.3\ mW}{0.8} = 19.1\ mW \quad (40)$$

11.1.3 Power consumption of SNSMAINS

The SNSMAINS function senses the mains voltage during half the time using a measurement resistor R_{MAINS} switched to close to the GND level.

Example:

- R_{mains} = 20 MΩ
- V_{mains} = 230 V (AC)

$$P_{Rmains} = \frac{1}{2} \times \frac{V_{mains}{}^2}{R_{mains}} = \frac{1}{2} \frac{230\ V^2}{20\ M\Omega} = 1.3\ mW \quad (41)$$

11.1.4 Power consumption of the resistive divider part for SNSCAP

During normal operation and burst mode operation, the average voltage on the resonant capacitor C_r is half the HBC input voltage V_{boost}. The resistive part of the SNSCAP divider connected to C_r consumes power from the system.

Example:

$$P_{RSNSCAP} = \frac{\left(\frac{V_{boost}}{2}\right)^2}{R_{SNSCAP(high)} + R_{SNSCAP(low)}} = \frac{\left(\frac{390\ V}{2}\right)^2}{4.9\ M\Omega + 20\ k\Omega} = 7.7\ mW \quad (42)$$

11.1.5 Power consumption of the resistive divider for SNSBOOST

During normal operation and burst mode operation, the resistive divider on V_{boost} consumes power from the system.

Example:

$$P_{RSNSBOOST} = \frac{V_{boost}{}^2}{R_{boost} + R_{meas(SNSBOOST)}} = \frac{390\ V^2}{15.6\ M\Omega + 100\ k\Omega} = 9.7\ mW \quad (43)$$

11.1.6 Power consumption estimation at very low load condition

At very low loads or under a standby condition, the power consumption can be estimated by adding the output power divided by the efficiency to the no-load power consumption. However, when the repetition frequency of the burst increases with the load and the conversion cannot be neglected anymore, this estimation becomes less accurate.

Example:

$$P_{mains(lowload)} = P_{mains(noload)} + \frac{P_{out(lowload)}}{\eta} \quad (44)$$

$$= 55\ mW + \frac{50\ mW}{0.8} = 117.5\ mW$$

11.2 Audible noise

In PFC and HBC power supplies that use burst mode operation, the HBC transformer is the main source for audible noise in most applications.

11.2.1 Audible noise PFC converter

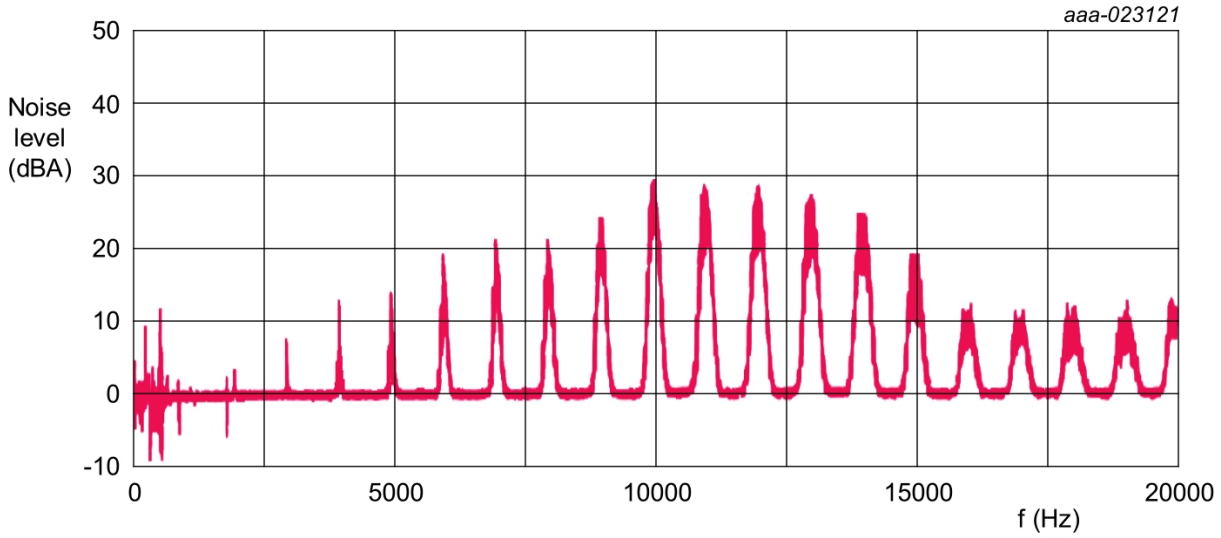
To minimize audible noise in the PFC burst mode and to prevent steep transients of PFC coil magnetization, a soft start and soft stop is included. The PFC burst mode operates independently from the HBC burst mode operation. At low output power, the HBC controller enables or disables PFC burst mode range. It activates the PFC burst mode in the lower output power part of the HBC burst mode range. The activation of the PFC burst mode is based on the duty cycle of the HBC burst.

11.2.2 Audible noise HBC converter

The converted energy in the HBC does not contribute to audible noise generation because the switching repetition is well above the audible frequency. However, in burst mode, the repetition frequency of the bursts is in the audible frequency range. The TEA19161 can be set to a steady repetition frequency of 1600 Hz, 800 Hz, 400 Hz, or 200 Hz. This operation can generate audible noise.

The LP mode enables the system to keep switching above the audible frequency down to low output power levels. The minimum energy-per-cycle (ECmin) can be set to modify the range of LP mode. A lower ECmin extends the LP range to lower power levels.

The main mechanism for producing noise is the interruption of magnetization current sequences (bursts), which leads to a mechanical force. The core of the resonant transformer is especially susceptible and starts acting like a loudspeaker. The noise amplitude is highest at the (mechanical) resonant frequency of the transformer. Normally, the resonant frequency of the transformer is a higher frequency than the burst repetition frequency. Harmonics of the burst repetition frequency produce the audible noise.



Because the resonance of the transformer is approximately 11 kHz, harmonics of 800 Hz produce most noise at the audio noise resonance frequency of the transformer.

Figure 70. Example of noise spectrum with 800 Hz burst repetition frequency

11.2.3 Measures in the coil and transformer construction

To reduce audible noise, measures can also be taken in the mechanical construction of the HBC transformer and PFC coil.

To reduce audible noise, a varnish is often put on the complete transformer. It is a commonly used method for systems that apply burst mode operation.

If the windings produce noise, filling glue between the windings can be applied. Because this method makes the transformer production more difficult, it is not often used.

To reduce the noise from the core, softer air-gap material can be used. Because it requires non-standard air-gap material, this method is not often used.

12 Practical system implementation topics

12.1 Questions and answers on settings options

How can the efficiency at low-load levels be increased?

- Increase the minimum energy-per-cycle (ECmin).
  Example: SNSSET R2 = 82 kΩ or R2 = open. For the same power levels, a higher current per cycle reduces the number of switching cycles in time.

How can the output ripple voltage be reduced?

- Reduce the minimum energy-per-cycle (ECmin).
  Example SNSSET R2 = 1 kΩ or R2 = 15 kΩ.
- Increase the burst mode repetition frequency.
  Example: R_{SNSOUT} = 10 kΩ or 6.8 kΩ. There are fewer cycles in each burst and a shorter time between bursts.
- Increase the value of the capacitors on the output voltage (not a setting).
  Energy in each cycle or burst leads to less voltage increase and, when not switching, to less voltage decrease.

How to reduce audible noise?

- Reduce the burst mode repetition frequency.
  Example: R_{SNSOUT} = 15 kΩ or 22 kΩ. Higher harmonics generate the highest level of audible noise. When the basic harmonic is lower, the amplitude of the audible noise is less as well.
- Reduce minimum energy-per-cycle (ECmin).
  Example: SNSSET R2 = 1 kΩ or R2 = 15 kΩ. The power range for burst mode decreases and LP mode (no audible noise) is extended.
- Mechanically improve the LLC transformer using a coating or flexible air gap material (not a setting).
  Reduces the audible noise level that the transformer produces at a certain repetitive current operation.

How can the initial primary resonant current be reduced at start-up?

- Reduce the value of R_{GATELS}.
  Example R_{GATELS} = 220 kΩ → 150 kΩ. The switching starts with lower V_{SNSCAP} levels (See Section 10.1).

The efficiency graph shows a lower efficiency in LP mode than just above the LP/HP transition in HP mode.

- The transition is probably near the highest efficiency region of the HP mode. Shift the LP/HP transition to a lower power level where it can improve the lower efficiency of the HP mode. Choose a lower transition level by decreasing the SNSSET R2 value. Example: SNSSET R2 = 27 kΩ or R2 = 6.8 kΩ.

How can a transition to BM at a lower power level be achieved using settings?

- For modifying the presettable transition levels, an offset can be added using an additional resistor and capacitor to SNSCAP (see Section 10.8).

12.2 Questions and answers on debugging

My newly built power supply does not start up but probably immediately enters a protection.

Disable PFC operation as shown in Figure 71. First check if there is any HBC switching.

- If the HBC switches during a short time but soon stops, the most likely protections triggered are OCP, OVP, or OPP. To see if the voltage on the SNSCUR and SNSOUT pins increases too much, this voltage can be measured. Another option is to disable the OCP function temporarily. Add two clamping diodes and disable the OVP function using a higher resistor value from the SNSOUT pin to the auxiliary winding signal.
  The triggering of the OPP can be recognized by the typical time until protection, which is 50 ms or 200 ms, depending on the setting. A cause for OPP can be an error in the SNSCAP divider. If there is a wrong value in the SNSCAP function or the regulation by SNSFB is not working properly, not working at all, or unstable, it can cause false triggering of OCP, OVP, or OPP.
- If the HBC switches do not start switching, something can be wrong with the start-up conditions:
  - The voltage on the SUPIC pin must have reached the start-up level.
  - The SUPREG pin must have reached the nominal voltage (11 V).
  - The GATELS signal must be high; during start-up, the GATELS resistor measurement must be seen (see Figure 61).
  - The value measurements on the SNSSET and SNSOUT pins must be observed.
  - The voltage on the SNSBOOST pin must be 2.3 V or higher.
  - The SNSCUR and SNSCAP pins must have a bias voltage of 2.5 V.
- If the HBC switching is OK, enable the PFC and observe the start-up. First check if there are any PFC switching cycles.
- If the PFC does not start switching, something can be wrong with the start-up conditions:
  - The voltage on the SUPIC pin must have reached the start-up level.
  - The PFCCOMP pin must have reached the initial bias voltage (±3.5 V).
  - The voltage on the SNSBOOST pin must reflect the rectified mains value on V_{boost}.
- If the PFC starts switching because of GATEPFC pulses but the result is incorrect:
  - The mains voltage is not detected and the X-capacitor discharge function is active (see Figure 39).
  - An external OTP is wrongly detected because of a value error in the circuit.
  - The regulation can be unstable. Observe the SNSBOOST voltage and the output voltage V_{boost}.
  - The SNSBOOST voltage remains too low because output power is limited by OCP. Check the SNSCUR function and the measurement resistor.

The mode transition levels are not as expected.

- Check if the OPP level is correct. If it is not, the SNSCAP divider must be modified (see Section 12.3.4).
- If the OPP level is correct, it is possible that signal delays are different from the value used as default for calculating the SNSCAP divider values (see Section 9.2.3 and Section 10.7.1).

12.3 Start-up and debugging

When starting a newly built application or when an error or incorrect behavior is observed during operation, it is possible to simplify analyses by operating the HBC or PFC separately. The simplification helps to locate errors easier and makes it possible to do a performance evaluation under conditions that restrict the influences from other circuit parts.

The following sections show several examples of splitting the converters.

12.3.1 HBC only operation with DC boost voltage

To prevent PFC operation (OLP), disconnect pin 5 of the TEA19162. To generate V_{boost} (approximately 390 V (DC)), connect an external DC source.

To stop TEA19162 operation completely, disconnect the SUPIC pin. However, in most situations stopping the TEA19162 is not required.

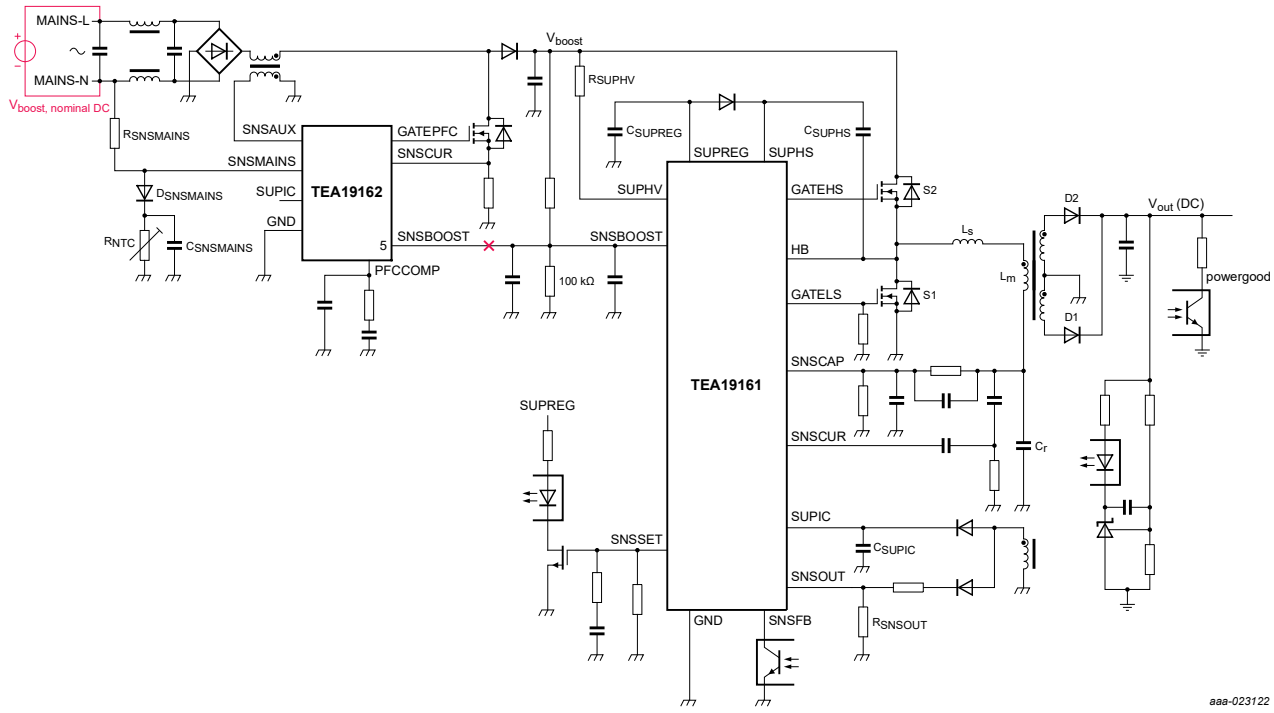


Figure 71. HBC only operation with DC boost voltage

Sometimes, it can be helpful to increase or decrease the DC boost voltage gradually to observe the HBC behavior. In this case, an external voltage of 2.5 V can be applied on TEA19161 pin 16 (SNSBOOST) to enable operation at a lower boost voltage. And an external source of 20 V can be connected to TEA19161 SUPIC pin 1 to supply the IC for operation.

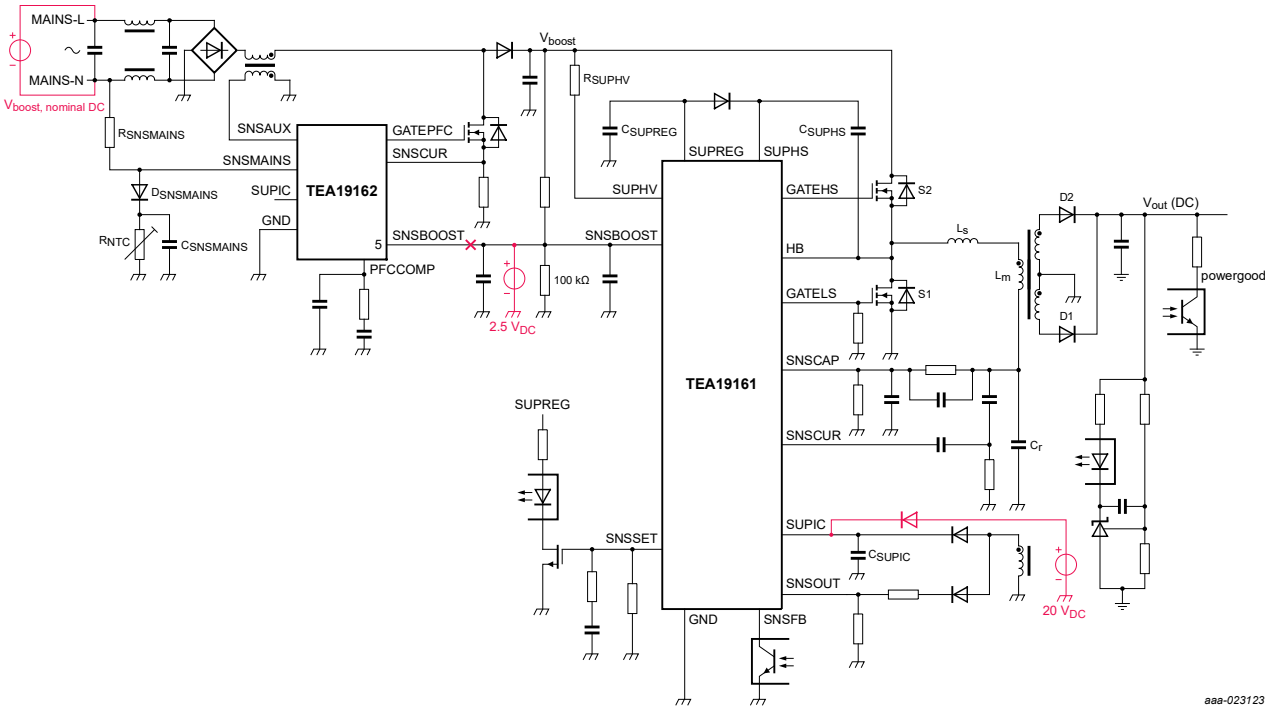


Figure 72. Observe the HBC behavior at variable V_{boost} voltages

12.3.2 PFC only operation

Keeping the TEA19161 SNSBOOST pin low prevents that the HBC starts operation. To keep the SNSBOOST pin low, disconnect the SNSBOOST pin. The start-up HV source can supply SUPIC. However, to prevent that the external HV source resistors become overheated, use an external power supply to generate SUPIC or to take over after start-up.

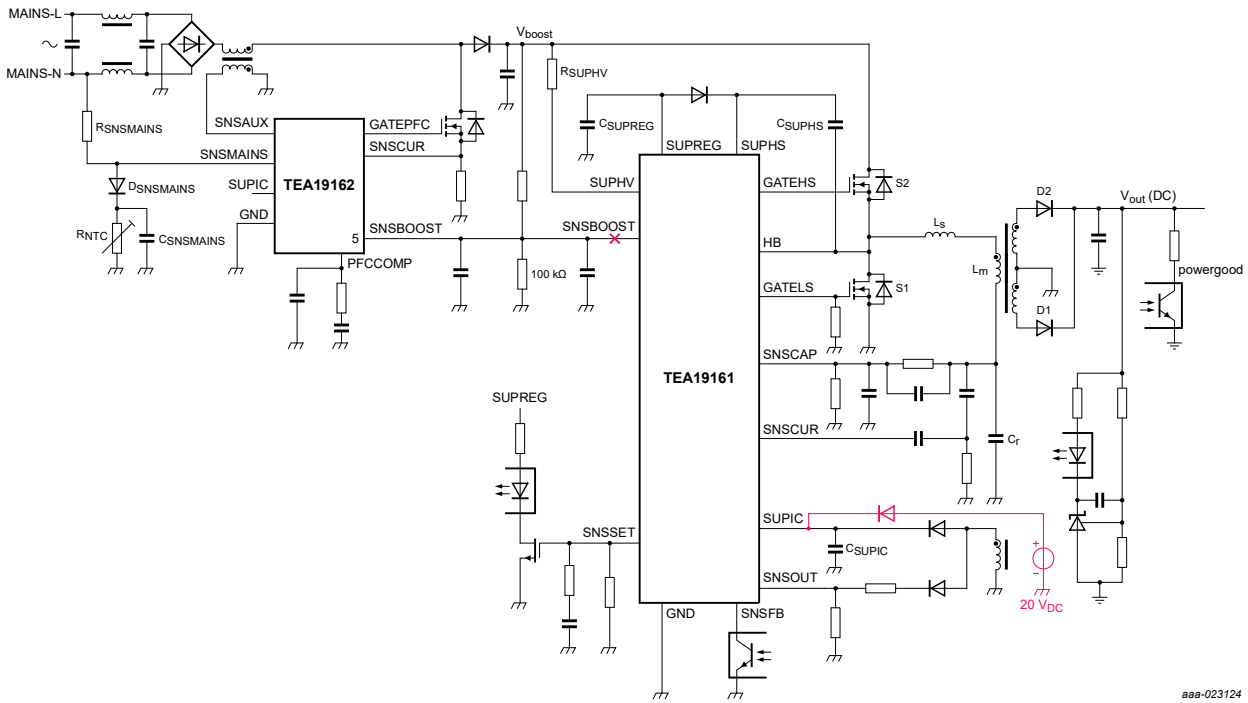


Figure 73. PFC only operation

12.3.3 Splitting SNSBOOST for PFC and HBC operation

It is important to prevent that the SNSBOOST signal that is used by both controllers is disturbed. Proper layout of the PCB can be helpful (see Section 13.1).

If the cause of problems is expected to be on this signal, it can be debugged by temporarily splitting the connection into two parts, each with a separate resistive divider. To split the connection, temporarily add a second resistive divider. In this way, the behavior of each converter (PFC and HBC) can be checked separately.

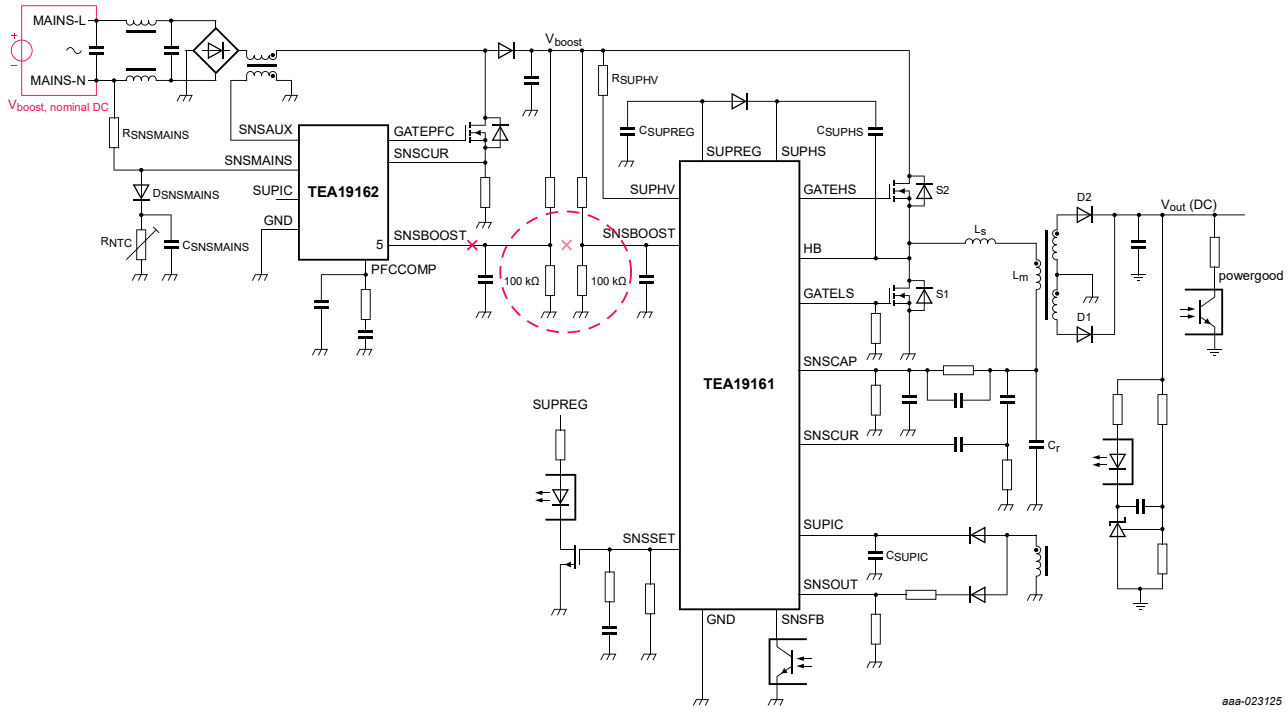


Figure 74. HBC only operation with DC boost voltage and split SNSBOOST divider

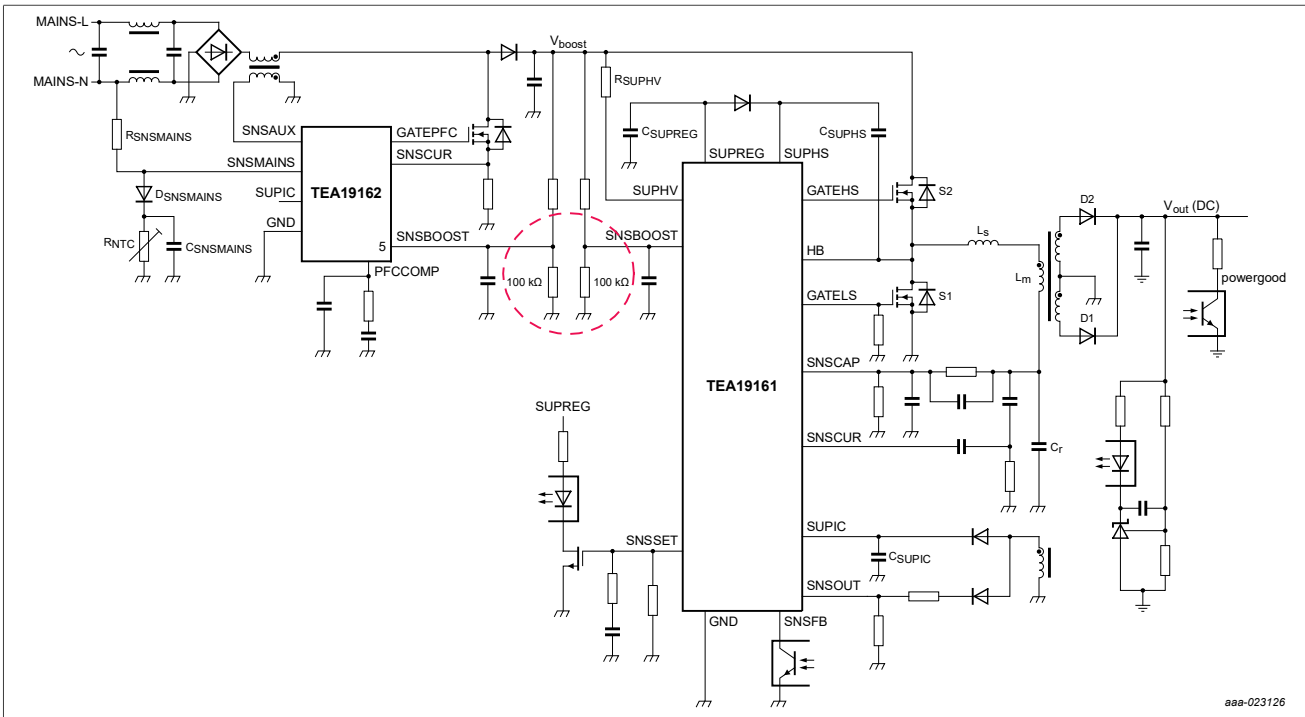


Figure 75. HBC and PFC operation with split SNSBOOST divider

12.3.4 Checking the SNSCAP divider

After implementing the estimated SNSCAP divider values, it is important to check the result to the OPP reference level in the real application. There can be some application-specific deviations from the values in the estimation. If the power level for triggering OPP is not correct, the divider values must be corrected for a good result.

By programming an electronic load with a load step sequence, the system can be analyzed in the application. See the example in Figure 76 for checking 125 % OPP after 200 ms with safe restart.

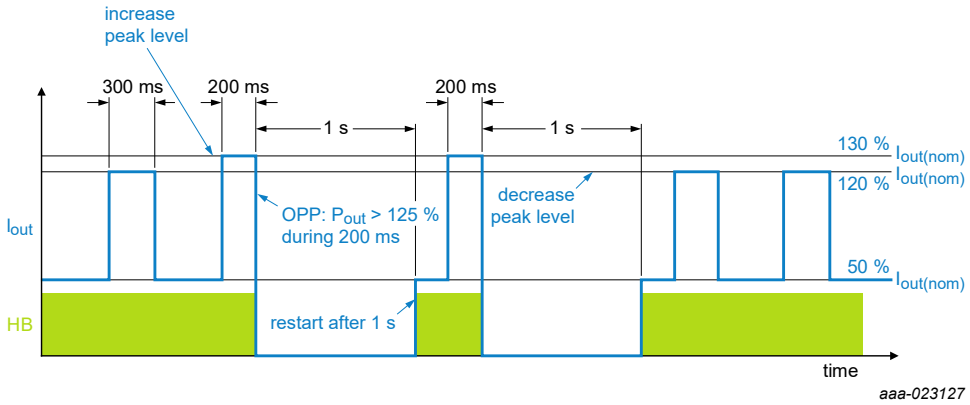


Figure 76. Testing the OPP level and timing

When the measured OPP level is incorrect, the SNSCAP divider must be modified. In practice, modifying the SNSCAP divider can be done by making a small change to the $C_{SNSCAP(low)}$ value.

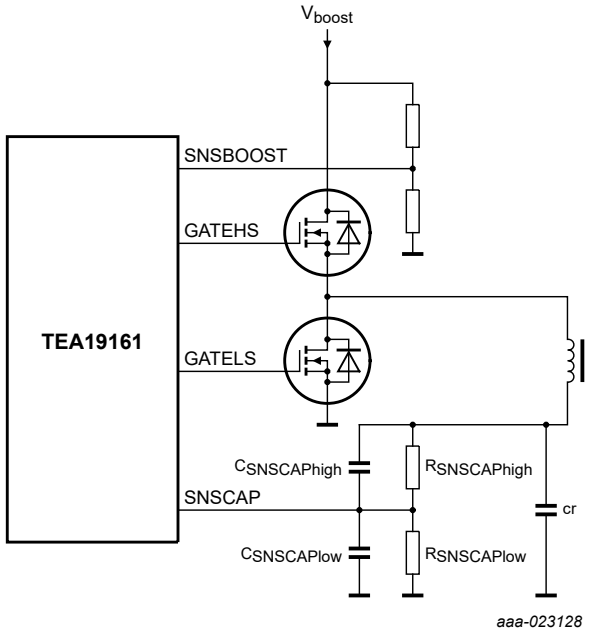


Figure 77. SNSCAP divider

12.4 Load sweep for checking the mode transitions and the behavior

To observe the complete power range of the power supply, it is useful to apply a load sweep from no load to nominal load for a longer period (seconds). In this way, several properties and the behavior of the regulation and modes can be studied in one oscilloscope picture. Connecting a function generator signal to an analog input that drives the current load value, enables this option for several electronic load devices.

Using this option, the following things can be checked:

- Regulation instability for certain load conditions
- Mode transitions at the expected or required power levels
- Output ripple voltage:
  Is the output ripple voltage at the expected level? Or is it higher because of disturbances or unstable operation at certain load conditions?
- Hysteresis at LP/HP transition:
  Different transition levels between output power increasing and decreasing.

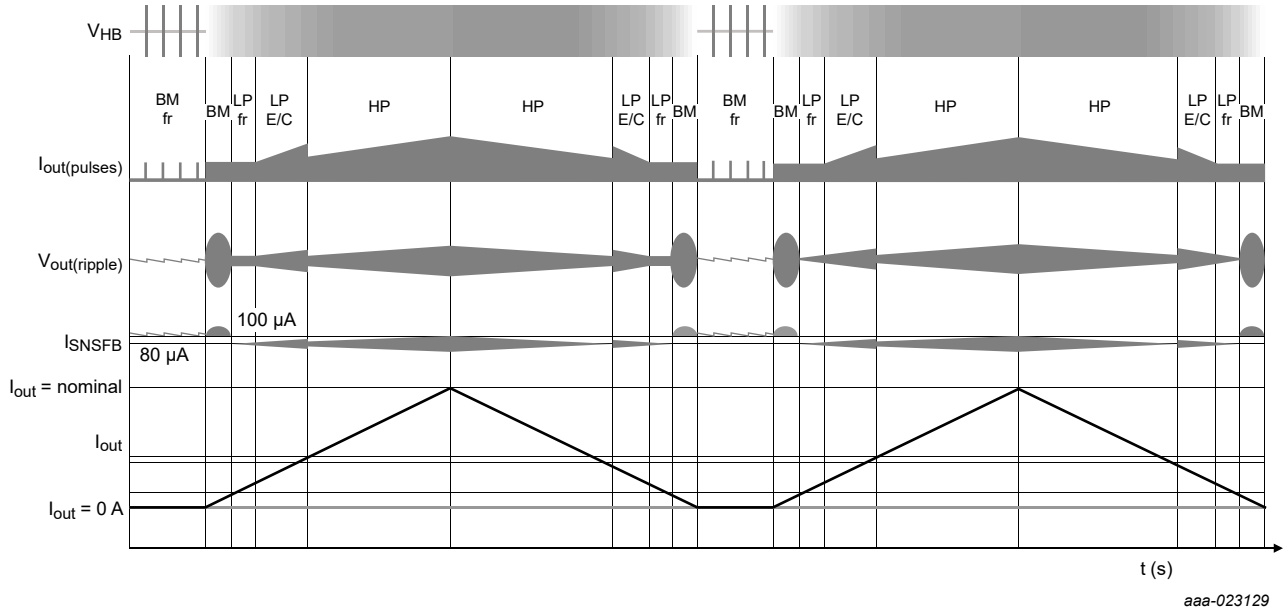
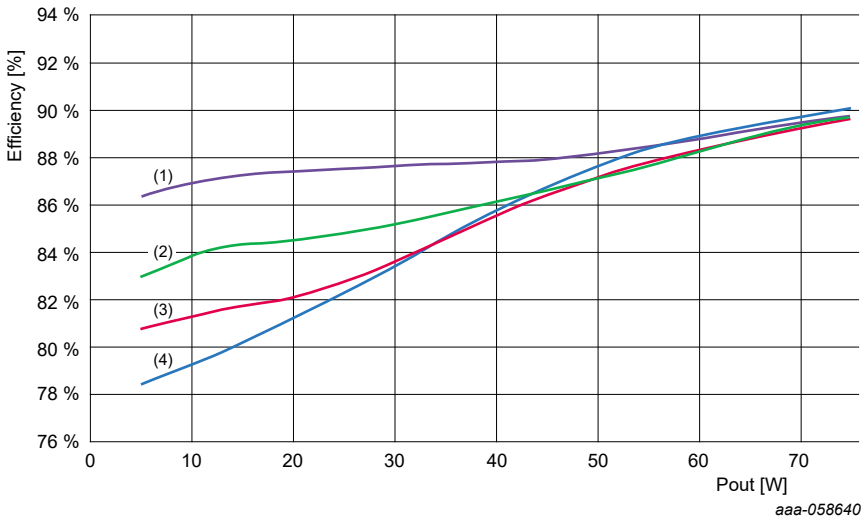


Figure 78. Load sweep to check the mode transitions and the behavior

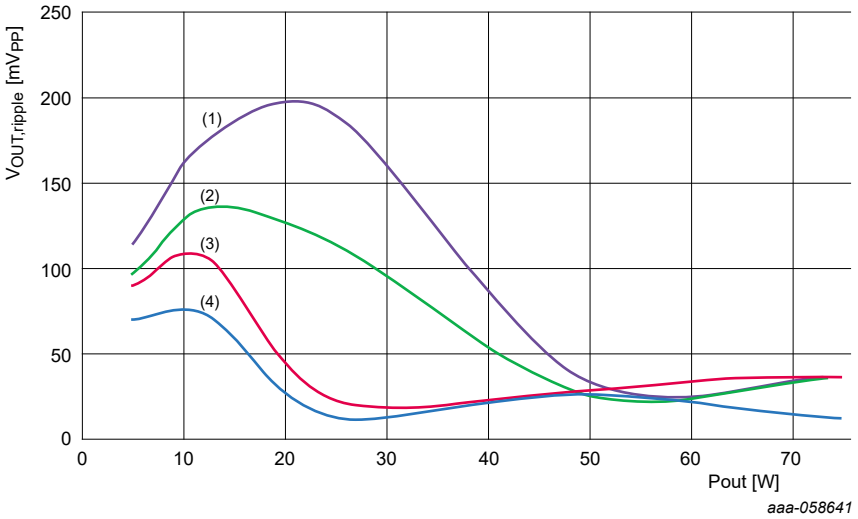
12.5 Trade-off between efficiency and output voltage ripple

The selection of the minimum energy-per-cycle requires a trade-off between output voltage ripple and efficiency performance at low-load conditions.Figure 79 shows an example for an 800 Hz BM setting with R_{SNSOUT} = 10 kΩ in the TEA1916DB1262 240 W demo board (see Section 15). And four different values for SNSSET R2 for the HP-LP transition, which indirectly determine the minimum energy-per-cycle (LP) and the efficiency at low load. The efficiency is higher at the cost of a higher output voltage ripple.

The output voltage ripple can be reduced independently by increasing the value of the output capacitance.



a. P_{out} (W) as a function of frequency (%)



b. P_{out} (W) as a function of $V_{OUT,ripple}$ (mV_{pp})

- (1) Open (EC_{min} = 16 %)
- (2) 82 kΩ (EC_{min} = 12 %)
- (3) 47 kΩ (EC_{min} = 6 %)
- (4) 1 kΩ (EC_{min} = 4 %)

Figure 79. SNSSET R2 requires a trade-off between efficiency and output voltage ripple

12.6 AC mains and OTP measurement required for start-up

Because the mains sensing is based on using the dV/dt of the SNSMAINS voltage to determine the peak level, the system cannot work with a DC input voltage. The start-up is blocked.

At start-up, when a mains voltage is detected, a first OTP measurement is done. When the current in the mains pin drops below 2.5 µA, the NTC measurement is performed.

This measurement is required for releasing the TEA1916 system to start up.

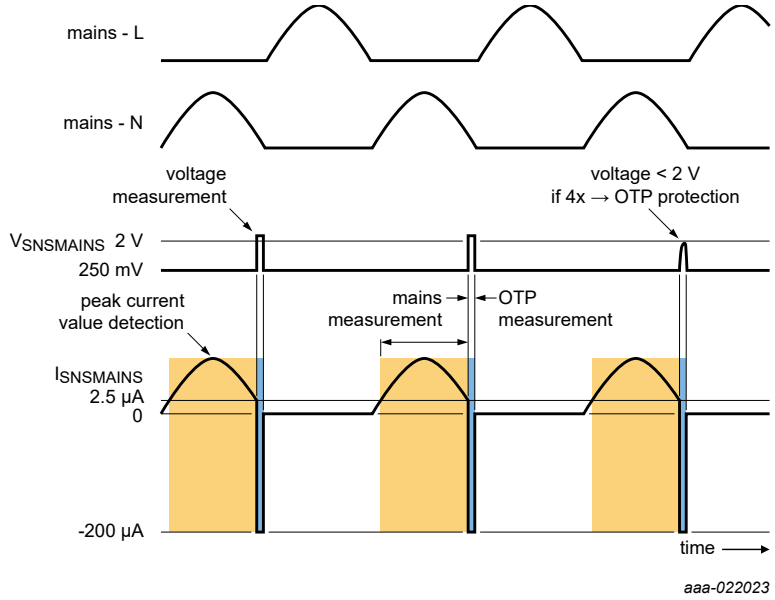


Figure 80. Mains voltage sensing and OTP sensing alternating in time (SNSMAINS pin)

In some special conditions, like a mains interruption during no-load operation, a DC current that parasitic elements cause can flow because the diode rectifier bridge is not conducting. It can block the start-up.

When parasitic elements become significant for the SNSMAINS current that the IC measures, it is more difficult to do measurements with an oscilloscope. Connecting a voltage probe can change the behavior. For measuring and calculating the SNSMAINS current, the voltage across the SNSMAINS series measurement resistor R_{mains} (typically 20 MΩ) can be measured. A normal voltage probe can be referenced to the IC GND pin. An alternative is to use a differential voltage probe.

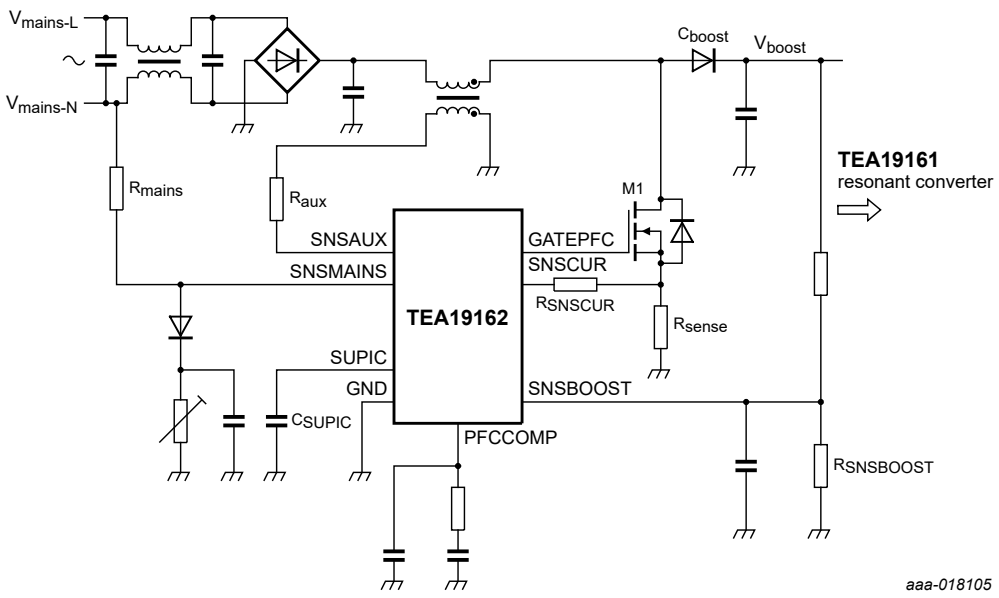


Figure 81. Mains voltage sensing and OTP (SNSMAINS pin)

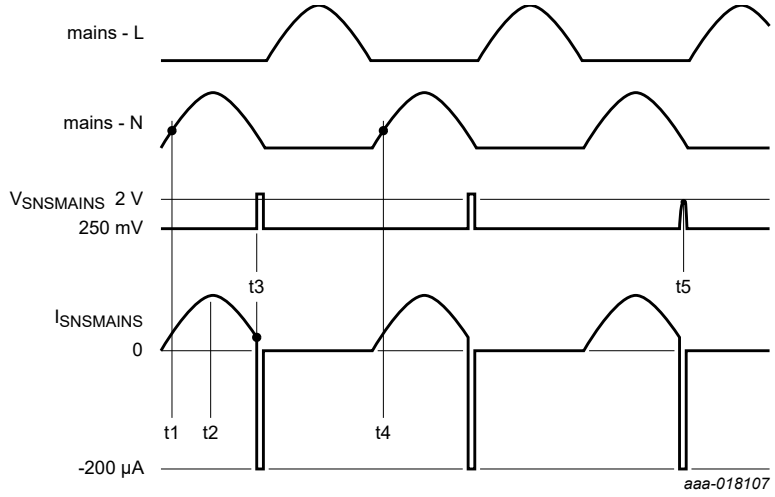


Figure 82. Mains voltage sensing and OTP sensing events

At t1, the voltage at the SNSMAINS pin is internally regulated to 250 mV. The current into the SNSMAINS pin is a measure of the system input mains voltage.

$I_{SNSMAINS} = (V_{L\ or\ N\ to\ GND} - 250\ mV) / R_{SNSMAINS}$

The TEA19162T continuously measures the SNSMAINS current. It waits until it detects a peak in the measured current (t2). This peak current value is internally stored and used as an input for the brownout/brownin detection and the mains compensation.

When, at t3, the current into the SNSMAINS pin is well below the brownin level (2.5 µA), the controller starts to measure the value of the external NTC. The external NTC is measured by sourcing a current of 200 µA out of the SNSMAINS pin. When, after a maximum measuring time of 1 ms, the voltage remains below 2 V during four consecutive NTC measurements, the OTP protection is triggered (t5).

To prevent that the PFC operates at very low mains-input voltages, the PFC stops switching when the measured peak current drops to below 5 µA (brownout). When the measured current exceeds 5.75 µA (brownin), the PFC restarts with a soft start.

12.7 Low impedance measurement on SNSMAINS and SNSBOOST

In some applications, it is critical to use resistive dividers with a high impedance. Figure 83 shows a workaround, which gives a lower impedance resistive divider for SNSMAINS and SNSBOOST. With this method, the total impedance is lower while the required impedance for correct working of the IC is still met.

The SNSBOOST pin of the TEA19161 must be connected to the SNSBOOST pin of the TEA19162 as usual.

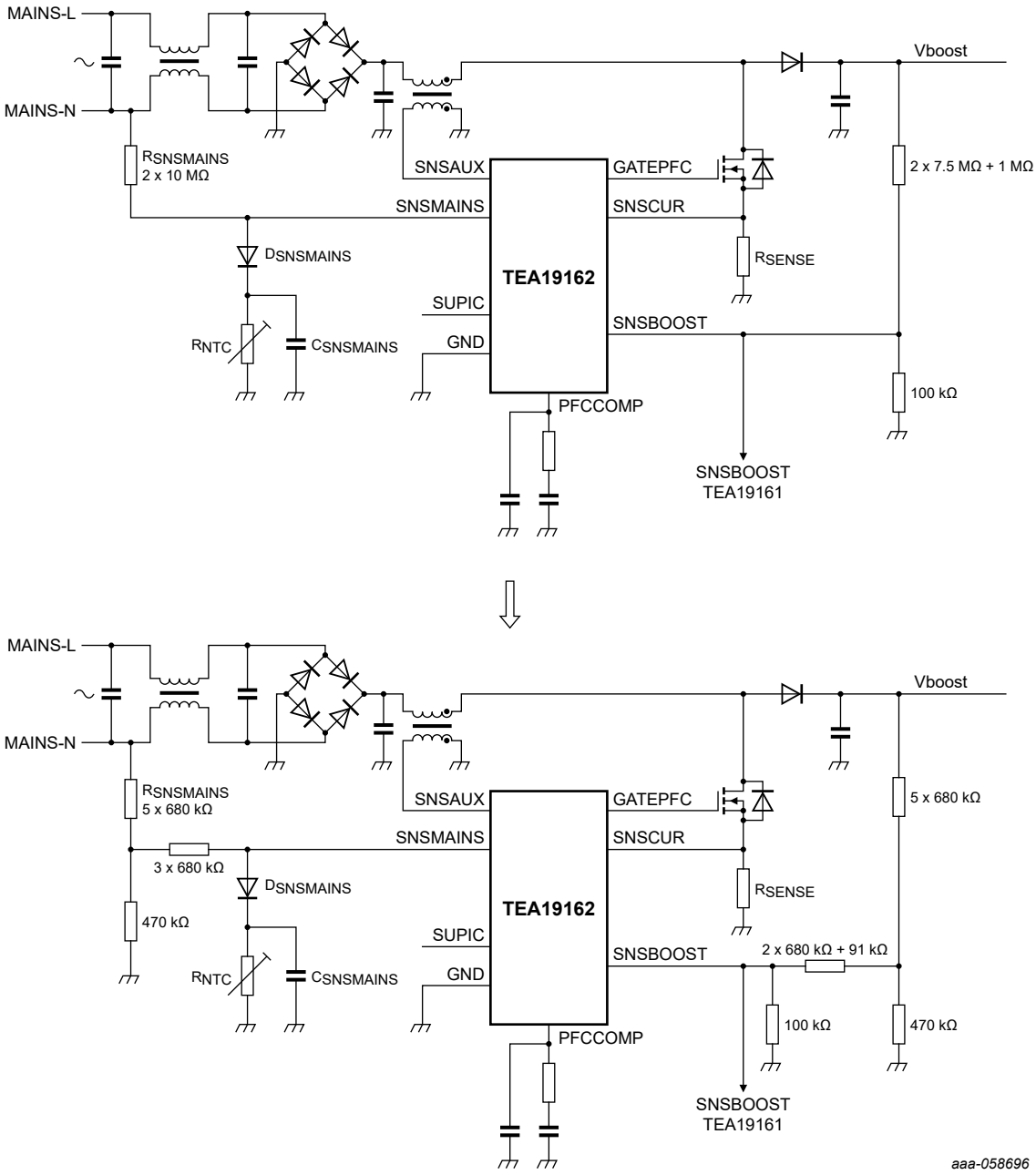


Figure 83. Low impedance measurement dividers on SNSMAINS and SNSBOOST

12.8 SNSFB on low bias-current operation

For energy saving at low power level operations, the SNSFB feedback circuit works on a low current level of 80 µA to 100 µA. The TEA19161 circuit is optimized for it. However, many secondary error-amplifier circuits are made for the higher bias current levels. They need a minimum current for the internal circuit to work properly. Attention must be given to selecting and designing the feedback circuits, such that they work properly at low currents.

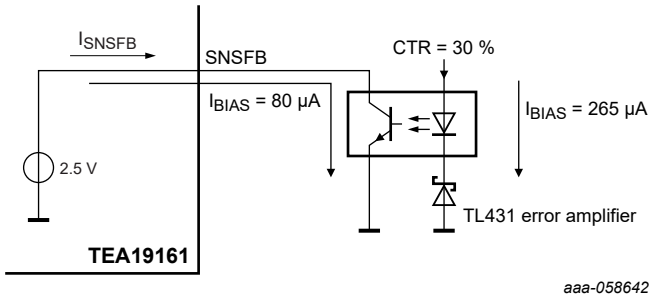


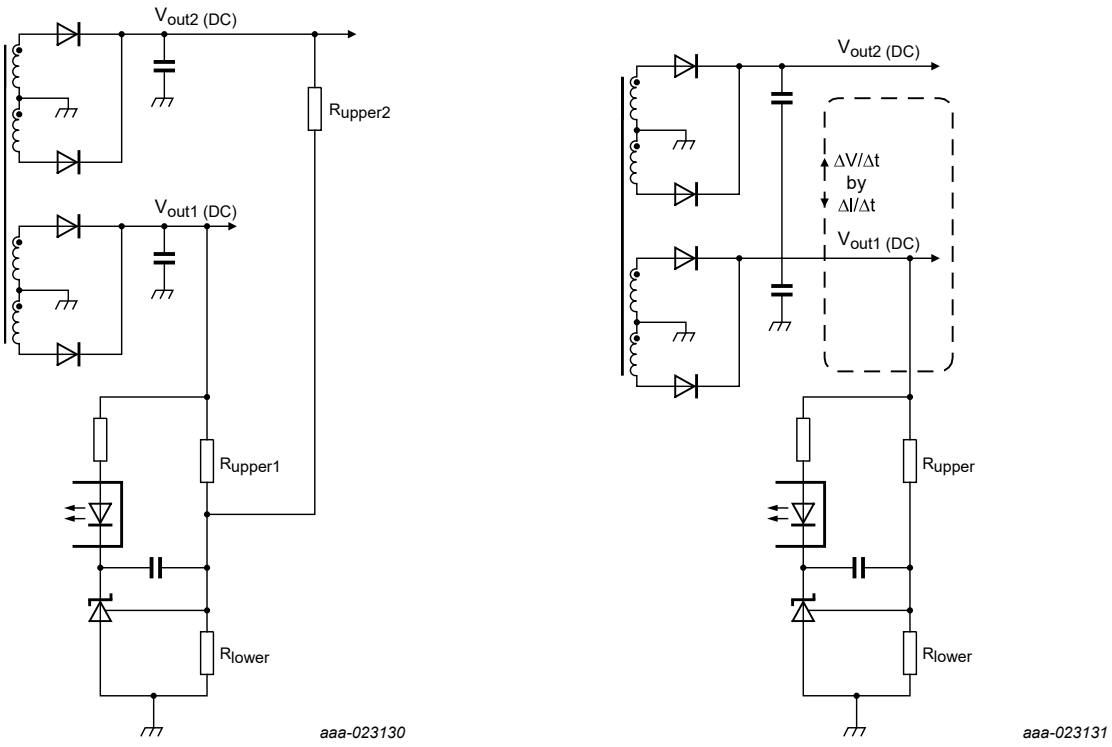
Figure 84. SNSFB working on low bias current

Figure 84 shows an example of the basic feedback circuit-bias current levels. Select a suitable error amplifier type, which can work on low current levels.

12.9 Converter with two output voltages

In some applications, two output voltages are required. The requirement of a high output voltage for LED backlight power in addition to the lower (12 V) supply voltage is typical for TV applications.

Because it is not possible to regulate two output voltages, regulation issues occur sometimes during load step testing.



a. Split feedback

b. Capacitive coupling of outputs

Figure 85. Two methods of improving application behavior when using two output voltages

12.9.1 Regulation of two output voltages using shared feedback

To regulate two output voltages, the output voltage sensing can be split (see Figure 85a). The upper resistor of the voltage divider can be split into R_{upper1} to V_{out1} and R_{upper2} to V_{out2}.

The contribution of each output can be chosen with the values of R_{upper1} and R_{upper2}. One of the outputs is more important or critical than the other.

A disadvantage of this type of regulation is that the load of each output changes the output voltage of the other output.

Calculation example:

- V_{out1} = 13 V
- V_{out2} = 160 V
- $V_{ref(error)amplifier}$ = 2.5 V
- R_{lower} = 10 kΩ

$$I_{lower} = I_{total} = \frac{2.5\ V}{10\ k\Omega} = 0.25\ mA \quad (45)$$

To find a solution, the value for resistor R_{upper1} or R_{upper2} must be slightly higher than but close to the value for a single output regulation.

The R_{upper1} value for a single output regulation becomes:

$$R_{upper1} = \frac{\left(V_{out1} - V_{ref(error)amplifier}\right)}{I_{total}} = \frac{13\ V - 2.5\ V}{0.25\ mA} = 42\ k\Omega \quad (46)$$

For split regulation, the value for R_{upper1} must be higher, for example, 51 kΩ. If R_{upper1} is 51 kΩ, the current from the 13 V becomes:

$$I_{Vout1} = \frac{\left(13\ V - 2.5\ V\right)}{51\ k\Omega} = 0.206\ mA \quad (47)$$

The remaining current must flow from the 160 V output:

$$I_{Vout2} = 0.25\ mA - 0.206\ mA = 0.044\ mA \quad (48)$$

$$R_{upper2} = \frac{\left(V_{out2} - V_{ref(error)amplifier}\right)}{I_{Vout2}} = \frac{\left(160\ V - 2.5\ V\right)}{0.044\ mA} = 3570\ k\Omega$$

So, $R_{upper2} \approx 3.6\ M\Omega$.

In the examples above, the regulation contribution of each output is:

- V_{out1}: $100 \times \frac{I_{Vout1}}{I_{total}} = 100 \times \frac{0.206\ mA}{0.25\ mA} = 82.4\ \%$
- V_{out2}: $100 \times \frac{I_{Vout2}}{I_{total}} = 100 \times \frac{0.044\ mA}{0.25\ mA} = 17.6\ \%$

12.9.2 Output voltage coupling by connecting output capacitors

It is also possible to regulate the main output voltage only and to connect the other output voltage to the main output voltage with the output capacitor (see Figure 85b).

The current from a voltage change through the capacitor of the unregulated output also flows through the capacitor of the regulated output. Voltage variations on the unregulated output, for example, during load steps, now have a similar effect on the regulated output. The feedback regulation for the constant output voltage corrects variations and also indirectly regulates the unregulated output voltage.

The steady state behavior is not compensated because the coupling with the capacitors only shows the variations in current or voltage.

12.10 Checking limiting values in an application

Checking the condition on an IC-pin in a running application can be difficult because of disturbances. Normally, to see if a voltage on a pin is not exceeding the limiting value, an oscilloscope with a voltage probe is used. Because of switching disturbances, the measurement can easily show a voltage that is not on the pin but added by the probe. Or the connection of the probe adds energy to the application because of an antenna function. Both undesired effects show a higher voltage level than there really is on the pin.

To minimize errors in the measurement:

- Minimize the influence of connecting a voltage probe to the circuit (add energy to the application)
- Minimize a voltage added to the measurement by the voltage probe (add signal to real signal)

12.10.1 Measuring recommendations

To minimize disturbances added to the measurement when the voltage probe is used, ensure that the measurement loop signal-to-ground is as small as possible. Figure 86 shows a manually modified probe connection for this purpose.

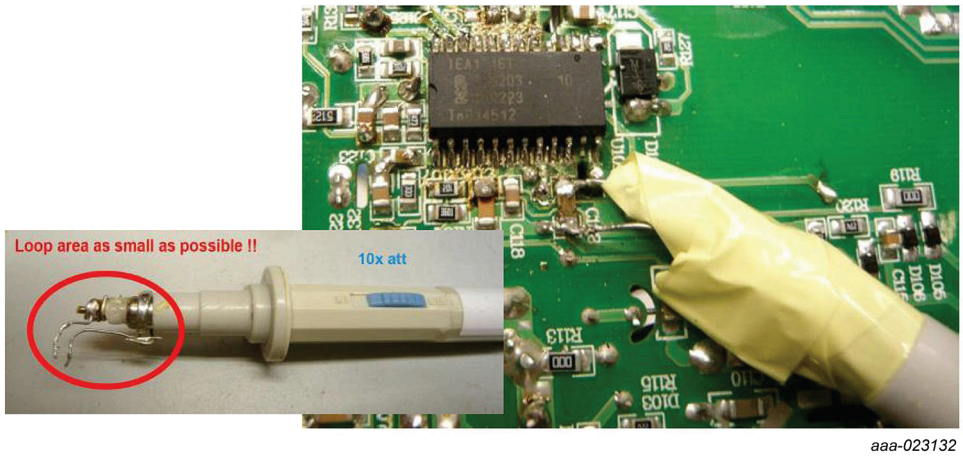


Figure 86. Manually modified probe connection

Even if the measurement is set up with great care, some disturbance still occurs in most measurements. Sometimes, it is difficult or impossible to prove that the application is within the limiting values. Some additional measurements can help to obtain more information on what is really happening. However, based on the collected information, engineering judgment is required to decide if the application is OK or if a problem occurs that must be solved.

12.10.1.1 Measurement to estimate the signal level that the voltage probe adds to the result

To get an indication on which part of the measurement result the voltage probe adds, a reference measurement can be done by connecting the probe to the ground connection of the probe.

The signal seen on the oscilloscope is similar to the signal that is added to the original measurement.

12.10.1.2 Extra check: Adding a peak rectifier circuit to the measurement probe

To indicate if voltage peaks that are too high occur on a pin, a peak rectifier circuit can be added temporarily.

The voltage measured on the capacitor is always lower than the peak voltage on the pin because of the forward voltage of the diode. So, if the voltage on the capacitor exceeds the limiting value, it is an indication that the peak voltages are too high.

The capacitor can have a value of 1 nF. A moderate capacitor discharge of, for example, 10 MΩ is present at the impedance of the voltage probe.

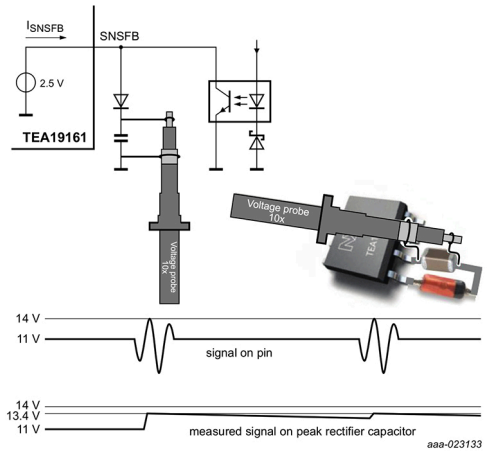


Figure 87. Peak rectifier measurement added on the SNSFB and GATEPFC pins

12.10.1.3 Measurements during high dV/dt

During high dV/dt events, a measurement result can still be unreliable.

When a hard switching event starts the converter, an extra high dV/dt can occur at the first cycle of HB. Expect measurement difficulties during these special events.

For examples and guidelines, see Section 12.11.1.

12.10.2 TEA19161 V_{SUPHS}, V_{HB}, V_{GATEHS}, V_{GATELS}, and TEA19162 $V_{GATEPFC}$ limiting values

In Section 7.6 and Section 7.7, the specific situations for the GATEPFC, GATELS, GATEHS, HB, and SUPHS pins are discussed.

12.10.3 TEA19161 and TEA19162 V_{SUPIC} limiting values

$-0.4\ V < V_{SUPIC} < +36\ V$

Normally, sufficient decoupling exists because of a capacitor on this pin. When the recommendations provided in Section 12.10.1 are applied, the measurement itself is not critical.

An auxiliary winding on the HBC transformer often generates the SUPIC voltage. Depending on the design, this voltage level can vary when the output power changes. Checking the voltage at different load conditions is good practice.

Transients can also make the SUPIC voltage vary temporarily. Check the load step conditions and the situation at start-up and stopping.

12.10.4 TEA19161 V_{SUPREG} limiting values

$-0.4\ V < V_{SUPREG} < +12\ V$

Normally, sufficient decoupling exists because of a capacitor on this pin. When the recommendations provided in Section 12.10.1 are applied, the measurement itself is not critical.

The IC generates the SUPREG voltage. The SUPREG pin can only source current. It cannot actively sink current at the voltage regulator function. The IC uses this voltage to supply the MOSFET drivers. In some applications, an unintended voltage increase can occur because of currents through grounding tracks.

Normally, the SUPREG voltage is also used to create the bootstrap function for supplying the SUPHS pin using a diode. The SUPHS pin shows the rectified voltage on the SUPREG pin. When the voltage on the SUPREG pin has higher voltage peaks, the voltage on the SUPHS pin is higher than normal.

12.10.5 TEA19161 V_{SNSFB} limiting values

$-0.4\ V < V_{SNSFB} < +12\ V$

Because the SNSFB function is current controlled at a relatively low voltage with only an optocoupler connected, the risk of reaching limiting values is small. When the recommendations provided in Section 12.10.1 are applied, the measurement itself is not critical.

12.10.6 TEA19161 V_{SNSOUT} limiting values

$-0.4\ V < V_{SNSOUT} < +12\ V$

Normally, sufficient decoupling exists because of a capacitor on this pin. When the recommendations provided in Section 12.10.1 are applied, the measurement itself is not critical.

The signal on SNSOUT is alternating according to the converter switching. Much margin exists for the positive voltage. The negative voltage is closer to the limiting value. The voltage can be checked during regular operation to see if a grounding problem occurs. If the grounding problem does occur, a negative voltage that is too low can become an issue.

12.10.7 TEA19161 V_{SNSSET} limiting values

$-0.4\ V < V_{SNSSET} < +12\ V$

The IC generates the voltage on this pin. The voltage is defined accurately. When the recommendations provided in Section 12.10.1 are applied, the measurement itself is not critical. No critical situations are expected on this pin.

12.10.8 TEA19161 V_{SNSCUR} limiting values

$-0.4\ V < V_{SNSCUR} < +12\ V$

The voltage on this pin is difficult to measure because attaching a probe seriously disturbs operation. An internal bias source puts the input signal on a DC voltage level of 2.5 V. A capacitor connects the AC voltage that represents the resonant current signal to this pin. The AC voltage part can best be checked on the measurement resistor and not on the pin.

When the recommendations provided in Section 12.10.1 are applied, the measurement itself is not critical. The voltage reserve on the pin compared to the limiting values is substantial. So, the voltage is not critical.

If measurement on the pin is required, use the rectifier method to observe the behavior.

12.10.9 TEA19161 V_{SNSCAP} limiting values

$-0.4\ V < V_{SNSCAP} < +12\ V$

Normally, sufficient decoupling exists because of the $C_{SNSCAP(low)}$ capacitor on this pin. When the recommendations provided in Section 12.10.1 are applied, the measurement itself is not critical.

An internal bias source puts the input signal on a DC voltage level of 2.5 V. The voltage reserve on the pin compared to the limiting values is substantial. So, the voltage is not critical.

12.10.10 TEA19161 $V_{SNSBOOST}$ limiting values

$-0.4\ V < V_{SNSBOOST} < +12\ V$

Normally, sufficient decoupling exists because of the $C_{SNSCAP(low)}$ capacitor on this pin. When the recommendations provided in Section 12.10.1 are applied, the measurement itself is not critical.

If the PFC loop regulation stability is critical or the track connecting the TEA19161 with the TEA19162 is long, a measurement with a voltage probe can disturb the PFC operation. Because the PFC regulation is at 2.5 V and a capacitor of several nanofarads is connected, this pin is not critical concerning limiting values.

12.10.11 TEA19162 $V_{SNSMAINS}$ limiting values

$-0.4\ V < V_{SNSMAINS} < +12\ V$

Because SNSMAINS is connected to the mains voltage with a high impedance (typical 20 MΩ), connecting a voltage probe influences the mains measurements a little. This impact is not directly a problem because operation normally continues in a similar way. The measurement can be made in alignment with the recommendations mentioned in Section 12.10.1.

12.10.12 TEA19162 $V_{PFCCOMP}$ limiting values

$-0.4\ V < V_{PFCCOMP} < +12\ V$

Normally, sufficient decoupling occurs because of the filter on the PFCCOMP pin. When the recommendations provided in Section 12.10.1 are applied, the measurement itself is not critical.

The IC generates the signal on this pin. So, it is not critical to limiting values.

12.10.13 TEA19162 V_{SNSAUX} limiting values

$-0.4\ V < V_{SNSAUX} < +12\ V$

The measurement can be made in alignment with the recommendations in Section 12.10.1. An auxiliary winding on the PFC coil generated the voltage on this pin. Because normally only a few turns make this winding, the voltage signal can be close to the limiting values. Although the allowed voltage range is wide, the measurement itself can be difficult because of the PFC switching, which can distort the measurement result.

12.10.14 TEA19162 V_{SNSCUR} limiting values

$-0.4\ V < V_{SNSCUR} < +12\ V$

The measurement can be made in alignment with the recommendations in Section 12.10.1. The measurement itself can be difficult because of the PFC switching, which can distort the measurement result.

Although the measured signal for this pin comes from a very low impedance resistor, voltage spikes can occur because of the PFC MOSFET switching. Also, if there is a PCB layout grounding problem, high converter currents through the ground tracks can add a signal to the SNSCUR pin.

The most critical situation is at a low mains voltage and a high output power.

12.10.15 TEA19162 $V_{SNSBOOST}$ limiting values

$-0.4\ V < V_{SNSBOOST} < +12\ V$

Normally, sufficient decoupling exists because of a capacitor on this pin. When the recommendations provided in Section 12.10.1 are applied, the measurement itself is not critical.

If the loop regulation is critical, a measurement with a voltage probe can disturb operation. Because regulation is at 2.5 V and a capacitor of several nanofarads is connected, this pin is not critical concerning limiting values.

12.11 Exceeding limiting values

The sections below contain information on extra checks that can be done when measurements during disturbing events provide unreliable information. When limiting values provided in the product data sheets (see Section 17) are exceeded, additional pin current measurements can be done to collect more information. The extra information is useful for finding out if there is risk for the expected lifetime in an application. Information and guidelines for acceptable levels and behavior are provided in this section.

12.11.1 Measurements with unreliable and unclear results

Checking the condition on an IC-pin in a running application can be difficult because of disturbances that can occur. Normally, to see if a voltage on a pin is not exceeding the limiting value, an oscilloscope with a voltage probe is used. Because of switching disturbances, the measurement can easily show a voltage, which is not on the pin but the probe has added. Or the connection of the probe adds energy to the application because of an antenna function. Both undesired effects show a higher voltage level than there really is on the pin.

Section 12.10 provides advice on how to do the voltage measurement.

In general, a bandwidth limit of 20 MHz can be used to limit high-frequency noise disturbances.

However, especially during high dV/dt events, the result can still be unreliable. Figure 88, Figure 89, and Figure 90 show examples of measurements.

When a hard switching event starts the converter, an extra high dV/dt can occur at the first cycle of HB. Expect measurement difficulties during these special events.

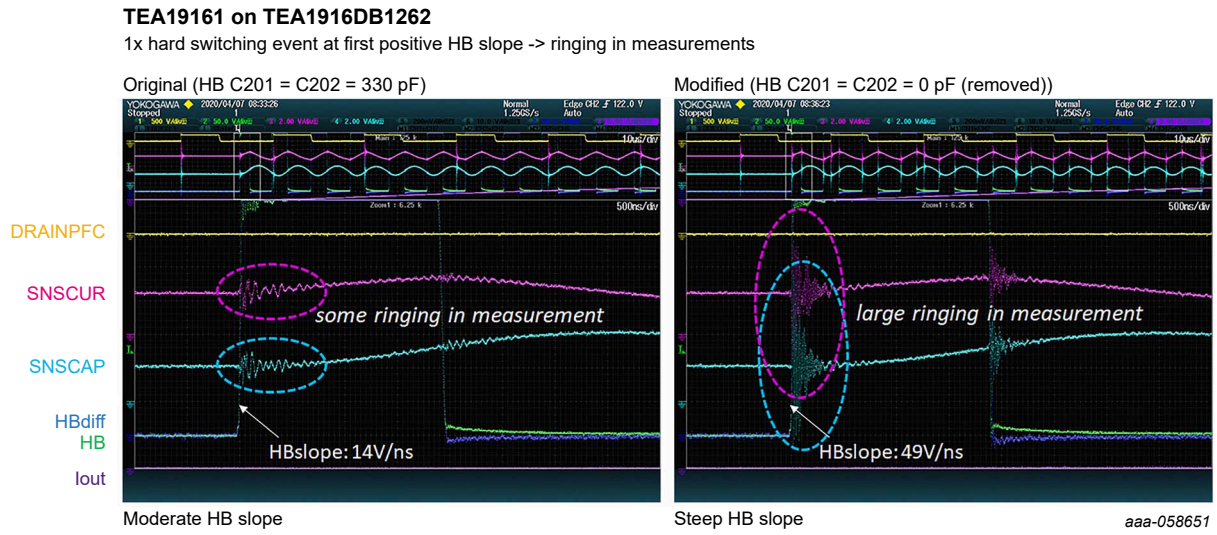


Figure 88. Example comparison of signal disturbance measured during a moderate and steep HB voltage slope

TEA19161 on TEA1916DB1262

At a high HB dV/dt, the voltage probe adds a ringing signal to the measurement. Adding a probe measuring the ground pin (which must be zero volt, in theory), we can see that the probes themselves add most of the ringing signal (see Figure 90).

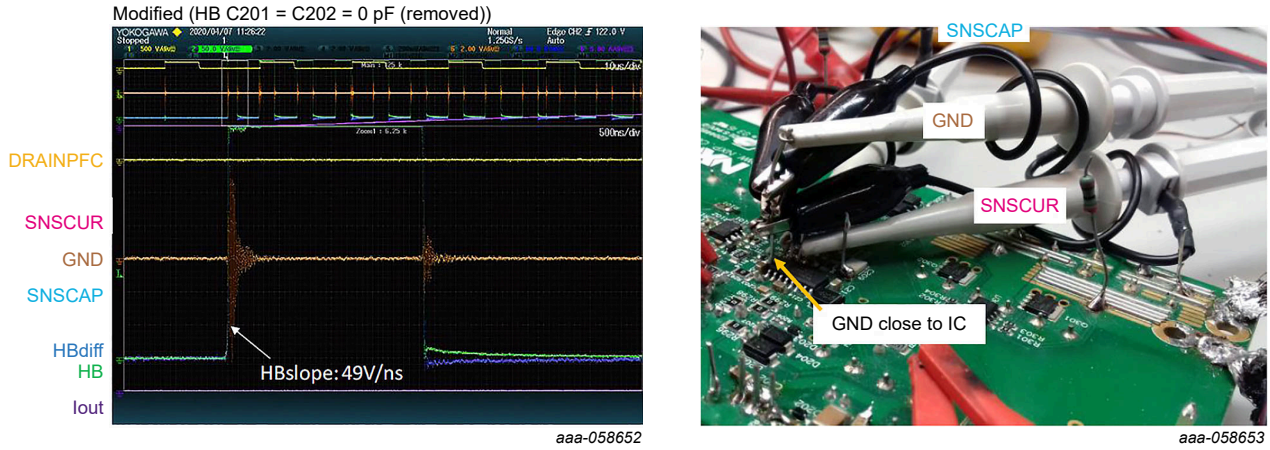


Figure 89. Example of signal disturbance added by the voltage probe during a steep HB voltage slope: GND

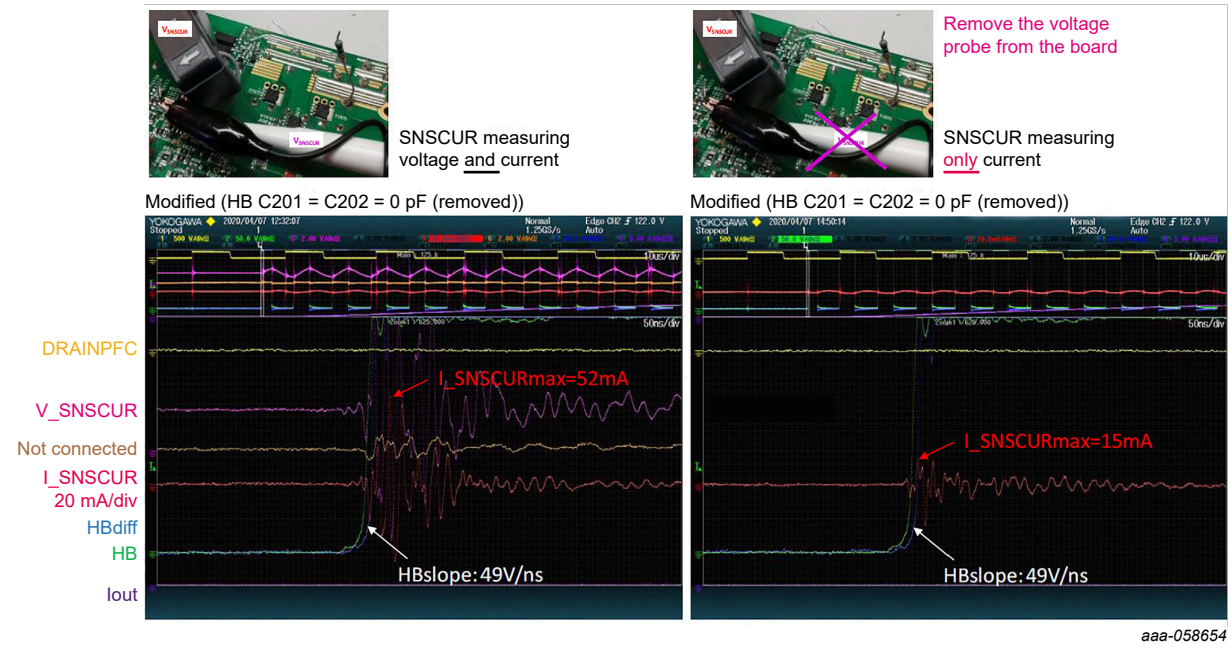


Figure 90. Example of the voltage probe adding signal in the circuit: measured current reduces when removed

12.11.2 Functional behavior and risk for expected lifetime

Disturbances on an IC pin can:

- Change functional behavior.
- Generate extra energy in the (IC) circuit.

When measuring disturbance on an IC pin, the functional change can usually be observed clearly because the operation changes: irregular switching or triggering a protection.

Limiting values are defined to avoid extra energy in the IC circuit that can affect the expected lifetime. They also help to avoid unintended functional behavior.

When limiting values are exceeded, both functional behavior and the extra energy in the IC can be checked. A small amount of disturbance can still be acceptable for functional behavior or expected life.

Section 12.11.3, Section 12.11.4, and Section 12.11.5 provide guidelines for acceptable levels concerning the expected life when exceeding limiting values as defined in the product data sheets (Section 17).

12.11.3 Low-voltage circuit IC pins

This section provides a (low voltage) IC pin current level for non-repetitive events that is acceptable for expected life.

When a voltage measurement on the low voltage IC pin shows that the level is below −0.4 V (limiting value), the current in the pin can be checked. In this way, how much energy the IC circuit connected to the pin contains, can be seen. Because of several parasitic elements in the circuit (application) and the IC, a voltage measurement is sometimes not conclusive or unreliable during a high dV/dt switching event.

The pin current can be checked using a DC current probe and an oscilloscope. Make sure that adding the current probe measurement does not (significantly) change the behavior of the circuit. The current can provide more reliable information to check if the operation is still safe for expected life.

When both conditions below are met, the reverse current is safe for non-repetitive events:

- The reverse current does not exceed 200 mA (peak).
- The duration of pulses is shorter than 50 ns during the event.

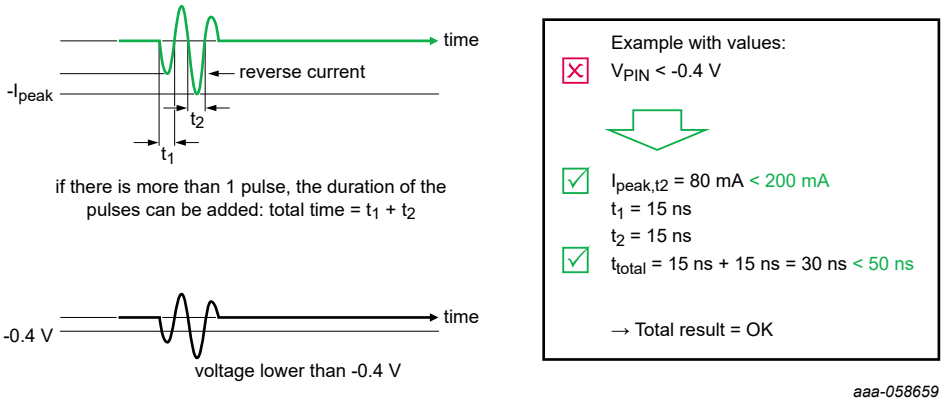


Figure 91. Example of the 200 mAp and 50 ns rule for the IC pins (see Figure 92)

This acceptable value rule is valid for pins 2, 3, 13, 14, 15, and 16 of the TEA19161 and for pins 3, 5, 6, and 7 of the TEA19162.

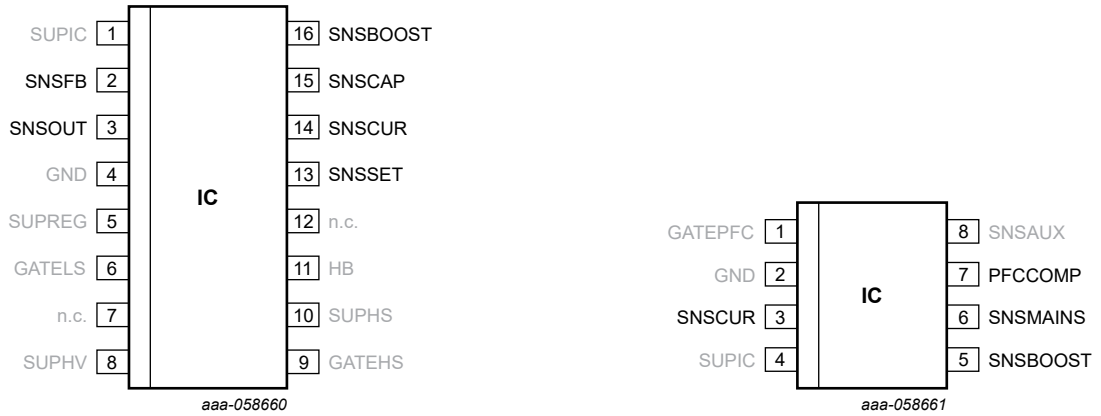


Figure 92. The 200 mAp and 50 ns rule can be used for the IC pins with black names

12.11.4 High-voltage circuit IC pins

Section 7.6 provides information about checking the limiting values for GATEHS, SUPHS, and HB.

Limiting values are based on voltage measurement. Measurement with a high HB dV/dt slope can show unreliable results and make it difficult to come to clear conclusions. Especially, at a negative voltage at the end of a negative HB slope.

Figure 93 shows the negative voltage for HB and GATEHS in point B.

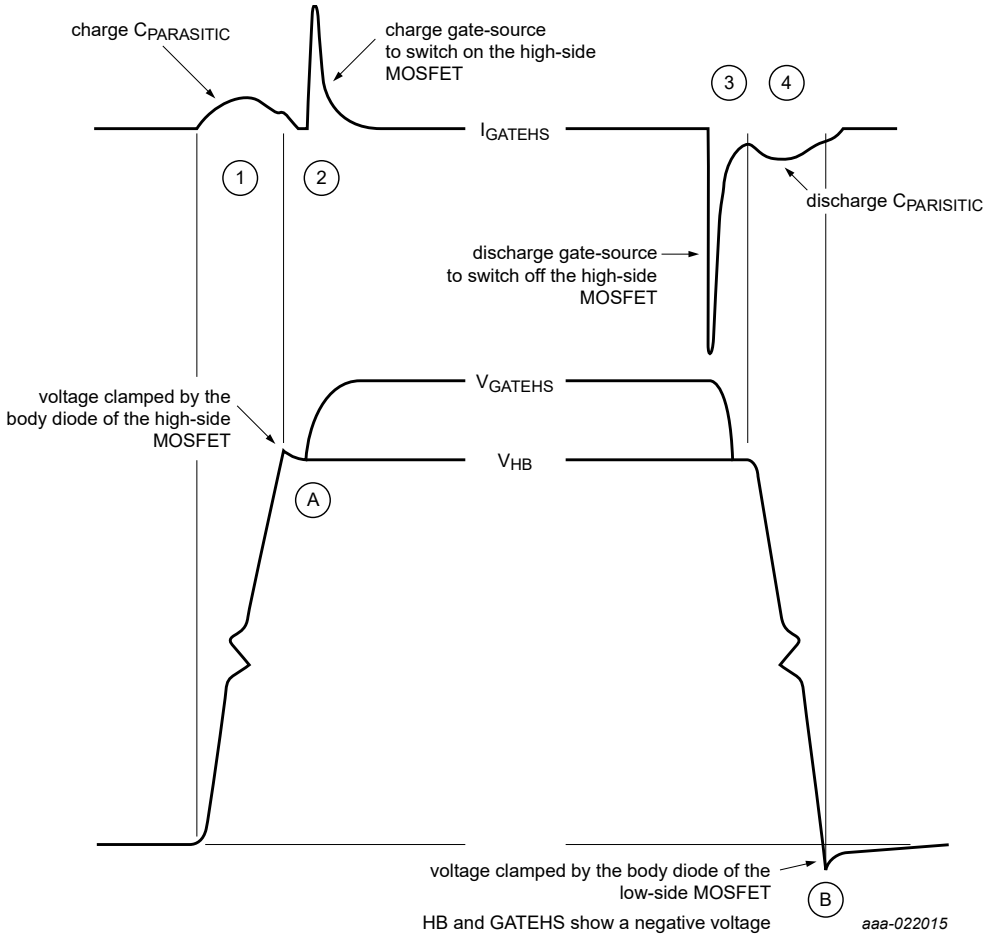


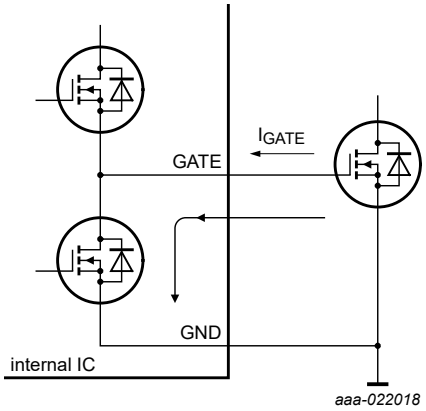
Figure 93. HB voltage and GATEHS current and voltage

Usually, a measurement with a good, calibrated voltage probe gives the most reliable result. A differential probe shows more voltage ringing and undershoot at point B.

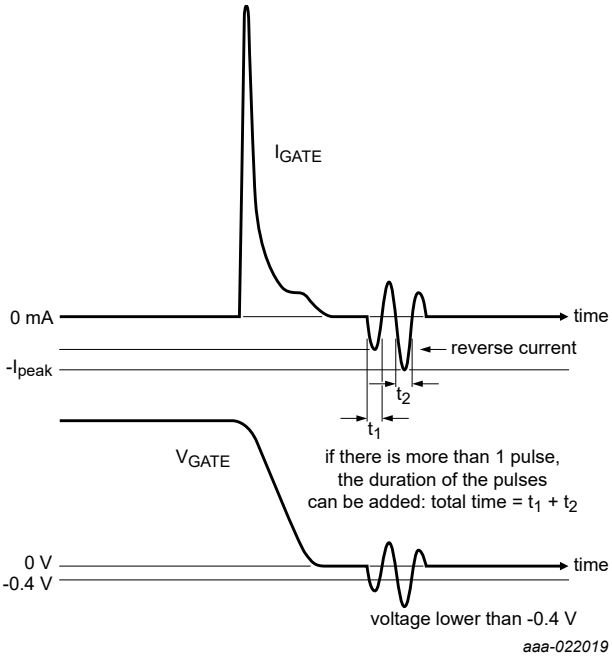
If the voltage measurement shows a critical voltage level or a voltage level that is too low (negative) in B, a current measurement of HB and GATEHS can help. When the current shows good functional behavior, like the GATEHS current shown in points 3 and 4, the result can be acceptable. The current must not show a change of direction (polarity).

12.11.5 Gate drivers GATEPFC and GATELS

Section 7.7 provides information concerning limiting values for TEA19162 pin 1 (GATEPFC) and TEA19161 pin 6 (GATELS). It also provides a guideline for acceptable levels when limiting values are exceeded for repetitive events (see Figure 94 and Figure 95).



a. Circuit



b. Measurement example

Figure 94. Ringing after GATE driver switch-off

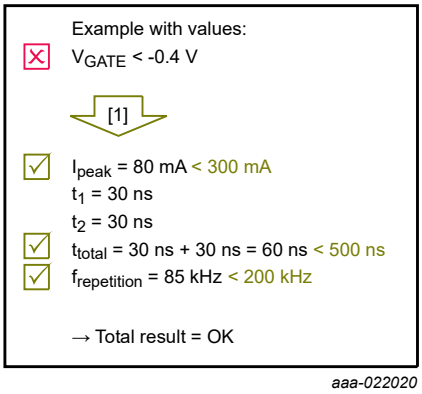


Figure 95. Example of checking if the gate driver reverse current is OK at switch-off

12.11.6 Other IC pins

12.11.6.1 SUPIC: TEA19161 pin 1 and TEA19162 pin 4

V_{SUPIC} limiting values: −0.4 V < V_{SUPIC} < +36 V

Usually, sufficient decoupling exists because of a capacitor on this pin. There is a large voltage margin to the limiting values. With accurate voltage measurement, there are no critical results.

A low voltage level shows a functional protection.

12.11.6.2 SUPREG: TEA19161 pin 5

V_{SUPREG} limiting values: −0.4 V < V_{SUPREG} < +12 V

Usually, sufficient decoupling exists because of a capacitor on this pin. With accurate voltage measurement, no unclear results are provided.

The IC generates the SUPREG voltage. The SUPREG pin can only source current. It cannot actively sink current at the voltage regulator function. In some applications, an unintended voltage increase can occur because of currents through grounding tracks. A low voltage level shows a functional protection. A SUPREG voltage higher than 12 V must be avoided because it can overstress or damage internal circuit components.

12.11.6.3 SUPHV: TEA19161 pin 8

V_{SUPHV} limiting values: −0.4 V < V_{SUPHV} < +700 V

Usually, the high bias voltage on this pin provides a great voltage margin to the limiting values. With accurate voltage measurement, no critical results are provided.

12.11.6.4 SNSAUX: TEA19162 pin 8

V_{SNSAUX} limiting values: −25 V < V_{SNSAUX} < +25 V

An auxiliary winding on the PFC coil generates the voltage on this pin. The voltage signal to this pin provides sufficient margin to avoid critical measurement results. With accurate voltage measurement, no unclear results are provided.

A special situation for this pin is the voltage during a mains surge test. An extra high voltage can be expected on the auxiliary winding of the PFC coil. The recommended 5.1 kΩ resistor and the internal 33 V zener diodes are intended to protect the IC. A peak current of 10 mA is acceptable.

12.11.6.5 GND: TEA19161 pin 4 and TEA19162 pin 2

Reference for voltage measurements.

12.11.7 Exceeding levels provided in the guidelines

When the general guidelines levels provided are exceeded, the situation can still be acceptable. However, expert judgment is required to collect observations and arguments and come to a conclusion.

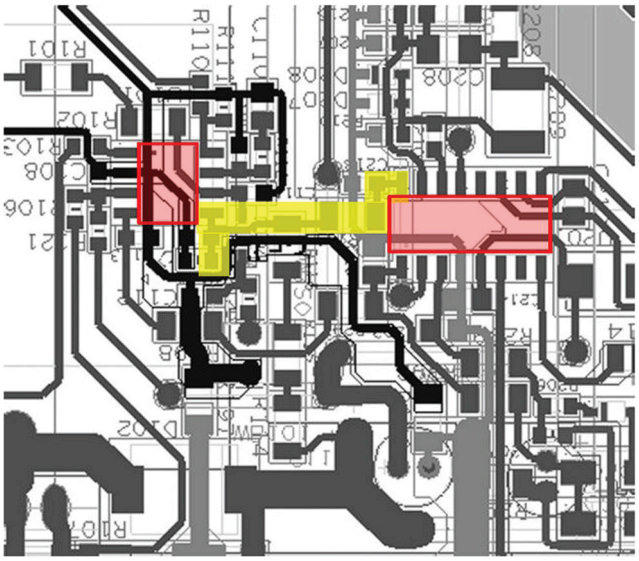
13 Important PCB layout design rules

13.1 Short SNSBOOST track length

To avoid mutual disturbance between the TEA19161 and the TEA19162 because of converter switching, both ICs must have a separate PCB layout structure. A greater distance between the converters can help. However, the SNSBOOST track that connects both controllers for communication and boost voltage sensing carries a high-impedance divider signal that is sensitive to disturbance.

To avoid disturbances:

- To minimize the length of the SNSBOOST track between the two ICs, the TEA19161 and TEA19162 ICs must be placed relatively close to each other.
- The SNSBOOST resistive divider position must be optimized for PFC regulation loop performance.
- Two disturbance filtering capacitors from SNSBOOST to GND must be present. A higher value (typical between 1 nF and 4.7 nF) near the TEA19162 (PFC) and a lower value (typical 680 pF) near the TEA19161 (HBC).



aaa-023134

- Yellow marked area: SNSBOOST connection
- Area marked red: TEA19161 and TEA19162 ICs

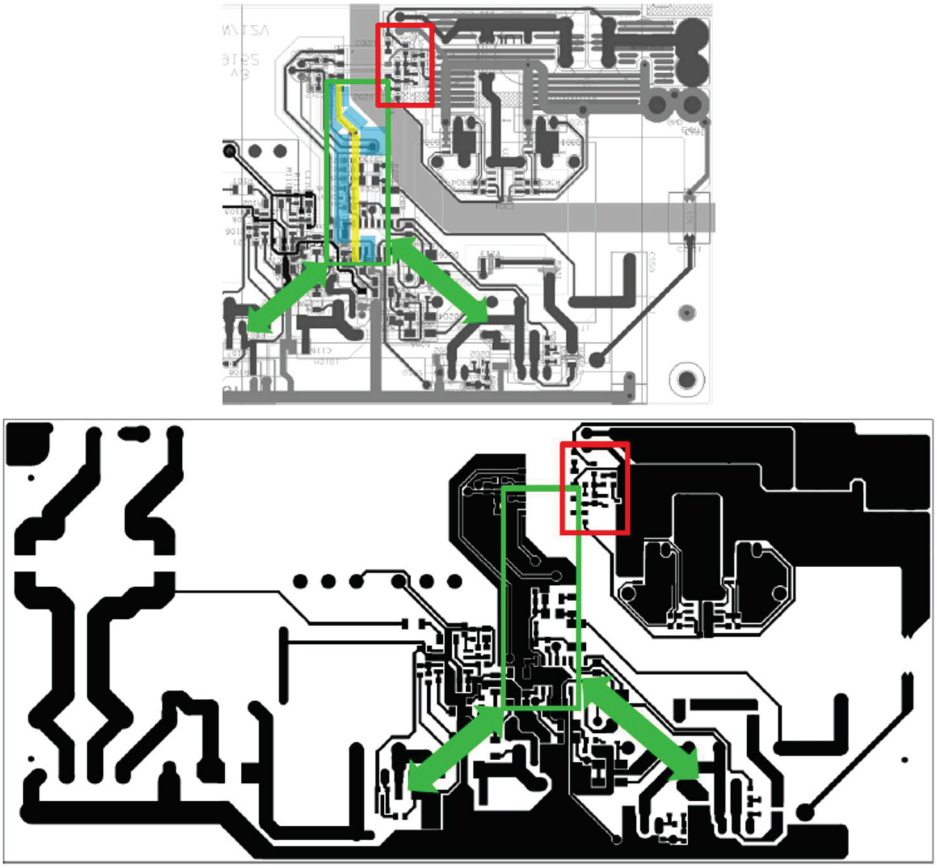
Figure 96. Short SNSBOOST track between TEA19161 and TEA19162

13.2 TEA19161: Shielding the SNSFB track

Because the SNSFB function works on small current levels to minimize energy consumption at no load, this signal is more sensitive to disturbances.

The main reason for disturbance that can make regulation unstable is capacitive coupling to converter switching tracks (HB or PFC-drain). To avoid disturbance in the SNSFB:

- The SNSFB track must be placed relatively far from the power part of the converters (HBC and PFC).
- To shield the SNSFB track, put grounded tracks alongside it (and a ground plane in case of double-sided copper design).
- The SNSFB track does not have to be short. To obtain a greater distance to HB, a longer track is required.



aaa-023143

- Yellow marked area: SNSFB
- Blue marked area: Shielding GND
- Green marking rectangle: SNSFB layout area
- Green arrows: Showing that SNSFB is placed far from HBC and PFC converter switching
- Area marked red: Shows a compact TL431 circuit design

Figure 97. SNSFB: A longer but shielded track far from the converter switching

13.3 TL431 circuit must be compact

Because the SNSFB function works on small current levels to minimize energy consumption at no load, this signal is more sensitive to disturbances.

To prevent disturbances because of PFC switching noise, the secondary part of the feedback circuit must also be compact. This type of disturbance leads to a 100 Hz or 120 Hz extra output voltage ripple. It is a mains voltage-related disturbance.

13.4 Separate GND connections for TEA19161 and TEA19162

To avoid mutual disturbances, the grounding of the PFC and HBC controllers must be connected separately in the PCB layout. Current pulses through ground tracks can lead to a wrong (voltage) value or signal on a pin that uses the ground level as a reference.

Figure 98 shows the energy flows. To avoid disturbances, these flows can be kept separate with a special grounding structure.

This concerns the length of the tracks but also the size of the loop surface (mm^2).

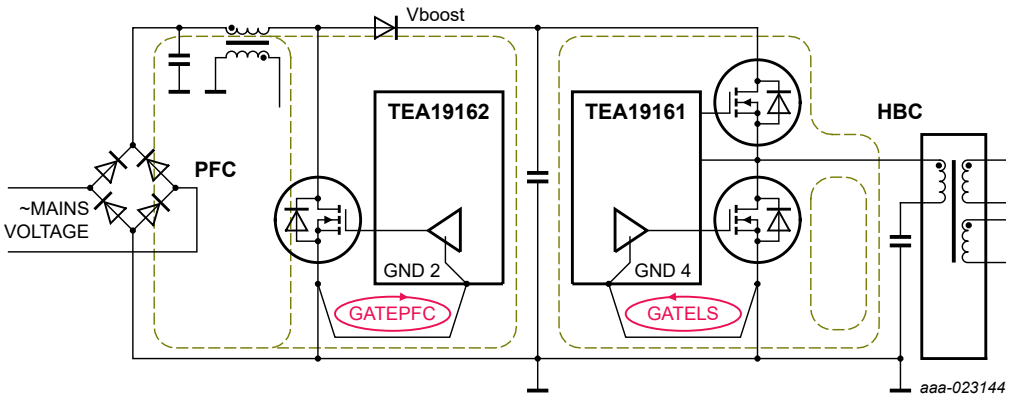


Figure 98. Grounding structure PFC and HBC controllers

Connecting the controller ICs with separate ground tracks to the shared bulk capacitor function, minimizes mutual disturbances.

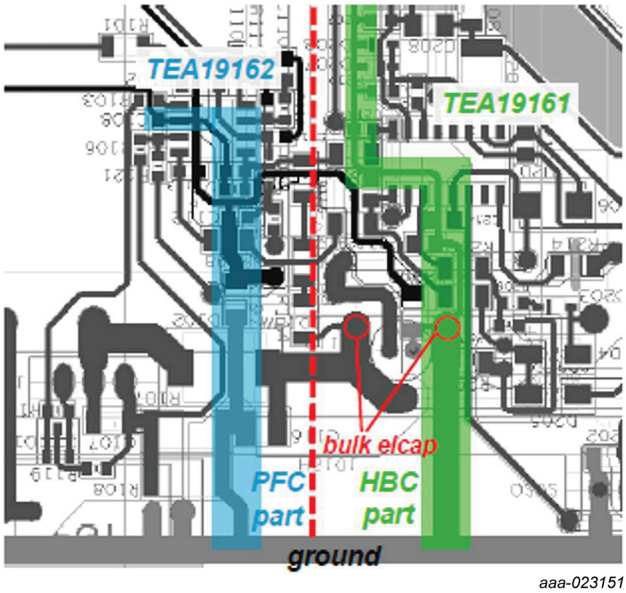


Figure 99. Example of connecting the controllers at separate grounding trees

13.5 Common-mode surge

Common-mode surge testing generates a current through the converter circuit. To prevent that current flows near sensitive components, like the controller IC, the PCB layout design must provide guidance. A star-point grounding structure can provide it.

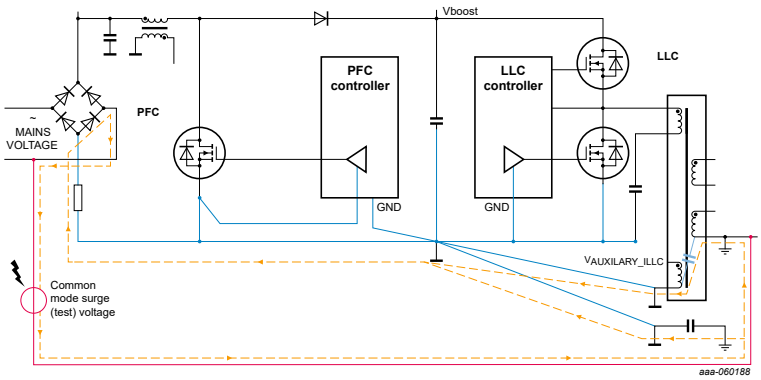


Figure 100. Grounding structure with CM surge current flow

13.6 TEA19161: Very short SNSCUR track

The TEA19161 SNSCUR function senses the input signal cycle-by-cycle at low voltage levels with a high-impedance input. The signal is applied to the pin with a decoupling capacitor that must be placed very close to the IC to avoid disturbances on the connecting track.

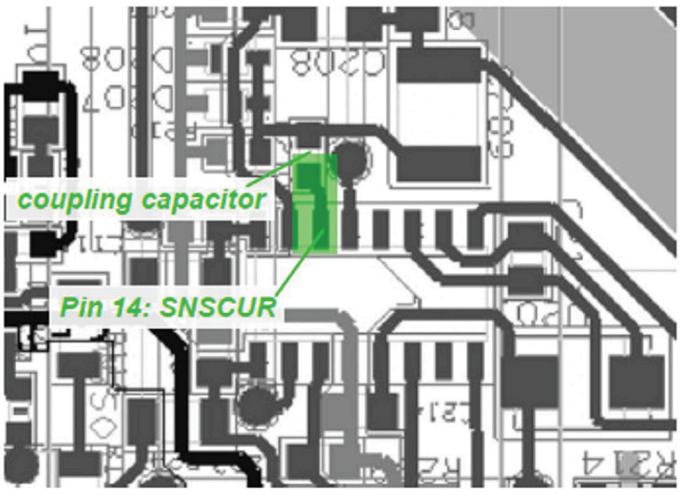


Figure 101. TEA19161 SNSCUR pin connection

13.7 TEA19162: Placing of SNSMAINS mains sensing resistors

To save power, the TEA19162 PFC controller SNSMAINS mains sensing function uses low current levels. To avoid disturbances, the mains sensing resistors must be placed close to the IC.

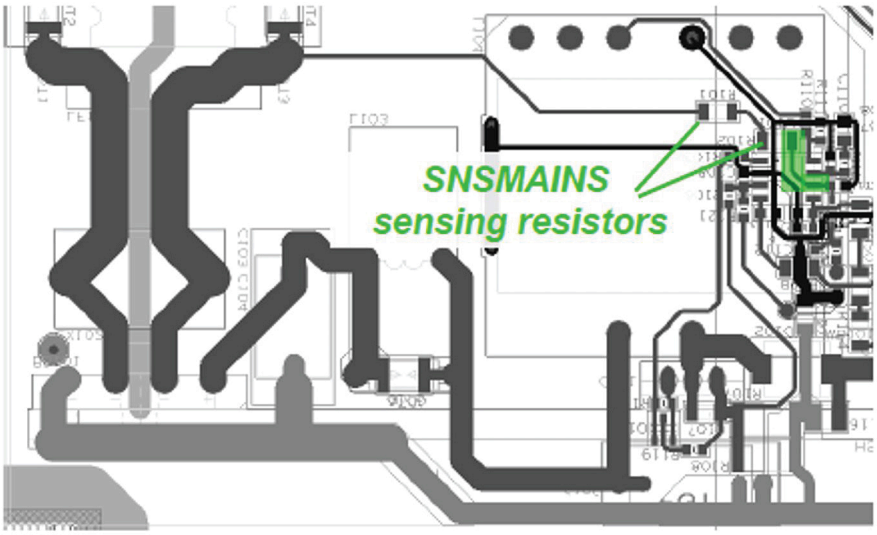


Figure 102. SNSMAINS mains sensing resistors placed close to the TEA19162

14 Protections

Table 15. Protections overview

Protection	Description	PFC action	HBC action
PFC protections			
UVP SUPIC	undervoltage protection	PFC = off; restart when V_{SUPIC} > 13 V	off
OTP-internal	internal overtemperature protection	latched (safe restart for CT version)	off
OTP-external	external overtemperature protection	latched (safe restart for CT version)	off
UVP SNSMAINS (brownout)	undervoltage protection	PFC = off; restart when $I_{SNSMAINS}$ > 5.75 µA	-
OVP SNSBOOST	overvoltage protection	PFC = off; restart when $V_{SNSBOOST}$ < 2.5 V	-
SCP SNSBOOST	short circuit protection	PFC = off; restart when $V_{SNSBOOST}$ > 0.4 V	-
OLP SNSBOOST	open-loop protection	PFC = off; restart when $V_{SNSBOOST}$ > 0.4 V	-
OCP SNSCUR	overcurrent protection	PFC MOSFET switched off; continue operation when V_{SNSCUR} = 0.5 V	-
HBC protections			
UVP SUPIC/SUPREG	undervoltage protection	-	LLC = off; recharge via SUPHV; restart when V_{SUPIC} > 19.1 V
UVP SUPHS	undervoltage protection	-	GateHS = off
UVP SNSBOOST	undervoltage protection	-	LLC = off; restart when $V_{SNSBOOST}$ > 2.3 V
OVP SNSOUT	overvoltage protection	off	latched (safe restart for CT version)
CMR	capacitive mode regulation	-	system ensures that the mode of operation is inductive
OCP SNSCUR	overcurrent protection	off	switch-off cycle-by-cycle; After 5 consecutive cycles, it follows the OPP setting for latched or safe restart. [1]
OTP	overtemperature protection	off	latched (safe restart for CT version)
OPP	overpower protection	off	latched/safe restart [1]

[1] External components set the latched/safe restart action.

The TEA19161CT and TEA19162CT are safe-restart IC versions. Table 15 shows the differences between the TEA19161T and TEA19162T.

14.1 Warning about disabling protection functions

Temporarily disabling a protection function during debugging of an application can be useful for analyzing unexpected behavior. But most protections are important for making a power supply safe. In principle, all protections must be active and working properly in the final development stage.

By exception, to meet certain requirements or avoid false triggering for a critical function, disabling a protection function can be considered. Methods are provided for disabling a protection function. Ensure that it does not compromise the safety of the product.

There are some dependencies between protection functions, like the LLC OCP following the selected follow-up for OPP (safe restart of latched). Table 15 provides an overview on protections.

14.2 PFC protections

14.2.1 UVP SUPIC

When the voltage on the SUPIC pin drops to below 9 V, the IC stops operation. A system reset is activated at 3.5 V. When SUPIC drops to below 13.2 V, a latched protection is reset.

When the SUPIC voltage drops to 14 V during the non-switching period in burst mode, the TEA19161 HV source is activated. It regulates the SUPIC voltage with a hysteresis of 0.9 V above 14 V, which avoids that the system stops during a long non-switching period (see Section 6).

14.2.2 SUPIC UVP and OPP

Because the output power is limited (150 % or 200 %), the output voltage drops when the requested output power (load) exceeds this level.

As a result of the dropping output voltage, the supply voltage of the TEA19161 via an auxiliary winding also drops.

Then either the OPP protection is triggered or the $V_{uvp(SUPIC)}$ protection. To ensure that the response is the same, the $V_{uvp(SUPIC)}$ follows the setting of the OPP protection concerning the follow-up. If the OPP is set for latched, the $V_{uvp(SUPIC)}$ is also latched.

However, there is an exception. When, a $V_{uvp(SUPIC)}$ protection is detected during start-up, an overpower condition cannot cause it. In this situation, a restart follows the SUPIC undervoltage protection.

14.2.3 Overtemperature protection (OTP)

The TEA19162 provides two OTP protections, an internal and external OTP. Both protections provide a latched protection until the decreasing of the SUPIC or SNSMAINS voltages resets the latched condition. For the CT versions, the OTP protections trigger a safe restart.

Pulling up the voltage on the SNSBOOST pin to above 2 V during engineering or production testing can also reset a latched protection.

14.2.3.1 Internal OTP

The IC contains an internal temperature protection. When the internal temperature exceeds 150 °C, the PFC stops operation. It also disables the HBC operation by pulling down the SNSBOOST voltage.

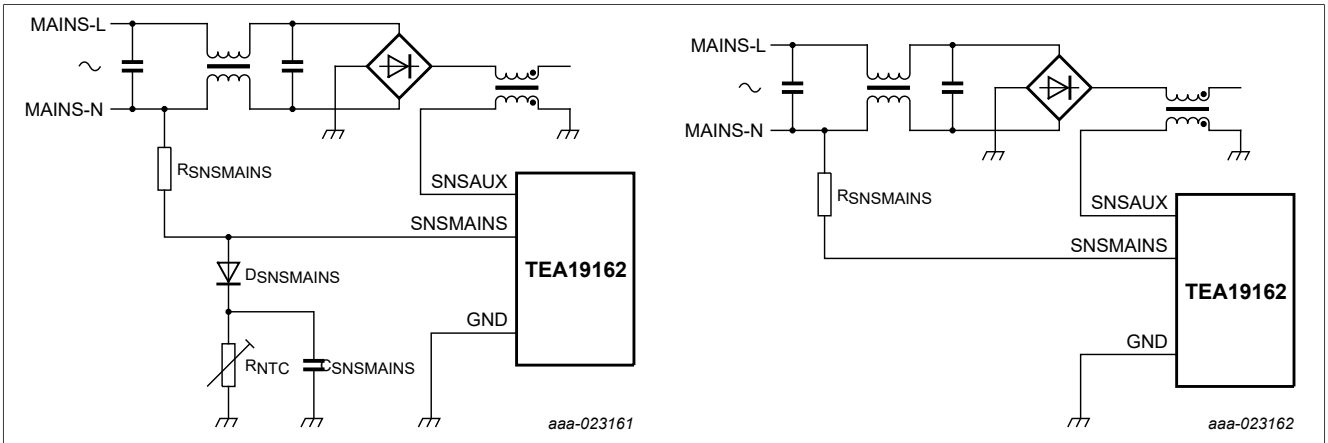
14.2.3.2 External OTP

The SNSMAINS pin combines two functions. The mains voltage sensing and the sensing of an external NTC for detecting an OTP. The functions are alternatingly active in time. Each function is active during a half-mains voltage cycle.

During OTP sensing, a current of 200 µA from an internal source flows from the pin through the external diode and NTC to ground. The resulting voltage on the pin is measured. When the voltage on the pin is below 2 V at four consecutive measuring cycles, the OTP protection is activated.

14.2.3.3 Not using the external OTP function

When no external OTP function is required, the external OTP components can be omitted.



a. SNSMAINS with external OTP

b. SNSMAINS without external OTP

Figure 103. SNSMAINS with and without OTP function using external NTC

14.2.4 UVP SNSMAINS

At an SNSMAINS peak current level of 5.75 µA, the PFC start-up is enabled (brownin). At 5 µA, the operation is disabled (brownout; see Section 8.3).

14.2.5 OVP SNSBOOST

The overvoltage protection circuit prevents output overvoltage during load steps and mains transients. When the voltage on the SNSBOOST pin exceeds 2.63 V for a period longer than 100 µs, the switching is stopped. When the voltage drops to below 2.53 V, the switching resumes with a soft start.

14.2.6 SCP and OLP SNSBOOST

The PFC does not start switching until the voltage on the SNSBOOST pin exceeds $V_{start(scp)}$ (0.5 V). This function protects against a short circuit and an open-loop condition on SNSBOOST.

14.2.7 OCP SNSCUR

Sensing the voltage across an external sense resistor in series with the source of the PFC MOSFET limits the maximum PFC peak current cycle-by-cycle. The voltage is measured via the SNSCUR pin. It is limited to 0.5 V. When the voltage on the SNSCUR pin reaches 0.5 V, the MOSFET is switched off (see Section 8.17).

14.3 HBC protections

14.3.1 UVP SUPIC and SUPREG

When the SUPIC voltage has reached the start level of 19.1 V, the IC operation is enabled. If the HV source supplies the IC, the SUPIC voltage is regulated with a hysteresis of 0.7 V. When the SUPIC voltage drops to below 13.2 V, the converter stops operating. When the SUPIC voltage reaches 3.5 V, a system reset is activated.

When the SUPIC voltage drops to 14 V during the non-switching period in burst mode, the HV source is activated. It regulates the SUPIC voltage with a hysteresis of 0.9 V above 14 V, which helps to avoid that the system stops during an incidental extra long period of not switching. The extra long period of not switching can happen after transients like load steps. As mentioned in Section 6.2.2, the activation of the HV source is an emergency function. The HV source backup system cannot always avoid protection triggering. To reduce the risk of accidental system protection, regular activation during normal low-load or no-load operation must be avoided. To avoid activation, the auxiliary winding SUPIC supply must keep sufficient margin to the 14 V ($V_{low(SUPIC)}$) level.

The series stabilizer for the SUPREG pin is charged along with the SUPIC pin. To enable HBC operation, the SUPREG voltage must reach the 11 V regulation level. When SUPREG voltage drops below 9 V, the IC stops operating (see Section 6).

14.3.2 UVP SUPHS

When the voltage across capacitor C_{SUPHS} ($V_{SUPHS} - V_{HB}$) drops to below 7 V, the driver stops operation to prevent unreliable switching (see Section 6.6).

14.3.3 UVP SNSBOOST

When the voltage on the SNSBOOST pin drops to below 1.6 V, the HBC stops switching when the low-side MOSFET is on. When the SNSBOOST voltage exceeds the start level of 2.3 V, the HBC start/restarts (see Section 9.1).

14.3.4 OVP SNSOUT

SNSOUT provides two main functions:

- Setting the burst mode repetition frequency
- OVP function at 3.5 V

The resistor value from SNSOUT to ground (R2) must be correct for the burst mode repetition frequency setting. The value of R1 can be used to make the correct resistive divider for sensing the peak voltage from the auxiliary winding that represents the HBC output voltage (V_{out}). When this voltage exceeds 3.5 V during the internal time delay, the system stops switching and enters a latched protection or a safe restart sequence.

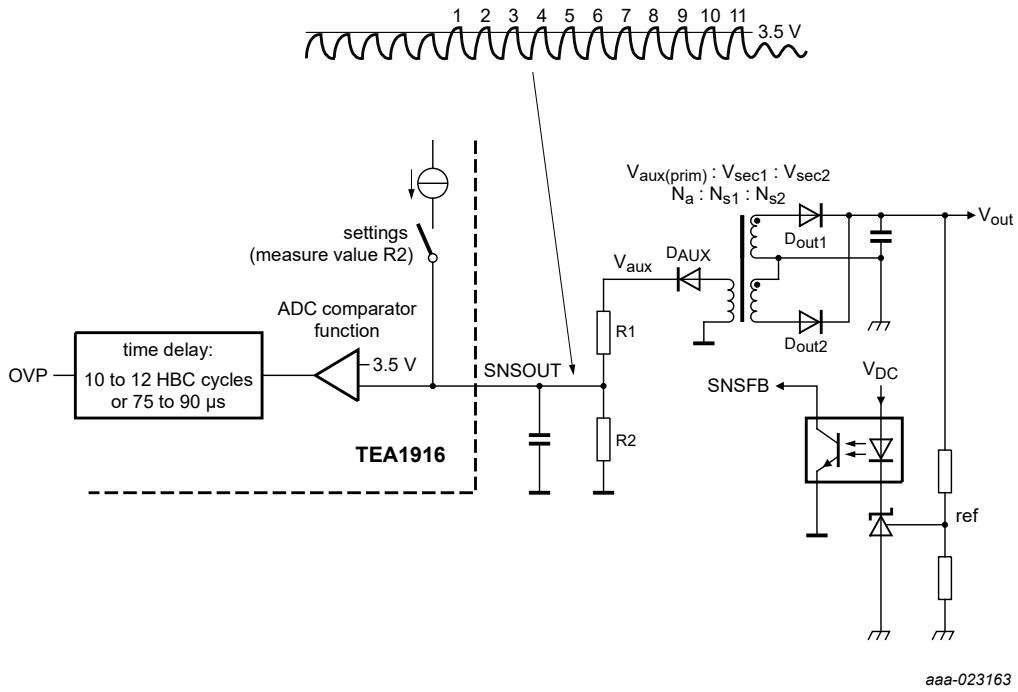


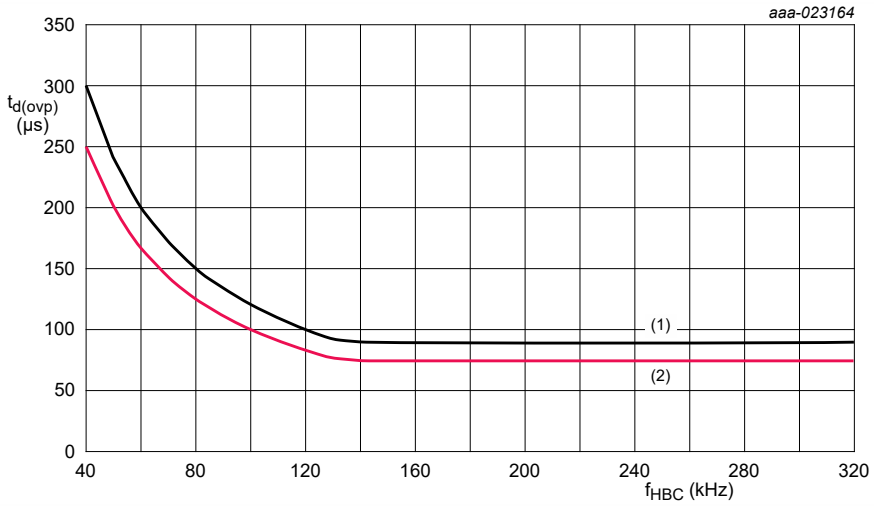
Figure 104. SNSOUT OVP function

14.3.4.1 Time delay until protection

To prevent false triggering by short events or disturbances, the OVP function includes a time delay. An internal counter monitors the number of cycles that show a higher SNSOUT voltage. When the number of pulses reaches approximately 11, the protection is activated (latched or safe-restart). Because of the internal sampling method that uses a digital-to-analog converter for several functions by time multiplexing, there can be an error of 1 cycle for the time delay. So, the delay can be 10, 11, or 12 cycles.

To prevent a short delay time for high-frequency switching, a minimum delay time is included. This extra function limits the delay time to between 75 µs and 90 µs.

Figure 105 shows the resulting OVP delay.



- (1) Maximum OVP delay time
- (2) Minimum OVP delay time

Figure 105. OVP delay time

The SNSOUT-OVP system (filter) counts in number of cycles, not in time.

If the frequency (time in each cycle) changes during the OVP counting, the resulting delay is a summation of all these times. So, if the 11 cycles (for example) consist of 5 × 20 µs + 5 × 22 µs + 1 × 24 µs, the total time delay is 234 µs.

14.3.4.2 Auxiliary winding construction for OVP sensing

When dealing with a mains insulated converter, the HBC output voltage can be measured using the auxiliary winding of the resonant transformer. To measure the secondary voltage of the primary circuit auxiliary winding accurately, a special transformer construction is required.

To work correctly, this winding must have a good coupling with the secondary winding and a minimum coupling with the primary winding. In this way, a good representation of the output voltage situation is obtained (see Section 6.3.2).

To meet the mains insulation requirements, triple insulated wire can be used.

14.3.4.3 Calculation of OVP sensing using auxiliary winding

This section provides a method that can be used to estimate the accuracy of indirect output voltage sensing using an auxiliary winding (See Section 14.3.4 for names and functions).

Transformer ratio:

- N_a is the number of turns on an auxiliary winding
- N_{s1} is the number of turns on the secondary (output) winding 1
- N_{s2} is the number of turns on the secondary (output) winding 2
- $N_{s1} = N_{s2} = N_s$

$$V_{aux} = V_{out} \times \frac{N_a}{N_s} \quad (49)$$

Voltage drop over the rectifier diodes:

- D_{aux} is the voltage drop over the diode of the auxiliary voltage
- D_{out1} is the voltage drop over the diode1 of the output voltage
- D_{out2} is the voltage drop over the diode2 of the output voltage

$$D_{out1} = D_{out2} = D_{out} \tag{50}$$

Combination Equation 46 and Equation 47:

$$V_{aux} = \left(\left(V_{out} + D_{out} \right) \times \frac{N_a}{N_s} \right) - D_{aux} \tag{51}$$

Relationship V_{aux} and the voltage on the SNSOUT pin:

$$V_{SNSOUT} = V_{aux} \times \frac{R2}{(R1 + R2)} \tag{52}$$

OVP protection:

V_{SNSOUT} = 3.5 V

Combination Equation 48 and Equation 49:

$$V_{SNSOUT} = 3.5\ V = V_{aux} \times \frac{R2}{(R1 + R2)} \tag{53}$$

$$V_{SNSOUT} = 3.5\ V = \left(\left(\left(V_{out} + D_{out} \right) \times \frac{N_a}{N_s} \right) - D_{aux} \right) \times \frac{R2}{R1 + R2}$$

Equation 50 calculates the nominal value and the relationship between the parameters.

14.3.4.4 Differences between theory and practice: Calibration

Because of several reasons (some of them given in the remarks), the calculated value can deviate from the value in practice. Still, the equations provide the relationship between several parameters.

If a parameter deviates from the theoretical nominal (for example +5 %) in reality, the deviation can be used to calibrate the theoretical calculation to the reality.

If there is a significant contribution, tolerance analyses can be done using the calibrated calculation.

14.3.4.5 Example of calibration and an estimation of tolerance

$$V_{SNSOUT} = 3.5\ V = \left(\left(\left(V_{out} + D_{out} \right) \times \frac{N_s}{N_a} \right) - D_{aux} \right) \times \frac{R2}{(R1 + R2)} \tag{54}$$

Using example values:

$$V_{SNSOUT} = 3.5\ V = \left(\left(\left(V_{out} + 0.7\ V \right) \times \frac{3}{2} \right) - 0.7\ V \right) \times \frac{10\ k\Omega}{56\ k\Omega + 10\ k\Omega} \tag{55}$$

$$V_{out} = \left(3.5 \times 6.6 + 0.7 \right) \times 0.667 - 0.7 = 15.2\ V = V_{out(ovp)calculated}$$

Calibration using OVP measurement results from the real application:

- I_{out} = 0.1 A; $V_{out(ovp)}$ = 15.3 V (measured)
- I_{out} = 10 A; $V_{out(ovp)}$ = 15.2 V (measured)
- I_{out} = 20 A; $V_{out(ovp)}$ = 15.1 V (measured)
- Correction: $V_{ovp(reality)} = V_{out(ovp)calculated} - 0.01I_{out} + 0.1\ V$

OVP protection tolerance analyses:

Analysis for the worst case condition when I_{out} = 0.1 A and the measured level for OVP was $V_{out(ovp)}$ = 15.3 V.

$$V_{out(ovp)} = (3.5 \times 6.6 + 0.7) \times 0.667 - 0.7 + 0.1 = 15.3\ V\ (nominal) \quad (56)$$

List of tolerances:

- V_{SNSOUT} = 3.5 V; 4 % (TEA19161 data sheet (Ref. 1/Ref. 3))
- Auxiliary resistive divider: 1 % (when using 1 % resistors)
- Forward voltage diode: 10 % (estimation/assumption)
- Transformer ratio: 3 % (transformer specification)
- Calibration factory: 10 % (estimation/assumption)

Using all worst case tolerances (highest voltage):

$$V_{out(ovp)} = \quad (57)$$

$$(3.64 \times 6.66 + 0.77) \times 0.687 - 0.63 + 0.11 = 16.66\ (worst\ case)$$

$V_{out(ovp)}$ is 10 % higher than the nominal value (15.3 V).

Using the statistical method (root of squares method) for nominal distributions and neglecting the minor contributions (forward voltage + calibration factor):

$$V_{out(ovp)} = V_{ovp(SNSOUT)} \times \frac{N_s}{N_a} \times \left(\frac{(R1+R2)}{R2}\right) \quad (58)$$

Expected tolerance: $\sqrt{(4^2 + 1^2 + 3^2)} = 5.1\ \%$

14.3.4.6 Output voltage increase because of time delay

The filter for false protection triggering introduces a waiting time until protection is activated. In a fault condition, the output voltage continues to increase during this period.

The additional voltage on the output can be estimated by measuring the systems voltage increase (dV/dt) and multiplying this measurement with the OVP delay (see Section 14.3.4.1).

Example:

Measured at start-up with no output load, the voltage near the OVP protection level increases with 30 mV/cycle. The maximum number of cycles for OVP delay is 12. So, the worst case is 12 × 30 mV = 360 mV voltage increase.

Together with the estimated tolerance (see Section 14.3.4.5), the maximum output voltage can be found.

In the example in Section 14.3.4.5, the statistical tolerance was 5.1 % on a nominal setting of 15.3 V. The maximum voltage including the output voltage increase from these examples is:

$$15.3\ V + (5.1\ \% \times 15.3\ V) + 0.36\ V = 16.44\ V$$

OVP sensing on the secondary side can improve the tolerance (see Section 14.3.4.7).

14.3.4.7 OVP triggering using an external signal

A latched or safe restart protection can be activated by pulling SNSOUT to a voltage exceeding 3.5 V. Figure 106 shows an example using an optocoupler and secondary output voltage sensing.

Even though the voltage on the SNSOUT pin is now constant and not pulsed, the protection delay remains valid.

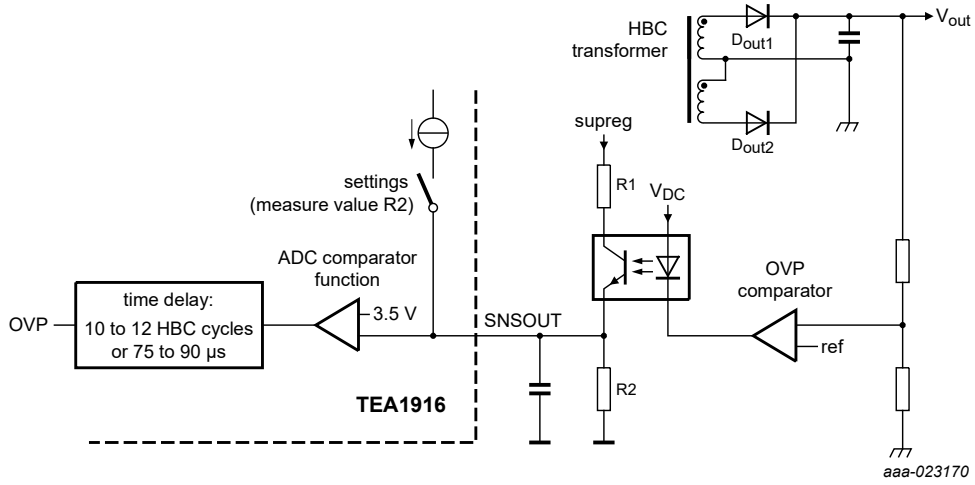


Figure 106. OVP triggering using an external function

OVP sensing is more accurate than auxiliary winding. However, for OVP sensing, an extra circuit is required.

Tolerance is only related to the measurement resistors (normally 1 % or less) and the OVP comparator (several commercial types offer 2 % or 1 % accuracy). The resulting statistical tolerance can be reduced to 2 % or less.

The effect of the signal delay time and the OVP delay time remains.

14.3.4.8 Disabling the OVP function on the SNSOUT pin

When the OVP function is not required, the SNSOUT pin can be connected for the setting function with only the R2 resistor to GND.

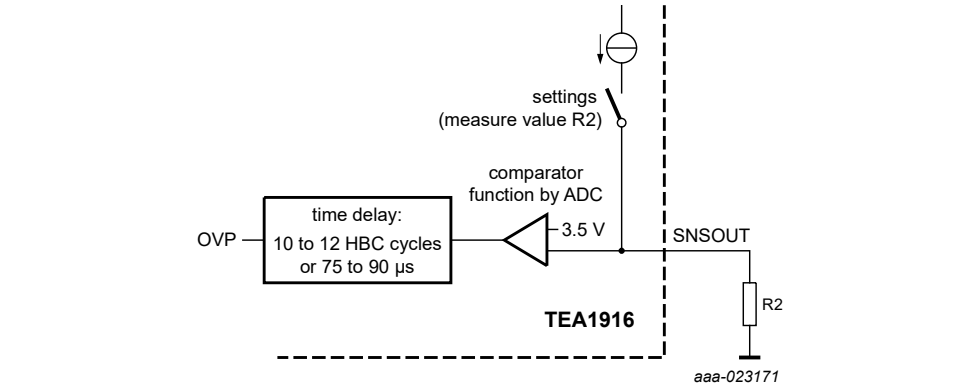


Figure 107. SNSOUT OVP not used; setting function only

14.3.5 Capacitive mode regulation (CMR)

The capacitive mode regulation is implemented via a forced switch-off at 2.4 V or 2.6 V (signal bias level on the SNSUR pin is 2.5 V) on the SNSCUR pin (see Section 9.3.7)

14.3.6 Overcurrent protection (OCP) on the SNSCUR pin

A small capacitor parallel to the resonant capacitor can sense the resonant current. A resistor R_m in series with this parallel capacitor shows a voltage that corresponds with the amplitude of the resonant current. This voltage can be used as an input for the SNSCUR pin.

The measured voltage must be connected to the SNSCUR pin using a 2.2 nF capacitor. The internal SNSCUR circuit adds a 2.5 V voltage bias to the signal on the pin.

If the measured voltage on resistor R_m exceeds the overcurrent level of ±1.5 V (4 V o 1 V on the SNSCUR pin), the corresponding switch (GATELS/GATEHS) is turned off. However, the system continues switching. In this way, the primary current is limited to the OCP level. If the OCP level is exceeded for 5 consecutive cycles (GATELS and/or GATEHS), the system stops switching and enters the protection mode. The PFC is disabled via the SNSBOOST pin.

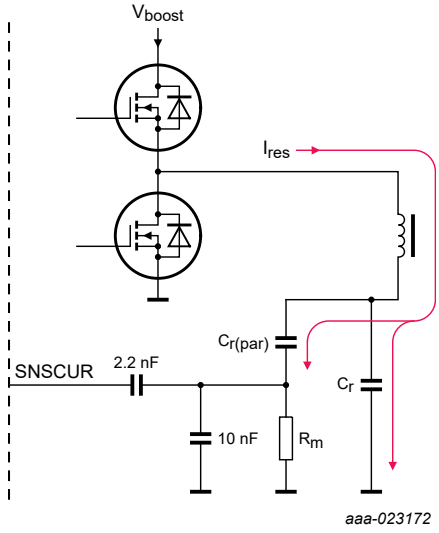


Figure 108. Typical current sensing circuit for SNSCUR

If the current measurement circuit in Figure 108 is used:

$$V_{peak(SNSCUR)} = R_m \times \left(\frac{C_{r(par)}}{\left(C_{r(par)} + C_r\right)}\right) \times I_{res(peak)} \quad (59)$$

The transformer (effective) turn ratio defines the relationship between the primary converter current and the secondary converter current.

$$V_{peak(SNSCUR)} = \frac{N_s}{N_p} \times I_{out(peak)} \quad (60)$$

In practice, the effective ratio between the currents is lower than the theoretical ratio of N_s/N_p. A measurement shows the correct value for a specific design. The relationship between the peak output current and the DC output current depends on the shape of the peak current. In practice, the multiplication factor (MF) is determined near the protection level for a specific design. Normally, a value close to 2.

$$I_{out(peak)} = MF_{peak\text{-}to\text{-}DC} \times I_{out(DC)} \quad (61)$$

When combining the various equations, the total of the relationships can be calculated:

$$V_{peak(SNSCUR)} = R_m \times \frac{N_s}{N_p} \times MF_{peak\text{-}to\text{-}DC} \times I_{out(DC)} \quad (62)$$

It is difficult to measure the voltage levels on the SNSCUR pin during operation because a voltage probe introduces serious disturbances. To monitor the behavior, check the signal across R_m.

14.3.7 Disabling the overcurrent protection (OCP)

The SNSCUR pin provides three functions:

- If the SNSCUR voltage − V_{bias} > ±1.5 V, the gate driver is switched off to limit the power to the OCP level. After 5 OCP cycles, a protection is activated.
- If the SNSCUR voltage − V_{bias} = ±100 mV for detecting the (almost) zero current level, the driver switches off to prevent capacitive mode switching.
- If the SNSCUR voltage − V_{bias} = ±13 mV for detecting the current polarity, This level is used as a parameter in the internal switching logic.

When two diodes are connected antiparallel to R_m, the OCP is disabled while the other two functions are still active.

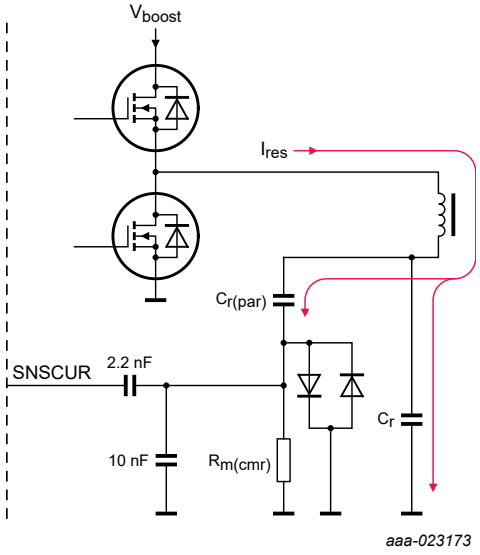


Figure 109. SNSCUR OCP function disabled using two diodes

14.3.8 Adapting trigger values for SNSCUR OCP and CMR

Normally, a suitable value for R_m can be found that works well for the OCP and the CMR functions. If finding a suitable value is not possible or critical, the circuit shown in Figure 110 can be used to set the trigger levels for OCP and CMR separately.

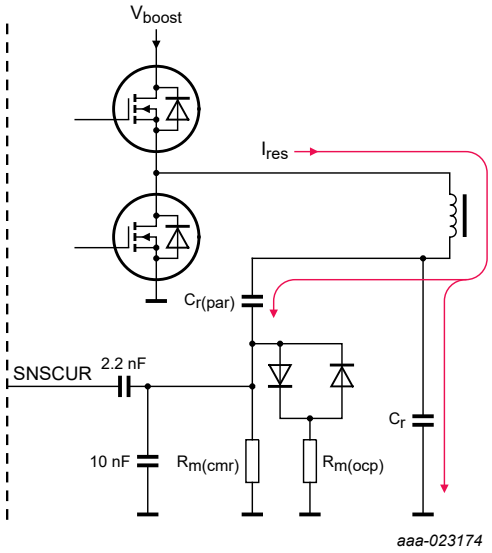


Figure 110. SNSCUR: Different R_m resistor values for OCP and CMR

14.3.9 Preventing unintended OCP triggering at start-up

At start-up, the primary current in the resonant converter can be high because the output voltage must still increase. To limit the primary current amplitude at start-up, the soft-start function is available by selecting the best R_{GATELS} value for a suitable start-up behavior (see Section 10.1).

To prevent that the OCP protection is triggered unintentionally, the resulting SNSCUR voltage levels must have sufficient reserves during start-up. Selecting a lower value for R_{GATELS} increases the reserves. The value of R_m in the SNSCUR circuit can also be reconsidered.

14.3.10 Internal OTP

When the internal junction temperature exceeds 140 °C, the internal overtemperature protection is triggered. Either a latched protection disables HBC and PFC switching or the system restarts after the temperature has dropped.

14.3.11 Overpower protection (OPP)

The OPP levels are related to $V_{hs(SNSCAP)}$ and $V_{ls(SNSCAP)}$ on the SNSCAP pin. The chosen setting can be either 125 % or 150 % power (see Section 10.2).

15 Application example: 240 W power supply

15.1 Circuit diagrams

15.1.1 PFC part

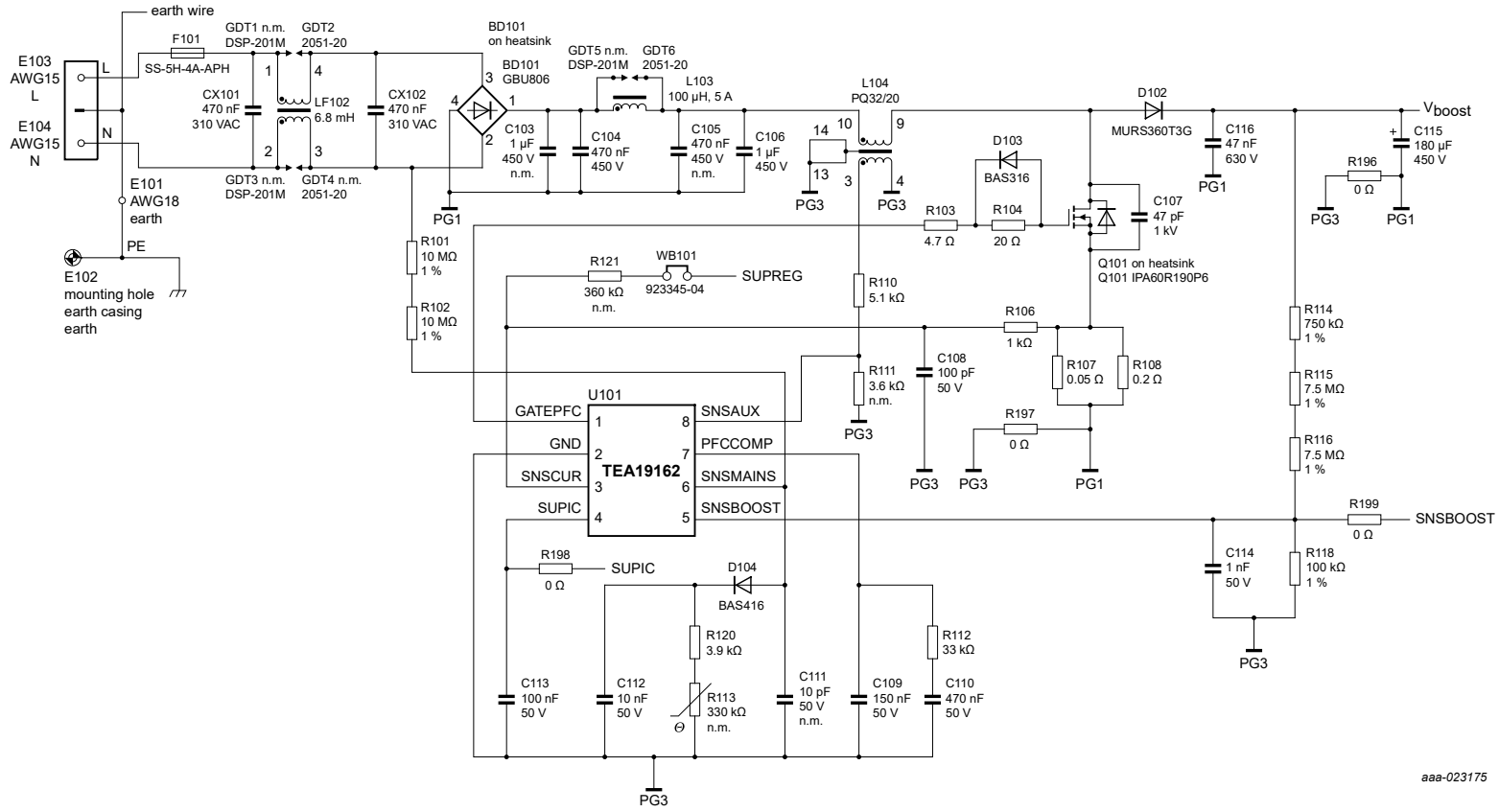


Figure 111. TEA1916 and TEA1995T 240 W power supply

15.1.2 LLC part

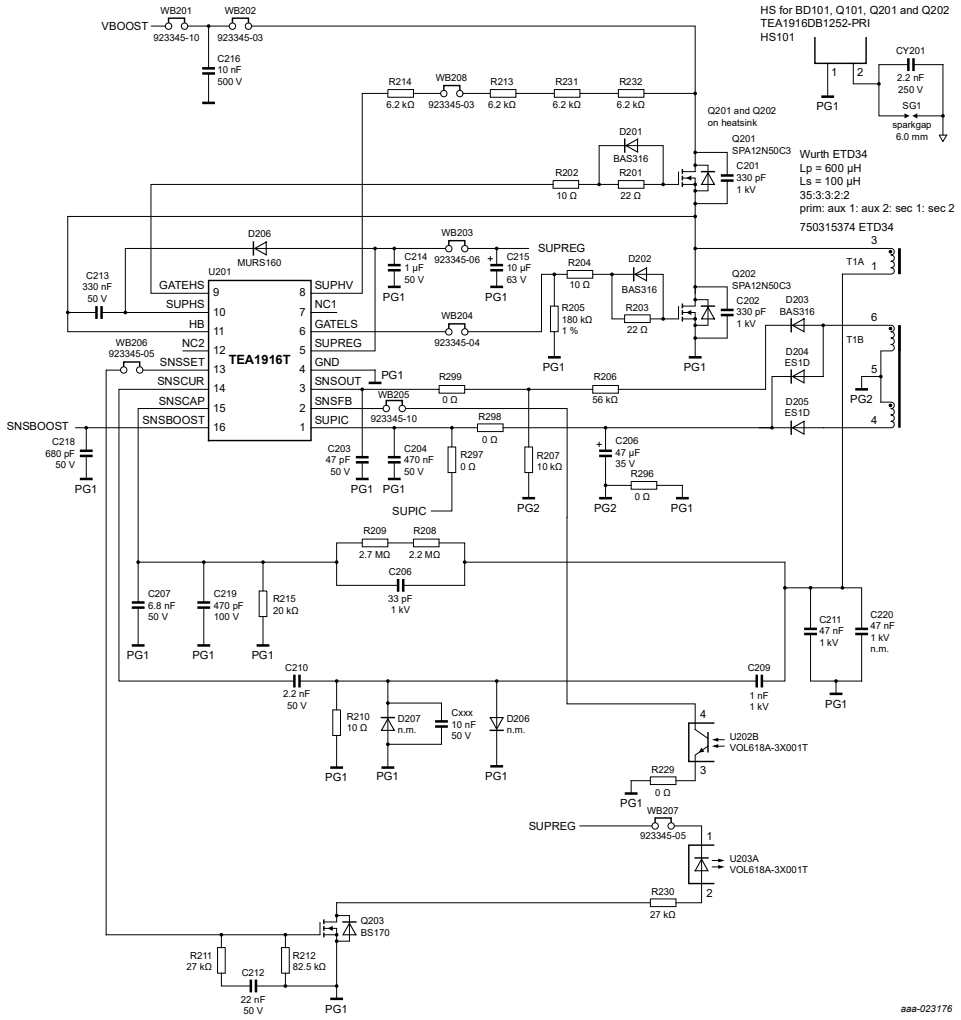


Figure 112. TEA1916 and TEA1995T 240 W power supply (LLC part)

15.1.3 SR part

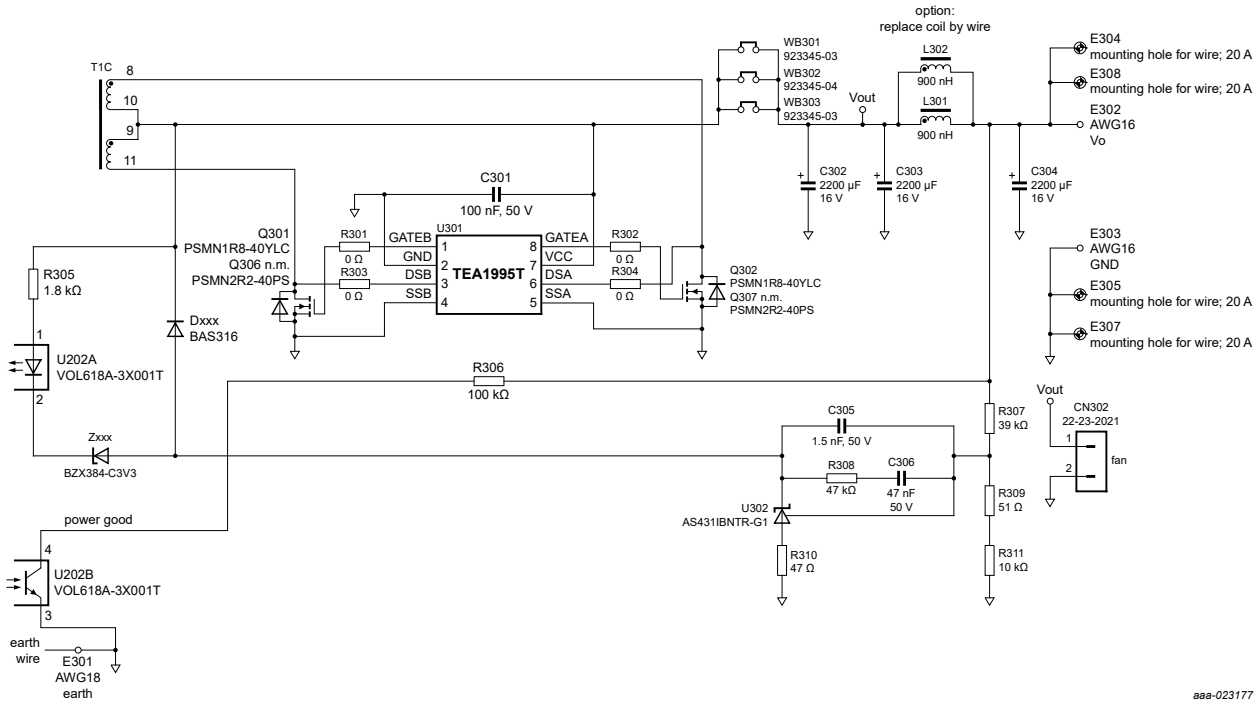


Figure 113. TEA1916 and TEA1995T 240 W power supply (SR part)

15.2 Circuit diagrams with function descriptions

15.2.1 PFC part

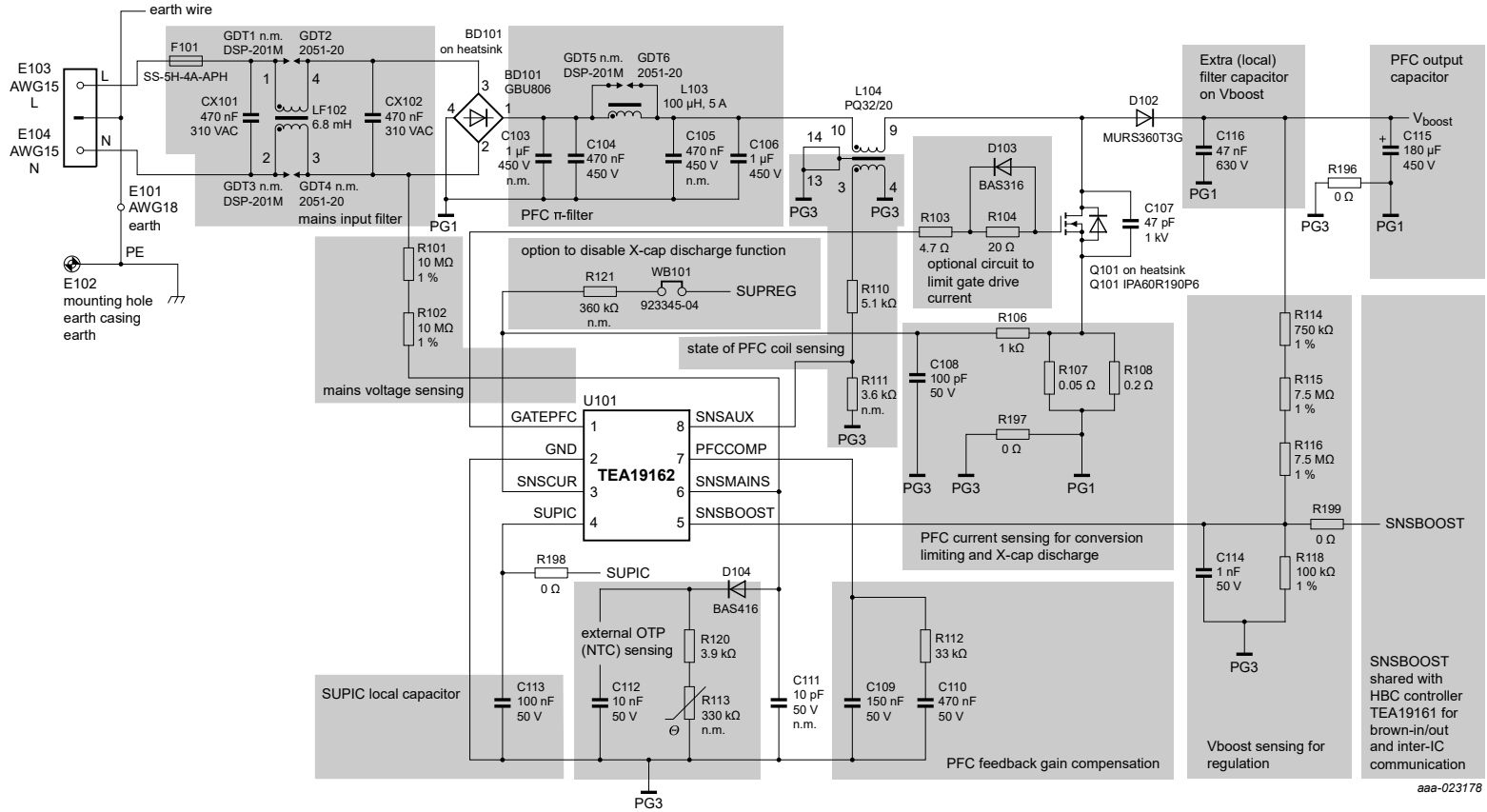


Figure 114. TEA1916 and TEA1995T 240 W power supply with function descriptions

15.2.2 LLC part

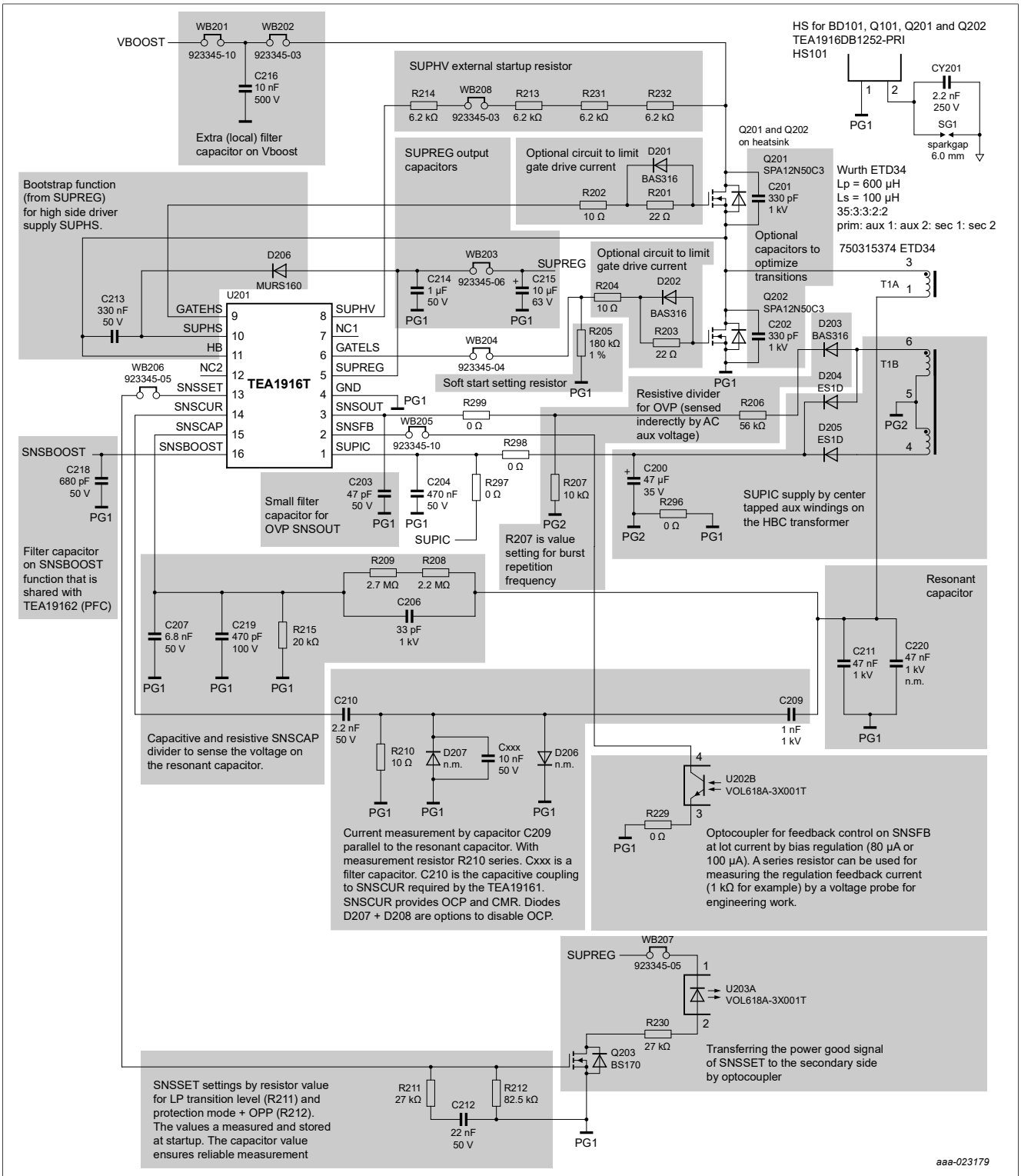


Figure 115. TEA1916 and TEA1995T 240 W power supply (LLC part) with function descriptions

15.2.3 SR part

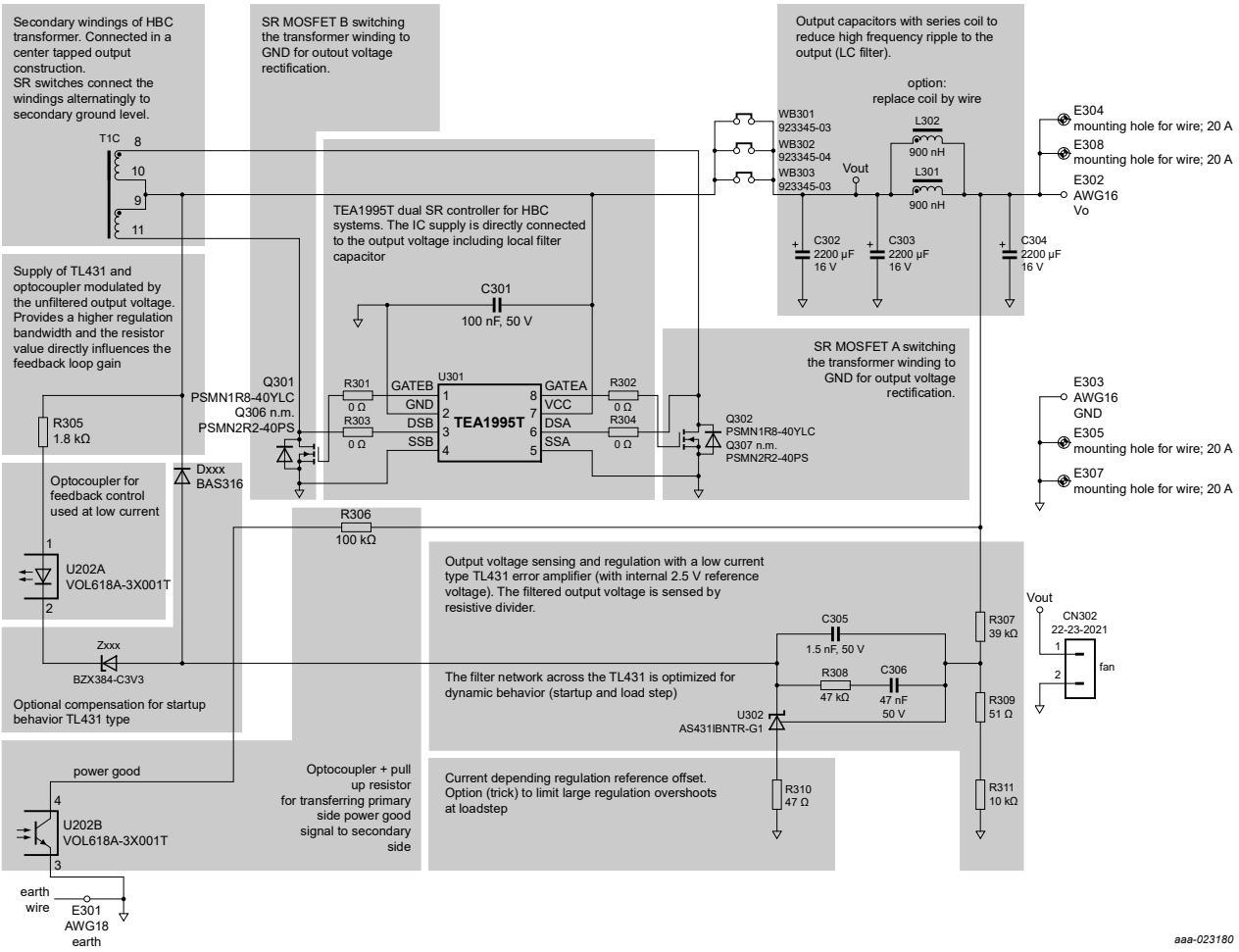


Figure 116. TEA1916 and TEA1995T 240 W power supply (SR part) with function descriptions

15.3 PCB layout

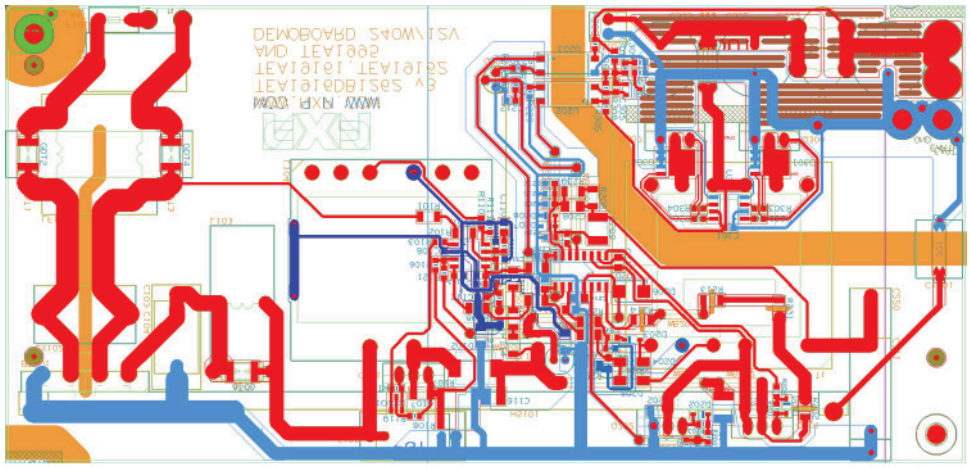


Figure 117. PCB layout

16 Abbreviations

Table 16. Abbreviations

Acronym	Description
ADT	adaptive dead time
BCD	bipolar CMOS DMOS
CMR	capacitive mode regulation
EMC	electromagnetic compatibility
EMI	electromagnetic interference
HB	half-bridge (node, stage, or converter)
HBC	half-bridge converter (or controller)
HP	high-power
HV	high-voltage
IC	integrated circuit
LCD	liquid crystal display
LP	low-power
MHR	mains harmonics reduction
OCP	overcurrent protection
OLP	open-loop protection
OPP	overpower protection
OTP	overtemperature protection
OVP	overvoltage protection
PCB	printed-circuit board
PWM	pulse width mode
QR	quasi-resonant
SCP	short-circuit protection
SOI	silicon-on insulator
SMD	surface-mounted device
SR	Synchronous Rectification
UVP	undervoltage protection

17 References

1	**TEA19161T data sheet**	Digital controller for high-efficiency resonant power supply; 2016, NXP Semiconductors
2	**TEA19162T data sheet**	PFC controller; 2016, NXP Semiconductors
3	**TEA19161CT data sheet**	Digital controller for high-efficiency resonant power supply; 2016, NXP Semiconductors
4	**TEA19162CT data sheet**	PFC controller; 2016, NXP Semiconductors

18 Revision history

Table 17. Revision history

Document ID	Release date	Description
AN11801 v.3.0	12 August 2025	• Third revision
AN11801 v.2.1	07 April 2021	• Update
AN11801 v.2.0	07 January 2019	• Second revision
AN11801 v.1.0	05 May 2017	• Initial revision

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