

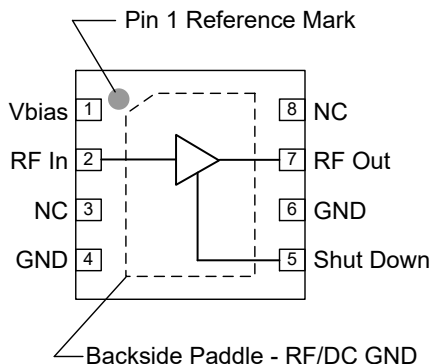
### General Description

The QPL9503 is a flat-gain, high-linearity, ultra-low noise amplifier in a small 2 x 2 mm surface-mount package. The LNA provides a gain flatness of 2 dB (peak-to-peak) over a wide bandwidth from 3 to 6 GHz. At 5.5 GHz, the amplifier typically provides 21.6 dB gain, +35.5 dBm OIP3 at a 56mA bias setting, and 0.95 dB noise figure. The LNA can be biased from a single positive supply ranging from 3.3 to 5 volts. The device is housed in a green/RoHS-compliant industry-standard 2x2 mm package.

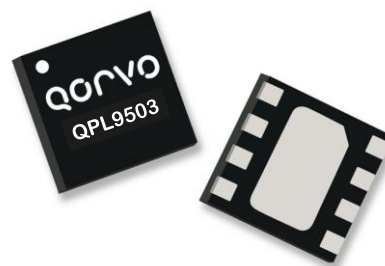
The QPL9503 is internally matched using a high-performance E-pHEMT process and only requires five external components for operation from a single positive supply: an external RF choke and blocking/bypass capacitors and a bias resistor going to pin 1. This LNA integrates a shut-down biasing capability to allow for operation in TDD applications.

The QPL9503 is optimized for linear performance across the 3 to 6 GHz frequency band but can operate down to 600 MHz.

### Functional Block Diagram



Top View



8 Pin 2X2 mm DFN Package

### Product Features

- 0.6-6 GHz Operational Bandwidth
- Ultra-low noise figure, 0.95 dB NF @ 5.5 GHz
- Bias adjustable for linearity optimization
- 35.5 dBm OIP3 at 65mA I<sub>DD</sub>
- Shut-down control pin with +1.8V Logic
- Unconditionally stable
- Integrated shutdown control
- Maintains OFF state with high power input
- +3V to +5V supply; no negative voltage required

### Applications

- 4.5G, 5G Massive MIMO
- Repeaters / DAS
- Mobile Infrastructure
- LTE-U / LAA
- L-band, S-band, C-band radios
- General Purpose Wireless
- TDD or FDD systems

### Ordering Information

| Part No.      | Description                   |
|---------------|-------------------------------|
| QPL9503TR7    | 2500 pcs on 7" reel           |
| QPL9503EVB-01 | 5-6GHz Tuned Evaluation Board |

## Absolute Maximum Ratings

| Parameter                         | Rating        |
|-----------------------------------|---------------|
| Storage Temperature               | -65 to +150°C |
| T <sub>CASE</sub> , Operational   | -40 to +125°C |
| Supply Voltage (V <sub>DD</sub> ) | +7 V          |
| RF Input Power, CW, 50Ω, T=25°C   | +30 dBm       |
| RF Input Power, WCDMA, 10dB PAR   | +27 dBm       |
| RF Input Power, CW, OFF State     | +30 dBm       |

Operation of this device outside the parameter ranges given above may cause permanent damage.

## Recommended Operating Conditions

| Parameter                          | Min | Typ | Max  | Units |
|------------------------------------|-----|-----|------|-------|
| Supply Voltage (V <sub>DD</sub> )  | 3.3 | 5.0 | 5.25 | V     |
| T <sub>CASE</sub>                  | -40 |     | +105 | °C    |
| Tj for >10 <sup>6</sup> hours MTTF |     |     | +190 | °C    |

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

## Electrical Specifications

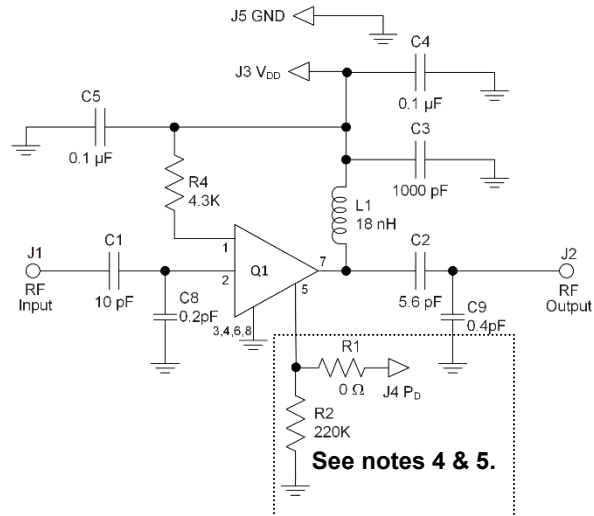
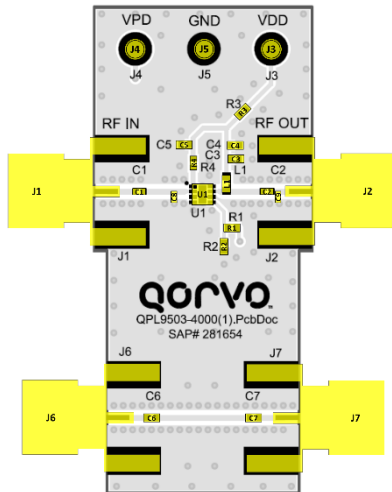
Test conditions unless otherwise noted: V<sub>DD</sub> = +5V, Temp = +25°C, 50 Ω system.

| Parameter                           | Conditions                                 | Min  | Typ   | Max             | Units |
|-------------------------------------|--|------|-------|-----------------|-------|
| Operational Frequency Range         |  | 600  |       | 6000            | MHz   |
| Test Frequency                      |  |      | 5500  |                 | MHz   |
| Gain                                |  | 18.5 | 21.6  | 22.5            | dB    |
| Input Return Loss                   |  |      | 10    |                 | dB    |
| Output Return Loss                  |  |      | 9     |                 | dB    |
| Noise Figure <sup>(1)</sup>         |  |      | 0.9   | 1.3             | dB    |
| Output P1dB                         |  |      | +19   |                 | dBm   |
| Output IP3                          | P <sub>out</sub> = +2 dBm/tone, Δf = 1 MHz | +30  | +35.5 |                 | dBm   |
| Voltage, Shut Down (pin 5)          | On state                                   | 0    |       | 0.63            | V     |
|                                     | Off state (Power down)                     | 1.17 |       | V <sub>DD</sub> | V     |
| Current, I <sub>DD</sub>            | On state                                   | 35   | 56    | 90              | mA    |
|                                     | Off state (Power down)                     |      | 3     |                 | mA    |
| Current, I <sub>SD</sub> (pin 5)    | V <sub>PD</sub> ≥ 1.17 V                   |      | 140   |                 | μA    |
| Switching Time                      | LNA ON to OFF                              |      | 20    |                 | ns    |
|                                     | LNA OFF to ON                              |      | 400   |                 | ns    |
| Thermal Resistance, θ <sub>jc</sub> | channel to case                            |      | 48    |                 | °C/W  |

Note:

1. Input trace loss deducted.

### QPL9503 Evaluation Board



#### Notes:

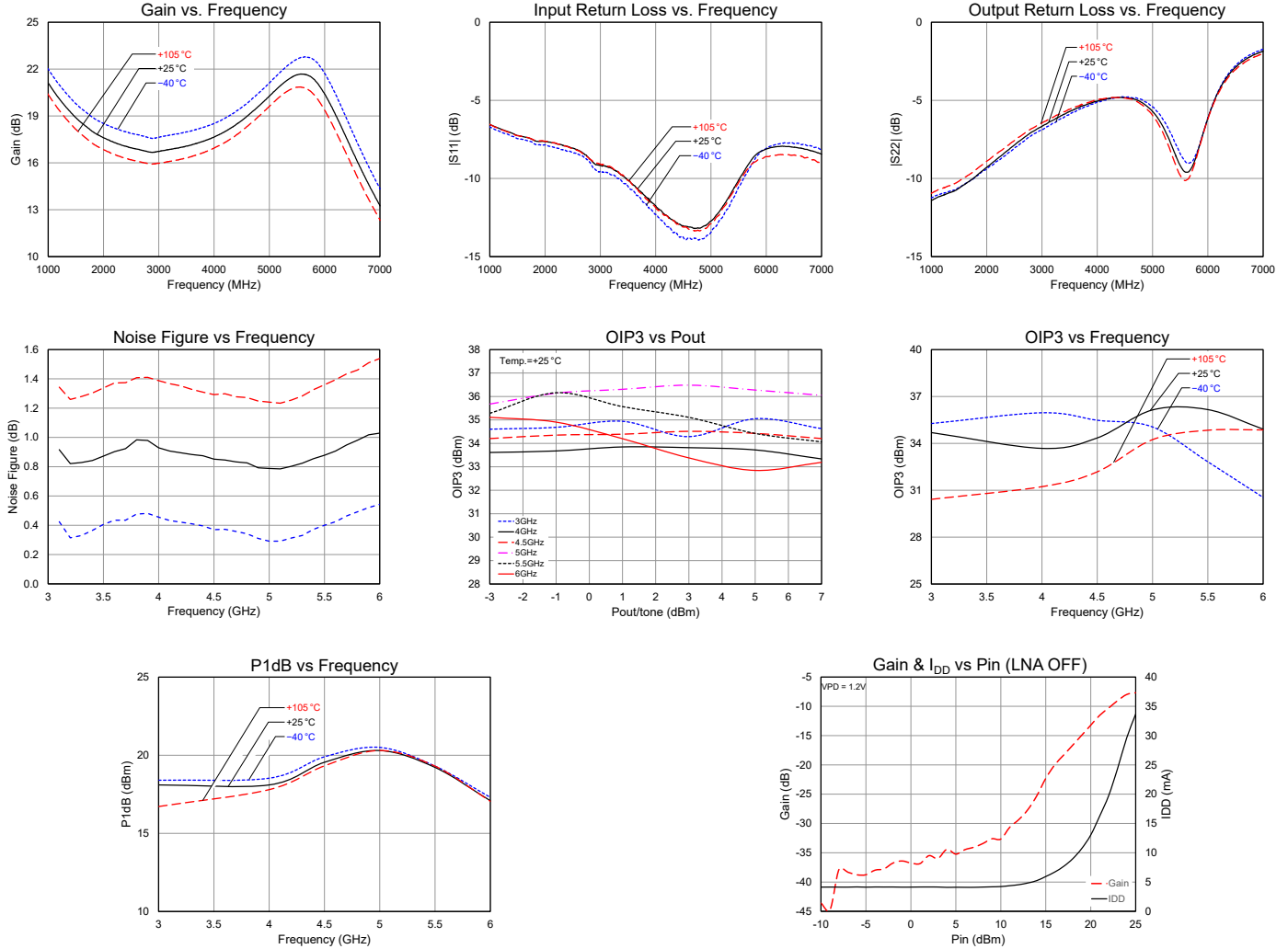
1. See Evaluation Board PCB Information section for material and stack-up.
2. R3 (0  $\Omega$  jumper) is not shown on the schematic and may be replaced with copper trace in the target application layout.
3. All components are of 0402 size unless stated on the schematic.
4. For TDD Applications: R1 = 0 $\Omega$  & R2 = 220K
5. For FDD Applications: R2 = 220K, or 0 $\Omega$ . R1 = DNP/Omitted
6. There is a through line on the evaluation board. It can be used for trace loss deduction.
7. R4 sets the  $I_{DD}$  current. Can be changed for the desired bias current.

### Bill of Material – QPL9503 Evaluation Board

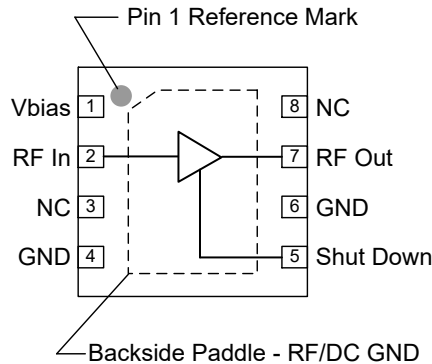
| Reference Des. | Value       | Description                                | Manuf.    | Part Number        |
|----------------|-------------|--|-----------|--------------------|
| -              | -           | Printed Circuit Board                      | Qorvo     |                    |
| U1             | -           | LNA, Ultra Low Noise, Flat Gain            | Qorvo     | QPL9503            |
| C1             | 10 pF       | CAP, 10 pF, 1%, 50V, Hi-Q, 0402            | Murata    | GJM1555C1H100FB01D |
| C2             | 5.6 pF      | CAP, 5.6 pF, $\pm 0.1$ pF, 50V, C0G, 0402  | Murata    | GRM1555C1H5R6BA01D |
| C3             | 1000 pF     | CAP, 1000 pF, 10%, 50V, X7R, 0402          | Murata    | GRM1555C1H102KA01D |
| C4, C5         | 0.1 $\mu$ F | CAP, 0.1 $\mu$ F, 10%, 10V, X5R, 0402      | various   | -                  |
| C6, C7         | 27 pF       | CAP, 27 pF, 5%, 50V, NPO, 0402             | Murata    | GRM1555C1H270JA01D |
| C8             | 0.2 pF      | CAP, 0.2 pF, $\pm 0.1$ pF, 50V, Hi-Q, 0402 | Murata    | GJM1555C1HR20BB01D |
| C9             | 0.4 pF      | CAP, 0.4 pF, $\pm 0.1$ pF, 50V, Hi-Q, 0402 | Murata    | GJM1555C1HR40BB01D |
| L1             | 18 nH       | IND, 18 nH, 2%, WW, 0402                   | Coilcraft | 0402CS-18NXGRW     |
| R1, R3         | 0 $\Omega$  | RES, 0 $\Omega$ , 1/16W, 0402              | various   | -                  |
| R2             | 220 K       | RES, 220 K, 5%, 1/16W, 0402                | various   | -                  |
| R4             | 4.3 K       | RES, 4.3 K, 5%, 1/16W, 0402                | various   | -                  |

## Performance Plots – QPL9503 Evaluation Board

Test conditions unless otherwise noted:  $V_{DD}=+5\text{ V}$ ,  $I_{DD}=65\text{ mA}$ ,  $\text{Temp}=+25^\circ\text{C}$ . Noise figure data has input trace loss deducted.



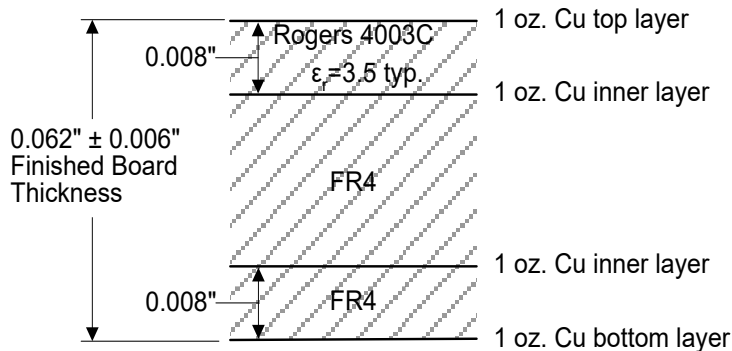
## Pin Configuration and Description



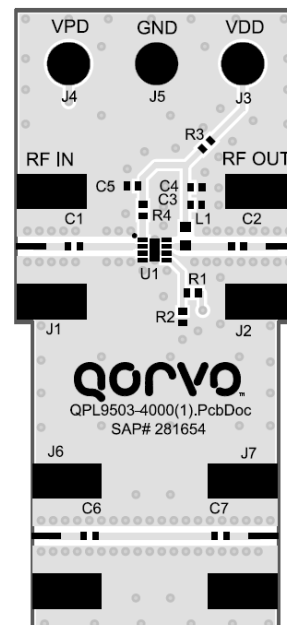
| Pin No.               | Label     | Description   |
|-----------------------|-----------|---|
| 1                     | Vbias     | Bias voltage input, Sets the $I_{DD}$ bias current for the device.  |
| 2                     | RF In     | RF Input pin. A DC Block is required.   |
| 5                     | Shut Down | Control voltage input, A voltage $\geq 1.17V$ turns off the device. If the pin is pulled to ground or driven with a voltage $\leq 0.63V$ , then the device will operate under LNA ON state. |
| 7                     | RF Out    | RF Output and DC voltage input through a RF choke/inductor for operation.   |
| 3, 8                  | NC        | No internal electrical connection. Provide grounded land pads for PCB mounting integrity.   |
| 4, 6, Backside Paddle | GND       | RF/DC ground. Use recommended ground via holes to minimize inductance and thermal resistance.   |

## Evaluation Board PCB Information

Qorvo PCB 281645 Material and Stack-up

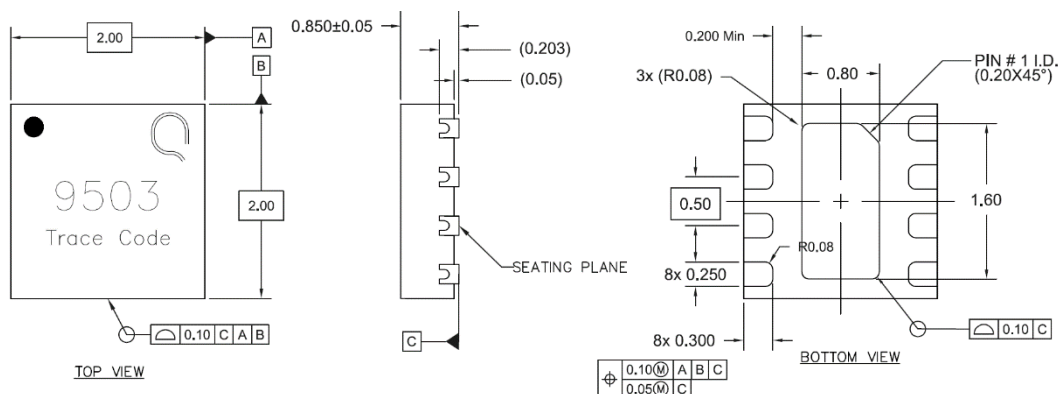


50  $\Omega$  line dimensions: width = 0.0182", spacing = 0.020"



## Package Marking and Dimensions

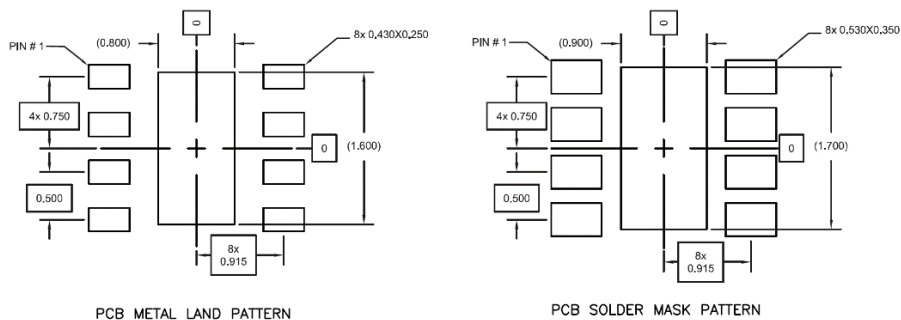
Marking: • – Pin 1 Marker  
9503 – Part Number  
Trace Code – Assigned by Sub-Contractor



### Notes:

1. All dimensions are in millimeters. Angles are in degrees.
2. Except where noted, this part outline conforms to JEDEC standard MO-220, Issue E (Variation VGGC) for thermally enhanced plastic very thin fine pitch quad flat no lead package (QFN).
3. Dimension and tolerance formats conform to ASME Y14.4M-1994.
4. The terminal #1 identifier and terminal numbering conform to JESD 95-1 SPP-012.

## PCB Mounting Pattern



### Notes:

1. All dimensions are in millimeters. Angles are in degrees.
2. Use 1 oz. copper minimum for top and bottom layer metal.
3. Minimum 3 via holes are required under the backside paddle of this device for proper RF/DC grounding and thermal dissipation. We recommend a 0.35mm (#80/.0135") diameter bit for drilling via holes and a final plated thru diameter of 0.25 mm (0.010").
4. Ensure good package backside paddle solder attach for reliable operation and best electrical performance.

0.30 ±0.05

R 0.30 MAX.

K<sub>0</sub>

SECTION A - A

2.00 ±0.05 SEE NOTE 2

4.00 SEE NOTE 1

4.00

Ø 1.00 MIN

Ø 1.5 +0.1/-0.0

8.0 +0.3/-0.1

1.75 ±0.10

3.50 ±0.05 SEE NOTE 2

A

A

B<sub>0</sub>

A<sub>0</sub>

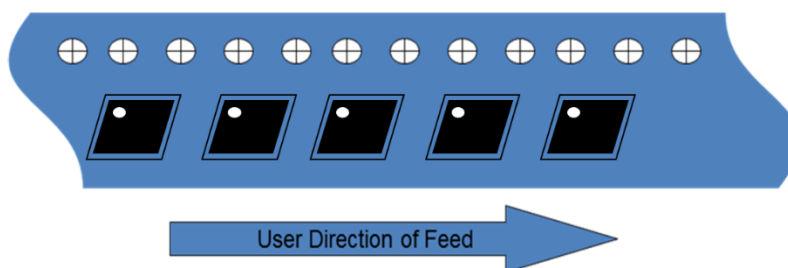
R 0.3 TYP.

NOTES:

1. 10 SPROCKET HOLE PITCH CUMULATIVE TOLERANCE ±0.2
2. POCKET POSITION RELATIVE TO SPROCKET HOLE MEASURED AS TRUE POSITION OF POCKET, NOT POCKET HOLE
3. A<sub>0</sub> AND B<sub>0</sub> ARE CALCULATED ON A PLANE AT A DISTANCE "R" ABOVE THE BOTTOM OF THE POCKET.

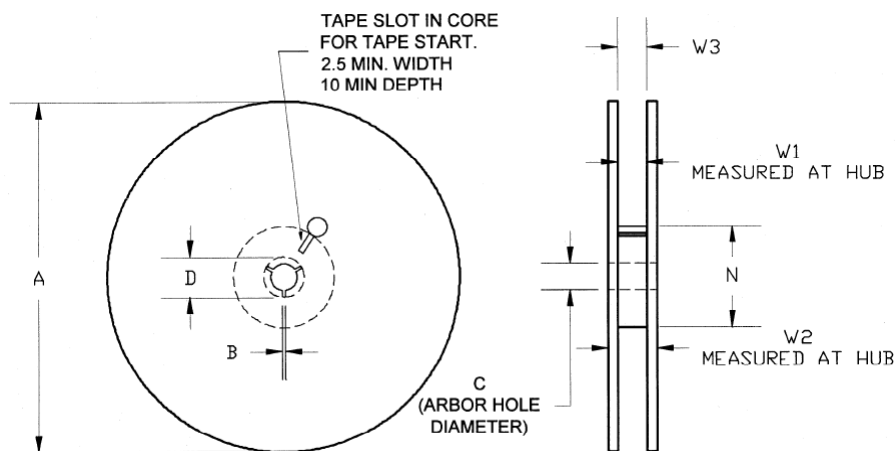
|                  |      |
|------------------|------|
| A <sub>0</sub> = | 2.30 |
| B <sub>0</sub> = | 2.30 |
| K <sub>0</sub> = | 1.30 |

| Feature             | Measure                                  | Symbol | Size (in) | Size (mm) |
|---------------------|--|--------|-----------|-----------|
| Cavity              | Length                                   | A0     | 0.091     | 2.30      |
|                     | Width                                    | B0     | 0.091     | 2.30      |
|                     | Depth                                    | K0     | 0.039     | 1.30      |
|                     | Pitch                                    | P1     | 0.157     | 4.00      |
| Centerline Distance | Cavity to Perforation - Length Direction | P2     | 0.079     | 2.00      |
|                     | Cavity to Perforation - Width Direction  | F      | 0.138     | 3.50      |
| Cover Tape          | Width (Reference Only)                   | C      | 0.213     | 5.40      |
| Carrier Tape        | Width                                    | W      | 0.315     | 8.00      |



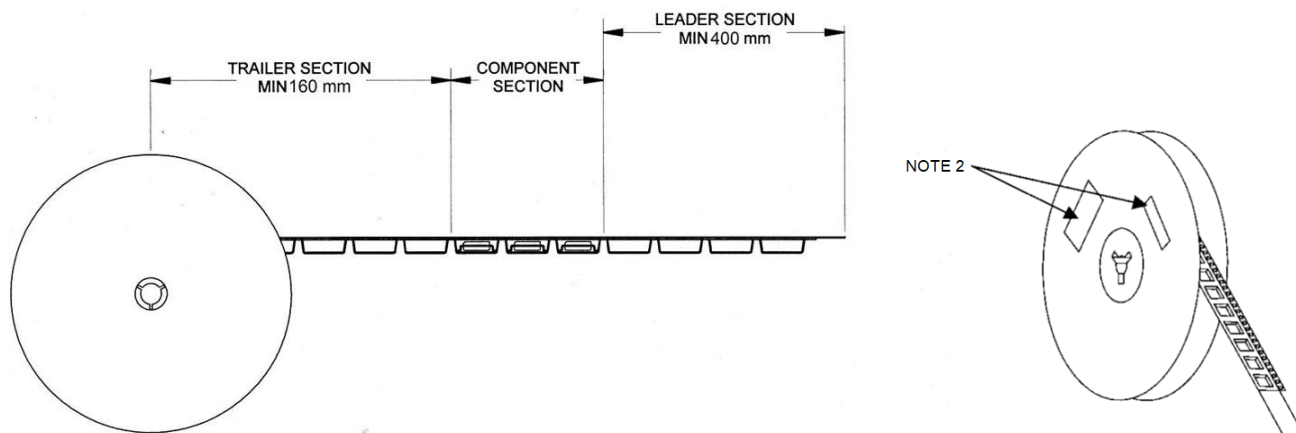
## Tape and Reel Information – Reel Dimensions

Standard T/R size = 2,500 pieces on a 7" reel.



| Feature | Measure              | Symbol | Size (in) | Size (mm) |
|---------|----------------------|--------|-----------|-----------|
| Flange  | Diameter             | A      | 6.969     | 177.00    |
|         | Thickness            | W2     | 0.559     | 14.20     |
|         | Space Between Flange | W1     | 0.346     | 8.80      |
| Hub     | Outer Diameter       | N      | 2.283     | 58.00     |
|         | Arbor Hole Diameter  | C      | 0.512     | 13.00     |
|         | Key Slit Width       | B      | 0.079     | 2.00      |
|         | Key Slit Diameter    | D      | 0.787     | 20.00     |

## Tape and Reel Information – Tape Length and Label Placement



### Notes:

1. Empty part cavities at the trailing and leading ends are sealed with cover tape. See EIA 481-1-A.
2. Labels are placed on the flange opposite the sprockets in the carrier tape.



## Handling Precautions

| Parameter                        | Rating   | Standard                 |
|----------------------------------|----------|--------------------------|
| ESD – Human Body Model (HBM)     | Class 1C | ESDA / JEDEC JS-001-2014 |
| ESD – Charged Device Model (CDM) | Class C3 | ESDA / JEDEC JS-002-2014 |
| MSL – Moisture Sensitivity Level | Level 1  | IPC/JEDEC J-STD-020      |



Caution!  
ESD-Sensitive Device

## Solderability

Compatible with lead-free (260°C max. reflow temp.) soldering process.

Solder profiles available upon request.

Contact plating: NiPdAu (*Thickness: Ni 0.508 ~ 1.524  $\mu\text{m}$ ; Pd 0.023 ~ 0.1016  $\mu\text{m}$ ; Au 0.00254 ~ 0.01016  $\mu\text{m}$* )

## RoHS Compliance

This part is compliant with 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment) as amended by Directive 2015/863/EU.

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A (C<sub>15</sub>H<sub>12</sub>Br<sub>4</sub>O<sub>2</sub>) Free
- PFOS Free
- SVHC Free



## Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

**Web:** [www.qorvo.com](http://www.qorvo.com)

**Tel:** 1-844-890-8163

**Email:** [customer.support@qorvo.com](mailto:customer.support@qorvo.com)

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