QPA4536

24.2 – 26.5 GHz K-Band Power Amplifier

Product Overview

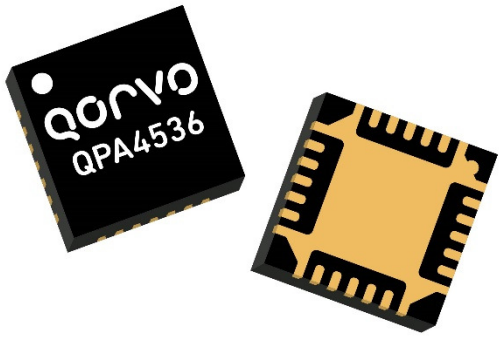
Qorvo QPA4536 is a K-Band Power Amplifier with integrated power detector. The QPA4536 operates from 24.2 – 26.5 GHz and is designed using Qorvo's power pHEMT production process.

The QPA4536 typically provides 31.5 dBm output power at 1dB gain compression, and 33 dBm of saturated output power. The small signal gain is 18 dB, and Third Order Intercept is 43 dBm at 23 dBm SCL.

To simplify system integration, the QPA4536 is fully matched to 50 ohms with integrated DC clocking caps on both I/O ports.

The QPA4536 is available in a low-cost, surface mount 28 lead 5x5 mm QFN package. It is ideally suited for supporting communications and radar applications in both commercial and military markets.

Lead-free and RoHS compliant

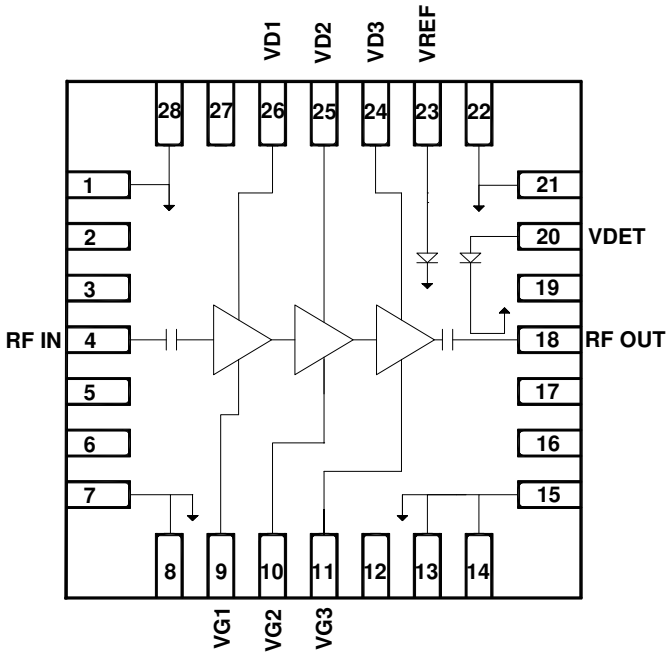


Key Features

- Frequency Range: 24.2 – 26.5 GHz
- P_{1dB} (P_{IN} ≈ 14 dBm): 31.5 dBm
- P_{SAT} (P_{IN} = 18 dBm): 32.5 dBm
- Small Signal Gain: 18 dB
- TOI (P_{OUT}/Tone = 23 dBm): 43 dBm
- Integrated Power Detector
- Bias: CW, V_D = 6 V, I_{DQ} = 1430 mA, V_G = -0.6 V typ.
- Package Dimensions: 5.0 x 5.0 x 1.3 mm

Performance is typical across frequency. Please reference electrical specification table and data plots for more details.

Functional Block Diagram



Applications

- Satellite Communications
- Point-to-Point Radio

Ordering Information

Part No.	Description
QPA4536TR7	250 pieces on a 7" reel (standard)
QPA4536EVB	Evaluation Board

Absolute Maximum Ratings

Parameter	Value / Rang
Drain to Gate Voltage, V_D - V_G	10 V
Drain Voltage (V_D)	6.5 V
Gate Voltage Range (V_G)	-3 V to 0 V
Drain Current (I_D)	3 A
Gate Current (I_G)	-14 to 110mA
Power Dissipation (P_{DISS}), T_{BASE} = 85 °C	14 W
Input Power (P_{IN}), 50 Ω, CW, V_D = 6 V, I_{DQ} = 1430 mA, T_{BASE} = 25 °C	25 dBm
Channel Temperature, T_{CH}	200 ºC
Mounting Temperature (30 seconds)	260 ºC
Storage Temperature	-55 to +150 ºC

Operation of this device outside the parameter ranges given above may cause permanent damage. These are stress ratings only, and functional operation of the device at these conditions is not implied.

Recommended Operating Conditions

Parameter	Min	Typ.	Max	Units
Drain Voltage (V_D)		6		V
Drain Current, Quiescent (I_D)		1430		mA
Drain Current, RF (I_{D_Drive})	See plot page 5, 6, 9			mA
Gate Voltage Typical Range (V_G)	–0.3 to -0.9			V
Gate Current, RF (I_{G_Drive})	See plot page 5, 6			mA
Input Power (P_{IN} @ P_{1dB})		14 (1)		
Operating Temp. Range T_{BASE} (2)	–40		+85	ºC

1. Limited by thermal; P_{IN} > 14 dBm (where P_{SAT} = 18 dBm P_{IN}) would degrade Median Lifetime, see p. 17
2. T_{BASE} is back side of QPA4536

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications

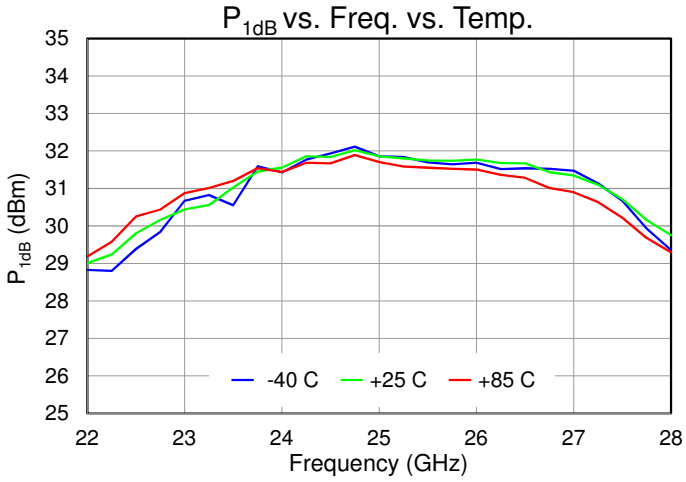
Parameter	Conditions (1) (2)	Freq. (GHz)	Min	Typ.	Max	Units
Operational Frequency Range			24.2		26.5	GHz
Output Power at 1dB Gain Compression, P_{1dB}	P_{IN} ≈ 14 dBm			31.5		dBm
Output Power at Saturation, P_{SAT} (3)	P_{IN} = 18 dBm (≈ P_{5dB})	24.2	32	33.0		dBm
		25.4	31	32.5		
		26.5	30	32.0		
Power Added Efficiency, PAE	P_{IN} = 14 dBm			12		%
Output TOI	P_{OUT}/Tone = 23 dBm, ΔF = 10 MHz			43		dBm
Small Signal Gain, S21	P_{IN} = -20 dBm	24.2	18	19.5		dB
		25.4	16	18		
		26.5	14	16		
Input/Output Return Loss, IRL/ORL	P_{IN} = -20 dBm			7		dB
P_{1dB} Temperature Coefficient	T_{DIFF} = -40 ºC to 85 ºC			-0.005		dBm/ºC
S21 Temperature Coefficient	T_{DIFF} = -40 ºC to 85 ºC			-0.02		dB/ºC

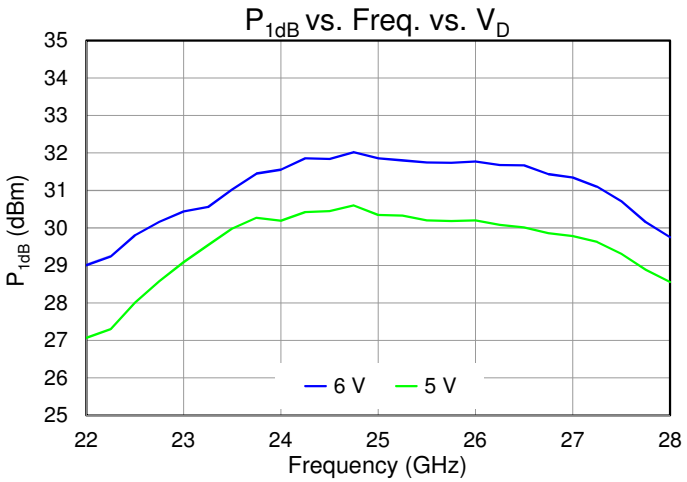
Notes:

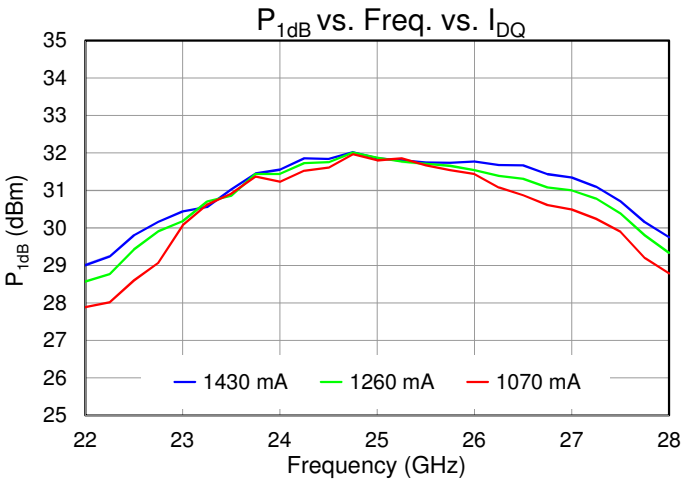
1. Test conditions unless otherwise noted: CW, V_D = 6 V, I_D = 1430 mA, V_G = -0.6 V +/- typical range, T_{BASE} = 25ºC, Z_0 = 50 Ω
2. T_{BASE} is back side of QPA4536
3. Limited by thermal; operating at P_{SAT} would degrade Median Lifetime (T_M) for T_{BASE} = 85^{0}C; see page 17. Recommended reducing T_{BASE} to improve T_M.

Performance Plots – Large Signal

Test conditions, unless otherwise noted: CW, V_D = 6 V, I_{DQ} = 1430 mA, T_{BASE} = +25 ºC (T_{BASE} is backside of QPA4536)







Performance Plots – Large Signal

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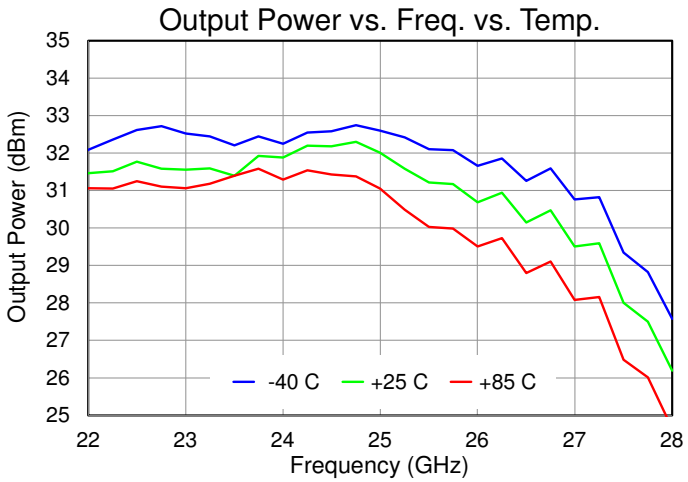

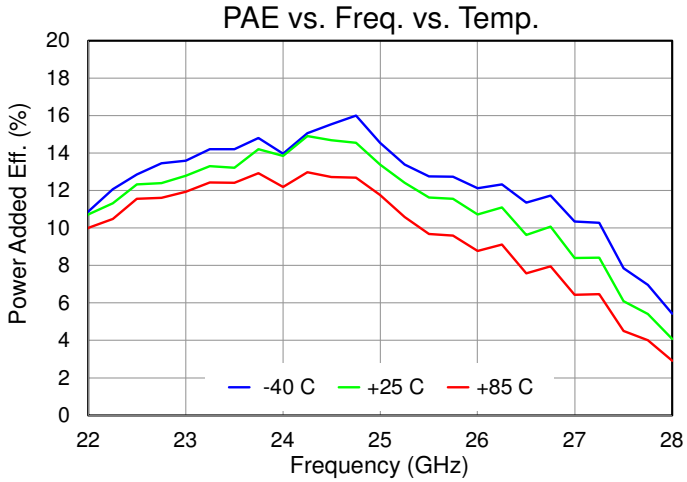

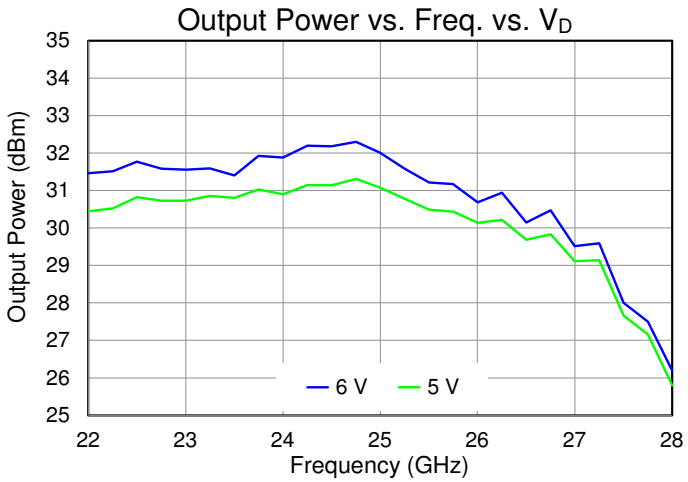

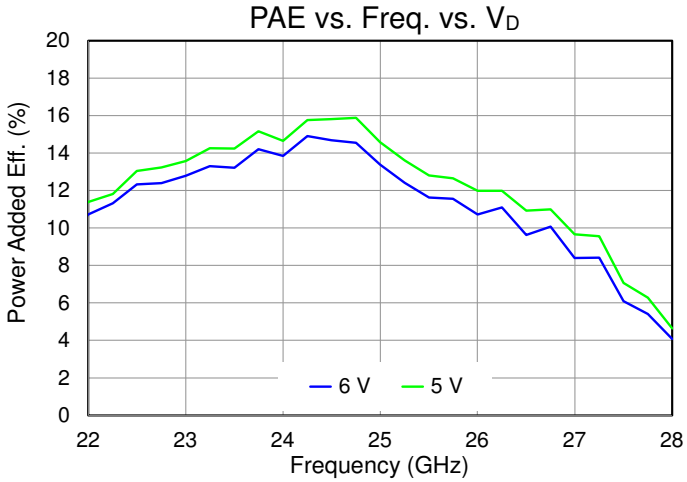

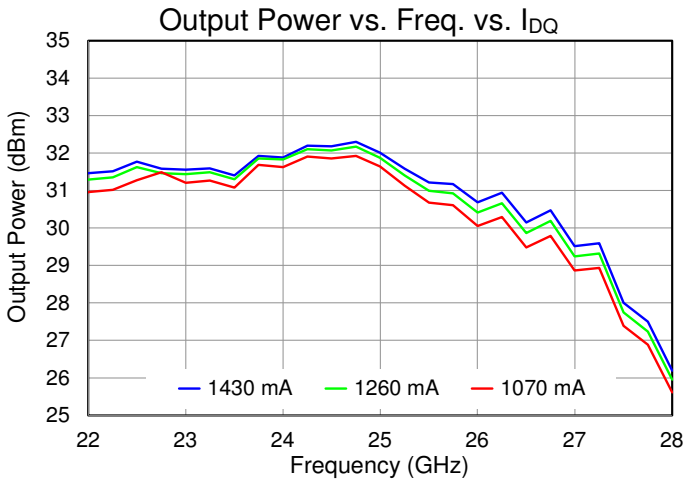

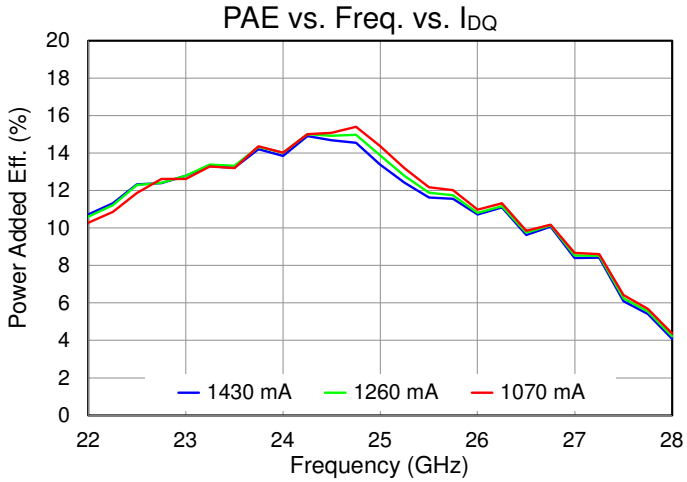

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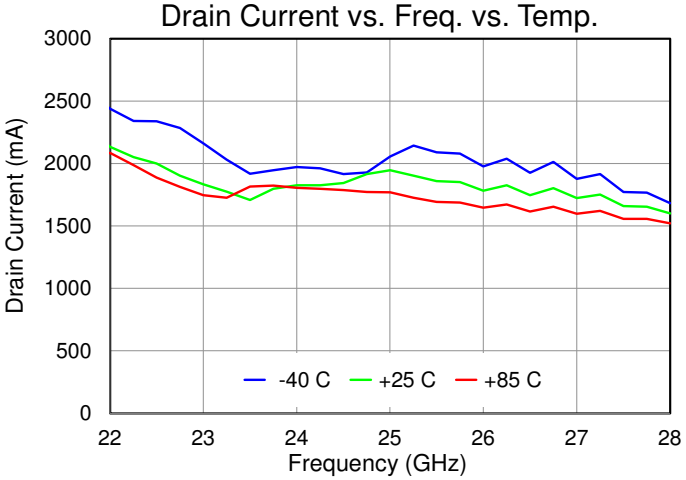
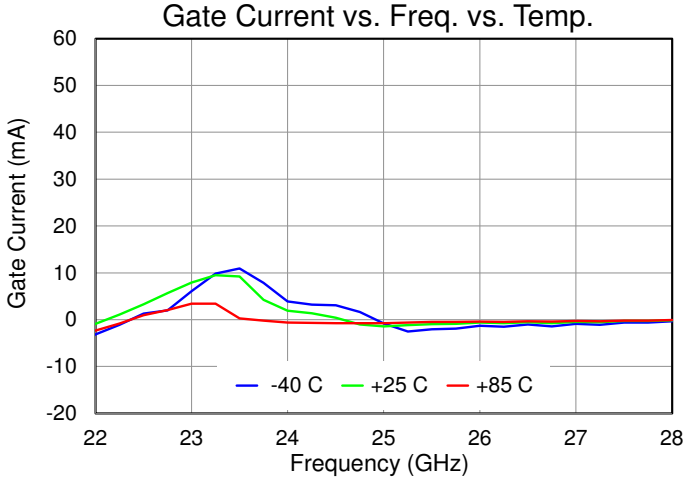
Test conditions, unless otherwise noted: CW, V_D = 6 V, I_{DQ} = 1430 mA, P_{IN} = 14 dBm, T_{BASE} = +25 ºC (T_{BASE} is backside of QPA4536)

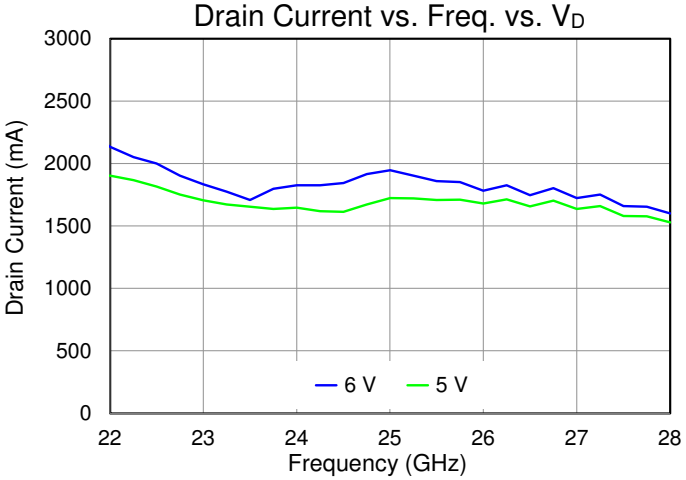
Drain Current vs. Freq. vs. Temp.



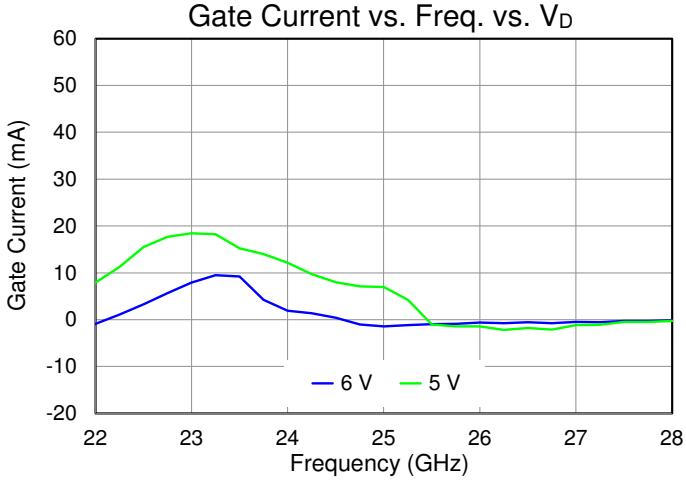
Gate Current vs. Freq. vs. Temp.



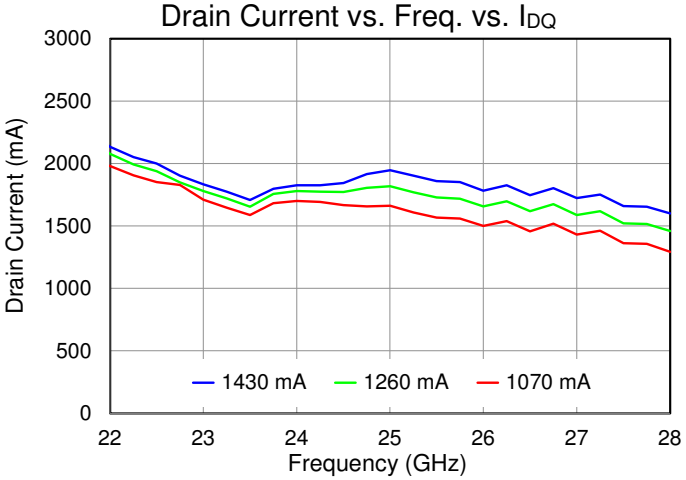
Drain Current vs. Freq. vs. V_D



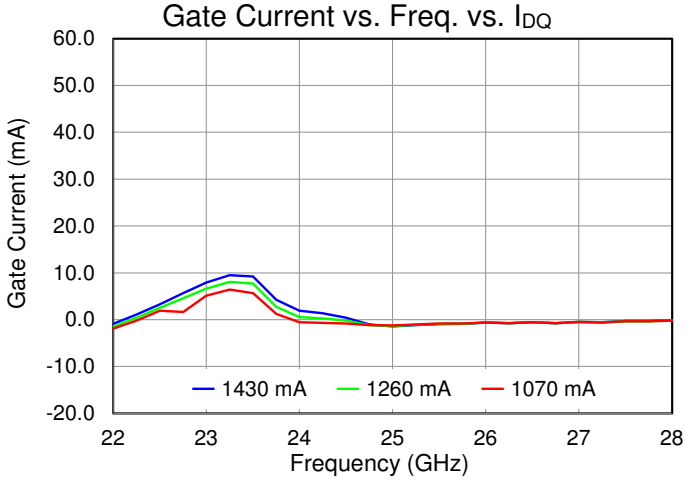
Gate Current vs. Freq. vs. V_D



Drain Current vs. Freq. vs. I_{DQ}



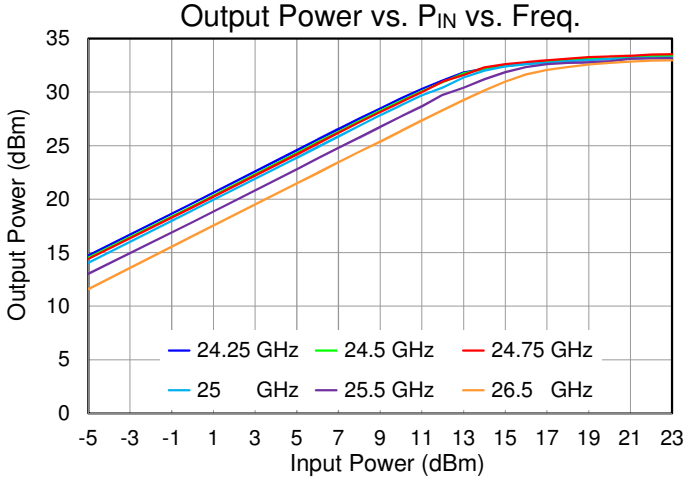
Gate Current vs. Freq. vs. I_{DQ}



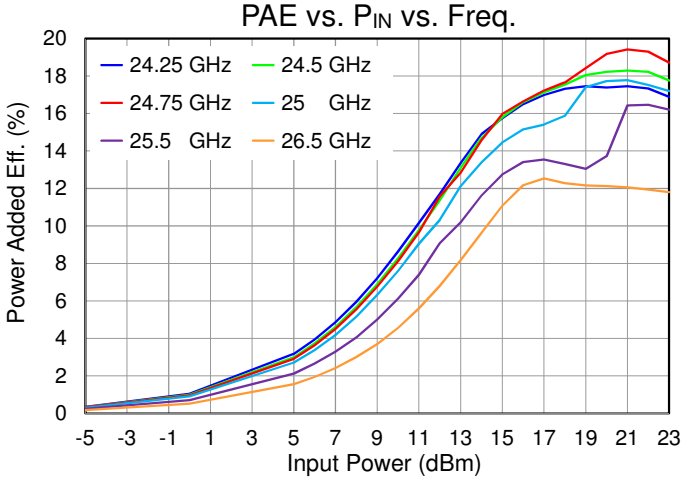
Performance Plots – Large Signal

Test conditions, unless otherwise noted: CW, V_D = 6 V, I_{DQ} = 1430 mA, T_{BASE} = +25 °C (T_{BASE} is backside of QPA4536)

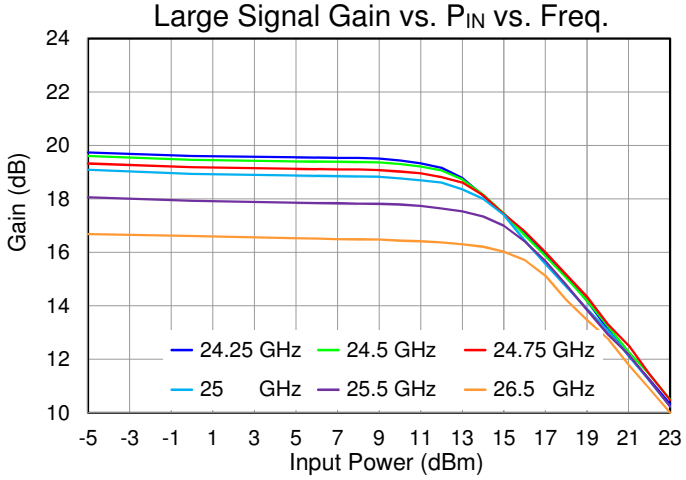
Output Power vs. P_{IN} vs. Freq.



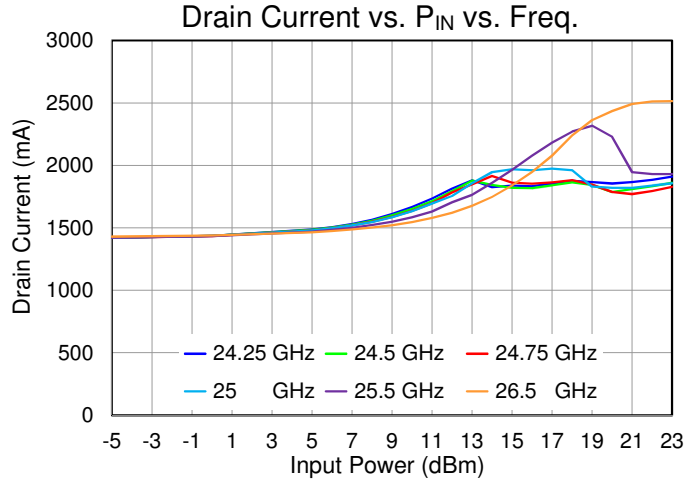
PAE vs. P_{IN} vs. Freq.



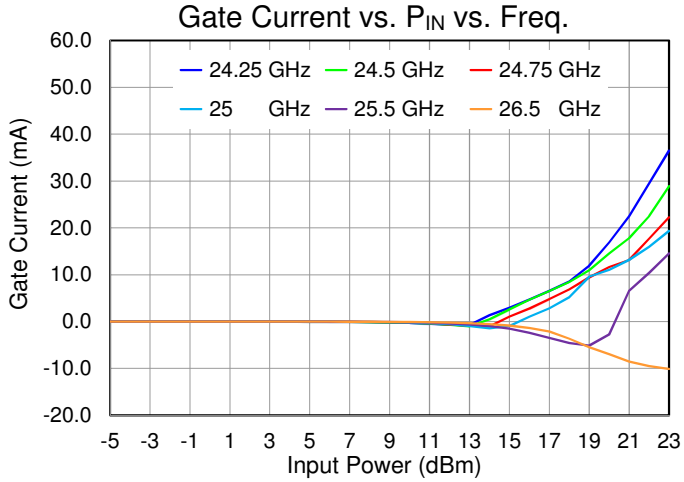
Large Signal Gain vs. P_{IN} vs. Freq.



Drain Current vs. P_{IN} vs. Freq.



Gate Current vs. P_{IN} vs. Freq.



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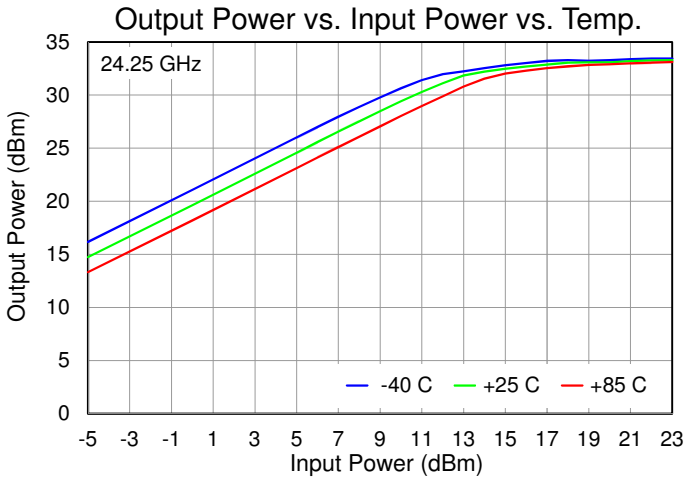

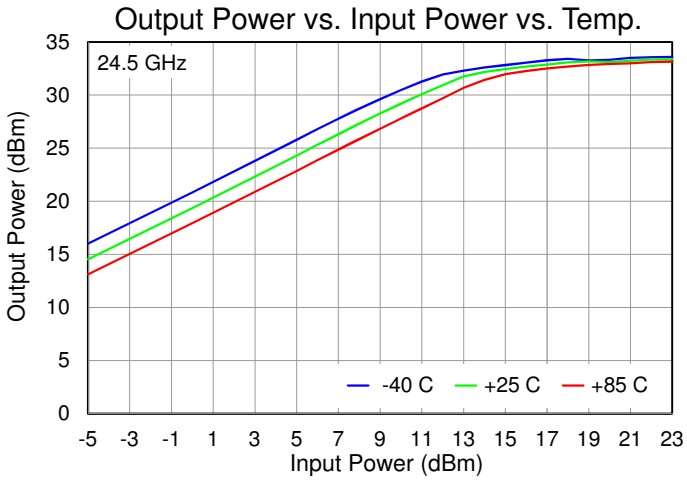

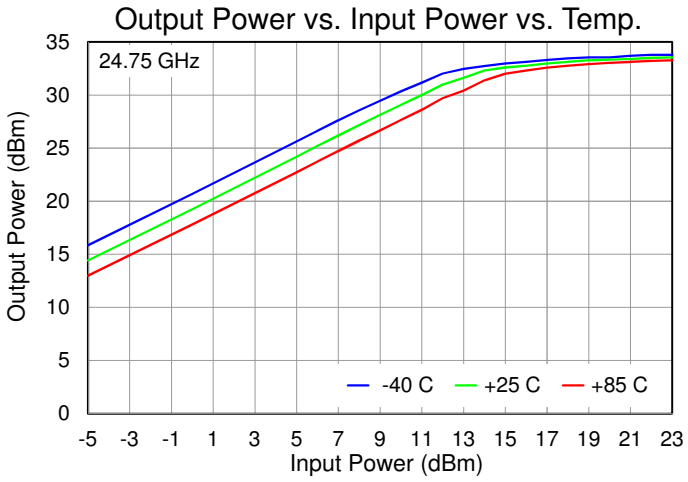

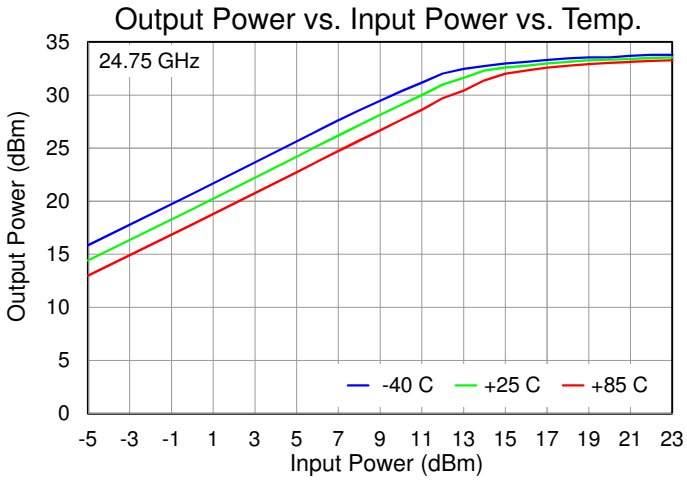

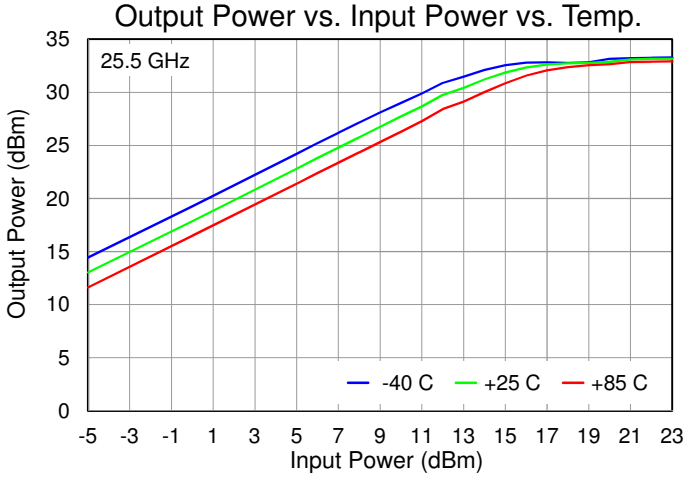

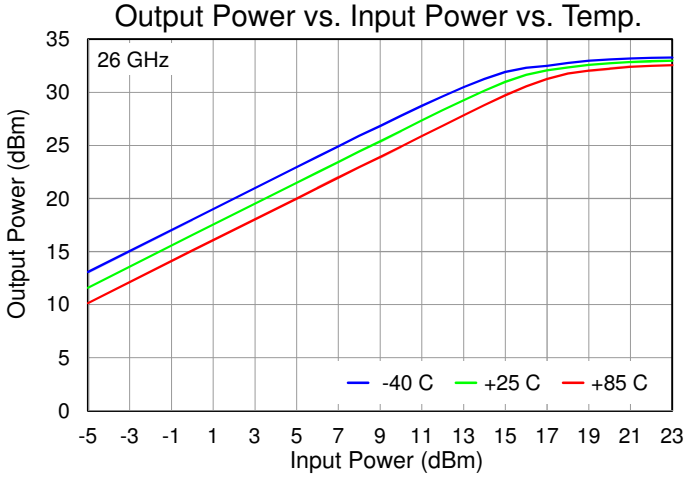

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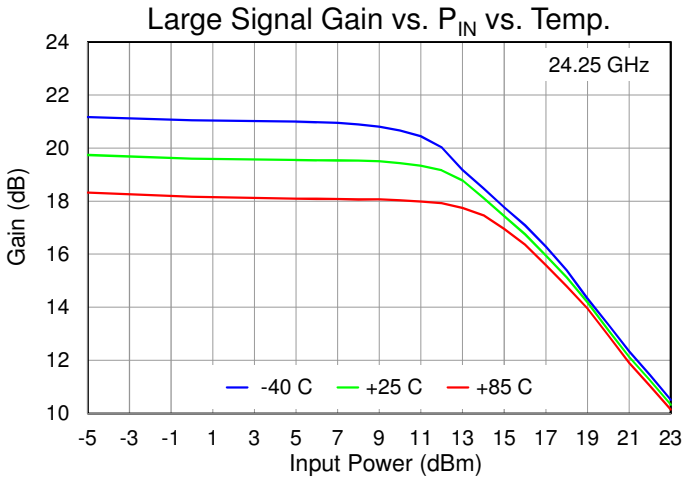

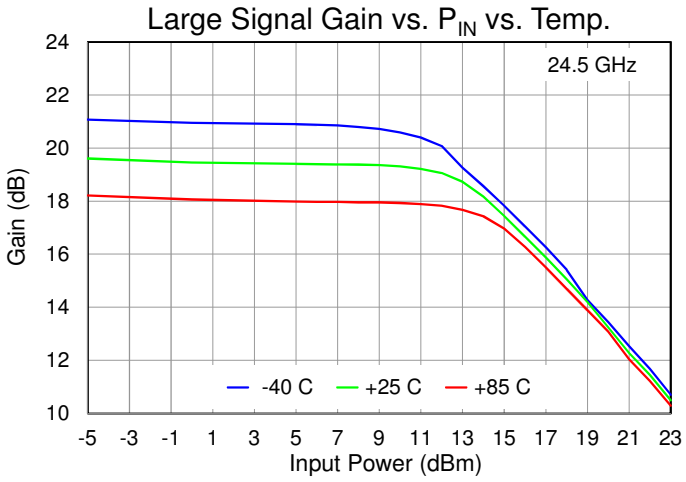

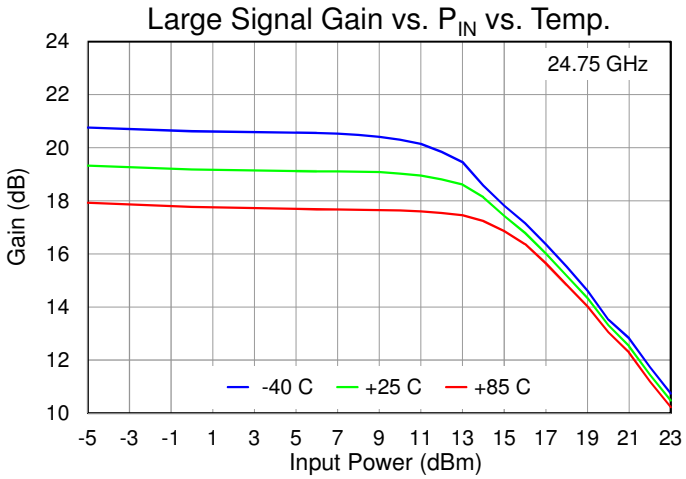

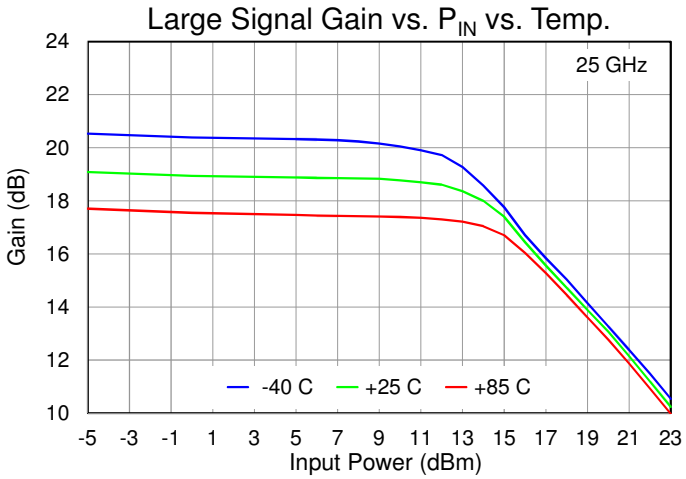

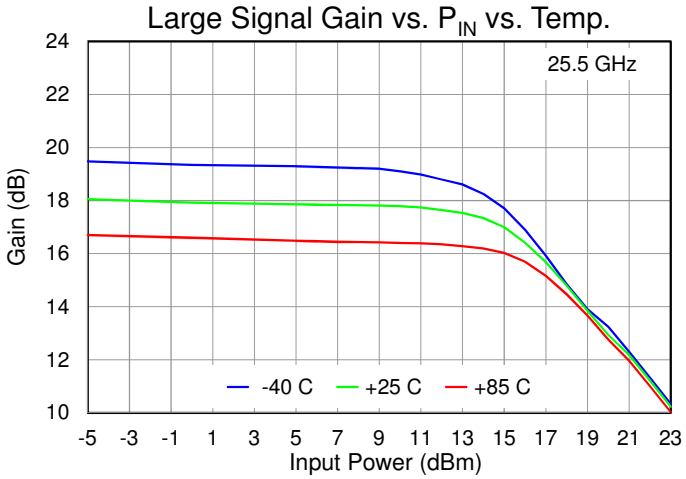

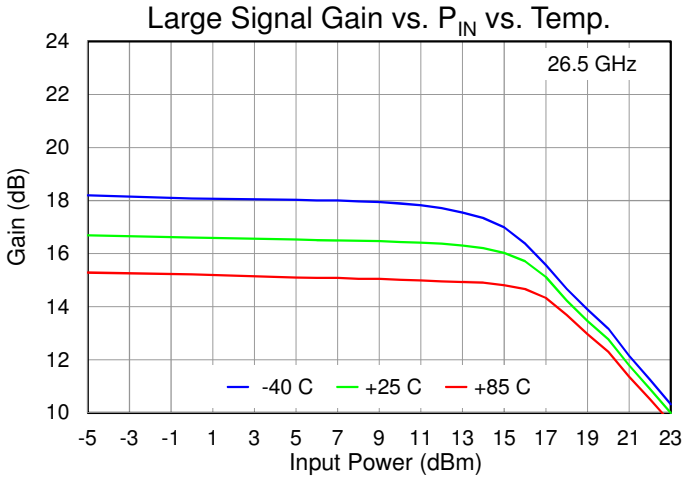

Performance Plots – Large Signal

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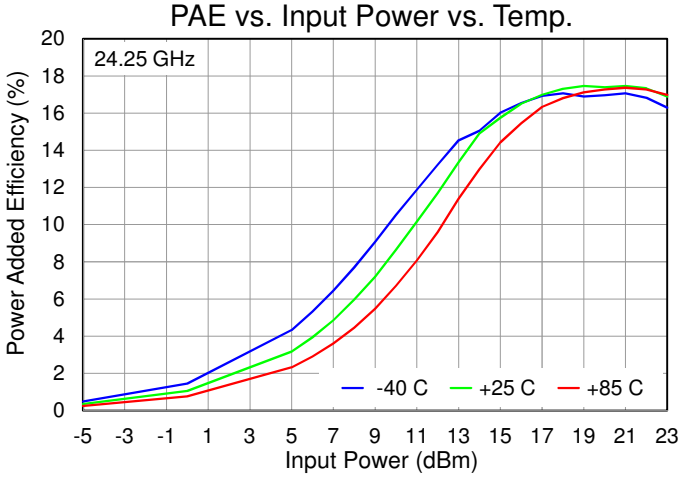
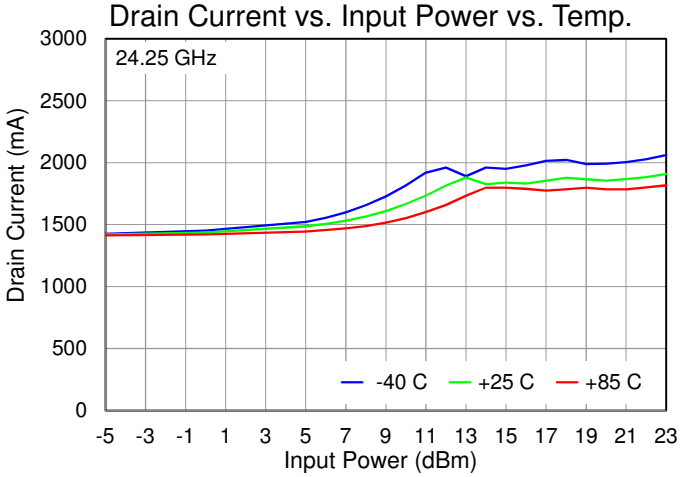
PAE vs. Input Power vs. Temp.



Drain Current vs. Input Power vs. Temp.



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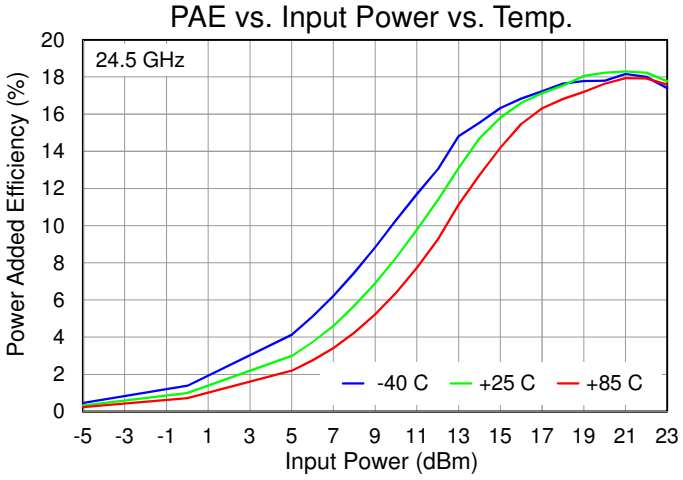

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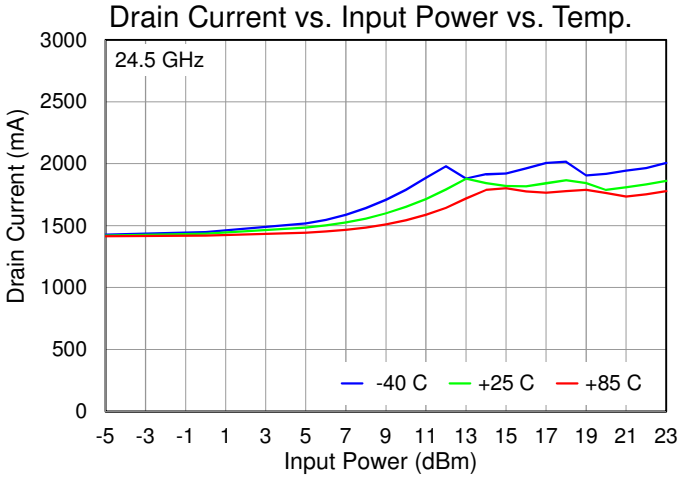

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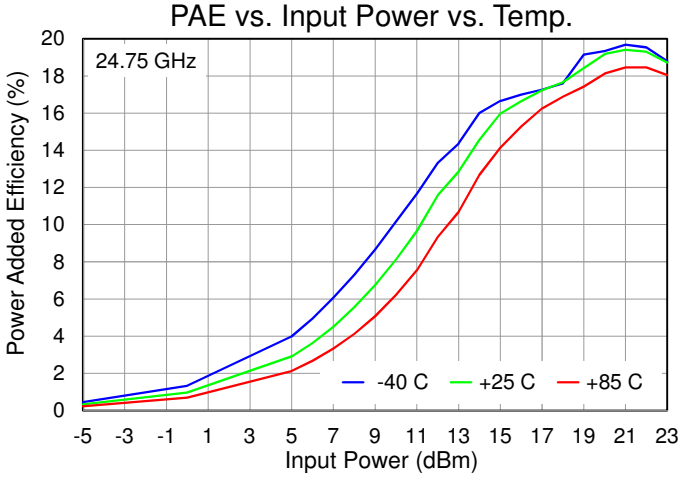

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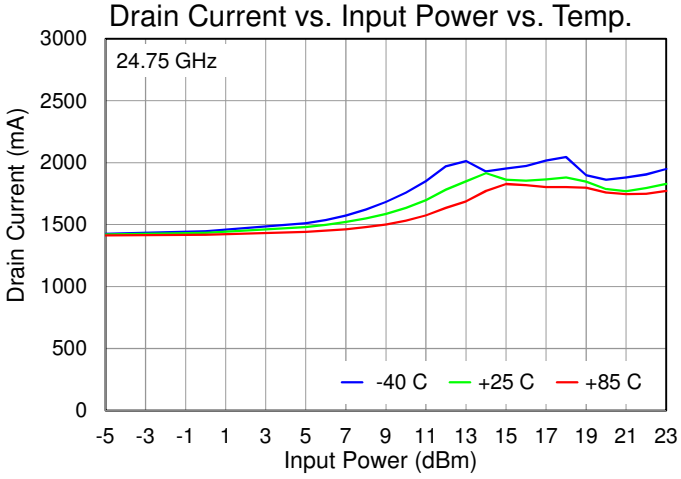

Performance Plots – Large Signal

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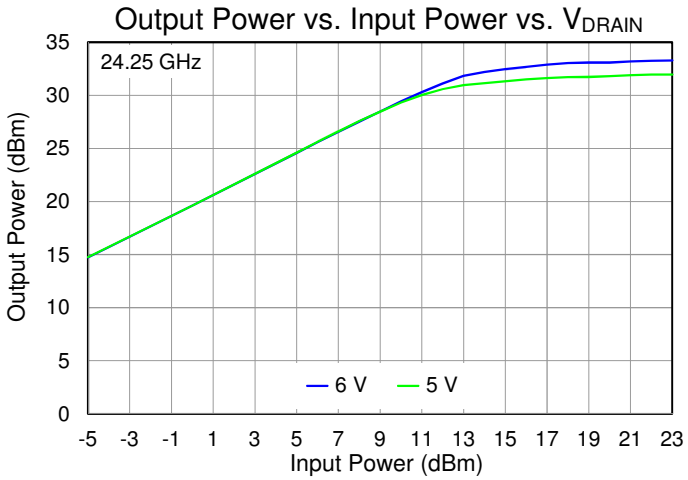
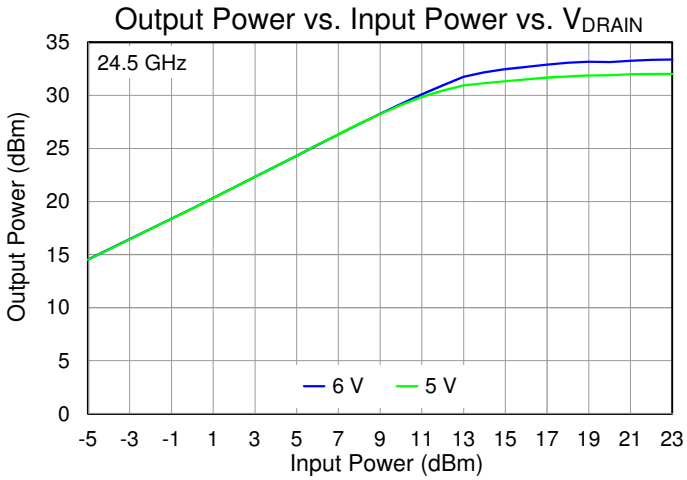
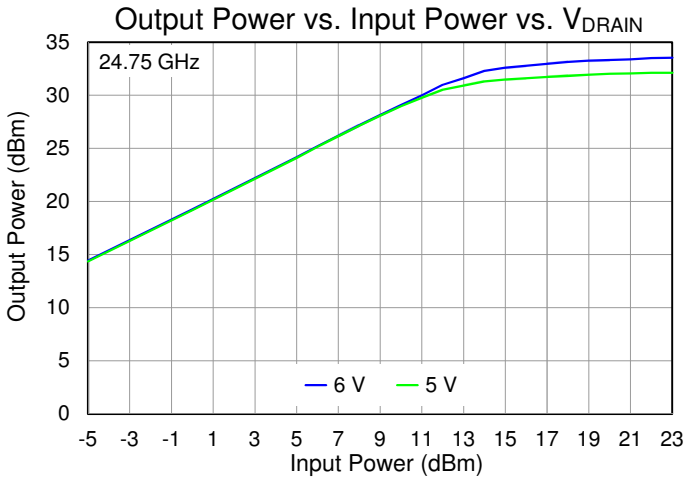
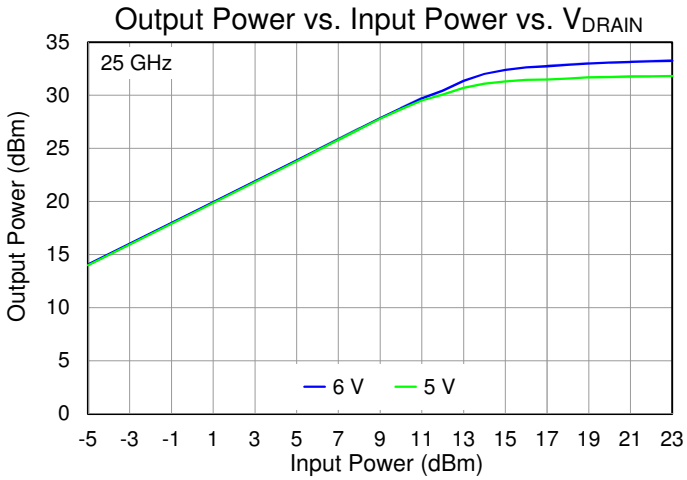
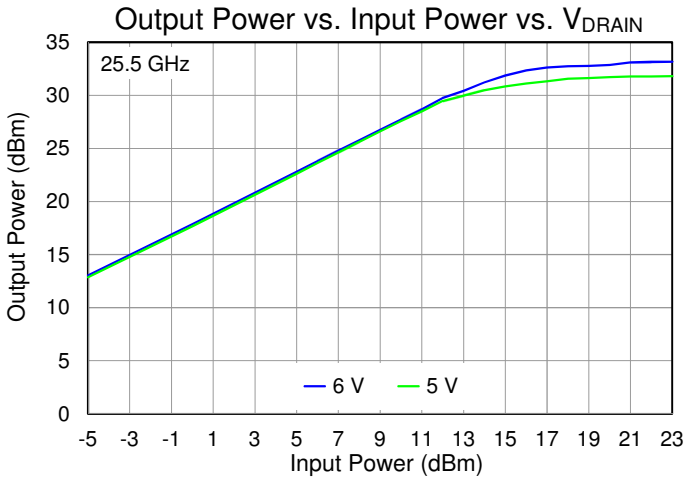
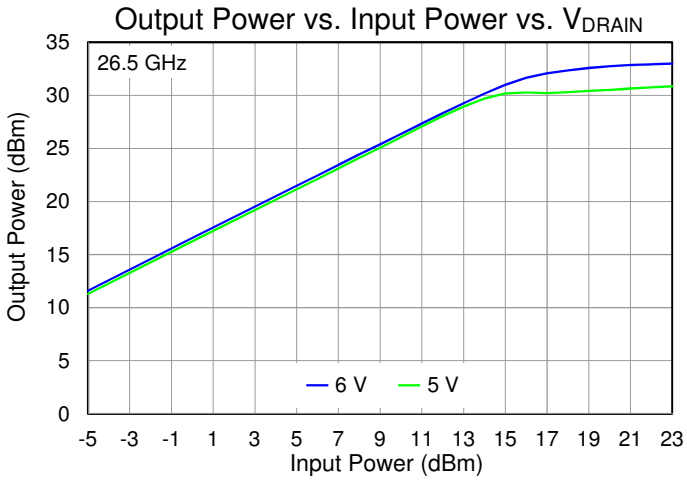






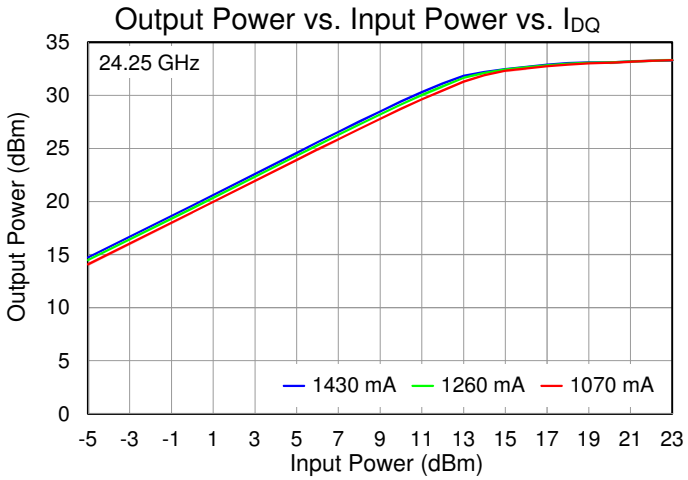


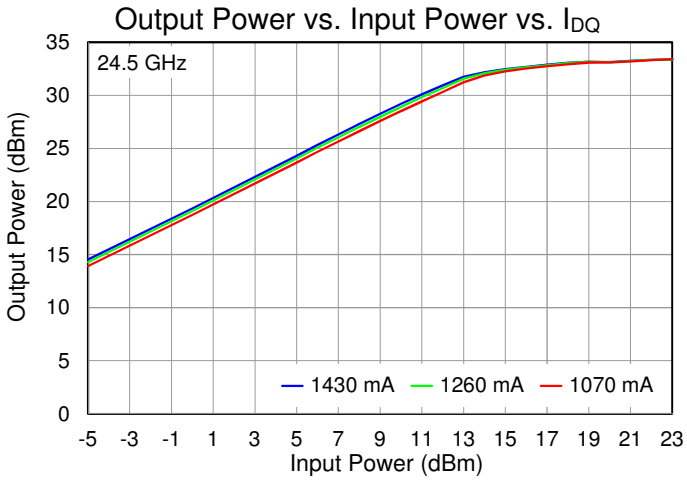


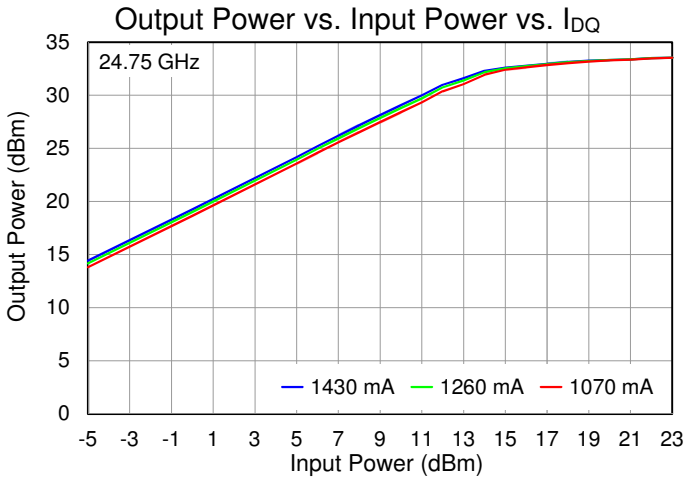


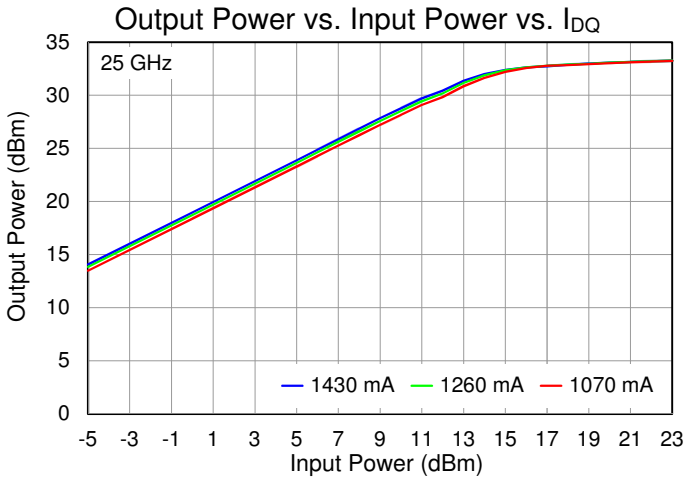
Performance Plots – Large Signal

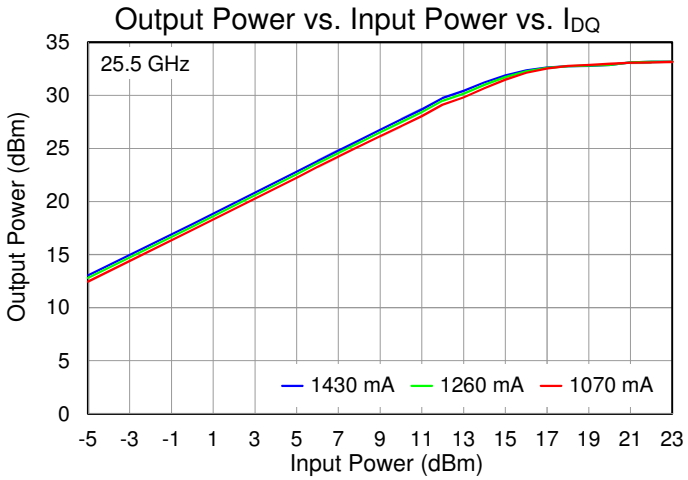
Test conditions, unless otherwise noted: CW, V_D = 6 V, I_{DQ} = 1430 mA, T_{BASE} = +25 °C (T_{BASE} is backside of QPA4536)

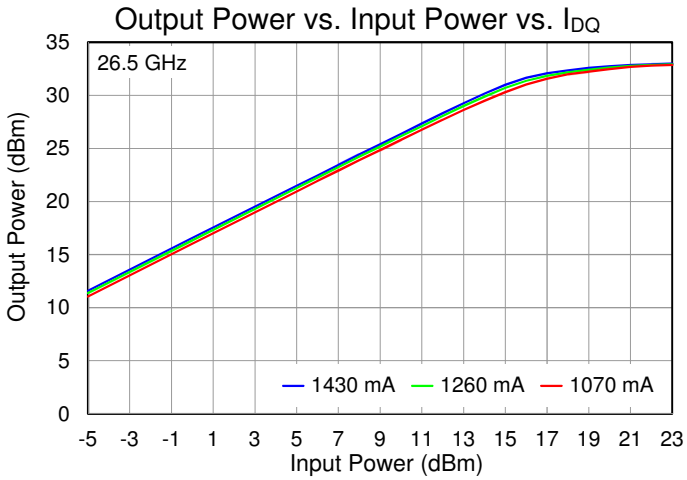








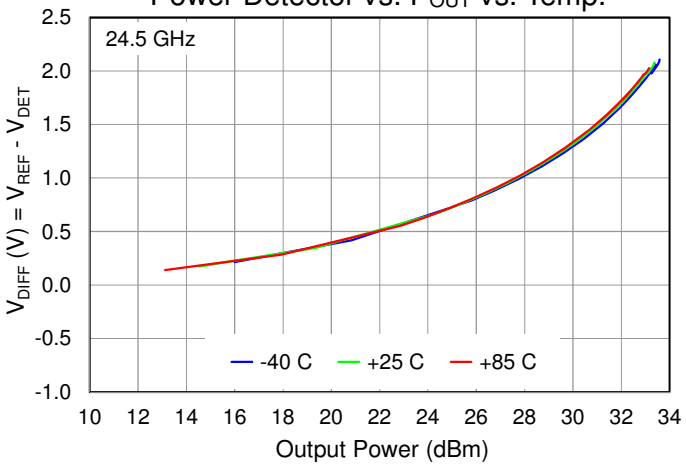




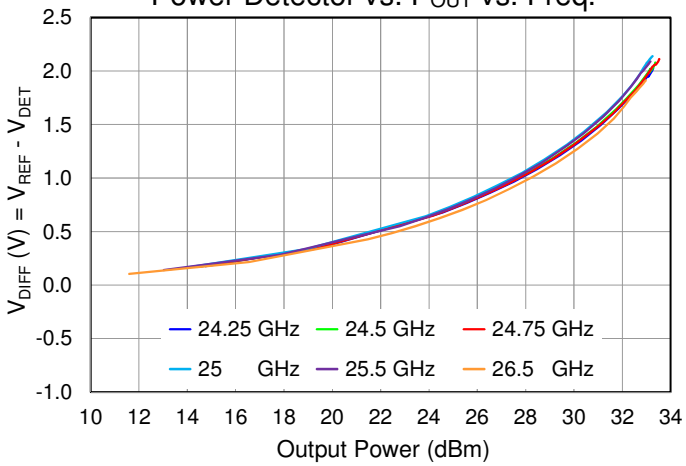
Performance Plots – Large Signal

Test conditions, unless otherwise noted: CW, V_D = 6 V, I_{DQ} = 1430 mA, T_{BASE} = +25 ºC (T_{BASE} is backside of QPA4536)

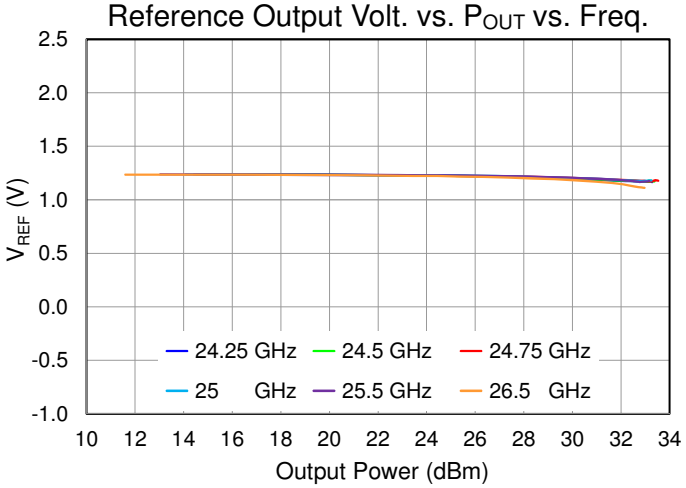
Power Detector vs. P_{OUT} vs. Temp.



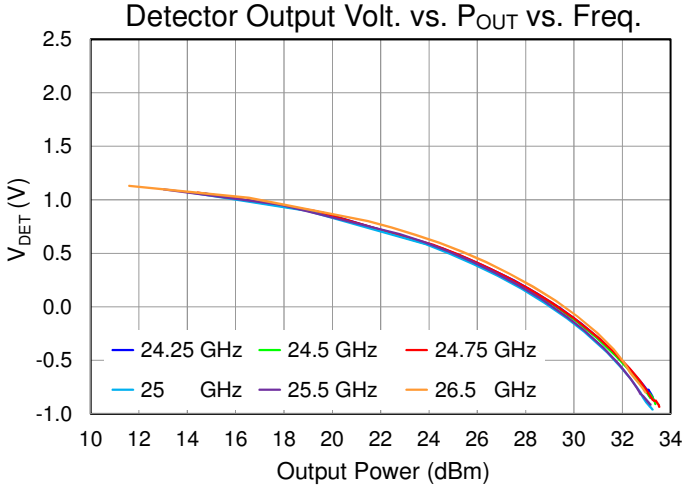
Power Detector vs. P_{OUT} vs. Freq.



Reference Output Volt. vs. P_{OUT} vs. Freq.



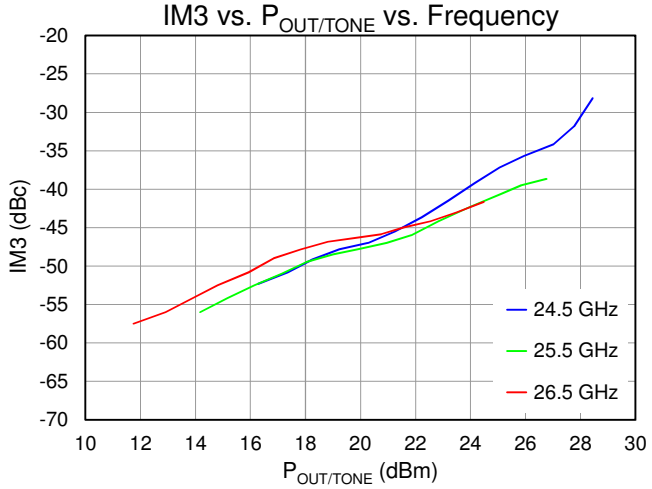
Detector Output Volt. vs. P_{OUT} vs. Freq.



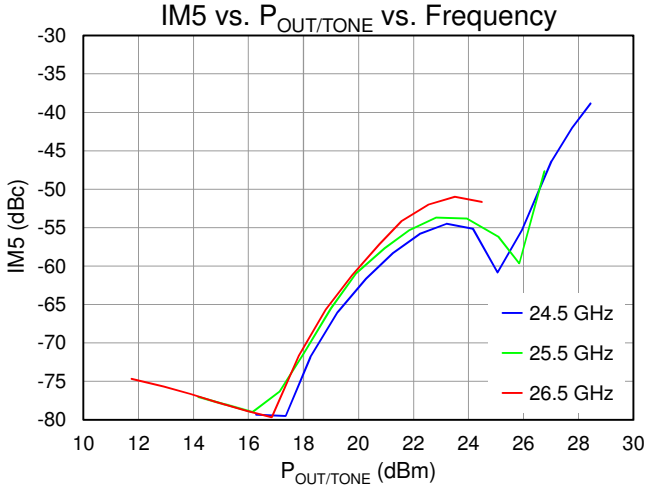
Performance Plots – Linearity

Test conditions, unless otherwise noted: CW, V_D = 6 V, I_{DQ} = 1430 mA, Δf = 10 MHz, T_{BASE} = +25 ºC (T_{BASE} is backside of QPA4536)

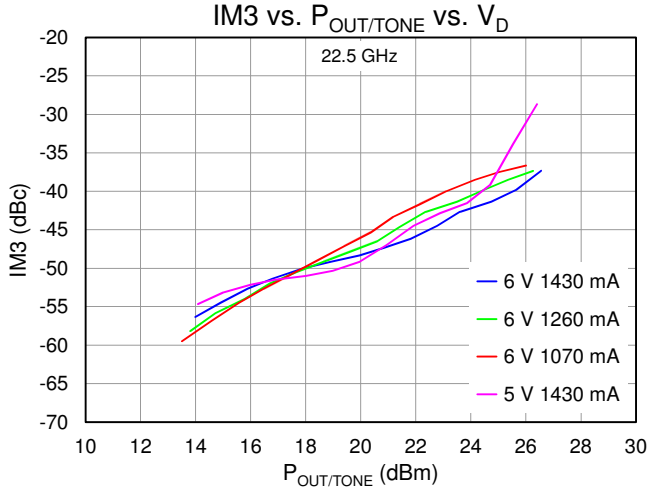
IM3 vs. $P_{OUT/TONE}$ vs. Frequency



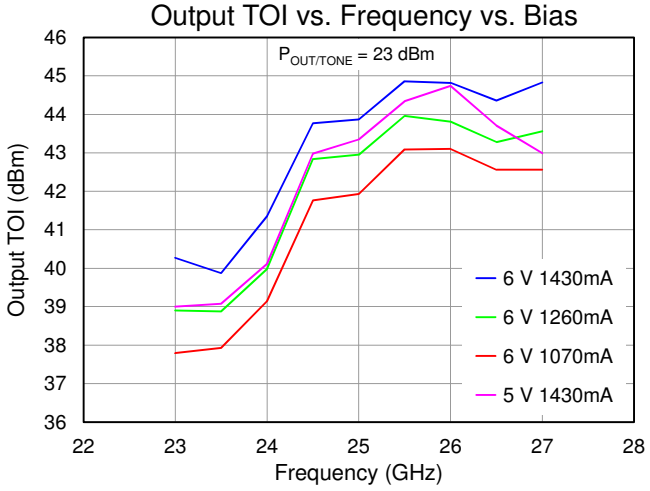
IM5 vs. $P_{OUT/TONE}$ vs. Frequency



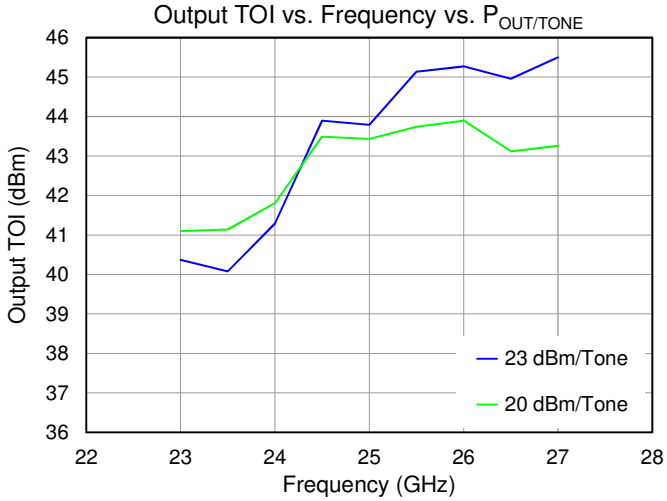
IM3 vs. $P_{OUT/TONE}$ vs. V_D



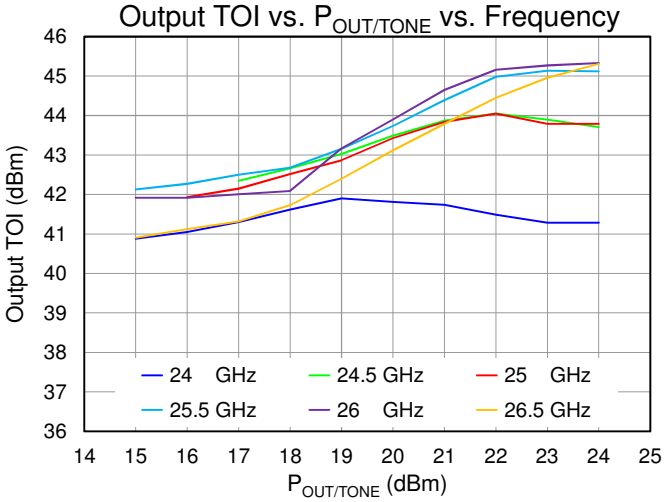
Output TOI vs. Frequency vs. Bias



Output TOI vs. Frequency vs. $P_{OUT/TONE}$



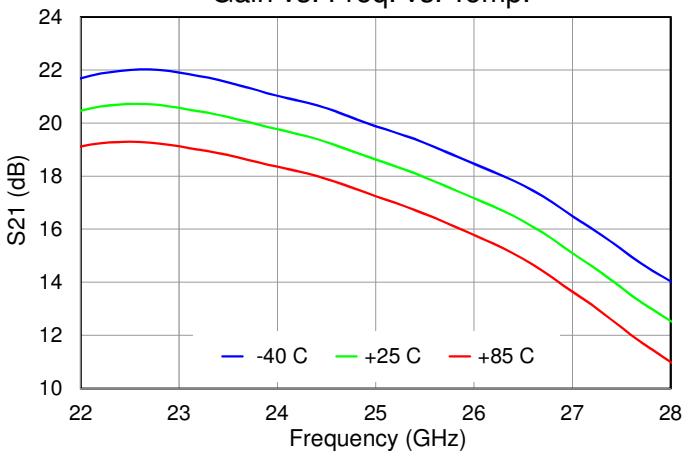
Output TOI vs. $P_{OUT/TONE}$ vs. Frequency



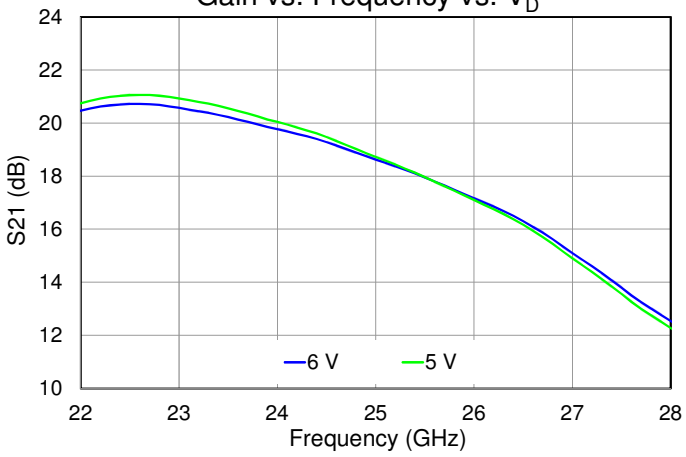
Performance Plots – Small Signal

Test conditions, unless otherwise noted: CW, V_D = 6 V, I_{DQ} = 1430 mA, P_{IN} = -20 dBm, T_{BASE} = +25 ºC (T_{BASE} is backside of QPA4536)

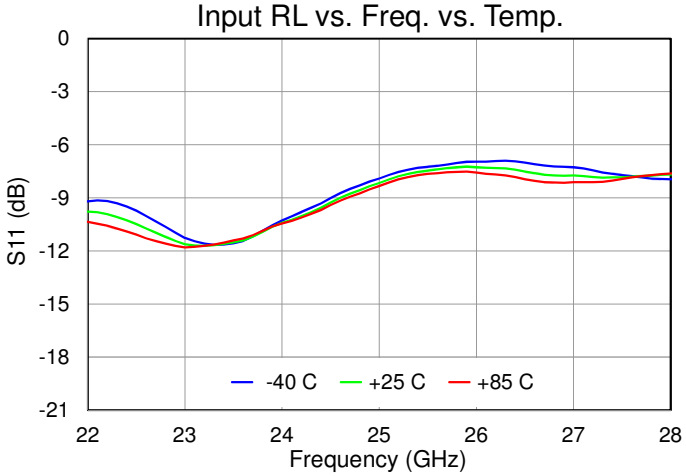
Gain vs. Freq. vs. Temp.



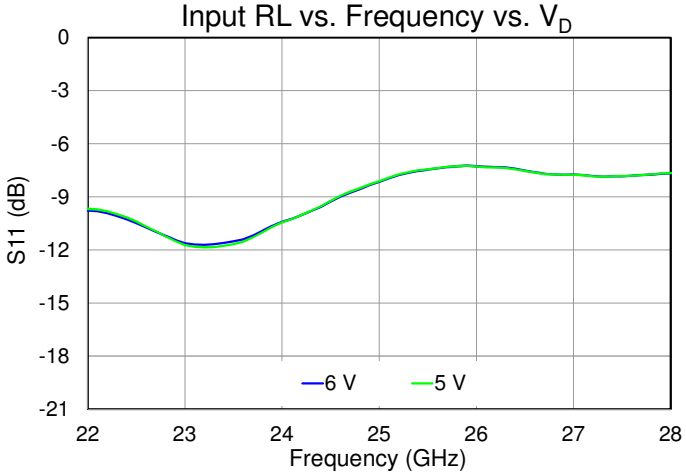
Gain vs. Frequency vs. V_D



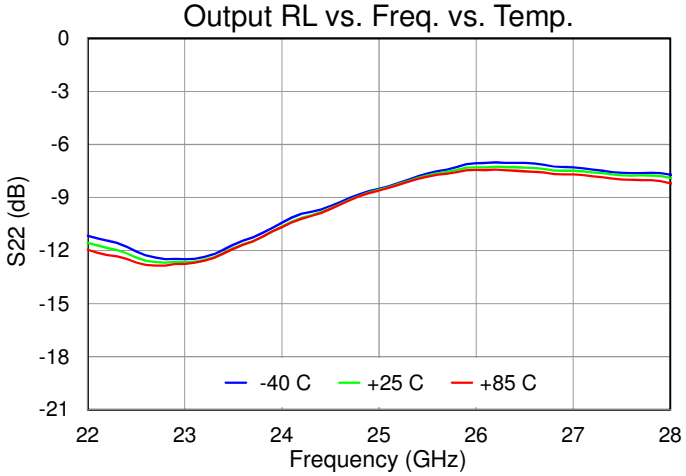
Input RL vs. Freq. vs. Temp.



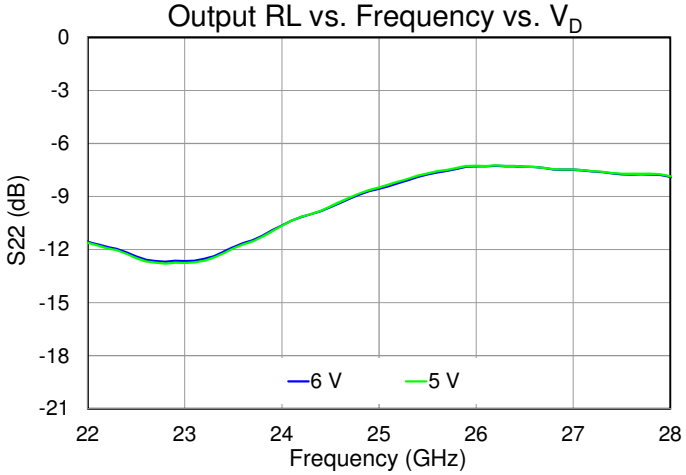
Input RL vs. Frequency vs. V_D



Output RL vs. Freq. vs. Temp.

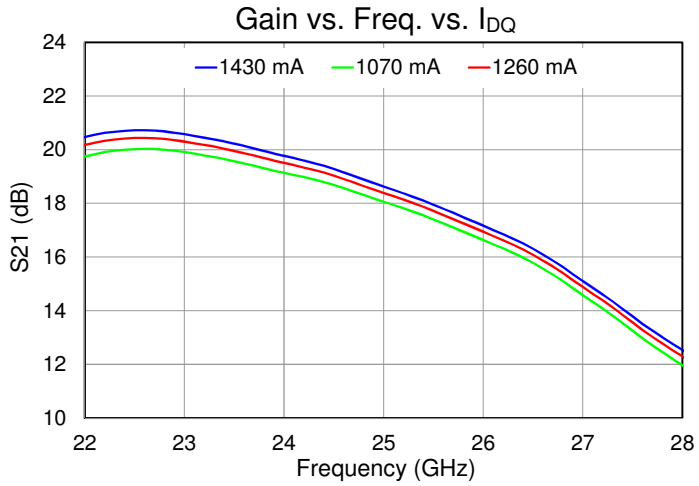


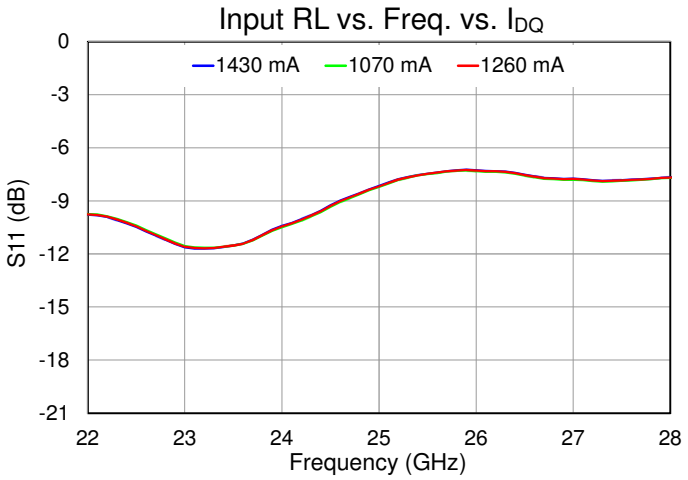
Output RL vs. Frequency vs. V_D

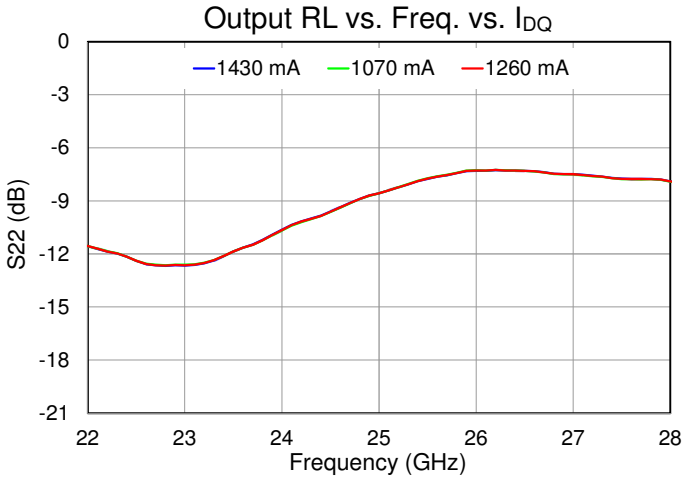


Performance Plots – Small Signal

Test conditions, unless otherwise noted: CW, V_D = 6 V, I_{DQ} = 1430 mA, P_{IN} = -20 dBm, T_{BASE} = +25 ºC (T_{BASE} is backside of QPA4536)

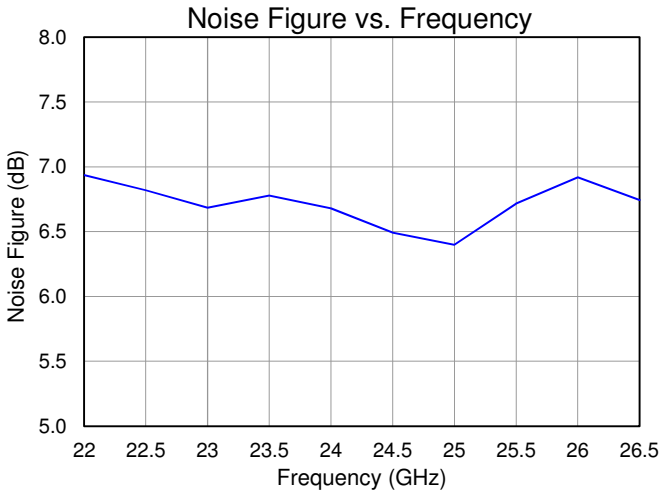


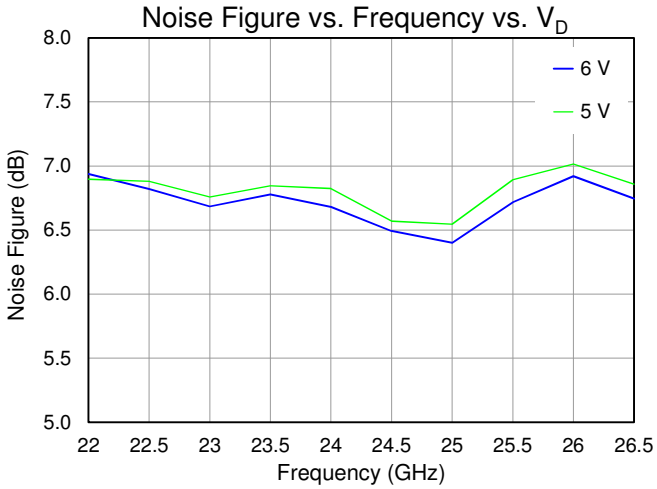


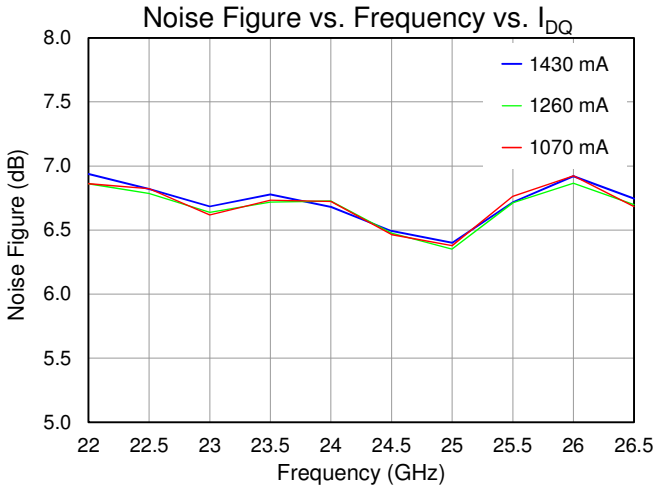


Performance Plots – Small Signal

Test conditions, unless otherwise noted: CW, V_D = 6 V, I_{DQ} = 1430 mA, T_{BASE} = +25 ºC (T_{BASE} is backside of QPA4536)





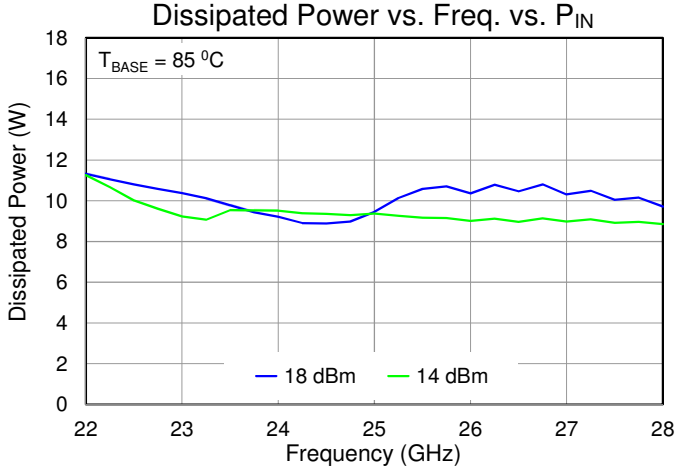


Thermal and Reliability Information

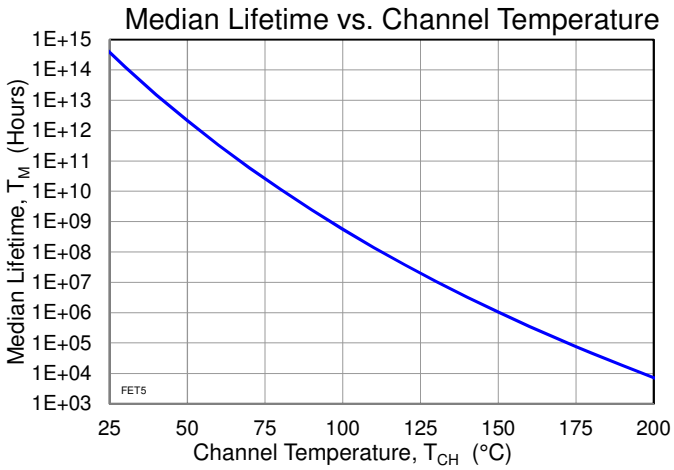
Parameter	Test Conditions	Value	Units
Thermal Resistance, θ_{JC} (1)	Quiescent, no RF T_{BASE} = 85 °C, V_D = 6 V, I_{DQ} = 1430 mA, P_{DISS} = 8.6 W	7.79	ºC/W
Channel Temperature, T_{CH}		152	°C
Thermal Resistance, θ_{JC} (1)	P_{IN} = 14 dBm, T_{BASE} = 85 °C, CW, V_D = 6 V, I_{DQ} = 1430 mA, Freq = 24.5 GHz, I_{D_DRIVE} = 1790 mA, P_{OUT} (P_{1dB}) = 31.5 dBm, P_{DISS} = 9.4 W	7.86	ºC/W
Channel Temperature, T_{CH}		159	°C
Thermal Resistance, θ_{JC} (1)	P_{IN} = 18 dBm (2), T_{BASE} = 85 °C (2), CW, V_D = 6 V, I_{DQ} = 1430 mA, Freq = 26.25 GHz, I_{D_DRIVE} = 2055 mA, P_{OUT} (P_{SAT}) = 32 dBm, P_{DISS} = 10.8 W	7.96	ºC/W
Channel Temperature, T_{CH}		171	°C

Notes:
1. Thermal resistance determined to T_{BASE} (T_{BASE} is backside of QPA4536)
2. Limited by thermal; operating at P_{SAT} (P_{IN} = 18 dBm) would degrade Median Lifetime (T_M); see plot below. Recommended reducing T_{BASE} to improve T_M.

Dissipated Power

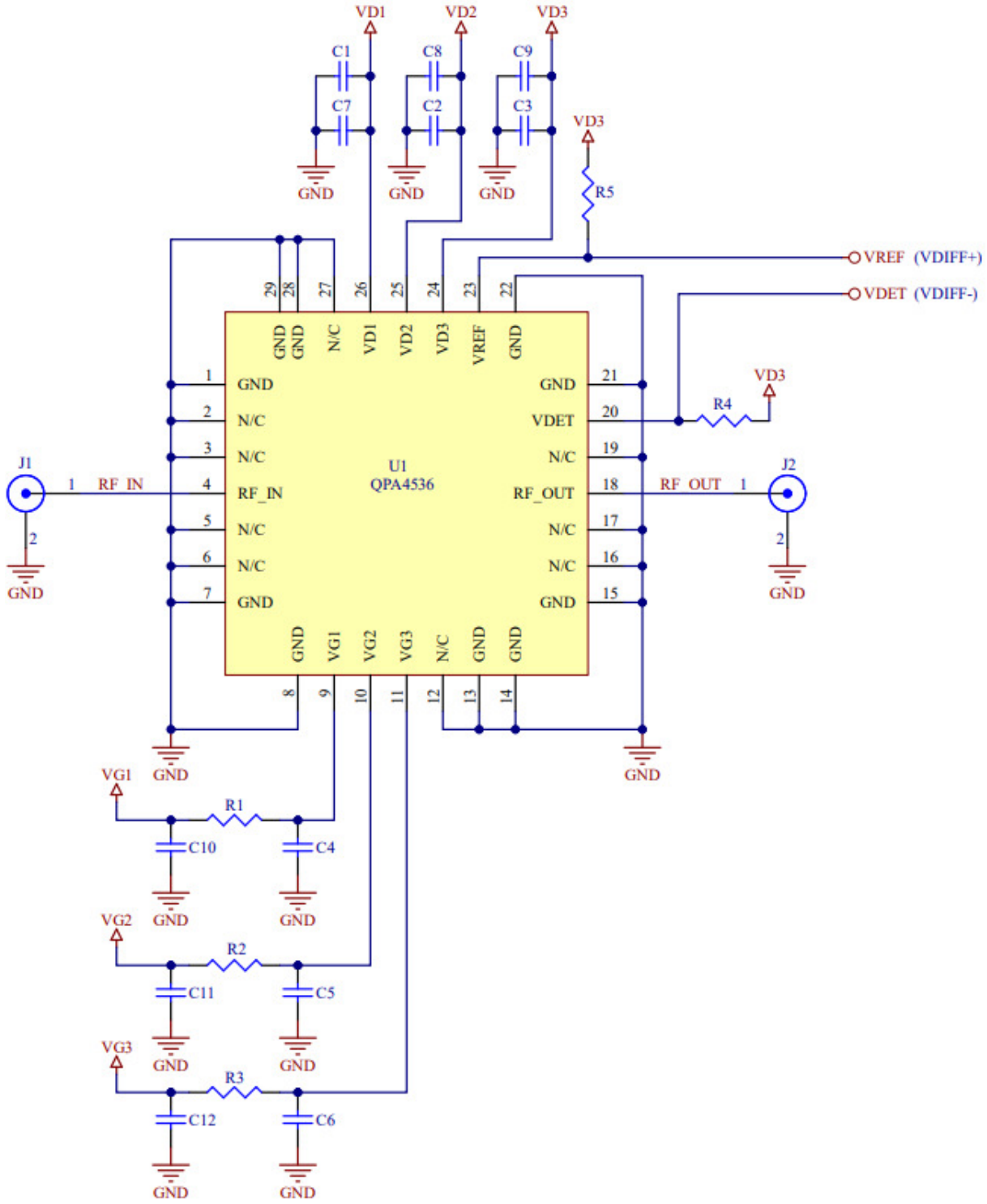


Test conditions: CW, V_D = 6 V, I_{DQ} = 1430 mA, T_{BASE} = 85 ºC (T_{BASE} is back side of QPA4536)



Test conditions: CW, V_D = 6 V, Failure Criterial = 10% reduction in I_{D_MAX}

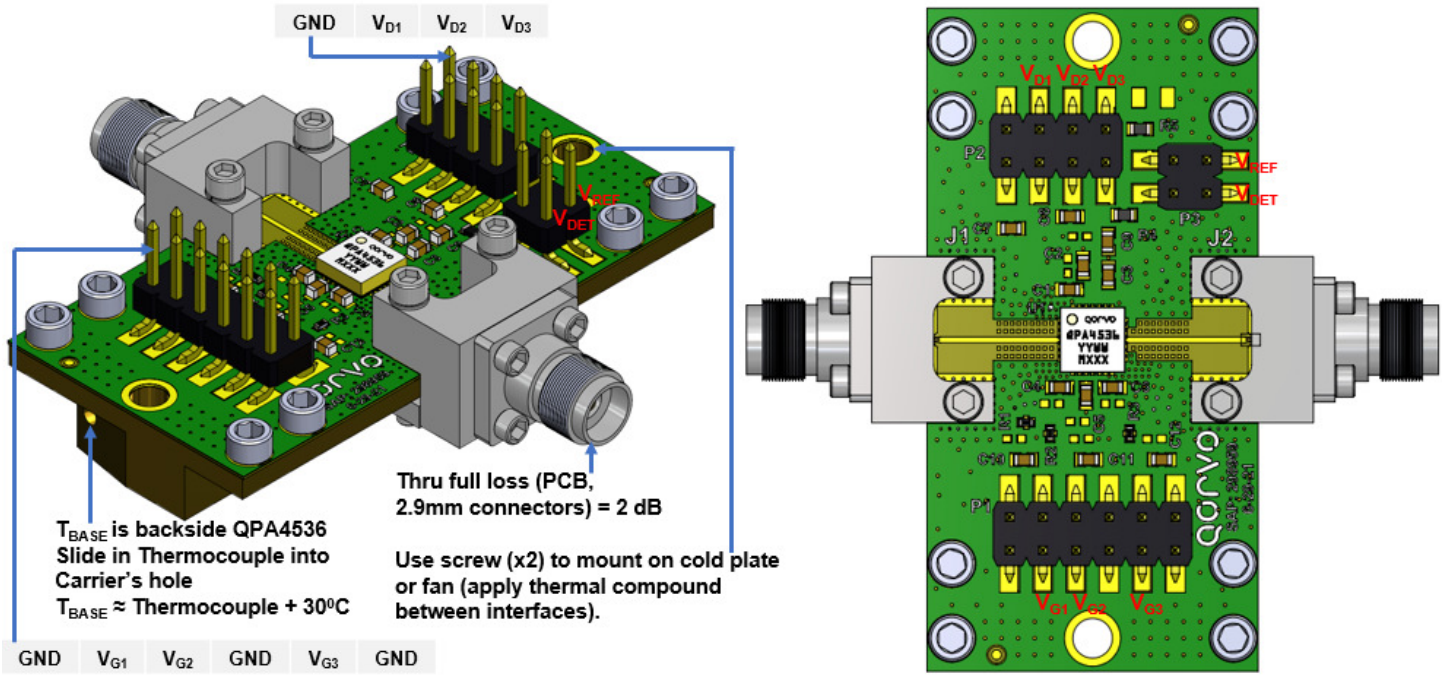
Applications Information

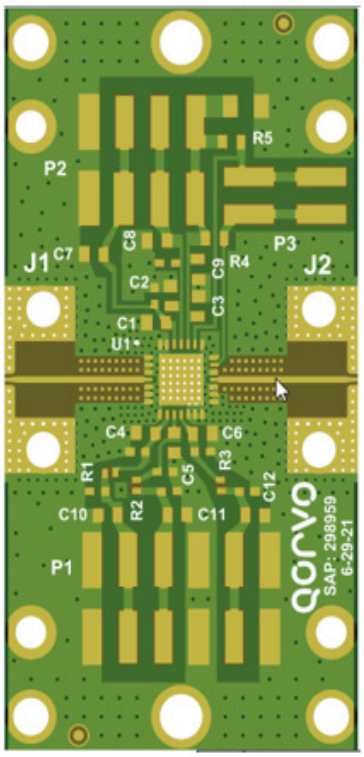


Combined $V_D = V_{D1} + V_{D2} + V_{D3}$, $V_G = V_{G1} + V_{G2} + V_{G3}$

See BOM page 20

Evaluation Board (EVB) Layout





LAYER STACK LEGEND

Material	Layer	Thickness	Dielectric Material	Type
	Top Overlay			Legend
Surface Material	Top Solder	0.0010in	Solder Resist	Solder Mask
Copper	Top Layer	0.0007in		Signal
Prepreg		*0.0080in*	*ROGERS 4003C*	*Dielectric*
Copper	Bottom Layer	0.0007in		Signal

Finished board thickness: 0.0104in

Recommend Cu-filled or Epoxy-filled Vias

Bill of Materials

Reference Des.	Qty	Value	Description	Part Number
C1 – C12	12	0.01 uF	CAP, 1uF, ±10%, 50V, X7R, 0603	
R1 – R3	3	10 Ω	RES, 10 Ohm, ±1%, 1/16W, 0402	
R4, R5	2	24K Ω	RES, 24K Ohm, ±5%, 1/10W, 0603	
PCB	1		PCB, see page 19	Qorvo, Custom
H1	1		CONN, HDR, 8 POS, Dual, SMD	
H2	1		CONN, HDR, 4 POS, 2 RAW, SMD, Au	
H3	1		CONN, HDR, ST, 2x6, 0.100”, SMD	
J1, J2	2		Connector, RF 2.92mm, F, Pin 0.007, Diel 0.039	Southwest Microwave 1092-04A-12
H-Block	1		H-Block, Copper C110, 1 x 2 x 0.0275T in	Qorvo, Custom
S1 – S8	8		Screw, Cap, Socket Head, 2-56X1/8”	
Solder Preform			Preform, Solder (SAC305) 1 x 1 x 0.002 in	
Solder			Paste, solder, Syntech, Sn63/Pb37	
TC			Thermal Compound, Silver 5GR	Artic Silver 5 AS5-5G

.

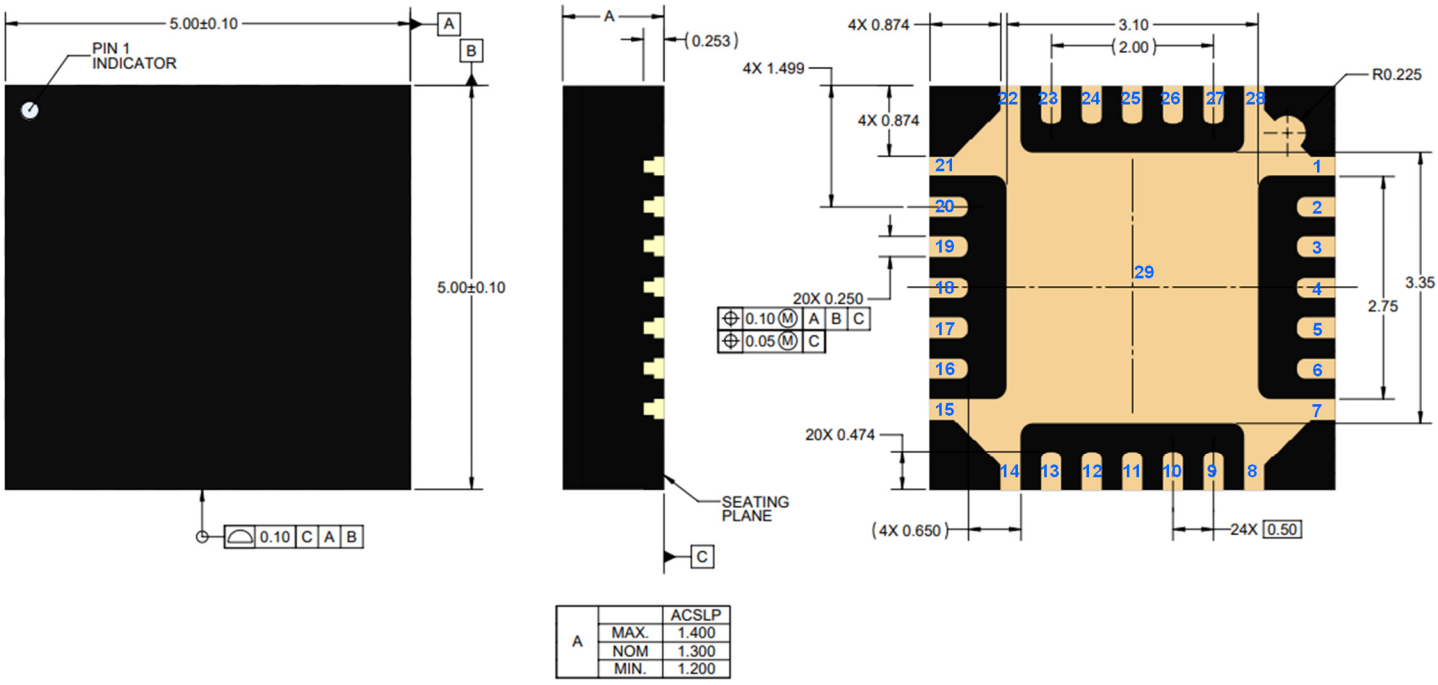
Bias-Up Procedure

1. Set I_D limit to 2.8 A, I_G limit to 60 mA
2. Set V_G to –1.5 V
3. Set V_D +6 V. Ensure I_{DQ} ~ 0 mA
4. Adjust V_G more positive until I_D = 1430 mA; V_G ≈ -0.6 V +/- V typical range
5. Apply RF signal

Bias-Down Procedure

1. Turn off RF signal
2. Reduce V_G to –1.5 V. Ensure I_{DQ} ~ 0 mA
3. Set V_D to 0 V
4. Turn off V_D supply
5. Turn off V_G supply

Mechanical Information



A		ACSLP
	MAX.	1.400
	NOM	1.300
	MIN.	1.200

Package is air-cavity and non-hermetic, leads are Au plated

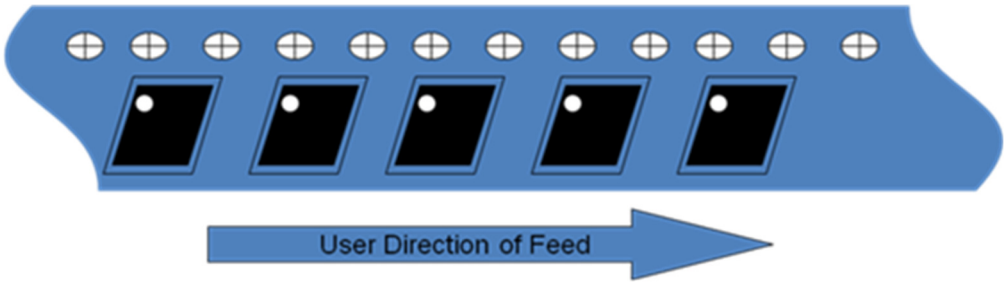
Pin Description

Pin Number	Symbol	Description
1, 7, 8, 13, 14, 15, 21, 22, 28, 29	GND	Ground and backside paddle (29); multiple vias should be employed to minimize inductance and thermal resistance
2, 3, 5, 6, 12, 16, 17, 19, 27	N/C	No internal connection; recommend grounding these pins for best RF performance and minimize inductance
4	RF_{IN}	RF Input. Matched to 50 Ω, DC blocked
9	V_{G1}	Gate voltage for stage 1(1)
10	V_{G2}	Gate voltage for stage 2(1)
11	V_{G3}	Gate voltage for stage 3(1)
18	RF_{OUT}	RF Output. Matched to 50 Ω, DC blocked
20	V_{DET}	Detector diode output voltage. Varies with RF output power
23	V_{REF}	Reference diode output voltage
24	V_{D3}	Drain voltage for stage 3(1)
25	V_{D2}	Drain voltage for stage 2(1)
26	V_{D1}	Drain voltage for stage 1(1)

1. External bypassing required; refer to page 18 for recommendation

Tape and reel Information

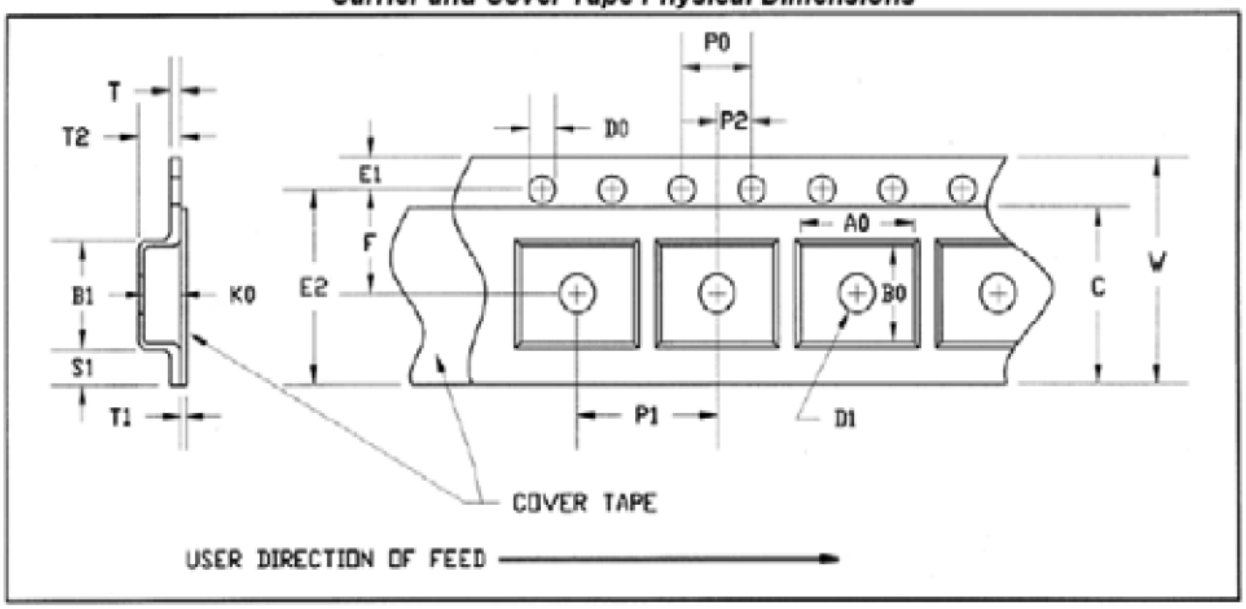
Standard T/R size = 250 pieces on a 7” reel



CARRIER AND COVER TAPE DIMENSIONS

Part	Feature	Symbol	Size (in)	Size (mm)
Cavity	Length	A0	0.209	5.3
	Width	B0	0.209	5.3
	Depth	K0	0.065	1.65
	Pitch	P1	0.314	8
Centerline Distance	Cavity to Perforation – Length Direction	P2	0.079	2
	Cavity to Perforation – Width Direction	F	0.217	5.5
Cover Tape	Width	C	0.362	9.2
Carrier Tape	Width	W	0.472	12

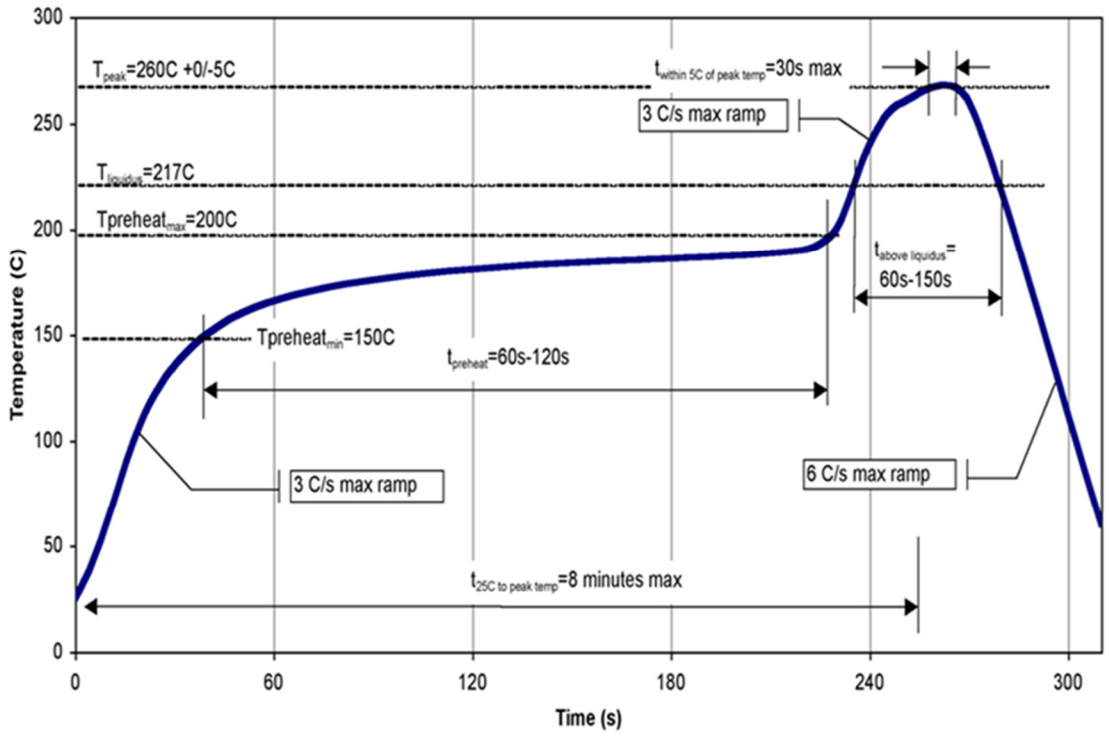
Carrier and Cover Tape Physical Dimensions



Solderability

- Compatible with the latest version of J-STD-020, Lead-free solder, 260 °C
- Do not expose the package lid to temperatures > 280 °C
- Contact plating: Ni-Au
- Solder rework not recommended

Recommended Soldering Temperature Profile



Handling Precautions

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	1A	ANSI/ESD/JEDEC JS-001
ESD – Charged Device Model (CDM)	C3	ANSI/ESD/JEDEC JS-002
MSL – Moisture Sensitivity Level	5A	IPC/JEDEC J-STD-020

Caution!

ESD-Sensitive Device

RoHS Compliance

This product is compliant with the 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment), as amended by Directive 2015/863/EU .

This product also has the following attributes:

- Lead Free
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_40_2$) Free
- PFOS Free
- SVHC Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

Web: www.qorvo.com

Tel: 1-844-890-8163

Email: customer.support@qorvo.com

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