QM78207

5G PAMiD Module

Product Description

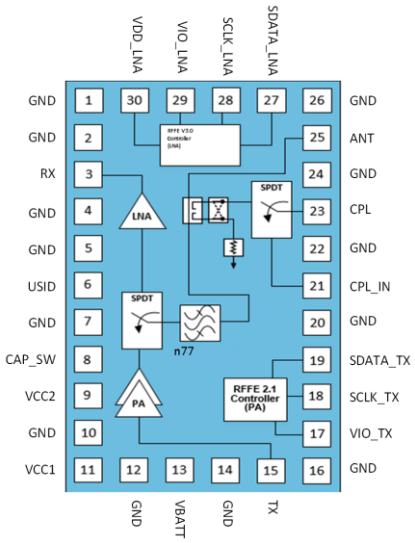
The Qorvo®QM78207 is a highly integrated Sub-6GHz UHB L-PAMiD compliant to both 4G-LTE and 5G-NR standards targeted for advanced RF devices including flagship/premium smartphones and data devices.

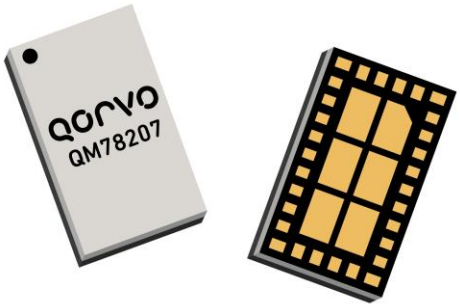
The module consists of Ultra-High Band PA, multi-gain LNA, high performance Filter, directional coupler,TxRx Switch with switchable VCC Bypass Capacitor for different Vcc bypass capacitance

The QM78207 supports Envelope Tracking (ET) as well as Average Power Tracking (APT). An integrated LNA provides low noise figure, high linearity, and optimal system sensitivity with support for high order carrier aggregation.

The QM78207 is packaged in a RoHS-compliant, 3mm x 5mm package.

Functional Block Diagram





Top View

30 Pin, 3.0 mm x 5.0 mm x 0.64 mm

Feature Overview

- Microshield™, self-shielded technology
- 5G-NR Bands n77, n78
- 4G LTE Bands B42, B48, B43
- Integrated UHB LNA and filtering
- VCC bypass Capacitor Switch
- Global CA Platform
- Forward and reverse coupler with daisy chain switch
- Dual core MIPI RFFE
- Preliminary RFFE MIPI 3.0 for RX control
- PC2 for n77 and n78

Ordering Information

PART NUMBER	DESCRIPTION
QM78207SB	5pc Bag
QM78207SR	7” reel, 100 pcs
QM78207TR13	13” reel, Qty to order (5k units)
QM78207PCK	Design Kit
QM78207EVB	Evaluation board

Absolute Maximum Ratings

Parameter	Symbol, Conditions	Rating	Units
Battery voltage	V_{BATT}	6.0	V
Max Supply Voltage	V_{CC1}, V_{CC2}	6.0	V
LNASupply Voltage	VDD_LNA	-0.3 to 2.5	V
RFFE Control Interface Bus	VIO1, SDATA1, SCLK1 and VIO2, SDATA2, SCLK2	2.0	V
Input RF Power	TX input, CW 50 Ohm,T=25 °C	+10.0	dBm
Ruggedness (No damage or permanent degradation)	VSWR (RFIN = +15 dBm, CW 50 % duty cycle/ 4 ms period/ 10 s duration at each VSWR phase in 30° steps, V_{BATT} = 6.0 V, Vcc = 5.5V, PA toggled ON/ OFF in accordance with RFIN, with enable applied 5 µs before RFIN)	10:1	-
Input RF Power	ANT port, Rx mode, in band frequencies	25	dBm
Storage Temperature	Tstorage	-40 to 150	°C
Operating Case Temperature	Tcase	-20 to 85	°C

Notes: Exceeding any one or combination of the Absolute Maximum Rating conditions may cause damage to the device. Extended application of the Absolute Maximum Rating conditions to the device may reduce device reliability. Specified typical operation of the device under Absolute Maximum Rating conditions is not implied.

Recommended Operating Conditions

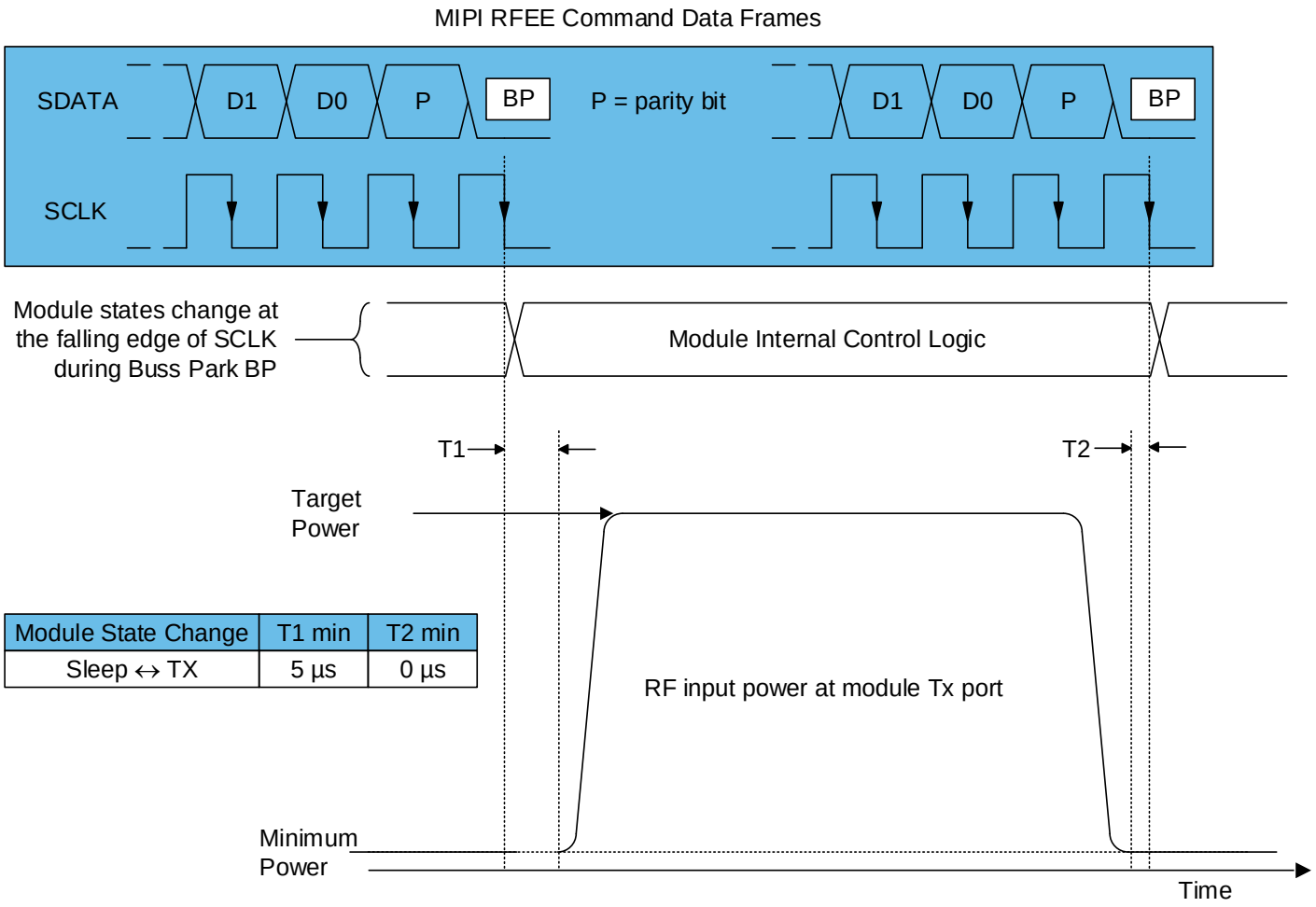
Parameter	Conditions	Min.	Typ.	Max.	Units
Supply Voltage	V_{BATT}	3	3.8	4.8	V
	VDD LNA	1.08	1.2	1.9	
	APT V_{CC1}, V_{CC2}	0.5	-	5.0	
	ET V_{CC1}, V_{CC2}	0.5	-	5.0	
	Leakage at V_{Batt}	-	-	20	uA
	Leakage at V_{cc1} & V_{cc2}	-	-	20	
Internal Load capacitance	Vcc1	-	70	-	pF
	Vcc2	-	30	-	
RFFE Control Interface Bus	VIO1, SDATA1, SCLK1 and VIO2, SDATA2, SCLK2	1.65	1.8	1.95	V
VIO Power On Reset Voltage	$VIO_{\_Reset}$	-	-	0.45	V
Logic Low		0	0	0.3*VIO	V
Logic High		0.7*VIO		VIO	V
Operating Case Temperature		-20	-	85	°C
Input and Output Impedance		-	50	-	Ω

Electrical Specifications are measured at specified test conditions. Specifications are not guaranteed over all operating conditions.

Timing Diagram

The QM78207 recommended control timing for Tx mode operation is shown below. The falling edge of SCLK during Bus Park (BP) is the master timing reference for all hardware events such as the application of RF input to the Tx input port of the module. Failure to comply with the specification below may result in RF output distortion or module damage.

For applications where MIPI RFEE V_{IO} is turned ON/OFF in accordance with MIPI RFEE bus activity, please refer to the **VIO Timing** specifications.



Module State Change	T1 min	T2 min
Sleep ↔ TX	5 µs	0 µs

Delay application of RF power to Tx input by at least T1 µs after switching to Tx mode (TRX_SW_Control Bus Park BP).
Do not exit Tx mode until T2 µs after RF power at the Tx input has been removed.
2µs are recommended typically.

5G NR Test Signal Configurations - All test signals are 3GPP TS38.101 compliant

WF TYPE	Modulation	MPR for all BW and SCS	
		OUTER	INNER
DFT-s-OFDM	Pi/2-BPSK	≤ 0.5	0
	QPSK	≤ 1	0
	16QAM	≤ 2	≤ 1
	64QAM	≤ 2.5	
	256QAM	≤ 4.5	
CP-OFDM	QPSK	≤ 3	≤ 1.5
	16QAM	≤ 3	≤ 2
	64QAM	≤ 3.5	
	256QAM	≤ 6.5	

5G NR Signal Configurations - All test signals are 3GPP TS38.101 compliant

5G Waveform	Duplex Mode	Channel BW	SCS	Modulation	RB Allocation	RB Allocated	RB start	MPR
NR10M00	TDD 40% DC	10	15	DFT-s-OFDM QPSK	Inner_Partial	1	24	0
NR100M00	TDD 40% DC	100	30	DFT-s-OFDM QPSK	Inner_Full	135	67	0
NR100M10	TDD 40% DC	100	30	DFT-s-OFDM QPSK	Outer_Full	270	0	1
NR100M30	TDD 40% DC	100	30	CP-OFDM QPSK	Outer_Full	273	0	3
NR100M45	TDD 40% DC	100	30	DFT-s-OFDM 256QAM	Outer_Full	270	0	4.5
NR100M65	TDD 40% DC	100	30	CP-OFDM 256QAM	Outer_Full	273	0	6.5

4G LTE Signal Configurations - All test signals are 3GPP TS25.101 compliant

NAME	DEFINITION	MPR (DB)
TC1	LTE partial RB: - 10M12RB, QPSK:	0
TC2	LTE full RB: - 10M50RB, QPSK: - 20M100RB, QPSK:	1
TC3	LTE UL-CA full RB: - LTE 20 + 20 MHz full RB intraband contiguous CA	2

5G NR n77 Tx Characteristics

Test conditions unless otherwise specified: V_{CC1} = V_{CC3} = 5.0V, V_{BATT} = +3.8 V, Temp. = 25 °C. Performance referenced to module pin location.

Parameter	Conditions	Product Spec.			Units
		Min.	Typ.	Max.	
Frequency		3300	-	4200	MHz
Output Power					
CW Output Power	P2dB, Vcc_1 = Vcc_2 = 5.0V		32		dBm
APT Linear Output Power	HPM, Vcc_1 = Vcc_2 ≤ 5.0V, Prated PC2	28.5			
	HPM, Vcc_1 = Vcc_2 ≤ 5.0V, Prated PC3	26.5			
	LPM, Vcc_1 = Vcc_2 = 2.5V	1.5			
Gain					
Gain (G)	P2dB, Vcc_1 = Vcc_2 = 5.0V		29		dB
	APT HPM, Vcc_1 = Vcc_2 ≤ 5.0V, Pout ≤ Prated PC2		32		
	APT HPM, Vcc_1 = Vcc_2 ≤ 5.0V, Pout ≤ Prated PC3		32		
	APT LPM, Vcc_1 = Vcc_2 = 2.5V		12		
Linearity					
Adjacent Channel Leakage Power Ratio (ACLR)	APT HPM, $EUTRA_{ACLR}$		-38		dBc
	APT LPM, $EUTRA_{ACLR}$, Pout = 1.5 dBm		-42		
EVM	APT HPM, NR100M65		1.8		%
Current & Efficiency					
Quiescent Current	Vbatt = 3.8V, Vcc_1 = Vcc_2 = 5.0V		315		mA
	Vbatt = 3.8V, Vcc_1 = Vcc_2 = 2.5V		14		
Current Consumption Total Current (I_{cc1} + I_{cc3} + I_{batt})	HPM, Vcc_1 = Vcc_2 ≤ 5.0V, Pout = Prated PC2		830		
	HPM, Vcc_1 = Vcc_2 ≤ 5.0V, Pout = Prated PC3		700		
	LPM, Vcc_1 = Vcc_2 ≤ 2.5V, Pout = 1.5dBm		12		
Ibatt	HPM		6		
PAE	HPM, Vcc_1 = Vcc_2 ≤ 5.0V, Pout = Prated PC2		17		%
	HPM, Vcc_1 = Vcc_2 ≤ 5.0V, Pout = Prated PC3		12.5		
HARMONICS					
2nd Harmonic	HPM, Pout ≤ Prated PC2, NR10M00		-40		dBm
3 rd Harmonic			-50		
4 th Harmonic			-35		
5 th Harmonic			-50		
Out of Band Gain					
GPS Band Gain	1574 – 1577 MHz		-46		dB
ISM Gain	2400 - 2481 MHz		-7		
VSWR					
Input VSWR	All Modes			3:1	-
Ouput VSWR				3:1	
STABILITY					
Spurious Levels	APT HPM, All Loads ≤ 6:1, in-band, all angles, closed loop to maintain Prated, Vbatt = 3.8V, Vcc_1 = Vcc_2 = 5.0V, Temp = -30 ºC to 85 ºC, NR10M00			-70	dBc

5G NR n77 Rx Characteristics

Test conditions unless otherwise specified: V_{DD_LNA} = +1.2 V, V_{BATT} = +3.8 V, Temp. = 25 °C, PA disabled.

Performance referenced to module pin location.

Parameter	Conditions	Gain State	Product Spec.			Units
			Min.	Typ.	Max.	
Frequency			3300	-	4200	MHz
Gain		**Range 0 / Range 1**				
RF Gain	Range 0 / Range 1	NA / G0		18.3		dB
		G0 / G1		16.5		
		G1 /NA		13		
		G2 / G2		10.7		
		G3 / NA		7.5		
		G4 / G3		5.3		
		G5 / NA		1.2		
		G6 / G4		-1.0		
		G7 / NA		-3.8		
		NA / G5		-6.4		
		NA / G7		-12.7		
Current Consumption		**Range 0 / Range 1**				
Drain Current	Range 0 / Range 1	NA / G0		12		mA
		G0 / G1		9		
		G1 /NA		6		
		G2 / G2		4.5		
		G3 / NA		4.5		
		G4 / G3		2.5		
		G5 / NA		2.5		
		G6 / G4		2.5		
		G7 / NA		0.001		
		NA / G5		0.001		
		NA / G7		0.001		

5G NR n77 Rx Characteristics - continued

Test conditions unless otherwise specified: V_{DD_LNA} = +1.2 V, V_{BATT} = +3.8 V, Temp. = 25 °C, PA disabled.

Performance referenced to module pin location.

Parameter	Conditions	Gain State	Product Spec.			Units
			Min.	Typ.	Max.	
Frequency			3300	-	4200	MHz
Noise Figure		**Range 0 / Range 1**				
Noise Figure	Range 0 / Range 1	NA / G0		2.4		dB
		G0 / G1		2.4		
		G1 /NA		2.5		
		G2 / G2		2.6		
		G3 / NA		2.8		
		G4 / G3		3.6		
		G5 / NA		4.6		
		G6 / G4		5.3		
		G7 / NA		3.4		
		NA / G5		6.3		
		NA / G7		10		
Impedance						
Input Return Loss		All Gain States		-13		dB
Output Return Loss		All Gain States		-11.5		
Isolation						
Reverse Isolation (1/|S12|^2)	RX OUT to ANT	Gain state 0 (G0)		-40		dB
Linearity		**Range 0 / Range 1**				
IIP3 dBm	Range 0 / Range 1	NA / G0		-6		dBm
		G0 / G1		-3.5		
		G1 /NA		-2		
		G2 / G2		1		
		G3 / NA		1.5		
		G4 / G3		5		
		G5 / NA		5.5		
		G6 / G4		5.5		
		G7 / NA		20		
		NA / G5		20		
		NA / G7		20		

5G NR n77 Rx Characteristics - continued

Test conditions unless otherwise specified: V_{DD_LNA} = +1.2 V, V_{BATT} = +3.8 V, Temp. = 25 °C, PA disabled.

Performance referenced to module pin location.

Parameter	Conditions	Gain State	Product Spec.			Units
			Min.	Typ.	Max.	
Frequency			3300	-	4200	MHz
Timing						
LNA Enable/ Disable Time	All Gain states, within 0.1dB				5	µs
LNA Gain Switching Time	To 90% of final value, adjacent active states only.				1	
Out of Band Attenuation						
1M-Low Frequency	1~702	Range0, G0		-73		dB
LB Tx	703~862	Range0, G0		-74		
B26/B8 Rx	869~960	Range0, G0		-73		
L2	1164~1250	Range0, G0		-67		
B11/B21	1427~1511	Range0, G0		-63		
GPS/GNSS	1559~1606	Range0, G0		-62		
B3/66 Tx	1710~1785	Range0, G0		-64		
Other MB bands Tx (only Tx freq)	1785~1980	Range0, G0		-65		
Other MB bands Rx (only Tx freq)	1805~2170	Range0, G0		-68		
2.4 GHz ISM	2400~2483	Range0, G0		-35		
B7 Tx	2500~2570	Range0, G0		-23		
B7 Rx	2496~2690	Range0, G0		-15		
OOB block (LB above 3.3GHz)	2690~2800	Range0, G0		-1		
OOB block (LB/B7 DC)	2800~3215	Range0, G0		9		
OOB block (LB under 4.2GHz)	4250~5045	Range0, G0		8		
5 GHz ISM	4900~5950	Range0, G0		-26		
Minimum rejection between harmonics	5950~12500	Range0, G0		-32		

5G NR n78 Tx Characteristics

Test conditions unless otherwise specified: V_{CC1} = V_{CC3} = 5.0V, V_{BATT} = +3.8 V, Temp. = 25 °C. Performance referenced to module pin location.

Parameter	Conditions	Product Spec.			Units
		Min.	Typ.	Max.	
Frequency		3300	-	3800	MHz
Output Power					
CW Output Power	P2dB, Vcc_1 = Vcc_2 = 5.0V		32		dBm
APT Linear Output Power	HPM, Vcc_1 = Vcc_2 ≤ 5.0V, Prated PC2	29.5			
	HPM, Vcc_1 = Vcc_2 ≤ 5.0V, Prated PC3	26.5			
	LPM, Vcc_1 = Vcc_2 = 2.5V	1.5			
Gain					
Gain (G)	P2dB, Vcc_1 = Vcc_2 = 5.0V		30		dB
	APT HPM, Vcc_1 = Vcc_2 ≤ 5.0V, Pout ≤ Prated PC2		33		
	APT HPM, Vcc_1 = Vcc_2 ≤ 5.0V, Pout ≤ Prated PC3		33		
	APT LPM, Vcc_1 = Vcc_2 = 2.5V		12		
Linearity					
Adjacent Channel Leakage Power Ratio (ACLR)	APT HPM, $EUTRA_{ACLR}$		-38		dBc
	APT LPM, $EUTRA_{ACLR}$, Pout = 1.5 dBm		-42		
EVM	APT HPM, NR100M65		1.8		%
Current & Efficiency					
Quiescent Current	Vbatt = 3.8V, Vcc_1 = Vcc_2 = 5.0V		315		mA
	Vbatt = 3.8V, Vcc_1 = Vcc_2 = 2.5V		14		
Current Consumption Total Current (I_{cc1} + I_{cc3} + I_{batt})	HPM, Vcc_1 = Vcc_2 ≤ 5.0V, Pout = Prated PC2		890		
	HPM, Vcc_1 = Vcc_2 ≤ 5.0V, Pout = Prated PC3		700		
	LPM, Vcc_1 = Vcc_2 ≤ 2.5V, Pout = 1.5dBm		12		
Ibatt	HPM		6		
PAE	HPM, Vcc_1 = Vcc_2 ≤ 5.0V, Pout = Prated PC2		19.5		%
	HPM, Vcc_1 = Vcc_2 ≤ 5.0V, Pout = Prated PC3		12.5		
HARMONICS					
2nd Harmonic	HPM, Pout ≤ Prated PC2, NR10M00		-40		dBm
3 rd Harmonic			-50		
4 th Harmonic			-35		
5 th Harmonic			-48		
Out of Band Gain					
GPS Band Gain	1574 – 1577 MHz		-46		dB
ISM Gain	2400 - 2481 MHz		-7		
VSWR					
Input VSWR	All Modes			3:1	-
Ouput VSWR				3:1	
STABILITY					
Spurious Levels	APT HPM, All Loads ≤ 6:1, in-band, all angles, closed loop to maintain Prated, Vbatt = 3.8V, Vcc_1 = Vcc_2 = 5.0V, Temp = -30 ºC to 85 ºC, NR10M00			-70	dBc

5G NR n78 Rx Characteristics

Test conditions unless otherwise specified: V_{DD_LNA} = +1.2 V, V_{BATT} = +3.8 V, Temp. = 25 °C, PA disabled.

Performance referenced to module pin location.

Parameter	Conditions	Gain State	Product Spec.			Units
			Min.	Typ.	Max.	
Frequency			3300	-	3800	MHz
Gain		**Range 0 / Range 1**				
RF Gain	Range 0 / Range 1	NA / G0		18.1		dB
		G0 / G1		16.5		
		G1 /NA		13		
		G2 / G2		10.5		
		G3 / NA		7.3		
		G4 / G3		5.0		
		G5 / NA		1.2		
		G6 / G4		-1.0		
		G7 / NA		-3.7		
		NA / G5		-6.4		
		NA / G7		-12.7		
Current Consumption		**Range 0 / Range 1**				
Drain Current	Range 0 / Range 1	NA / G0		12		mA
		G0 / G1		9		
		G1 /NA		6		
		G2 / G2		4.5		
		G3 / NA		4.5		
		G4 / G3		2.5		
		G5 / NA		2.5		
		G6 / G4		2.5		
		G7 / NA		0.001		
		NA / G5		0.001		
		NA / G7		0.001		

5G NR n78 Rx Characteristics - continued

Test conditions unless otherwise specified: V_{DD_LNA} = +1.2 V, V_{BATT} = +3.8 V, Temp. = 25 °C, PA disabled.

Performance referenced to module pin location.

Parameter	Conditions	Gain State	Product Spec.			Units
			Min.	Typ.	Max.	
Frequency			3300	-	3800	MHz
Noise Figure		**Range 0 / Range 1**				
Noise Figure	Range 0 / Range 1	NA / G0		2.4		dB
		G0 / G1		2.4		
		G1 /NA		2.5		
		G2 / G2		2.6		
		G3 / NA		2.8		
		G4 / G3		3.5		
		G5 / NA		4.5		
		G6 / G4		5.2		
		G7 / NA		3.3		
		NA / G5		6.2		
		NA / G7		10		
Impedance						
Input Return Loss		All Gain States		-13		dB
Output Return Loss		All Gain States		-11.5		
Isolation						
Reverse Isolation (1/|S12|^2)	RX OUT to ANT	Gain state 0 (G0)		-40		dB
Linearity		**Range 0 / Range 1**				
IIP3 dBm	Range 0 / Range 1	NA / G0		-6		dBm
		G0 / G1		-3.5		
		G1 /NA		-2		
		G2 / G2		1		
		G3 / NA		1.5		
		G4 / G3		5		
		G5 / NA		5.5		
		G6 / G4		5.5		
		G7 / NA		20		
		NA / G5		20		
		NA / G7		20		

5G NR n78 Rx Characteristics - continued

Test conditions unless otherwise specified: V_{DD_LNA} = +1.2 V, V_{BATT} = +3.8 V, Temp. = 25 °C, PA disabled.

Performance referenced to module pin location.

Parameter	Conditions	Gain State	Product Spec.			Units
			Min.	Typ.	Max.	
Frequency			3300	-	3800	MHz
Noise Figure						
Timing						
LNA Enable/ Disable Time	All Gain states, within 0.1dB				5	µs
LNA Gain Switching Time	To 90% of final value, adjacent active states only.				1	
Out of Band Attenuation						
1M-Low Frequency	1~702	Range0, G0		-73		dB
LB Tx	703~862	Range0, G0		-74		
B26/B8 Rx	869~960	Range0, G0		-73		
L2	1164~1250	Range0, G0		-67		
B11/B21	1427~1511	Range0, G0		-63		
GPS/GNSS	1559~1606	Range0, G0		-62		
B3/66 Tx	1710~1785	Range0, G0		-64		
Other MB bands Tx (only Tx freq)	1785~1980	Range0, G0		-65		
Other MB bands Rx (only Tx freq)	1805~2170	Range0, G0		-68		
2.4 GHz ISM	2400~2483	Range0, G0		-35		
B7 Tx	2500~2570	Range0, G0		-23		
B7 Rx	2496~2690	Range0, G0		-15		
OOB block (LB above 3.3GHz)	2690~2800	Range0, G0		-1		
OOB block (LB/B7 DC)	2800~3215	Range0, G0		9		
OOB block (LB under 4.2GHz)	4250~5045	Range0, G0		8		
5 GHz ISM	4900~5950	Range0, G0		-26		
Minimum rejection between harmonics	5950~12500	Range0, G0		-32		

5G NR n77/78 Coupler Characteristics

Test conditions unless otherwise specified: V_{CC1} = V_{CC2} = 5.0V, VBATT = +3.8 V, Temp. = 25 °C. PA = HPM

Performance referenced to module pin location.

Parameter	Conditions	Coupler	Product Spec.			Units
		Mode	Min.	Typ.	Max.	
Frequency			3300	-	4200	MHz
Coupling Factor						
Forward Coupling Factor	CPLR switch in FWD mode, PA in HPM	FWD		25		dB
Reverse Coupling Factor	CPLR switch in RVS mode, PA in HPM	RVS		23		
Directivity						
Forward Directivity	CPLR switch in FWD mode, PA in HPM	FWD		24		dB
Reverse Directivity	CPLR switch in RVS mode, PA in HPM	RVS		15		dB
Insertion Loss						
Daisy-chain Coupler Insertion Loss	CPL to CPL_OUT	Daisy-chain Mode		1		dB
Timing						
Switch time between FWD and RVS	CPLR switch transition from FWD to RVS or RVS to FWD mode, PA in HPM	FWD <-> RVS			3	µs

PA_CTRL Register, Address 0x01 (RFFE1)

Data Bits	Qorvo Bit Field Name	Default	Description	BSID/GSID Support	Trigger Support	Mask Write Support	R/W
Reg01[7:3]	reserved	5b00000	reserved	Yes	T0	No	R/W
Reg01[2]	PA_ENABLE	1b0	PA Enable 0: PA disabled 1: PA enabled	Yes	T0	No	R/W
Reg01[1]	PA_POWERMODE	1b0	Power Mode 0: High Power 1: Low Power (OR'd with Reg04[2])	Yes	T0	No	R/W
Reg01[0]	PA_OPMODE	1b0	PA Operation Mode 0: Iso mode [ET] (VCC cap switched diasbled) 1: Bypass mode [APT] (VCC cap switched enabled) (OR'd with Reg05[0])	Yes	T0	No	R/W

PA_BIAS1 Register, Address 0x02 (RFFE1)

Data Bits	Qorvo Bit Field Name	Default	Description	BSID/GSID Support	Trigger Support	Mask Write Support	R/W
Reg02[7:4]	DAC_FS_RES[3:0]	4b0000	Bias PA Final Stage Resistor Linearly scales bias current for given output stage voltage set in DAC_FS_HPM. Higher values increase current. Note: In LPM, DAC_FS_READ and DAC_DS_READ are combined into an 8-bit resistor value. The maximum value for the combined fields of DAC_DS_RES and DAC_FS_RES is 221 (bias current may clip above this)	Yes	T0	No	R/W
Reg02[3:0]	DAC_DS_RES[3:0]	4b0000	Bias Driver Stage Resistor Linearly scales bias current for given driver stage voltage set in DAC_DS_HPM and DAC_DS_LPM. Higher values increase current.	Yes	T0	No	R/W

CPLR_CTRL Register, Address 0x03 (RFFE1)

Data Bits	Qorvo Bit Field Name	Default	Description	BSID/GSID Support	Trigger Support	Mask Write Support	R/W
Reg03[7:4]	Reserved	5b00000	Reserved	Yes	T2	No	R/W
Reg03[3:3]	CPLR_FREQ	1b0	Coupler Frequency Select 0: Low frequency range (LR), optimized for n78 1: Full frequency range (FR) Coupler frequency select when CPLR_SEL=2b01	Yes	T2	No	R/W
Reg03[2:1]	CPLR_SEL[1:0]	2b00	Coupler Output Select 00: Coupler off 01: Coupler selected 10: reserved 11: Alt Coupler selected (CPLR_IN connected to CPLR, "daisy chain mode")	Yes	T2	No	R/W
Reg03[0]	CPLR_DIR	1b0	Coupler Direction 0: Forward direction 1: Reverse direction	Yes	T2	No	R/W

TX_RX_CTRL1 Register, Address 0x04 (RFFE1)

Data Bits	Qorvo Bit Field Name	Default	Description	BSID/GSID Support	Trigger Support	Mask Write Support	R/W
Reg04[7:3]	Reserved	5b00000	Reserved	Yes	T1	No	R/W
Reg04[2]	PA_POWERMODE_ALT	1b0	Alternate Power Mode Control 0: High Power 1: Low Power (OR'd with Reg01[1])	Yes	T1	No	R/W
Reg04[1:0]	TX_RX[1:0]	2b00	TX_RX_Select (also acts as PA enable) 00: TX_RX_Off 01: TX (also enables PA , if PA_ENABLE is set too) 10: RX 11: Reserved (equal 00)	Yes	T1	No	R/W

PA_MODE_CTRL Register, Address 0x05 (RFFE1)

Data Bits	Qorvo Bit Field Name	Default	Description	BSID/GSID Support	Trigger Support	Mask Write Support	R/W
Reg05[7:1]	Reserved	7b0000000	Reserved	Yes	T0	No	R/W
Reg05[0]	PA_OPMODE_ALT	2b00	PA Operation Mode Alternative 0: ET mode (VCC bypass cap disabled) 1: APT mode (VCC bypass cap enabled) (OR'd with Reg01[0])	Yes	T0	No	R/W

PA_BIAS2 Register, Address 0x06 (RFFE1)

Data Bits	Qorvo Bit Field Name	Default	Description	BSID/GSID Support	Trigger Support	Mask Write Support	R/W
Reg06[7:6]	DAC_DS_RES_HPM_STEPS[1:0]	2b10	Resistor step size for HPM driver Stage	Yes	No	No	R/W
Reg06[5:0]	DAC_DS_HPM[5:0]	6b010010	DAC Voltage for HPM driver stage 16 mV steps from 2.212 V to 3.220 V 0x00: 2.212V 0x01: 2.228V … 0x3F: 3.220V	Yes	No	No	R/W

PA_BIAS3 Register, Address 0x07 (RFFE1)

Data Bits	Qorvo Bit Field Name	Default	Description	BSID/GSID Support	Trigger Support	Mask Write Support	R/W
Reg07[7:6]	DAC_FS_RES_HPM_STEPS[1:0]	2b11	Resistor step size for HPM final Stage	Yes	No	No	R/W
Reg07[5:0]	DAC_FS_HPM[5:0]	6b010010	DAC Voltage for HPM final stage 16 mV steps from 2.212 V to 3.220 V 0x00: 2.212V 0x01: 2.228V … 0x3F: 3.220V	Yes	No	No	R/W

PA_BIAS4 Register, Address 0x08 (RFFE1)

Data Bits	Qorvo Bit Field Name	Default	Description	BSID/GSID Support	Trigger Support	Mask Write Support	R/W
Reg08[7:6]	Reserved	2b00	Reserved	Yes	No	No	R/W
Reg08[5:0]	DAC_DS_LPM[5:0]	6b010010	DAC Voltage for LPM (single stage architecture) 16 mV steps from 2.212V to 3.220V 0x00: 2.212V 0x01: 2.228V … 0x3F: 3.220V	Yes	No	No	R/W

PM_TRIG Register, Address 0x1C (RFFE1)

Data Bits	Qorvo Bit Field Name	Default	Description	BSID/GSID Support	Trigger Support	Mask Write Support	R/W
Reg28[7]	PWR_MODE	1b1	0: Normal operation (ACTIVE) 1: Secondary mode (LOW POWER)	Yes	No	No	R/W
Reg28[6]	PWR_STATE	1b0	0: Normal operation 1: initialization state Note - this bit always reads 0. Writing a 1 to this bit forces a reset.	Yes	No	No	R/W
Reg28[5:3]	TriggerMask[2:0]	3b000	Setting these bits to '1' will cause the corresponding triggers to be masked (disabled), and RFFE writes to corresponding registers will change configuration immediately (no trigger command necessary). TriggerMask[2] = TriggerMask_2, TriggerMask[1] = TriggerMask_1, & TriggerMask[0] = TriggerMask_0	No	No	No	R/W
Reg28[2:0]	Trigger[2:0]	3b000	Setting these bits to '1' will cause the registers associated with that trigger to be loaded with the contents of its corresponding shadow register. Trigger[2] = Trigger_2, Trigger[1] = Trigger_1, and Trigger[0] = Trigger_0	Yes	No	No	R/W

PRODUCT_ID Register, Address 0x1D (RFFE1)

Data Bits	Qorvo Bit Field Name	Default	Description	BSID/GSID Support	Trigger Support	Mask Write Support	R/W
Reg29[7:0]	PRODUCT_ID[7:0]	8b00110000	This is a read-only register. However, during the programming of the USID a write command sequence is performed on this register, even though the write does not change its value.	No	No	No	R

MAN_ID Register, Address 0x1E (RFFE1)

Data Bits	Qorvo Bit Field Name	Default	Description	BSID/GSID Support	Trigger Support	Mask Write Support	R/W
Reg30[7:0]	MANUFACTURER_ID_LSB [7:0]	8b11000110	This is a read-only register. However, during the programming of the USID, a write command sequence is performed on this register, even though the write does not change its value. Note: This is the lower 8 least significant bits of the RFFE's MANUFACTURER_ID. MANUFACTURER_ID[7:0]=MANUFACTURER_ID_LSB[7:0]	No	No	No	R

MAN_US_ID Register, Address 0x1F (RFFE1)

Data Bits	Qorvo Bit Field Name	Default	Description	BSID/GSID Support	Trigger Support	Mask Write Support	R/W
Reg31[7:4]	MANUFACTURER_ID_MSB [3:0]	4b0011	These bits are read-only. However, during the programming of the USID, a write command sequence is performed on this register even though the write does not change its value. Note: This is the up 4 most significant bits of the RFFE's MANUFACTURER_ID. MANUFACTURER_ID[11:8] =MANUFACTURER_ID_MSB[3:0]	No	No	No	R
Reg31[3:0]	USID[3:0]	4b111x	Programmable USID. Performing a write to this register using the described programming sequences will program the USID in devices supporting this feature. These bits store the USID of the device. Note – LSB (x) of default USID is set by USID hardware pin (pulled to VIO -> LSB = 1, pulled to GND -> LSB = 0).	No	No	No	RM

EXT_PRODUCT_ID Register, Address 0x20 (RFFE1)

Data Bits	Qorvo Bit Field Name	Default	Description	BSID/GSID Support	Trigger Support	Mask Write Support	R/W
Reg32[7:0]	EXT_PRODUCT_ID[7:0]	8b00000000	This is a read-only register. However, during the programming of the USID a write command sequence is performed on this register, even though the write does not change its value.	No	No	No	RM

REVISION_ID Register, Address 0x21 (RFFE1)

Data Bits	Qorvo Bit Field Name	Default	Description	BSID/GSID Support	Trigger Support	Mask Write Support	R/W
Reg33[7:0]	REVISION_ID[7:0]	8b00000000	This is an RFFE2 register to contain information about the revision of this module. The intent here is to use this as a type of scratch register -- to contain various information or serialization.	No	No	No	RM

GROUP_ID2 Register, Address 0x22 (RFFE1)

Data Bits	Qorvo Bit Field Name	Default	Description	BSID/GSID Support	Trigger Support	Mask Write Support	R/W
Reg34[7:4]	GSID0_2[3:0]	4b0000	Group slave ID 0 There is only 1 register for GSID0 & GSID1, but this register can be accessed from either Reg27 or Reg34. This means that write to Reg34 will reflect in Reg27 also, and vice versa	No	No	No	R/W
Reg34[3:0]	GSID1_2[3:0]	4b0000	Group slave ID 1 There is only 1 register for GSID0 & GSID1, but this register can be accessed from either Reg27 or Reg34. This means that write to Reg34 will reflect in Reg27 also, and vice versa	No	No	No	R/W

UDR_RST (RFFE_STATUS2) Register, Address 0x23 (RFFE1)

Data Bits	Qorvo Bit Field Name	Default	Description	BSID/GSID Support	Trigger Support	Mask Write Support	R/W
Reg35[7]	SW_RESET_2	1b0	0: Normal operation 1: Software reset (reset of all configurable registers to default values, except for USID)	No	No	No	R/W
Reg35[6:0]	Reserved	7b0000000	Reserved	No	No	No	R/W

ERR_SUM (RFFE_STATUS3) Register, Address 0x24 (RFFE1)

Data Bits	Qorvo Bit Field Name	Default	Description	BSID/GSID Support	Trigger Support	Mask Write Support	R/W
Reg36[7]	Reserved	1b0	Reserved	No	No	No	R
Reg36[6]	CMD_FRAME_P_ERR_2	1b0	Command sequence received with parity error – discard command	No	No	No	R
Reg36[5]	CMD_LEN_ERR_2	1b0	Command length error	No	No	No	R
Reg36[4]	ADDR_FRAME_P_ERR_2	1b0	Address frame parity error	No	No	No	R
Reg36[3]	DATA_FRAME_P_ERR_2	1b0	Data frame with parity error	No	No	No	R
Reg36[2]	READ_UNUSED_REG_2	1b0	Read command to an invalid address	No	No	No	R
Reg36[1]	WRITE_UNUSED_REG_2	1b0	Write command to an invalid address	No	No	No	R
Reg36[0]	BID_GID_ERR_2	1b0	Read command with a Broadcast_ID or GROUP_ID	No	No	No	R

BUS_LOAD Register, Address 0x2B (RFFE1)

Data Bits	Qorvo Bit Field Name	Default	Description	BSID/GSID Support	Trigger Support	Mask Write Support	R/W
Reg43[7:4]	Reserved	4b0000	Reserved	No	No	No	R/W
Reg43[3:0]	BUS_LOAD[3:0]	4b0100	SDATA Driver strength in Readback Mode 0x0: 10pf 0x1: 20pf 0x2: 30pf 0x3: 40pf 0x4: 50pf 0x5: 60pf 0x6: 80pf 0x7: 100pf 0x8: 120pf 0x9: 140pf 0xA: 160pf 0xB: 180pf 0xC: 200pf 0xD: 250pf 0xE-0xF: reserved	No	No	No	R/W

GAIN_RANGE_SELECT Register, Address 0x00 (RFFE2)

Data Bits	Qorvo Bit Field Name	Default	Description	BSID/GSID Support	Trigger Support	Mask Write Support	R/W
Reg00[7:1]	reserved	7b0000000	reserved	No	No	No	R/W
Reg00[0]	GAIN_RANGE_SELECT	1b0	LNA Gain range select 0: Range0 LNA gain modes 1: Range1 LNA gain modes Selects LNA gain ranges defined in Reg01[2:0]	No	No	Yes	R/W

LNA_CTRL0 Register, Address 0x01 (RFFE2)

Data Bits	Qorvo Bit Field Name	Default	Description	BSID/GSID Support	Trigger Support	Mask Write Support	R/W
Reg01[7]	TRIGGER_BYPASS	1b0	Trigger Bypass 0: disabled 1: enabled When set to 1 during a write to Reg01, the write will occur as though the mT-A trigger was not enabled. This bit will always read back as 0.	No	No	Yes	R/W
Reg01[6]	LNA_ENABLE	1b0	LNA Enable 0: LNA disabled 1: LNA enabled (OR'd with Reg02[0])	No	mT-A	Yes	R/W
Reg01[5:3]	LNA_BIAS_CS[2:0]	3b000	LNA CS Bias Current 000: LNA_Bias0 (lowest, 0A) 001: LNA_Bias1 010: LNA_Bias2 011: LNA_Bias3 100: LNA_Bias4 101: LNA_Bias5 (normal) 110: LNA_Bias6 111: LNA_Bias7 (highest)	No	mT-A	Yes	R/W
Reg01[2:0]	LNA_GAIN[2:0]	3b000	Selects the LNA module gain Range0 Range1 000: G0 (max) 17.5dB, 19.5dB 001: G1 14.5dB, 17.5dB 010: G2 11.5dB, 11.5dB 011: G3 8.5dB, 5.5dB 100: G4 5.5dB, -0.5dB (passive) 101: G5 2.5dB, -6.5dB (passive) 110: G6 -0.5dB (passive) -9.5dB (passive) 111: G7 -3.5dB (passive) -12.5dB (passive)	No	mT-A	Yes	R/W

LNA_CTRL1 Register, Address 0x02 (RFFE2)

Data Bits	Qorvo Bit Field Name	Default	Description	BSID/GSID Support	Trigger Support	Mask Write Support	R/W
Reg02[7:1]	Reserved	7b0000000	Reserved	No	No	Yes	R/W
Reg02[0]	LNA_EN	1b0	LNA Enable 0: LNA disabled 1: LNA enabled (OR'd with Reg01[6])	No	T1	Yes	R/W

LNA_CTRL3 Register, Address 0x03 (RFFE2)

Data Bits	Qorvo Bit Field Name	Default	Description	BSID/GSID Support	Trigger Support	Mask Write Support	R/W
Reg03[7:3]	Reserved	5b00000	Reserved	No	No	Yes	R/W
Reg03[2:0]	LNA_BIAS_CG[2:0]	3b110	LNA CG Current 000: LNA_Bias_CG0 (lowest, 0A) 001: LNA_Bias_CG1 010: LNA_Bias_CG2 011: LNA_Bias_CG3 100: LNA_Bias_CG4 101: LNA_Bias_CG5 (normal) 110: LNA_Bias_CG6 111: LNA_Bias_CG7 (highest)	No	mT-A	Yes	R/W

CTRIGCFG1 Register, Address 0x16 (RFFE2)

Data Bits	Qorvo Bit Field Name	Default	Description	BSID/GSID Support	Trigger Support	Mask Write Support	R/W
Reg22[7:4]	Reserved	4b0000	Reserved	No	N/A	No	R/W
Reg22[3:0]	MTRIG_A[3:0]	4b0000	Assigns the trigger used by the mT-A register set. 0000: Extended Trigger ET3 0001: Extended Trigger ET4 0010: Extended Trigger ET5 0011: Extended Trigger ET6 0100: Extended Trigger ET7 0101: Extended Trigger ET8 0110: Extended Trigger ET9 0111: Extended Trigger ET10 1000 - 1111: no trigger (trigger is masked)	No	N/A	Yes	R/W

PM_TRIG Register, Address 0x1C (RFFE2)

Data Bits	Qorvo Bit Field Name	Default	Description	BSID/GSID Support	Trigger Support	Mask Write Support	R/W
Reg28[7]	PWR_MODE	1b1	0: Normal operation (ACTIVE) 1: Secondary mode (LOW POWER)	Yes	No	No	R/W
Reg28[6]	PWR_STATE	1b0	0: Normal operation 1: initialization state Note - this bit always reads 0. Writing a 1 to this bit forces a reset.	Yes	No	No	R/W
Reg28[5:3]	TriggerMask[2:0]	3b000	Setting these bits to '1' will cause the corresponding triggers to be masked (disabled), and RFFE writes to corresponding registers will change configuration immediately (no trigger command necessary). TriggerMask[2] = TriggerMask_2, TriggerMask[1] = TriggerMask_1, & TriggerMask[0] = TriggerMask_0	No	No	No	R/W
Reg28[2:0]	Trigger[2:0]	3b000	Setting these bits to '1' will cause the registers associated with that trigger to be loaded with the contents of its corresponding shadow register. Trigger[2] = Trigger_2, Trigger[1] = Trigger_1, and Trigger[0] = Trigger_0	Yes	No	No	R/W

PRODUCT_ID Register, Address 0x1D (RFFE2)

Data Bits	Qorvo Bit Field Name	Default	Description	BSID/GSID Support	Trigger Support	Mask Write Support	R/W
Reg29[7:0]	PRODUCT_ID[7:0]	8b00110001	This is a read-only register. However, during the programming of the USID a write command sequence is performed on this register, even though the write does not change its value.	No	No	No	RM

MAN_ID Register, Address 0x1E (RFFE2)

Data Bits	Qorvo Bit Field Name	Default	Description	BSID/GSID Support	Trigger Support	Mask Write Support	R/W
Reg30[7:0]	MANUFACTURER_ID_LSB [7:0]	8b11000110	This is a read-only register. However, during the programming of the USID, a write command sequence is performed on this register, even though the write does not change its value. Note: This is the lower 8 least significant bits of the RFFE's MANUFACTURER_ID (i.e. MANUFACTURER_ID[7:0] = MANUFACTURER_ID_LSB[7:0]	No	No	No	R

MAN_US_ID Register, Address 0x1F (RFFE2)

Data Bits	Qorvo Bit Field Name	Default	Description	BSID/GSID Support	Trigger Support	Mask Write Support	R/W
Reg31[7:4]	MANUFACTURER_ID_MSB [3:0]	4b0011	These bits are read-only. However, during the programming of the USID, a write command sequence is performed on this register even though the write does not change its value. Note: This is the up 4 most significant bits of the RFFE's MANUFACTURER_ID. MANUFACTURER_ID[11:8] = MANUFACTURER_ID_MSB[3:0]	No	No	No	R
Reg31[3:0]	USID[3:0]	4b001x	Programmable USID. Performing a write to this register using the described programming sequences will program the USID in devices supporting this feature. These bits store the USID of the device. Note – LSB (x) of default USID is set by USID hardware pin (pulled to VIO -> LSB = 1, pulled to GND -> LSB = 0).	No	No	No	RM

EXT_TRIGGER_MASK Register, Address 0x2D (RFFE2)

Data Bits	Qorvo Bit Field Name	Default	Description	BSID/GSID Support	Trigger Support	Mask Write Support	R/W
Reg45[7:0]	EXT_TRIGGER_MASK[7:0]	8b00000000	Setting these bits to '1' will cause the corresponding triggers to be masked (disabled), and RFFE writes to corresponding registers will change configuration immediately (no trigger command necessary). Ext_Trigger_Mask[7] = TriggerMask_10 ... Ext_Trigger_Mask[0] = TriggerMask_3 Note: if the part is in LPM and a write to this register changes the masks, the change to the masks takes effect.	No	No	No	R/W

EXT_TRIGGER Register, Address 0x2E (RFFE2)

Data Bits	Qorvo Bit Field Name	Default	Description	BSID/GSID Support	Trigger Support	Mask Write Support	R/W
Reg46[7:0]	EXT_TRIGGER[7:0]	8b00000000	Setting these bits to '1' will cause the registers associated with that trigger to be loaded with the contents of its corresponding shadow register. Ext_Trigger[7] = Trigger_10 ... Ext_Trigger[0] = Trigger_3 Note: if the part is in LPM and a write to this register changes the triggers, the change to the triggers is ignored.	Yes	No	No	R/W

EXT_TRIG_CNT_3[L|H] Register, Address 0x38 (RFFE2)

Data Bits	Qorvo Bit Field Name	Default	Description	BSID/GSID Support	Trigger Support	Mask Write Support	R/W
Reg56[7:0]	EXT_TRIG_CNT_3[7:0]	8b00000000	Ext Trig programmable countdown Counter Reg 3.	Yes	No	No	R/W

EXT_TRIG_CNT_4[L|H] Register, Address 0x39 (RFFE2)

Data Bits	Qorvo Bit Field Name	Default	Description	BSID/GSID Support	Trigger Support	Mask Write Support	R/W
Reg57[7:0]	EXT_TRIG_CNT_4[7:0]	8b00000000	Ext Trig programmable countdown Counter Reg 4.	Yes	No	No	R/W

EXT_TRIG_CNT_5[L|H] Register, Address 0x3A (RFFE2)

Data Bits	Qorvo Bit Field Name	Default	Description	BSID/GSID Support	Trigger Support	Mask Write Support	R/W
Reg58[7:0]	EXT_TRIG_CNT_5[7:0]	8b00000000	Ext Trig programmable countdown Counter Reg 5.	Yes	No	No	R/W

EXT_TRIG_CNT_6[L|H] Register, Address 0x3B (RFFE2)

Data Bits	Qorvo Bit Field Name	Default	Description	BSID/GSID Support	Trigger Support	Mask Write Support	R/W
Reg59[7:0]	EXT_TRIG_CNT_6[7:0]	8b00000000	Ext Trig programmable countdown Counter Reg 6.	Yes	No	No	R/W

EXT_TRIG_CNT_7[L|H] Register, Address 0x3C (RFFE2)

Data Bits	Qorvo Bit Field Name	Default	Description	BSID/GSID Support	Trigger Support	Mask Write Support	R/W
Reg60[7:0]	EXT_TRIG_CNT_7[7:0]	8b00000000	Ext Trig programmable countdown Counter Reg 7.	Yes	No	No	R/W

EXT_TRIG_CNT_8[L|H] Register, Address 0x3D (RFFE2)

Data Bits	Qorvo Bit Field Name	Default	Description	BSID/GSID Support	Trigger Support	Mask Write Support	R/W
Reg61[7:0]	EXT_TRIG_CNT_8[7:0]	8b00000000	Ext Trig programmable countdown Counter Reg 8.	Yes	No	No	R/W

EXT_TRIG_CNT_9[L|H] Register, Address 0x3E (RFFE2)

Data Bits	Qorvo Bit Field Name	Default	Description	BSID/GSID Support	Trigger Support	Mask Write Support	R/W
Reg62[7:0]	EXT_TRIG_CNT_9[7:0]	8b00000000	Ext Trig programmable countdown Counter Reg 9.	Yes	No	No	R/W

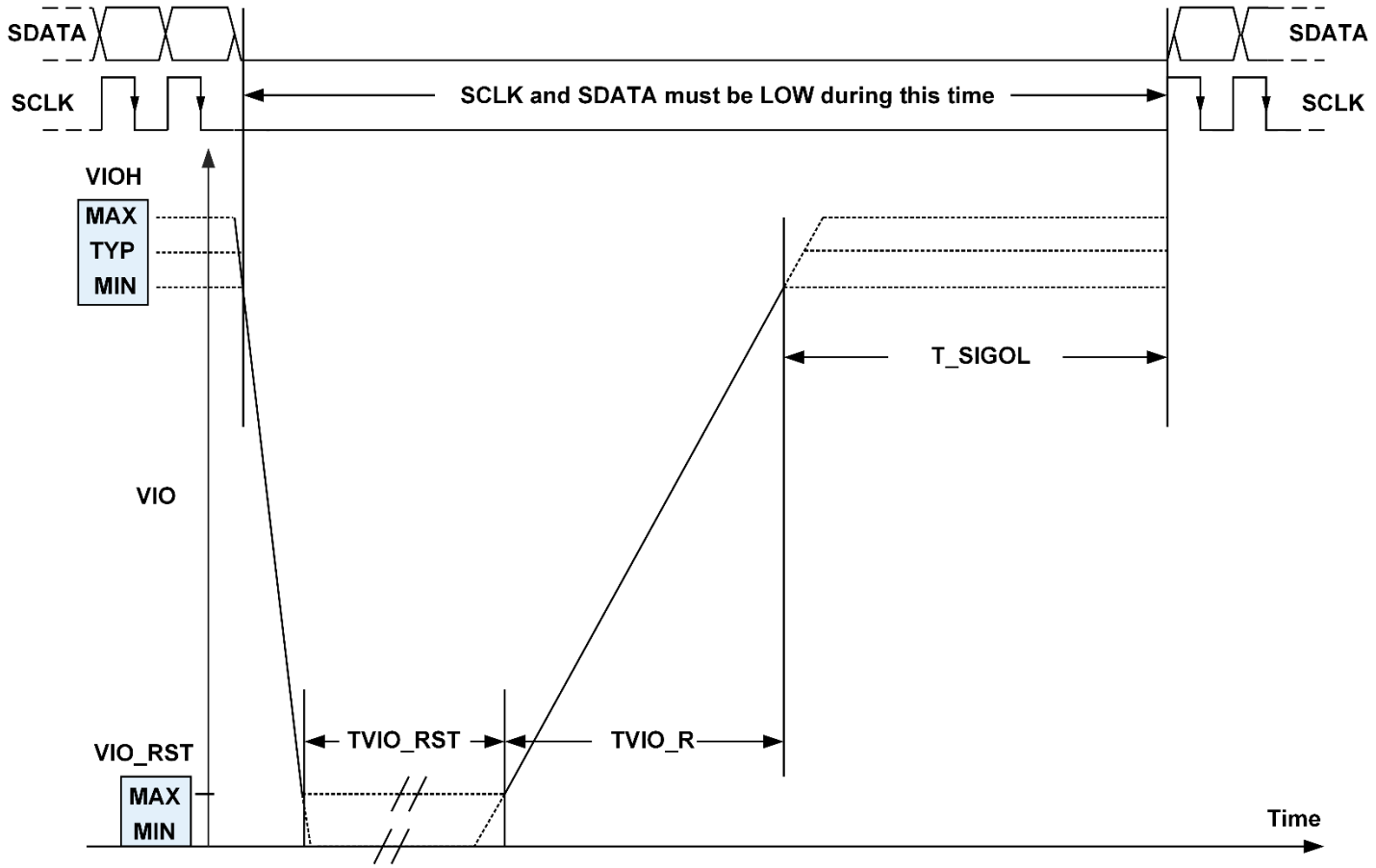
EXT_TRIG_CNT_10[L|H] Register, Address 0x3F (RFFE2)

Data Bits	Qorvo Bit Field Name	Default	Description	BSID/GSID Support	Trigger Support	Mask Write Support	R/W
Reg63[7:0]	EXT_TRIG_CNT_10[7:0]	8b00000000	Ext Trig programmable countdown Counter Reg 10.	Yes	No	No	R/W

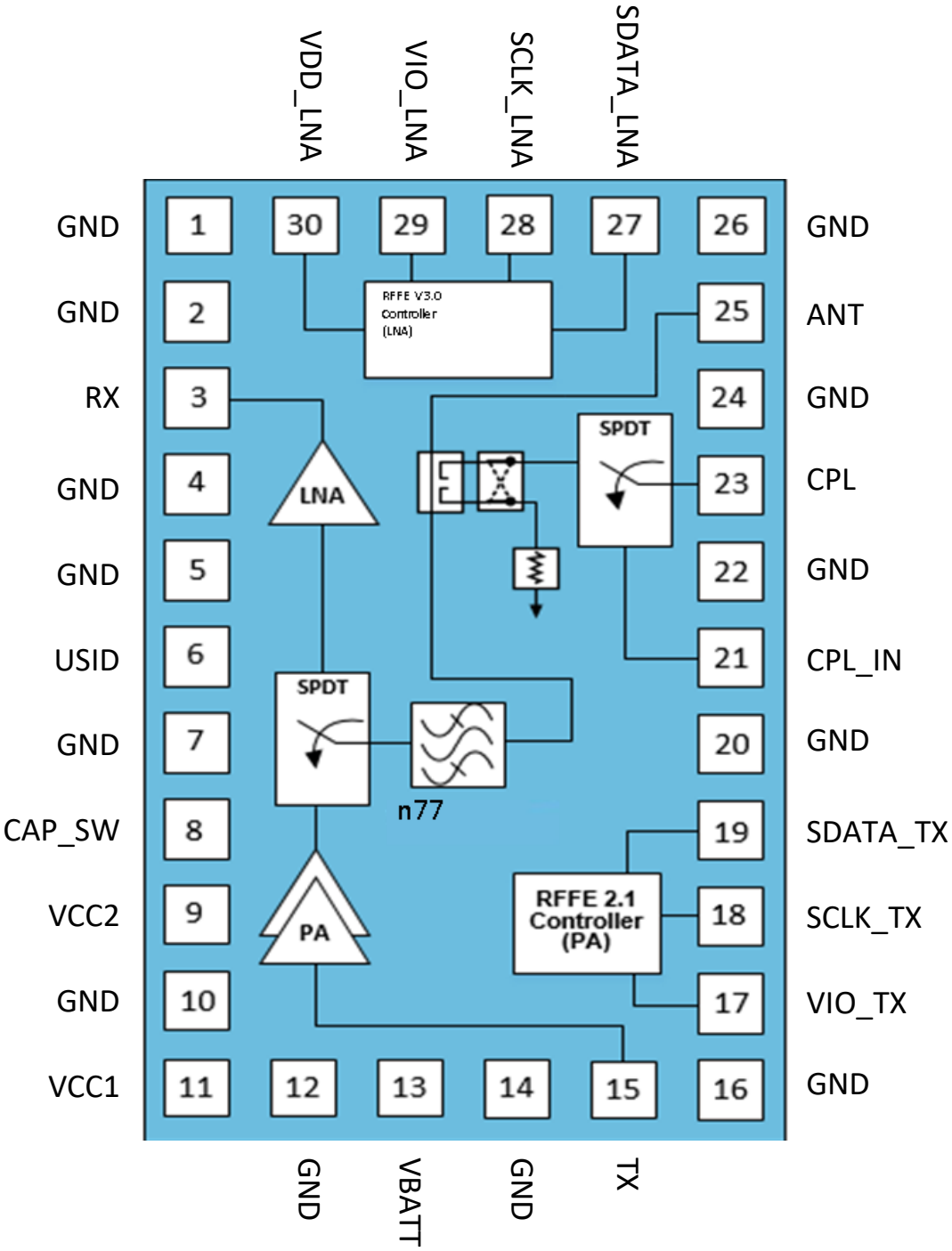
VIO Power On Reset (POR) Timing

For applications where MIPI RFEE VIO is turned ON/OFF in accordance with MIPI RFEE bus activity, the timing recommendations below should be used to ensure error-free RFEE register writes following VIO power on reset (POR)

Parameter	Description	MIN	TYP	MAX
VIOH	VIO High Voltage	1.65V	1.80V	1.95V
VIO_RST	VIO Reset Voltage	0V	0V	0.45V
TVIO_RST	VIO Reset Time	10µs	-	-
TVIO_RST	VIO Rise Time	1µs	-	400µs
T_SIGOL	Minimum Wait Time after TVIO_R	190µs	-	-



Pin Configuration and Description

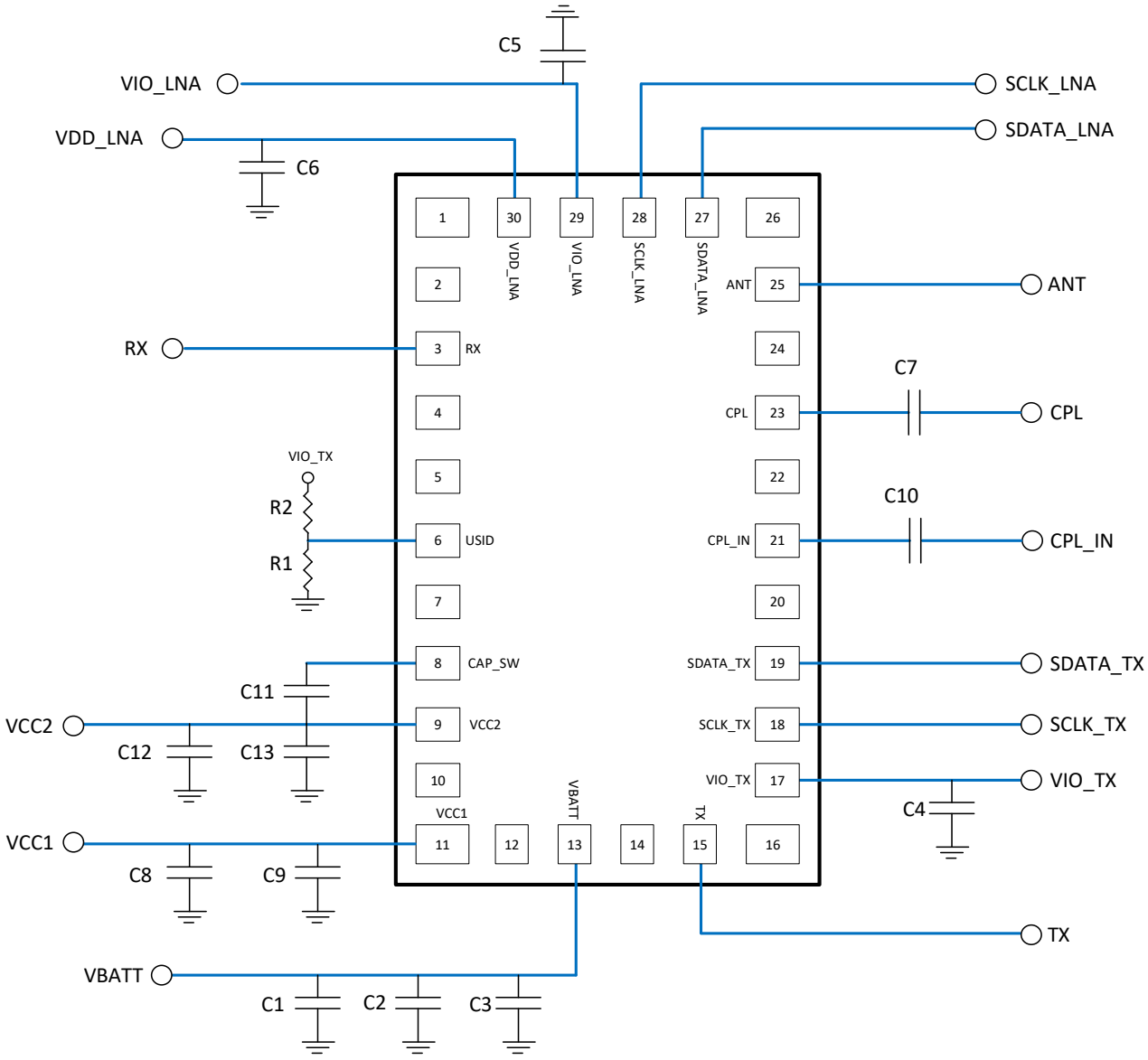


Top View (looking through device)

Pin Configuration and Description (continued)

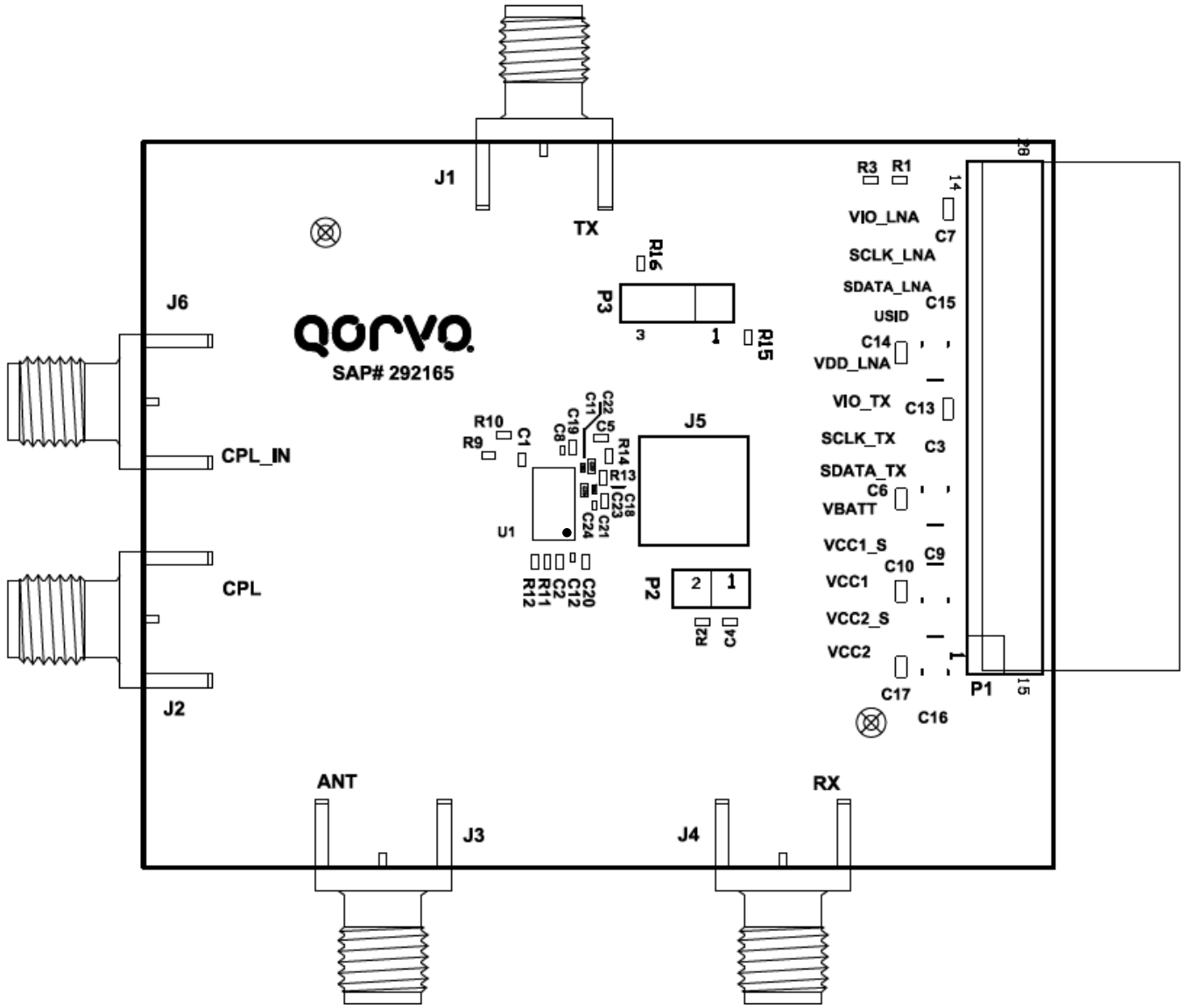
PIN NUMBER	LABEL	DESCRIPTION
1	GND	Ground
2	GND	Ground
3	RX	RX Output
4	GND	Ground
5	GND	Ground
6	USID	User ID
7	GND	Ground
8	CAP_SW	Switch VCC bypass capacitor to GND
9	VCC2	Supply voltage for 2nd stage PA
10	GND	Ground
11	VCC1	Supply voltage for 1st stage PA
12	GND	Ground
13	VBATT	Battery supply voltage
14	GND	Ground
15	TX	PA RF Input
16	GND	Ground
17	VIO_Tx	Supply voltage for PA MIPI RFFE interface
18	SCLK_Tx	Clock signal for PA MIPI RFFE interface
19	SDATA_Tx	Data signal for PA MIPI RFFE interface
20	GND	Ground
21	CPL_IN	Coupler Input Port
22	GND	Ground
23	CPL	Coupler Output Port
24	GND	Ground
25	ANT	Antenna Port
26	GND	Ground
27	SDATA_LNA	Data signal for LNA MIPI RFFE interface
28	SCLCK_LNA	Clock signal for LNA MIPI RFFE interface
29	VIO_LNA	Supply voltage for LNA MIPI RFFE interface
30	VDD_LNA	Supply voltage for LNA

Application Schematic

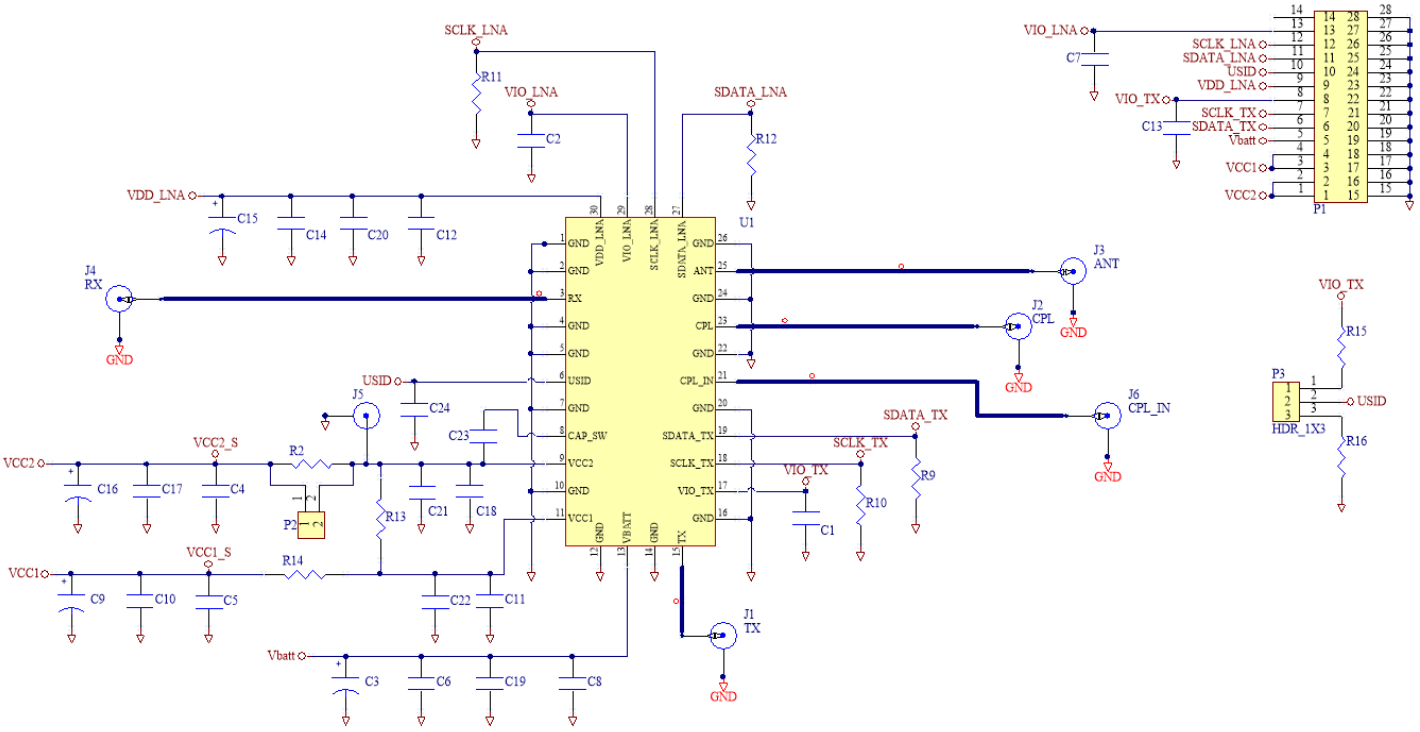


REF. DES	RECOMMENDED VALUE	PURPOSE
C1	4.7 uF	Bypass
C2, C8, C12	220 nF	Bypass
C3, C4, C5, C9, C13	100 pF	Bypass
C6	1 uF	Bypass
C7, C10	18 pF	DC block
C11	220 nF	Vcc2 switchable bypass cap
R1	TBD or NC	Pull-down resistor (NC if R2 is used)
R2	TBD or NC	Pull-up resistor (NC if R1 is used)
Note: Either R1 or R2 must be populated.		

Evaluation Board Layout



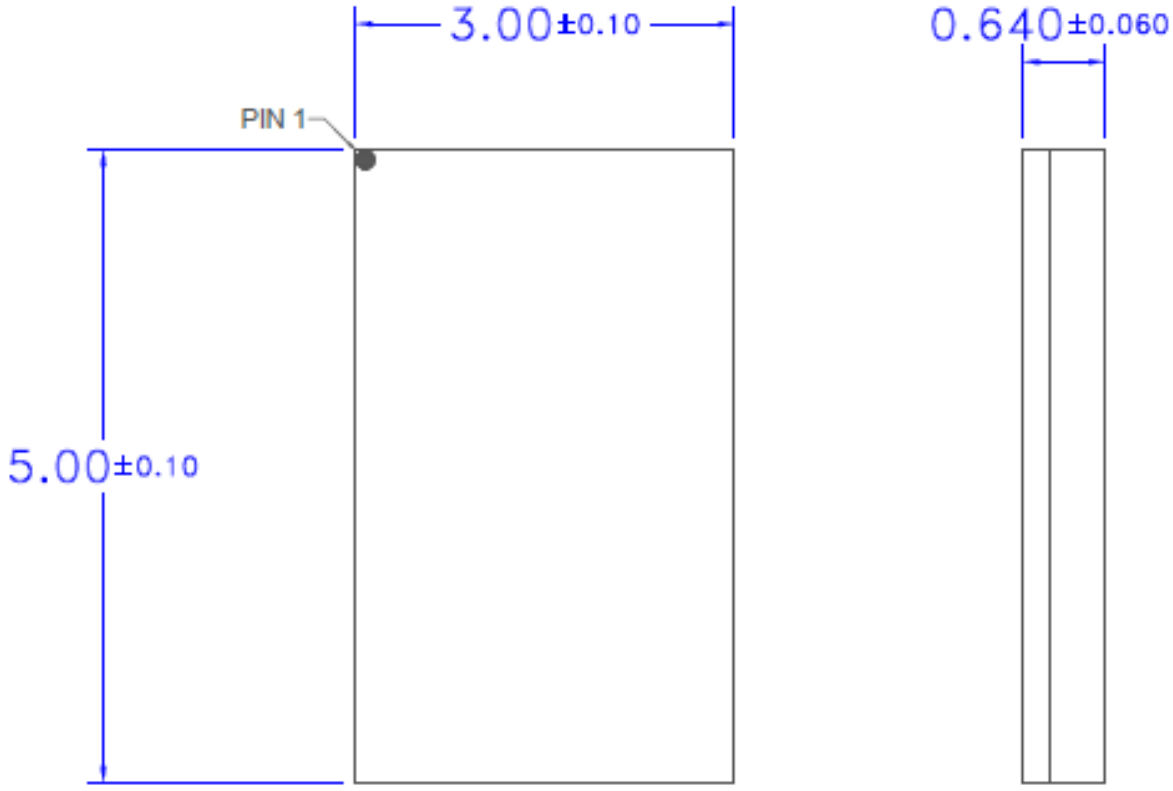
Evaluation Board Schematic



Evaluation Board Bill of Materials (BOM)

Quantity	Part designator	Description	Manufacturer	Manufacturer P/N
2	C1, C2	CAP, 100pF, 5%, 50V, C0G, 0402	TAIYO YUDEN (SINGAPORE) PTE LTD	RM UMK105 CG101JV-F
2	C11, C18	CAP, 100pF, 10%, 25V, X5R, 0201	Qorvo	CAP1216
4	C3, C9, C15, C16	CAP, 22uF, 10%, 10V, TANT-A	AVX Asia Limited	TAJA226K010RNJ
4	C4, C5, C19, C20	CAP, 0.1uF, 10%, 35V, X5R, 0402	TAIYO YUDEN (SINGAPORE) PTE LTD	GMK105BJ104KV-F
6	C6, C7, C10, C13, C14, C17	CAP, 4.7uF, 10%, 16V, X5R, 0603	TDK SINGAPORE (PTE) LTD	C1608X5R1C475K080AC
2	C8, C12	CAP, 1000pF, 10%, 50V, X7R, 0201	MURATA ELECTRONICS SINGAPORE PTE LT	GRM033R71H102KA12D
3	C21, C22, C23	Cap, 0.22uF, 10%, 16V, X5R, 0402	TAIYO YUDEN (SINGAPORE) PTE LTD	EMK105BJ224KV-F
1	C24	CAP, 39pF, 5%, 25V, C0G, 0201	Qorvo	CAP1211
1	U1	QM78207	Qorvo	
5	J1, J2, J3, J4, J6	CONN, SMA, END LAUNCH, JACK, 50 OHM, PCB	Amphenol RF	901-10044-6RFX
1	J5	CONN, SMB, ST PLUG REC, T/H	Aliner Industries, Inc.	21-003B0-T
1	P1	CONN, HDR, RT ANG, 28-PIN, 0.100"	MOLEX	90122-0774
1	P2	CONN, HDR, ST, 2-PIN, 0.100"	SAMTEC INC.	TSW-102-07-G-S
1	P3	CONN, HDR, ST, 3-PIN, 0.100"	SAMTEC INC.	TSW-103-07-G-S
1		PCB	TTM TECHNOLOGIES INC	QM78207-4000(1)
4	R1, R14, R15, R16	RES, 0 OHM, 5%, 1/10W, 0402	Kamaya, Inc	RMC1/16SJPTH
7	R2, R3, R9, R10, R11, R12, R13	RES, 0 OHM, 5%, 1/10W, 0402 (DNI)	Kamaya, Inc	RMC1/16SJPTH

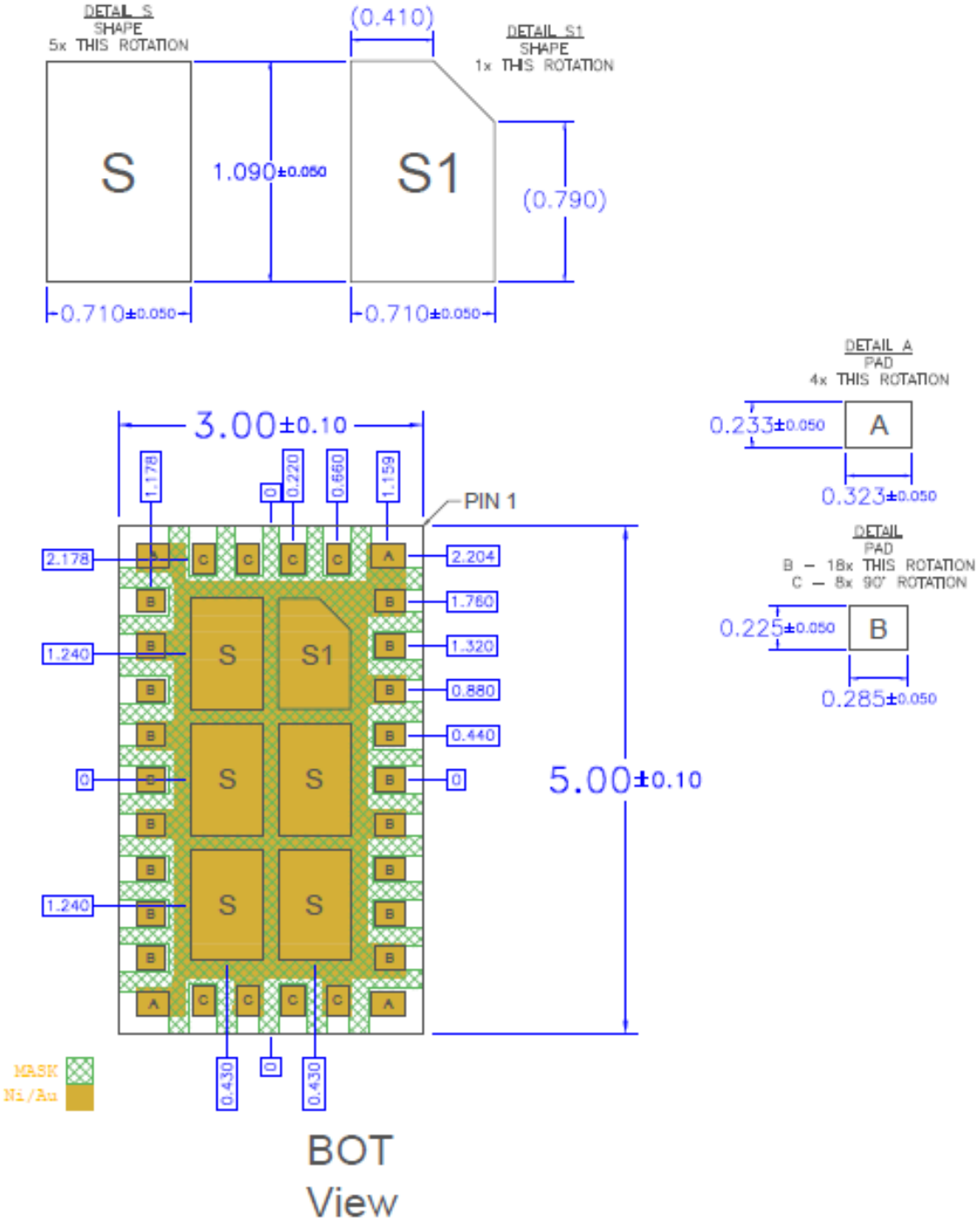
Mechanical Information – Package Dimensions



Notes:

1. All dimensions are in mm. Angles are in degrees.
2. Dimension and tolerance formats conform to ASME Y14.4M-1994.
3. The terminal #1 identifier and terminal numbering conform to JESD 95-1 SPP-012

Mechanical Information – Package Dimensions



Notes:

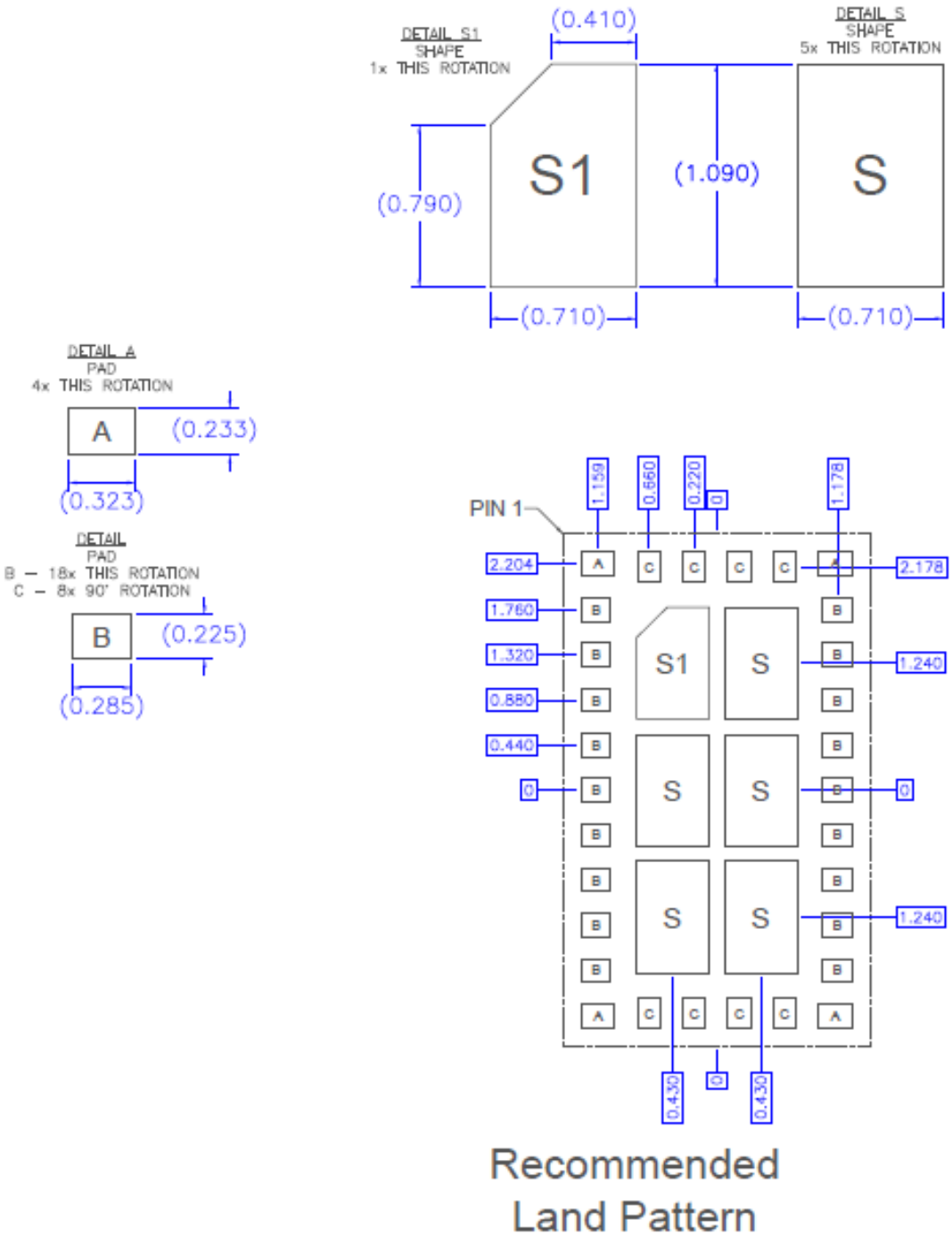
1. All dimensions are in mm. Angles are in degrees.
2. Dimension and tolerance formats conform to ASME Y14.4M-1994.
3. The terminal #1 identifier and terminal numbering conform to JESD 95-1 SPP-012

Mechanical Information – Package Marking

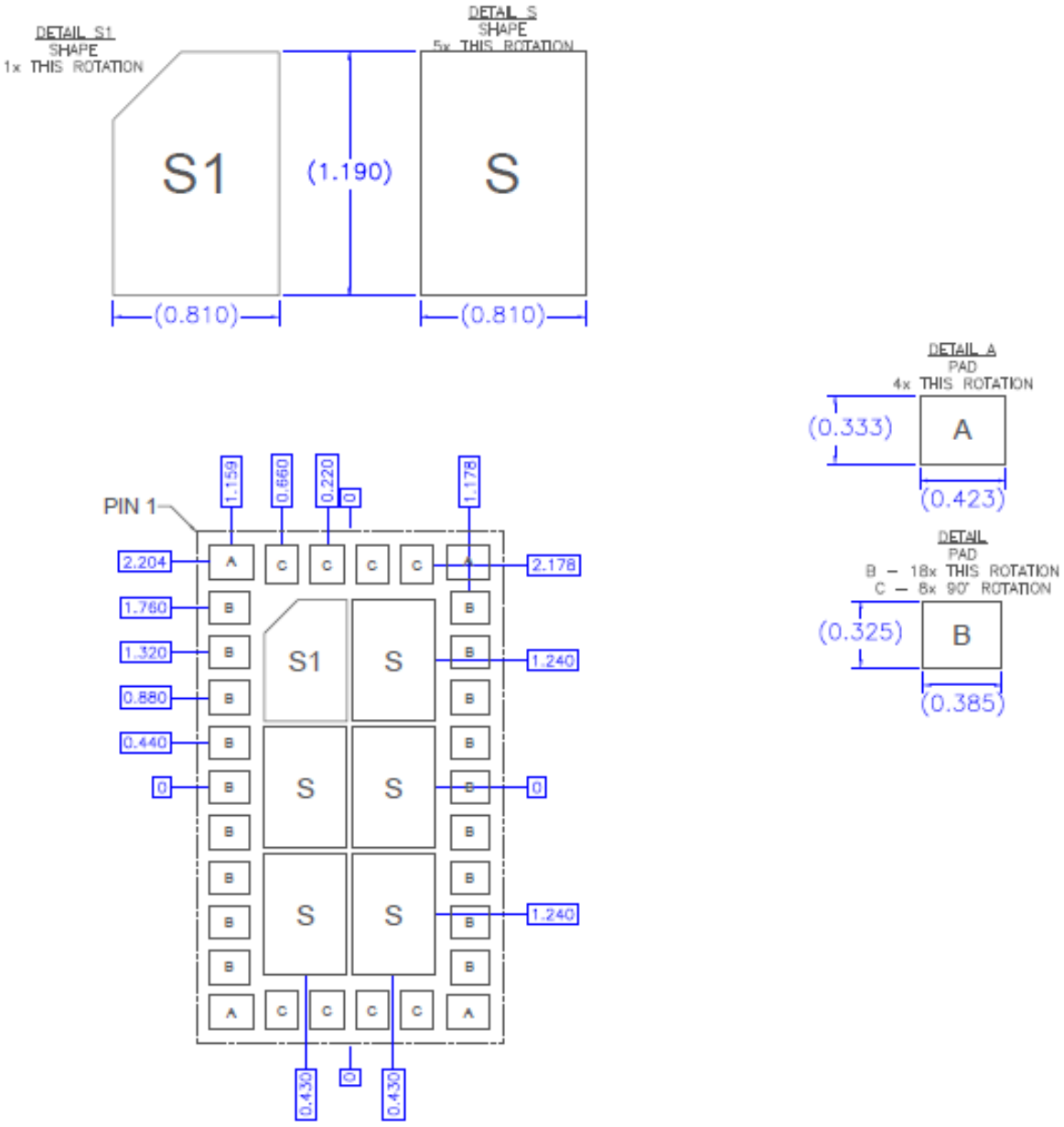
Package Marking and Dimensions

Marking: Part number –QM78207

Mechanical Information – Recommended Land Pattern



Mechanical Information – Recommended Land Pattern Mask



Handling Precautions

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	Class 1C	ESDA/JEDEC JS-001-2012
ESD – Charged Device Model (CDM)	Class C3	JEDEC JESD22-C101F
MSL – Moisture Sensitivity Level	MSL3	IPC/JEDEC J-STD-020

Caution!

ESD sensitive device

Solderability

Compatible with both lead-free (260 °C max. reflow temperature) and tin/lead (245 °C max. reflow temperature) soldering processes.

Package lead plating: Electrolytic plated Au over Ni

RoHS Compliance

This part is compliant with the 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment), as amended by Directive 2015/863/EU.

This product also has the following attributes:

- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
- SVHC Free

REVISION HISTORY

REVISION	DATE	DESCRIPTION
A	2020-04-28	Initial Release
B	2020-07-10	Updated typicals
C	2020-08-04	Updated specs, ordering information changes

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

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Email: customer.support@qorvo.com

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