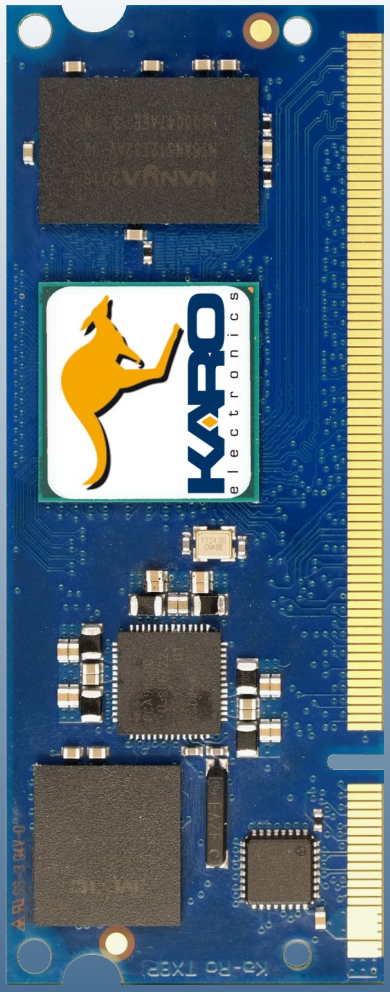
TX8P

TX Family Computer On Module

- Processor 1.6 GHz Quad ARM® Cortex®-A53 based NXP i.MX 8M Plus
- RAM 2 GB LPDDR4 SDRAM
- ROM 8 GB eMMC
- Power supply 3.3V to 5V
- Size 26 mm SO-DIMM
- Grade Industrial
- Temperature -30°C to 85°C



Quad Cortex®-A53

Key Features

- Quad ARM® Cortex®-A53
- Display support:
  - Display interfaces: LVDS, MIPI-DSI, HDMI 2.0a
  - GC520L 2D GPU
  - GC7000UL 3D GPU
  - 1080p60 video de-/encode
- Vision and Machine Learning
  - Camera interfaces: 2x MIPI-CSI (4-lane each)
  - Dual Camera ISP (2x HD/1x 12MP) HDR, dewarp
  - Machine Learning Accelerator: 2.3 TOPS
  - Tensilica® HiFi4 DSP up to 800 MHz

Connectivity

- 2x Ethernet
  - 10/100 Ethernet with PHY
  - Gb Ethernet with IEEE®1588, AVB, TSN
- 2x USB (1x USB 3.0, 1x USB 2.0)
- 4x UART, 4x I²C, 3x SPI, 2x CAN-FD, 1x eMMC/SD
- 1x PCIe® Gen 3, 1-lane
- 3.3V I/O

OS Support

- Linux

Ka-Ro electronics GmbH - Pascalstr. 22, D-52076 Aachen, Germany - Tel.: +49 2408 1402-0 (FAX -10)
www.karo-electronics.de

i.MX 8M Plus

i.MX 8M Plus applications processors excel in machine learning, vision, advanced multimedia and industrial IoT applications. Elevating edge intelligence, i.MX 8M Plus processors are the solid foundation for smart homes to smart cities, Industry 4.0 and beyond.

Neural Processing Unit (NPU)

The i.MX 8M Plus is a powerful quad-core Arm® Cortex®-A53 applications processor running at up to 1.8 GHz with an integrated neural processing unit (NPU) delivering up to 2.3 TOPS. As the first i.MX processor with a machine learning accelerator, the i.MX 8M Plus processor delivers substantially higher performance for ML inference at the edge. Using its integrated NPU, the i.MX 8M Plus processor simultaneously detects multiple highly complex neural network functions, including human pose and emotion detection, multi-object surveillance, and the recognition of over 40,000 English words. Moving ML inference to the edge removes cloud dependency and preserves individual privacy while providing a superior user experience.

Image Signal Processor (ISP)

An intelligent vision system based on the i.MX 8M Plus ISP and camera interfaces with resolution up to 12 MP is capable of an input rate of up to 375 MP/s and acts as the eyes of the i.MX 8M Plus. The integrated ISP brings real-time image processing to high-definition video and performs algorithms that extract the maximum image details in high-contrast scenes. A de-warp engine performs fisheye lens correction reversing the effects of wide-angle lens distortion. It also corrects distortions from low-cost lenses and ensures high image quality.

TX Computer on Module

- NXP i.MX 8M Plus Quad
- 2GB LPDDR4 SDRAM
- 8GB eMMC
- DIMM200-module (67,6mm x 26 mm x 4mm)

Standard TXCOM pinout:

Highly scalable design options allow a single platform to cover multiple products. Pin-compatible TX modules allow a single PCB as a platform for different features as product needs dictate.

- 4-wire UARTs (x3)
- I2C / PWM
- Serial Audio Interface
- 4-wire SD-Card/SDIO

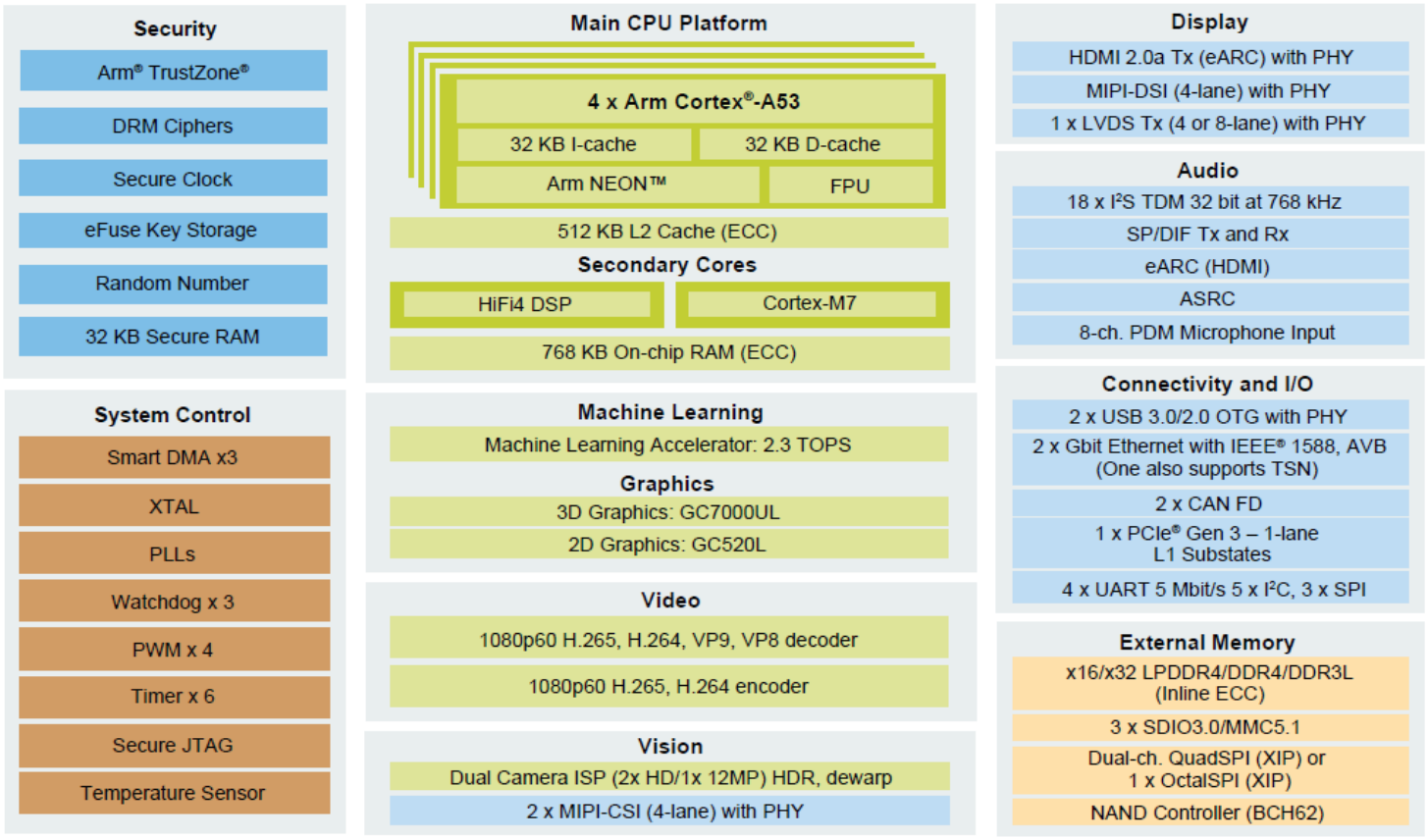
High-Speed communication interfaces incl. onboard Ethernet PHY / on-chip USB PHY allows direct use of connectors/magnetics on the baseboard without the need for additional logic:

- 10/100 Mbps Ethernet
- USB 2.0 OTG (Host or Device)
- USB 3.0 Host

Read more in our TX-Guide:

www.karo-electronics.com/tx-guide

i.MX 8M Plus Block Diagram



Ordering Information

Order Number	CPU	SDRAM	Flash	
TX8P/ML8C/2GS/8GF/E85	1.6 GHz i.MX 8M Plus Quad	2GB	8GB	

2024-02-26

PINOUT

PIN	Type	TX Standard	i.MX8M Plus Pad Name	Alternate functions	GPIO	Description (refer to i.MX8M Plus manuals for details)
POWER SUPPLY & RESET						
1-4	power	VIN				Module power supply input.
5-7, 9-12	power	VOUT				3.3V power supply output. Supplied by Buck 4
8	3V3	BOOTMODE				Boot mode select H: Boot from eMMC / L: Boot from UART/USB
13	Not connected					
14						
15	3V3	#RESET_OUT	SD2_RESET_B	SRC_SYSTEM_RESET	GPIO2[19]	#RESET_OUT may be used to reset peripherals on the carrier board. This signal can be controlled by a GPIO function during runtime.
16	1V8	#POR		Connected to PMIC_RST_B	10K-PU to 1V8	PMIC reset input pin. It is internally pulled up with LDO1 power rail. Once it is asserted low, PMIC performs reset.
17	1V8	#RESET_IN	POR_B		10K-PU to 1V8	Also connected to PMIC POR_B
18	GND	GND				
Ethernet						
19	analog	ETN_TXN				Transmit Data Negative: 100Base-TX or 10Base-T differential transmit output to magnetics.
20	3V3	#ETN_LED2				Active low - output is driven active when the operating speed is 100Mbps. This LED will go inactive when the operating speed is 10Mbps or during line isolation.
21	analog	ETN_TXP				Transmit Data Positive: 100Base-TX or 10Base-T differential transmit output to magnetics.
22	power	ETN_3V3				+3.3V analog power supply output to magnetics
23	analog	ETN_RXN				Receive Data Negative: 100Base-TX or 10Base-T differential receive input from magnetics.
24	3V3	#ETN_LED1				Active low - output is driven active whenever the device detects a valid link, and blinks indicating activity.
25	analog	ETN_RXP				Receive Data Positive: 100Base-TX or 10Base-T differential receive input from magnetics.
26	GND	GND				
USB-HOST						
27	3V3	USBH_VBUSEN	GPIO1_IO14	USB2_OTG_PWR, USDHC3_CD_B PWM3_OUT, CCM_CLKO1	GPIO1[14] 10K-PU	Active high VBUS supply enable. This pin can be used to enable a VBUS power supply switch.
28	3V3	#USBH_OC	GPIO1_IO15	USB2_OTG_OC, USDHC3_WP PWM4_OUT, CCM_CLKO2	GPIO1[15] 10K-PU	Active low over-current indicator input
29	analog	USBH_DM	USB2_DN			D- pin of the USB cable
30	5V	USBH_VBUS	USB2_VBUS			USB supply voltage input. 4K7 / 10K voltage divider is used to drive USB2_VBUS@3.3V
31	analog	USBH_DP	USB2_DP			D+ pin of the USB cable
32	GND	GND				
USB-OTG						
33	3V3	USBOTG_ID	USB1_DNU	Not available - do not use		
34	3V3	USBOTG_VBUSEN	GPIO1_IO12	USB1_OTG_PWR AUDIOMIX_EXT_EVENT[1]	GPIO1[12] 10K-PU	Active high VBUS supply enable. This pin can be used to enable a VBUS power supply switch.
35	analog	USBOTG_DM	USB1_DN			D- pin of the USB cable
36	3V3	#USBOTG_OC	GPIO1_IO13	USB1_OTG_OC PWM2_OUT	GPIO1[13] 10K-PU	Active low over-current indicator input connected to a GPIO.
37	analog	USBOTG_DP	USB1_DP			D+ pin of the USB cable
38	5V	USBOTG_VBUS	USB1_VBUS			USB supply voltage input. 4K7 / 10K voltage divider is used to drive USB1_VBUS@3.3V
39	GND	GND				
I2C						
40	3V3	I2C_DATA	I2C2_SDA	ENET_QOS_1588_EVENT1_OUT USDHC3_WP, ECSPI1_SS0	GPIO5[17]	I2C Data
41	3V3	I2C_CLK	I2C2_SCL	ENET_QOS_1588_EVENT1_IN USDHC3_CD_B, ECSPI1_MISO ENET_QOS_1588_EVENT1_AUX_IN	GPIO5[16]	I2C Clock
PWM						
42	3V3	PWM	GPIO1_IO01	PWM1_OUT, CCM_EXT_CLK2 ISP_SHUTTER_TRIG_0	GPIO1[1]	PWM Output

PIN	Type	TX Standard	i.MX8M Plus Pad Name	Alternate functions	GPIO	Description (refer to i.MX8M Plus manuals for details)
43	LDO5*)		SAI1_RXD3	AUDIOMIX_SAI1_RX_DATA[3] AUDIOMIX_SAI5_RX_DATA[3] AUDIOMIX_BIT_STREAM[3] ENET1_MDIO	GPIO4[5]	
CSPI – Configurable Serial Peripheral Interface						
44	3V3	CSPI_SS	ECSPI1_SS0	UART3_RTS_B I2C2_SDA AUDIOMIX_SAI7_TX_SYNC	GPIO5[9]	Slave Select (Selectable polarity) signal
45	LDO5*)	CSPI_SS	SAI1_RXD2	AUDIOMIX_SAI1_RX_DATA[2] AUDIOMIX_SAI5_RX_DATA[2] AUDIOMIX_BIT_STREAM[2] ENET1_MDC	GPIO4[4]	Slave Select (Selectable polarity) signal
46	3V3	CSPI_MOSI	ECSPI1_MOSI	UART3_TX I2C1_SDA AUDIOMIX_SAI7_RX_BCLK	GPIO5[7]	Master Out/Slave In signal
47	3V3	CSPI_MISO	ECSPI1_MISO	UART3_CTS_B I2C2_SCL AUDIOMIX_SAI7_RX_DATA[0]	GPIO5[8]	Master In/Slave Out signal
48	3V3	CSPI_SCLK	ECSPI1_SCLK	UART3_RX I2C1_SCL AUDIOMIX_SAI7_RX_SYNC	GPIO5[6]	Serial Clock signal
49	3V3	CSPI_RDY	ECSPI2_SCLK	UART4_RX I2C3_SCL AUDIOMIX_SAI7_TX_BCLK	GPIO5[10]	
50	GND	GND				
1st SD – Secure Digital Interface						
51	3V3	SD1_CD	SD2_CD_B	USDHC2_CD_B	GPIO2[12]	SD Card Detect
52	3V3	SD1_D[0]	SD2_DATA0	USDHC2_DATA0 I2C4_SDA UART2_RX AUDIOMIX_BIT_STREAM[0]	GPIO2[15]	
53	3V3	SD1_D[1]	SD2_DATA1	USDHC2_DATA1 I2C4_SCL UART2_TX AUDIOMIX_BIT_STREAM[1]	GPIO2[16]	
54	3V3	SD1_D[2]	SD2_DATA2	USDHC2_DATA2 ECSPI2_SS0 AUDIOMIX_SPDIF_OUT AUDIOMIX_BIT_STREAM[2]	GPIO2[17]	
55	3V3	SD1_D[3]	SD2_DATA3	USDHC2_DATA3 ECSPI2_MISO AUDIOMIX_SPDIF_IN AUDIOMIX_BIT_STREAM[3] SRC_EARLY_RESET	GPIO2[18]	
56	3V3	SD1_CMD	SD2_CMD	USDHC2_CMD ECSPI2_MOSI UART4_TX AUDIOMIX_CLK	GPIO2[14]	SD Command bidirectional signal
57	3V3	SD1_CLK	SD2_CLK	USDHC2_CLK ECSPI2_SCLK UART4_RX	GPIO2[13]	SD Output Clock.
58	GND	GND				
1st UART						
59	3V3	TXD	UART1_TXD	ECSPI3_MOSI	GPIO5[23]	Application UART 1 Transmit Data output signal
60	3V3	RXD	UART1_RXD	ECSPI3_SCLK	GPIO5[22]	Application UART 1 Receive Data input signal
61	3V3	RTS	UART3_TXD	UART1_RTS_B USDHC3_VSELECT GPT1_CLK CAN2_RX	GPIO5[27]	Application UART 1 Request to Send **input** signal
62	3V3	CTS	UART3_RXD	UART1_CTS_B USDHC3_RESET_B GPT1_CAPTURE2 CAN2_TX	GPIO5[26]	Application UART 1 Clear to Send **output** signal
2nd UART						
63	3V3	TXD	UART2_TXD	ECSPI3_SS0 GPT1_COMPARE2	GPIO5[25]	Application UART 2 Transmit Data output signal
64	3V3	RXD	UART2_RXD	ECSPI3_MISO GPT1_COMPARE3	GPIO5[24]	Application UART 2 Receive Data input signal

PIN	Type	TX Standard	i.MX8M Plus Pad Name	Alternate functions	GPIO	Description (refer to i.MX8M Plus manuals for details)
65	3V3	RTS	SAI3_RXD	AUDIOMIX_SAI3_RX_DATA[0] AUDIOMIX_SAI2_RX_DATA[3] AUDIOMIX_SAI5_RX_DATA[0] UART2_RTS_B AUDIOMIX_BIT_STREAM[1]	GPIO4[30]	Application UART 2 Request to Send **input** signal
66	3V3	CTS	SAI3_RXC	AUDIOMIX_SAI3_RX_BCLK AUDIOMIX_SAI2_RX_DATA[2] AUDIOMIX_SAI5_RX_BCLK GPT1_CLK UART2_CTS_B AUDIOMIX_CLK	GPIO4[29]	Application UART 2 Clear to Send **output** signal
3rd UART						
67	3V3	TXD	UART4_TXD	UART2_RTS_B GPT1_CAPTURE1 I2C6_SDA	GPIO5[29]	Application UART 3 Transmit Data output signal
68	3V3	RXD	UART4_RXD	UART2_CTS_B PCIE_CLKREQ_B GPT1_COMPARE1 I2C6_SCL	GPIO5[28]	Application UART 3 Receive Data input signal
69	3V3	RTS	ECSPI2_SS0	UART4_RTS_B I2C4_SDA CCM_CLKO2	GPIO5[13]	Application UART 3 Request to Send **input** signal
70	3V3	CTS	ECSPI2_MISO	UART4_CTS_B I2C4_SCL AUDIOMIX_SAI7_MCLK CCM_CLKO1	GPIO5[12]	Application UART 3 Clear to Send **output** signal
71	GND	GND				
Module Specific Signals						
72	3V3		HDMI_DDC_SCL	HDMIMIX_EARC_SCL I2C5_SCL CAN1_TX	GPIO3[26]	
73	3V3		HDMI_DDC_SDA	HDMIMIX_EARC_SDA I2C5_SDA CAN1_RX	GPIO3[27]	
74	3V3		HDMI_CEC	HDMIMIX_EARC_CEC I2C6_SCL CAN2_TX	GPIO3[28]	
75	LDO5*)		SAI5_RXFS	AUDIOMIX_SAI5_RX_SYNC AUDIOMIX_SAI1_TX_DATA[0] PWM4_OUT I2C6_SCL	GPIO3[19]	
76	3V3	TXCAN	SPDIF_TX	AUDIOMIX_SPDIF_OUT PWM3_OUT I2C5_SCL GPT1_COMPARE1 CAN1_TX	GPIO5[3]	
77	HDMI	No standard TX assignment	HDMI_TXC_N	No Muxing		HDMI interface part 1/2
78	HDMI		HDMI_TX0_N			
79	HDMI		HDMI_TXC_P			
80	HDMI		HDMI_TX0_P			
81	3V3	RXCAN	SPDIF_RX	AUDIOMIX_SPDIF_IN PWM2_OUT I2C5_SDA GPT1_COMPARE2 CAN1_RX	GPIO5[4]	
82	GND	GND				
Serial Audio Interface						
83	3V3	SSI1_INT	SAI2_MCLK	AUDIOMIX_SAI2_MCLK AUDIOMIX_SAI5_MCLK ENET_QOS_1588_EVENT3_IN CAN2_RX ENET_QOS_1588_EVENT3_AUX_IN AUDIOMIX_SAI3_MCLK	GPIO4[27]	
84	3V3	SSI1_RXD	SAI2_RXD0	AUDIOMIX_SAI2_RX_DATA[0] AUDIOMIX_SAI5_TX_DATA[0] ENET_QOS_1588_EVENT2_OUT AUDIOMIX_SAI2_TX_DATA[1] UART1_RTS_B AUDIOMIX_BIT_STREAM[3]	GPIO4[23]	Serial Audio Interface serial data line 1

PIN	Type	TX Standard	i.MX8M Plus Pad Name	Alternate functions	GPIO	Description (refer to i.MX8M Plus manuals for details)
85	3V3	SSI1_TXD	SAI2_TXD0	AUDIOMIX_SAI2_TX_DATA[0] AUDIOMIX_SAI5_TX_DATA[3] ENET_QOS_1588_EVENT2_IN CAN2_TX ENET_QOS_1588_EVENT2_AUX_IN SRC_BOOT_MODE[4]	GPIO4[26]	Serial Audio Interface serial data line 0
86	3V3	SSI1_CLK	SAI2_TXC	AUDIOMIX_SAI2_TX_BCLK AUDIOMIX_SAI5_TX_DATA[2] CAN1_RX AUDIOMIX_BIT_STREAM[1]	GPIO4[25]	Serial Audio Interface serial bit clock
87	3V3	SSI1_FS	SAI2_TXFS	AUDIOMIX_SAI2_TX_SYNC AUDIOMIX_SAI5_TX_DATA[1] ENET_QOS_1588_EVENT3_OUT AUDIOMIX_SAI2_TX_DATA[1] UART1_CTS_B AUDIOMIX_BIT_STREAM[2]	GPIO4[24]	Serial Audio Interface left/right clock
88	GND	GND				
HDMI						
89	HDMI	No standard TX assignment	HDMI_TX1_N	No Muxing		HDMI interface part 2/2
90	HDMI		HDMI_TX2_N			
91	HDMI		HDMI_TX1_P			
92	HDMI		HDMI_TX2_P			
93	3V3		HDMI_HPD	HDMIMIX_EARC_DC_HPD AUDIOMIX_EARC_HDMI_HPD_O I2C6_SDA CAN2_RX	GPIO3[29]	
94	GND	GND				
MISC						
95	LDO5*)		SAI1_TXD6	AUDIOMIX_SAI1_TX_DATA[6] AUDIOMIX_SAI6_RX_SYNC AUDIOMIX_SAI6_TX_SYNC ENET1_RX_ER	GPIO4[18]	
96	LDO5*)		SAI1_TXD7	AUDIOMIX_SAI1_TX_DATA[7] AUDIOMIX_SAI6_MCLK AUDIOMIX_CLK ENET1_TX_ER	GPIO4[19]	
97	LDO5*)		SAI1_MCLK	AUDIOMIX_SAI1_MCLK AUDIOMIX_SAI5_MCLK AUDIOMIX_SAI1_TX_BCLK ENET1_TX_CLK	GPIO4[20]	
98	LDO5*)		SAI1_RXFS	AUDIOMIX_SAI1_RX_SYNC AUDIOMIX_SAI5_RX_SYNC ENET1_1588_EVENT0_IN	GPIO4[0]	
99	LDO5*)		SAI1_RXC	AUDIOMIX_SAI1_RX_BCLK AUDIOMIX_SAI5_RX_BCLK AUDIOMIX_CLK ENET1_1588_EVENT0_OUT	GPIO4[1]	
100	LDO5*)		SAI1_RXD0	AUDIOMIX_SAI1_RX_DATA[0] AUDIOMIX_SAI5_RX_DATA[0] AUDIOMIX_SAI1_TX_DATA[1] AUDIOMIX_BIT_STREAM[0] ENET1_1588_EVENT1_IN	GPIO4[2]	
101	LDO5*)		SAI1_RXD1	AUDIOMIX_SAI1_RX_DATA[1] AUDIOMIX_SAI5_RX_DATA[1] AUDIOMIX_BIT_STREAM[1] ENET1_1588_EVENT1_OUT	GPIO4[3]	
102	GND	GND				
103	LDO5*)		SAI1_TXC	AUDIOMIX_SAI1_TX_BCLK AUDIOMIX_SAI5_TX_BCLK ENET1_RGMII_RXC	GPIO4[11]	
104	LDO5*)		SAI1_TXFS	AUDIOMIX_SAI1_TX_SYNC AUDIOMIX_SAI5_TX_SYNC ENET1_RGMII_RX_CTL	GPIO4[10]	
105	LDO5*)		SAI1_RXD4	AUDIOMIX_SAI1_RX_DATA[4] AUDIOMIX_SAI6_TX_BCLK AUDIOMIX_SAI6_RX_BCLK ENET1_RGMII_RD0	GPIO4[6]	

PIN	Type	TX Standard	i.MX8M Plus Pad Name	Alternate functions	GPIO	Description (refer to i.MX8M Plus manuals for details)
106	LDO5*)		SAI1_RXD5	AUDIOMIX_SAI1_RX_DATA[5] AUDIOMIX_SAI6_TX_DATA[0] AUDIOMIX_SAI6_RX_DATA[0] AUDIOMIX_SAI1_RX_SYNC ENET1_RGMII_RD1	GPIO4[7]	
107	LDO5*)		SAI1_RXD6	AUDIOMIX_SAI1_RX_DATA[6] AUDIOMIX_SAI6_TX_SYNC AUDIOMIX_SAI6_RX_SYNC ENET1_RGMII_RD2	GPIO4[8]	
108	LDO5*)		SAI1_RXD7	AUDIOMIX_SAI1_RX_DATA[7] AUDIOMIX_SAI6_MCLK AUDIOMIX_SAI1_TX_SYNC AUDIOMIX_SAI1_TX_DATA[4] ENET1_RGMII_RD3	GPIO4[9]	
109	LDO5*)		SAI1_TXD4	AUDIOMIX_SAI1_TX_DATA[4] AUDIOMIX_SAI6_RX_BCLK AUDIOMIX_SAI6_TX_BCLK ENET1_RGMII_TX_CTL	GPIO4[16]	
110	LDO5*)		SAI1_TXD5	AUDIOMIX_SAI1_TX_DATA[5] AUDIOMIX_SAI6_RX_DATA[0] AUDIOMIX_SAI6_TX_DATA[0] ENET1_RGMII_TXC	GPIO4[17]	
111	GND	GND				
112	LDO5*)		SAI1_TXD3	AUDIOMIX_SAI1_TX_DATA[3] AUDIOMIX_SAI5_TX_DATA[3] ENET1_RGMII_TD3	GPIO4[15]	
113	LDO5*)		SAI1_TXD2	AUDIOMIX_SAI1_TX_DATA[2] AUDIOMIX_SAI5_TX_DATA[2] ENET1_RGMII_TD2	GPIO4[14]	
114	LDO5*)		SAI1_TXD1	AUDIOMIX_SAI1_TX_DATA[1] AUDIOMIX_SAI5_TX_DATA[1] ENET1_RGMII_TD1	GPIO4[13]	
115	LDO5*)		SAI1_TXD0	AUDIOMIX_SAI1_TX_DATA[0] AUDIOMIX_SAI5_TX_DATA[0] ENET1_RGMII_TD0	GPIO4[12]	
116	GND	GND				
LVDS / MIPI-DSI Display						
117	MIPI		MIPI_DSI_D2_N	No Muxing		
118	MIPI		MIPI_DSI_D1_N			
119	MIPI		MIPI_DSI_D2_P			
120	MIPI		MIPI_DSI_D1_P			
121	MIPI		MIPI_DSI_D3_N			
122	MIPI		MIPI_DSI_D0_N			
123	MIPI		MIPI_DSI_D3_P			
124	MIPI		MIPI_DSI_D0_P			
125	MIPI		MIPI_DSI_CLK_N			
126	LVDS	LVDS0_TX3_P	LVDS0_TX3_P			
127	MIPI		MIPI_DSI_CLK_P			
128	LVDS	LVDS0_TX3_N	LVDS0_TX3_N			
129	GND	GND				
130	LVDS	LVDS0_CLK_P	LVDS0_CLK_P	No Muxing		
131	LVDS	LVDS0_TX2_P	LVDS0_TX2_P			
132	LVDS	LVDS0_CLK_N	LVDS0_CLK_N			
133	LVDS	LVDS0_TX2_N	LVDS0_TX2_N			
134	LVDS	LVDS0_TX1_P	LVDS0_TX1_P			
135	LVDS	LVDS0_TX0_P	LVDS0_TX0_P			
136	LVDS	LVDS0_TX1_N	LVDS0_TX1_N			
137	LVDS	LVDS0_TX0_N	LVDS0_TX0_N			

PIN	Type	TX Standard	i.MX8M Plus Pad Name	Alternate functions	GPIO	Description (refer to i.MX8M Plus manuals for details)
USB3-SS						
138	USB3	No standard TX assignment	USB2_RX_N	No Muxing		
139	USB3		USB2_TX_N			
140	USB3		USB2_RX_P			
141	USB3		USB2_TX_P			
142	GND	GND				
143	LDO5*)		SAI5_RXD3	AUDIOMIX_SAI5_RX_DATA[3] AUDIOMIX_SAI1_TX_DATA[5] AUDIOMIX_SAI1_TX_SYNC AUDIOMIX_SAI5_TX_DATA[0] AUDIOMIX_BIT_STREAM[3] CAN2_TX	GPIO3[24]	
144	LDO5*)		SAI5_MCLK	AUDIOMIX_SAI5_MCLK AUDIOMIX_SAI1_TX_BCLK PWM1_OUT I2C5_SDA CAN2_RX	GPIO3[25]	
145	LDO5*)		SAI5_RXC	AUDIOMIX_SAI5_RX_BCLK AUDIOMIX_SAI1_TX_DATA[1] PWM3_OUT I2C6_SDA AUDIOMIX_CLK	GPIO3[20]	
146	3V3		SPDIF_EXT_CLK	AUDIOMIX_SPDIF_EXT_CLK PWM1_OUT GPT1_COMPARE3	GPIO5[5]	
147	GND	GND				
Module Specific Signals						
148	3V3		I2C3_SCL	PWM4_OUT, GPT2_CLK ECSPI2_SCLK	GPIO5[18]	
149	3V3		I2C3_SDA	PWM3_OUT, GPT3_CLK ECSPI2_MOSI	GPIO5[19]	
150	3V3		I2C4_SCL	PWM2_OUT, PCIE_CLKREQ_B ECSPI2_MISO	GPIO5[20]	
151	3V3		I2C4_SDA	PWM1_OUT ECSPI2_SS0	GPIO5[21]	
152	3V3		GPIO1_IO00	CCM_ENET_PHY_REF_CLK_ROOT ISP_FL_TRIG_0, CCM_EXT_CLK1	GPIO1[00]	
153	3V3		GPIO1_IO02	WDOG1_WDOG_B ISP_FLASH_TRIG_0 WDOG1_WDOG_ANY SJC_DE_B	GPIO1[02] 10K-PU to 3V3	Connected to PMIC WDOG_B
154	3V3		GPIO1_IO04	USDHC2_VSELECT ISP_SHUTTER_OPEN_0 SDMA1_EXT_EVENT[1]	GPIO1[04]	
155	3V3		GPIO1_IO05	M7_NMI, ISP_FL_TRIG_1 CCM_PMIC_READY	GPIO1[05]	
156	3V3		GPIO1_IO06	ENET_QOS_MDC ISP_SHUTTER_TRIG_1 USDHC1_CD_B CCM_EXT_CLK3	GPIO1[06]	
157	3V3		GPIO1_IO07	ENET_QOS_MDIO ISP_FLASH_TRIG_1 USDHC1_WP CCM_EXT_CLK4	GPIO1[07]	
158	3V3		GPIO1_IO08	ENET_QOS_1588_EVENT0_IN PWM1_OUT ISP_PRELIGHT_TRIG_1 ENET_QOS_1588_EVENT0_AUX_IN USDHC2_RESET_B	GPIO1[08]	
159	3V3		GPIO1_IO09	ENET_QOS_1588_EVENT0_OUT PWM2_OUT ISP_SHUTTER_OPEN_1 USDHC3_RESET_B AUDIOMIX_EXT_EVENT[0]	GPIO1[09]	
160	GND	GND				
161	3V3		GPIO1_IO10	USB1_OTG_ID PWM3_OUT	GPIO1[10]	
162	3V3		GPIO1_IO11	USB2_OTG_ID, PWM2_OUT USDHC3_VSELECT CCM_PMIC_READY	GPIO1[11]	
163	LDO5*)		SAI5_RXD0	AUDIOMIX_SAI5_RX_DATA[0] AUDIOMIX_SAI1_TX_DATA[2] PWM2_OUT, I2C5_SCL AUDIOMIX_BIT_STREAM[0]	GPIO3[21]	

PIN	Type	TX Standard	i.MX8M Plus Pad Name	Alternate functions	GPIO	Description (refer to i.MX8M Plus manuals for details)
164	LDO5*)		SAI5_RXD1	AUDIOMIX_SAI5_RX_DATA[1] AUDIOMIX_SAI1_TX_DATA[3] AUDIOMIX_SAI1_TX_SYNC AUDIOMIX_SAI5_TX_SYNC AUDIOMIX_BIT_STREAM[1] CAN1_TX	GPIO3[22]	
165	LDO5*)		SAI5_RXD2	AUDIOMIX_SAI5_RX_DATA[2] AUDIOMIX_SAI1_TX_DATA[4] AUDIOMIX_SAI1_TX_SYNC AUDIOMIX_SAI5_TX_BCLK AUDIOMIX_BIT_STREAM[2] CAN1_RX	GPIO3[23]	
PCIe						
166	LVDS		PCIE_REF_PAD_CLK_P			
167	LVDS		PCIE_RXN_N			
168	LVDS		PCIE_REF_PAD_CLK_N			
169	LVDS		PCIE_RXN_P			
170	LVDS		PCIE_TXN_N			
171	GND	GND				
172	LVDS		PCIE_TXN_P			
173	GND					
MIPI CSI						
174	GND					
175	MIPI		MIPI_CSI2_DATA0_P			
176	MIPI		MIPI_CSI1_DATA3_N			
177	MIPI		MIPI_CSI2_DATA0_N			
178	MIPI		MIPI_CSI1_DATA3_P			
179	MIPI		MIPI_CSI2_DATA1_P			
180	MIPI		MIPI_CSI1_DATA2_N			
181	MIPI		MIPI_CSI2_DATA1_N			
182	MIPI		MIPI_CSI1_DATA2_P			
183 184	GND					
185	MIPI		MIPI_CSI2_CLK_P			
186	MIPI		MIPI_CSI1_CLK_N			
187	MIPI		MIPI_CSI2_CLK_N			
188	MIPI		MIPI_CSI1_CLK_P			
189 190	GND					
191	MIPI		MIPI_CSI2_DATA2_P			
192	MIPI		MIPI_CSI1_DATA1_N			
193	MIPI		MIPI_CSI2_DATA2_N			
194	MIPI		MIPI_CSI1_DATA1_P			
195	MIPI		MIPI_CSI2_DATA3_P			
196	MIPI		MIPI_CSI1_DATA0_N			
197	MIPI		MIPI_CSI2_DATA3_N			
198	MIPI		MIPI_CSI1_DATA0_P			
199 200	GND	GND				

LDO5*) PCA9450 PMIC LDO5 / Default 3V3 / Can be set to 1V8 for low voltage RGMII support

Onboard peripherals wiring

USED FOR		i.MX8M Plus Pad Name	Alternate functions	GPIO	Description
		Refer to i.MX8M Plus manuals for details!			
eMMC	CMD	NAND_WP_B	USDHC3_CMD	GPIO3[18]	
	CLK	NAND_WE_B	USDHC3_CLK	GPIO3[17]	
	DAT0	NAND_DATA04	USDHC3_DATA0	GPIO3[10]	
	DAT1	NAND_DATA05	USDHC3_DATA1	GPIO3[11]	
	DAT2	NAND_DATA06	USDHC3_DATA2	GPIO3[12]	
	DAT3	NAND_DATA07	USDHC3_DATA3	GPIO3[13]	
	DAT4	NAND_RE_B	USDHC3_DATA4	GPIO3[15]	
	DAT5	NAND_CE2_B	USDHC3_DATA5	GPIO3[3]	
	DAT6	NAND_CE3_B	USDHC3_DATA6	GPIO3[4]	
	DAT7	NAND_CLE	USDHC3_DATA6	GPIO3[5]	
	DS	NAND_CE1_B	USDHC3_STROBE	GPIO3[2]	
PMIC	SDA	I2C1_SDA	I2C1_SDA	GPIO5[15]	10K-PU
	SCL	I2C1_SCL	I2C1_SCL	GPIO5[14]	1K-PU
	IRQ_B	GPIO1_IO03		GPIO1[3]	
	POR_B	POR_B			10K-PU
	PMIC_ON_REQ	PMIC_ON_REQ			
	PMIC_STBY_REQ	PMIC_STBY_REQ			
	WDOG_B	GPIO1_IO02		GPIO1[2]	10K-PU
	CLK_32K_OUT	RTC_XTALI			
ETHERNET LAN8710 RMII	MDC	ENET_MDC	ALT0 - ENET_MDC	GPIO1[16]	
	MDIO	ENET_MDIO	ALT0 - ENET_MDIO	GPIO1[17]	1K-PU
	RXD0	ENET_RD0	ALT0 - ENET_RD0	GPIO1[26]	
	RXD1	ENET_RD1	ALT0 - ENET_RD1	GPIO1[27]	
	RXER	ENET_RXC	ALT1 - RMII_RXER	GPIO1[25]	
	TXEN	ENET_TX_CTL	ALT0 - RMII_TX_EN	GPIO1[22]	
	TXD0	ENET_TD0	ALT0 - ENET_TD0	GPIO1[21]	
	TXD1	ENET_TD1	ALT0 - ENET_TD1	GPIO1[20]	
	COL/CRS_DV	ENET_RX_CTL	ALT1 - RMII_RX_EN (CRS_DV)	GPIO1[24]	10K-PU
	nRST	SAI2_RXC		GPIO4[22]	10K-PU
	nINT	SAI2_RXFS		GPIO4[21]	10K-PU
	XTAL1/CLKIN	ENET_TD2	ALT1 - RMII_REF_CLK	GPIO1[19]	
	POWER	ENET_TXC		GPIO1[23]	