Evaluating the ADF4030 10-Channel Precision Synchronizer

FEATURES

- EV-ADF4030SD1Z evaluation board including the ADF4030 10-channel precision synchronizer, Arduino interface, and voltage regulators
- Allows multiple ways to provide a reference clock to the ADF4030
  - Single-ended from a signal generator
  - Differential from another device or additional ADF4030 devices
- Gives access to all 10 ADF4030 BSYNC bidirectional I/O lines using twinax and SMA connectors
- Facilitates interfacing the ADF4030 clocks with an oscilloscope or other boards using an interposer board
- SDP-K1 controller board functions as an interface between a PC and the evaluation board
- Up to 16 EV-ADF4030SD1Z evaluation boards can be stacked up using the Arduino connector
- Windows®-based software allows control of all ADF4030 functions from a PC

EVALUATION BOARD KIT CONTENTS

- EV-ADF4030SD1Z evaluation board
- Interposer board
- One SDK-K1 controller kit
- One 12 V, 24 W AC/DC external wall mount (Class II) adapter
- One twinax cable

EQUIPMENT NEEDED

- Windows-based PC with USB 2.0 port for evaluation software
- Reference clock source
- Oscilloscope with SMA cables (optional)

REQUIRED SOFTWARE

- ACE software, Version 1.30 or higher
- ADF4030 plugin, Version 1.2024.26400-dev0030 or higher

GENERAL DESCRIPTION

The EV-ADF4030SD1Z evaluates the performance of the ADF4030 10-channel precision synchronizer. The SDP-K1 controller board must be connected to the EV-ADF4030SD1Z using the Arduino connector underneath the evaluation board. Multiple EV-ADF4030SD1Z evaluation boards can be stacked up onto the SDP-K1 controller board using the Arduino connector.

A photograph of the evaluation board with the SDP-K1 controller board is shown in Figure 1. The evaluation board contains the ADF4030 10-channel precision synchronizer, the power supply connectors, and the Arduino connector used to connect to the SDP K1 board. This combination allows software programming of the evaluation board using ACE software.

Full specifications for the ADF4030 precision synchronizer are available in the product data sheet, which must be consulted in conjunction with this user guide when working with the evaluation board.

EVALUATION BOARD PHOTOGRAPH

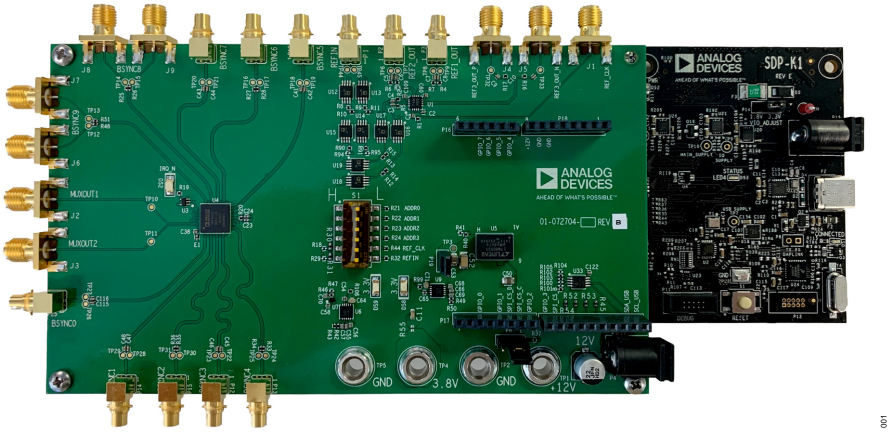

Figure 1. EV-ADF4030SD1Z Plugged into SDP K1 Controller Board

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REVISION HISTORY

10/2024—Revision 0: Initial Version

GETTING STARTED

SOFTWARE INSTALLATION PROCEDURES

To install the ACE software and ADF4030 plugin, perform the following steps:

1. Install the latest version of the ACE software.
2. If the ADF4030 plugin appears automatically, the software installation is complete.
3. Otherwise, double click the ADF4030 plugin file, **Board.ADF4030.nnn.acezip**, in which nnn is a number identifying the plugin version. Remove the **.txt** extension first if the plugin has it in the file name.

When notified that a new version of the ACE software is available, feel free to install it.

EVALUATION BOARD SETUP PROCEDURES

To run the evaluation software, perform the steps outlined in the Evaluation Board Software section.

EVALUATION BOARD HARDWARE

The EV-ADF4030SD1Z evaluation board must be connected to the SDP K1 controller board through the Arduino connectors P5, P17, P18, and P16. The SDP K1 board is connected underneath the EV-ADF4030SD1Z, as in Figure 1.

The EV-ADF4030SD1Z schematics and artwork are shown in the Evaluation Board Schematics and Artwork section.

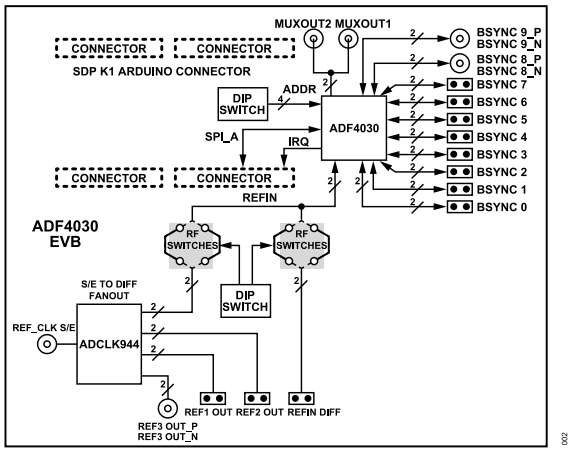

Figure 2. EV-ADF4030SD1Z Evaluation Board Block Diagram

Figure 2 presents the block diagram of the EV-ADF4030SD1Z.

The Arduino connector is used for the SDP K1 controller board to connect to the EV-ADF4030SD1Z from underneath. Additional EV-ADF4030SD1Z evaluation boards may be stacked up using the Arduino connectors.

The four positions labeled ADDR0, ADDR1, ADDR2, and ADDR3 of the S1 dual in-line package (DIP) switch determine the serial peripheral interface (SPI) address of the ADF4030 placed on the evaluation board. By default, the four switches are off, which means the ADF4030 SPI address is set to 0000. When multiple evaluation boards are stacked, assign a different SPI address to each board.

The last two positions of the DIP switch, labeled REF_CLK and REFIN, manage which channel is used to provide the reference clock of the ADF4030. See the Reference Clock Input (REFIN) section for more details.

POWER SUPPLIES

Figure 3 presents a block diagram of the EV-ADF4030SD1Z power supply scheme. The SDP K1 is supplied by connecting the provided USB cable to the PC. Ensure the VIO adjust jumper on the SDP K1 board is connected between the middle pin and the pin identified by the 1.8 V label. This makes the input and output pins available at the Arduino connector work at 1.8 V.

The ADF4030 can be supplied through the provided 12 V, 24 W wall mount adapter or from a 12 V isolated DC power supply at banana plugs TP1 and TP2. Make sure the Jumper P6 is connected between Pin 1 and Pin 2 and Jumper P19 is inserted. This approach uses the LTM8053 µModule regulator (Figure 4). The LTM8053 3.9 V output is then used by one ADP7112 and two ADP7159 to create 1.8 V and 3.3 V supplies, respectively, for the ADF4030 ICs.

As an alternative to using the LTM8053, an isolated DC power supply can be set to apply 3.9 V at banana plugs TP4 and TP5 (GND). Unplug Jumper P19 and install a 0 Ω resistor at R55. This approach bypasses the LTM8053 independent of the power supply. Do not plug in the jumper at P19 and supply 12 V at TP1 and TP2 while also providing 3.9 V at TP4 and TP5.

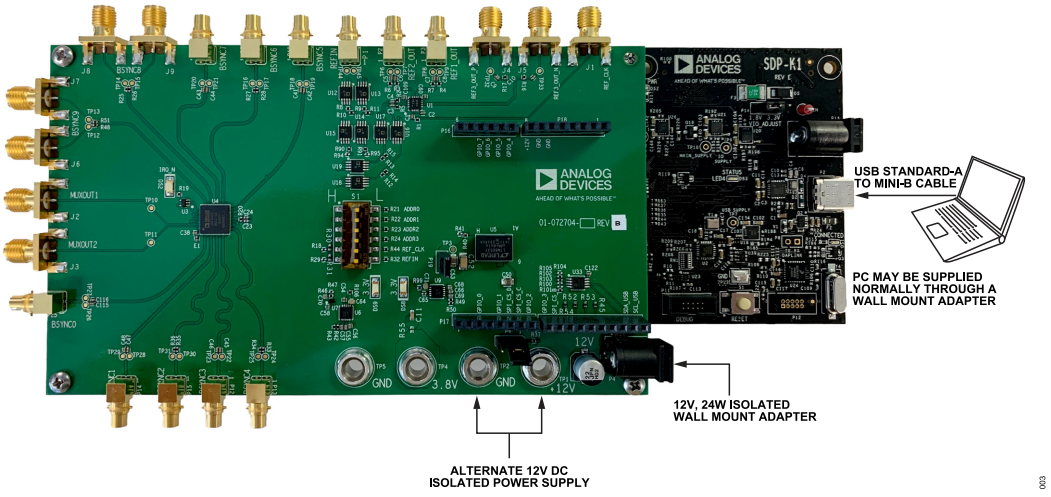

Figure 3. ADF4030 Evaluation Board and SDP K1 Controller Board Power Supply Scheme

EVALUATION BOARD HARDWARE

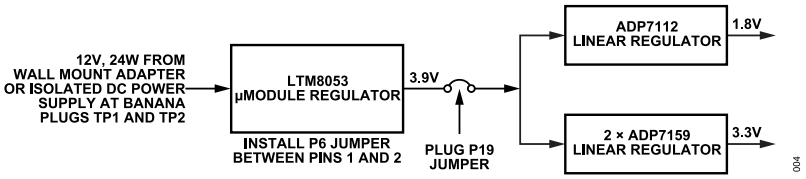

Figure 4. ADF4030 Evaluation Board Supply using 12 V Wall Mount Adapter

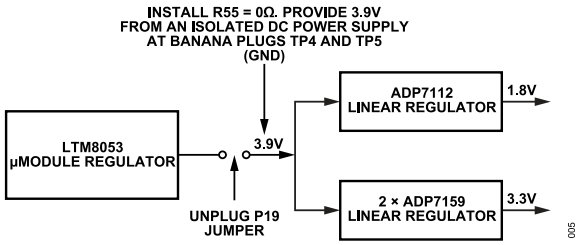

Figure 5. ADF4030 Evaluation Board Supply using a 3.9 V Isolated DC Power Supply

EVALUATION BOARD HARDWARE

REFERENCE CLOCK INPUT (REFIN)

The EV-ADF4030SD1Z has two ways to create the ADF4030 REFIN clock, a clock between 10 MHz and 250 MHz (see Figure 2) as follows:

- Using a J1 Subminiature Version A (SMA) connector (REF_CLK S/E in (Figure 2). Apply a 4 dBm signal, which means a 1 V p-p clock. A 50 Ω load resistor to ground (R1) is populated on board.
- Using a P1 twinax connector (REFIN DIFF in Figure 2). Apply a 320 mV p-p to 2 V p-p differential voltage. This must be a AC-coupled input to the ADF4030. This connector is suitable for connecting the reference clock from another EV-ADF4030SD1Z (Figure 7).

The channels labeled REF_CLK and REFIN of the DIP switch S1 select the corresponding clock applied to the REFIN pins of the ADF4030. Set the switch of the desired channel to on. By default, the DIP switches are off, which means no reference clock is allowed towards the ADF4030. Do not select both channels to be provided at the ADF4030.

If multiple EV-ADF4030SD1Z evaluation boards need to work together, provide one clock at REF_CLK S/E connector at one evaluation board: EVB0 in Figure 7. Then, use a twinax cable to connect one of REF1 OUT (P3 connector) or REF2 OUT (P2 connector) to REFIN DIFF (P1 connector) of the other evaluation board (EVB1 in Figure 7). Set the EVB0 REF_CLK switch to on and the EVB1 REFIN switch to off.

Alternatively, connect an SMA to SMA cable from one of the EVB0 REF3 OUT SMA connectors (J4 or J5) to EVB1 REF_CLK S/E connector. Set both the EVB0 and the EVB1 REF_CLK switches to on. See Figure 6 .

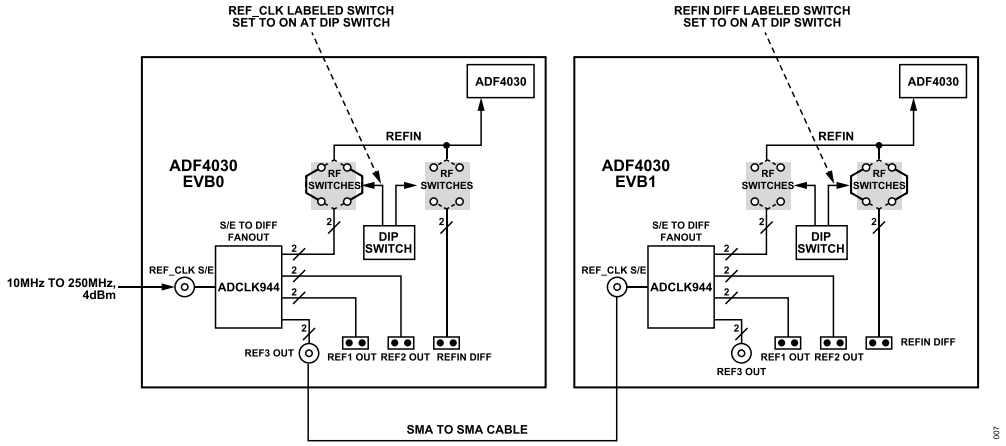

Figure 6. Transmitting REFIN Clock from One EV-ADF4030SD1Z to Another Using an SMA to SMA Cable

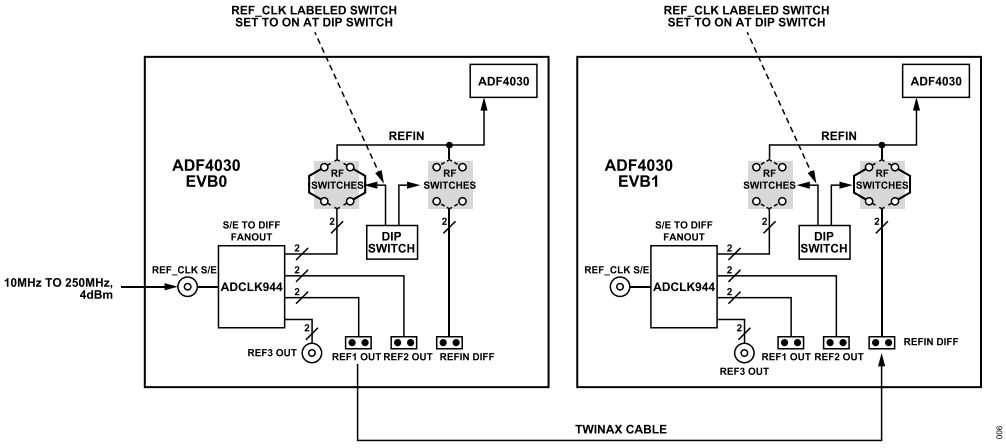

Figure 7. Transmitting REFIN Clock from One EV-ADF4030SD1Z to Another Using a Twinax Cable

EVALUATION BOARD HARDWARE

BSYNCX BIDIRECTIONAL INPUTS AND OUTPUTS

The EV-ADF4030SD1Z offers access to all BSYNC0, BSYNC1, …, BSYNC7 inputs and outputs using the twinax connectors P25, P14, P15, P12, P13, P10, P8, and P11, respectively. The BSYNC8 and BSYNC9 inputs and outputs are accessible using the J8, J9, J6, and J7 SMA connectors, respectively.

The printed circuit board (PCB) traces from the ADF4030 that pin to the twinax connectors of the BSYNC0 to BSYNC7 channels are matched to have equal length within ±1/1000 of 1.5 in, that is 0.0381 mm, and to allow time delays between various BSYNC clocks to be measured without errors. The BSYNC8 and BSYNC9 PCB traces are also matched to have equal length within 1/1000 of 1.5 in, but the length is different from the length of BSYNC0 to BSYNC7 traces.

The BSYNC0, BSYNC1, BSYNC3, BSYNC5, and BSYNC7 channels are AC-coupled, while the BSYNC2, BSYNC4, BSYNC6, BSYNC8, and BSYNC9 channels are DC-coupled. Although AC coupling degrades the ADF4030 time-to-digital converter (TDC) accuracy somewhat, no meaningful alignment differences have been observed relative to aligning the DC-coupled clocks.

All BSYNC channels are unterminated, that is, no 100 Ω load is connected between the + and − related pins outside of the ADF4030. Use the evaluation software to configure the BSYNC channel terminations appropriately for the desired configuration. See the Configuring the BSYNC Terminations and Drivers section.

To facilitate interfacing the EV-ADF4030SD1Z BSYNC channels that have twinax connectors, an interposer board is provided. See the Using the Interposer Board section for more details.

DEFAULT CONFIGURATION

The EV-ADF4030SD1Z is configured by default with a P6 jumper connected between Pin 1 and Pin 2 and with the P19 jumper plugged in. This means the board is set to be supplied using the wall mount adapter.

By default, the DIP switches labeled REF_CLK and REFIN that manage which reference clock goes through the ADF4030 REFIN pins are open. If a signal generator is used to provide the REFIN clock, set the switch that enables the reference clock to the ADF4030 coming from J1 SMA connector to on. Then, apply a 100 MHz, 4 dBm clock from a signal generator at J1.

By default, the ADF4030 is set to generate 100 MHz BSYNC clocks, with the BSYNC1 channel being enabled as a transmitter in voltage driver mode with the common-mode voltage set at 455.5 mV. Make sure a 100 Ω termination is at the receiver.

EVALUATION BOARD SOFTWARE

The ACE software is the main platform that is used to control the EV-ADF4030SD1Z. The ADF4030 plugin includes user interfaces relating to the ADF4030 and that allow evaluation of the device. Use the following steps to open the main control window of the ADF4030.

1. Connect the EV-ADF4030SD1Z to the SDP K1 board as shown in Figure 1.
2. Set the S1 DIP switches that manage the SPI address of the ADF4030 and select which J1 or P1 connector is used to provide the REFIN clock.
3. Connect the provided standard USB-A to mini-B cable to the SDP K1 board. Do not connect the cable to the PC yet.
4. Supply the EV-ADF4030SD1Z through one of the ways presented in the Power Supplies section.
5. Apply a clock between 10 MHz and 250 MHz at the J1 SMA connector or at the P1 twinax connector. See Reference Clock Input (REFIN) for more details. By default, the ADF4030 is configured to receive 100 MHz clock.
6. Connect the USB cable to the PC.
7. Launch the ACE application. The attached hardware appears in the graphical user interface (GUI) as shown in Figure 8.
8. Double click **ADF4030 Board**, and the window shown in Figure 9 appears.
9. Double click **ADF4030** to open the main control window shown in Figure 10.
10. The ADF4030 user interface configures the ADF4030 to receive REFIN = 100 MHz and output BSYNC clocks of 100 MHz. If this is acceptable, just click **Apply Changes** on the top left of the dialog box. Otherwise, modify the REFIN, PLL parameters, and ODIVA or ODIVB distribution dividers as desired. Click **Apply Changes** when finished. This assumes that the REFIN clock input into the control window matches the clock provided at REFIN pins of the ADF4030.
11. Click **CHECK LOCK STATUS** inside the **PLL/VCO** dialog box. The **REF OK** green LED inside the **REF IN Clock** dialog box and the green LED inside the **PLL/VCO** dialog box should both turn green (Figure 11). The first LED shows that the ADF4030 considers the REFIN clock as valid, and the second shows the PLL has locked onto the REFIN reference clock. If the PLL has not locked, the typical cause is the reference clock not meeting the data sheet specifications. This may happen even when the ADF4030 deems the reference as valid.
12. At this point, the ADF4030 is ready to execute other functions.

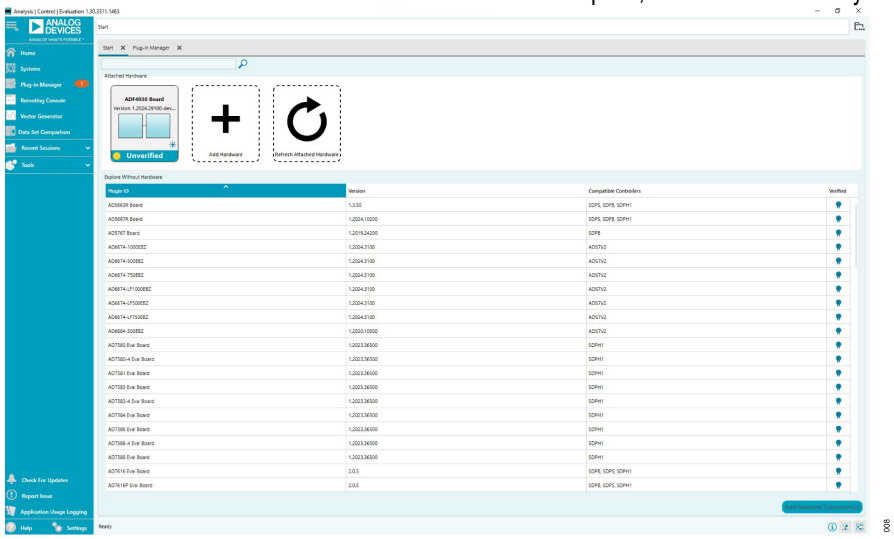

Figure 8. ACE Start Page Showing the EV-ADF4030SD1Z and SDP K1 Controller Boards Available

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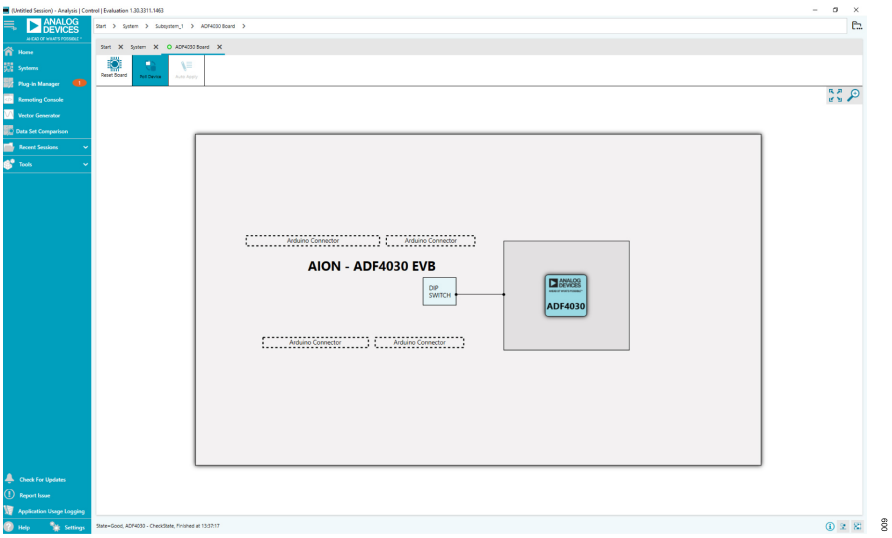

Figure 9. ACE Board Page, Device Selection

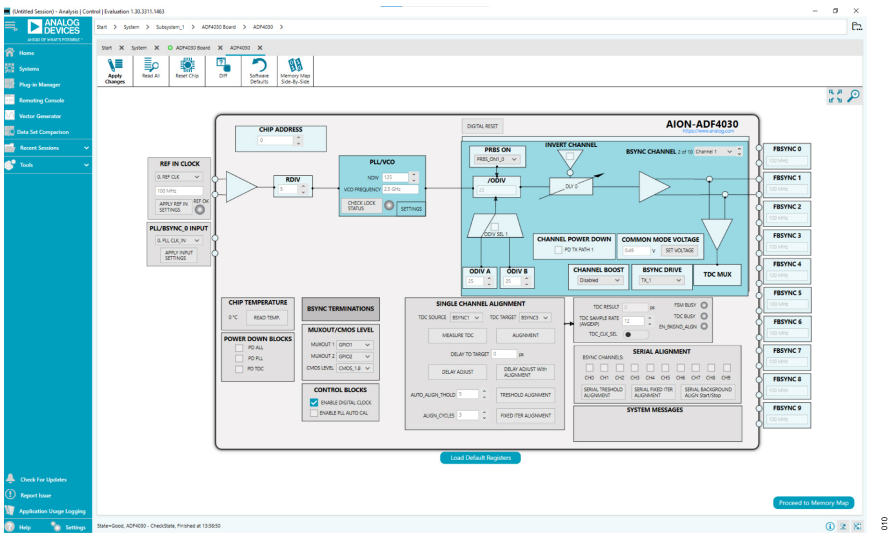

Figure 10. ACE User Interface After Launch

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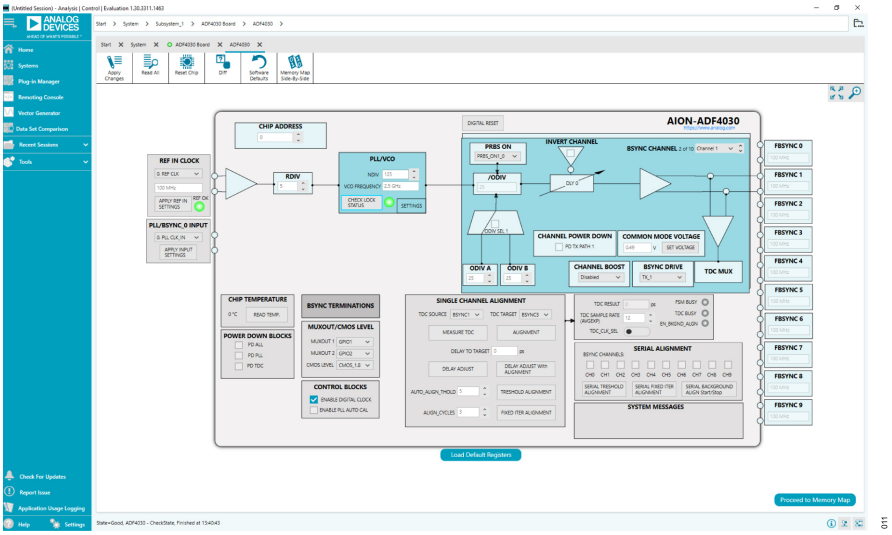

Figure 11. ACE after PLL has locked

LOAD DEFAULT REGISTERS BUTTON

Click the **Load Default Registers** button to configure the ADF4030 with the initial values (see the Device Initialization section in the ADF4030 data sheet).

CONFIGURING THE BSYNC TERMINATIONS AND DRIVERS

In order to make the ADF4030 perform time measurements, the BSYNC channels planned to be used must be configured.

First, select the desired transmit configuration based on Table 1. The evaluation board does not have pads reserved for connecting a 100 Ω load, so the easiest choice is to use the interposer channels that have 50 Ω loads to ground (see the Using the Interposer Board section). Choose the desired common-mode voltage. By default, the common-mode voltage is 504.3 mV. If a different value is required, see the Transmit Configurations section in the ADF4030 data sheet.

Table 1. BSYNC Transmit Configurations Possible with the Evaluation Board

FLOAT_TXx	LINK_TXx	Transmit Configuration	Required Terminations Outside Evaluation Board
0	0	Voltage Driver (default)	100 Ω
1	1	Current Driver, terminated	50 Ω to ground

Select the desired receive configuration based on Table 2. For DC-coupled connections, use BSYNC2, BSYNC4, BSYNC6, BSYNC8, and/or BSYNC9 channels configured as differential, internal 100 Ω, DC-coupled termination. On the evaluation board, BSYNC2, BSYNC4, BSYNC6, BSYNC8, and BSYNC9 channels are DC-coupled. For AC-coupled connections, use the BSYNC0, BSYNC1, BSYNC3, BSYNC5, and/or BSYNC7 channels that are configured as AC-coupled. On the evaluation board, BSYNC0, BSYNC1, BSYNC3, BSYNC5, and BSYNC7 channels are AC-coupled.

Table 2. BSYNC Receive Configurations

Float_RXx	Link_RXx	AC_COUPLEDx	Receive Configuration	Remarks
1	1	0	Internal 100 Ω (default)	Use it on DC-coupled BSYNC2, 4, 6, 8, and 9 channels
1	Does not matter	1	AC-coupled termination	Use it on AC-coupled BSYNC0, 1, 3, 5, and 7 channels
0	Does not matter	0	Grounded common-mode	Use it on DC-coupled BSYNC2, 4, 6, 8, and 9 channels with HCSL clocks

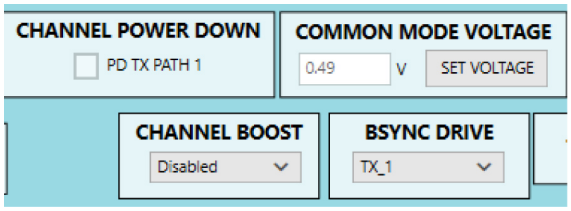

Figure 12. Configure the BSYNC Channels using this GUI section

Click the **BSYNC CHANNEL** dropdown menu to select the BSYNC channel to be configured (Figure 12). Choose the driver boost using the **CHANNEL BOOST** dropdown menu.

- **CHANNEL BOOST** = Disabled (uses the 14 mA driver)
- **CHANNEL BOOST** = Enabled (uses the 20 mA driver)

Type the desired common-mode voltage in the **COMMON MODE VOLTAGE** dialog box . The common-mode voltage is a value between 0.5043 V and 1.3 V when the driver is 14 mA and a value between 0.7204 V and 1.863 V when the driver is 20 mA. Enable

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the driver in the **BSYNC DRIVE** section. Then, uncheck the **PD TX PATH** checkbox if a transmit driver is to be enabled.

Click the **Apply Changes** button for the ADF4030 registers to be updated accordingly.

MEASURE TDC BUTTON

The measure TDC function measures the phase delay between two BSYNC channels and visualizes it into the **TDC RESULT** dialog box expressed in picoseconds.

First, select the **TDC SAMPLE RATE (AVGEXP)**. The evaluation software sets **AVGEXP** = 12, which means the TDC postprocessor averages 64 × 2^{12} = 262,144 samples. Select the **TDC SOURCE** and **TDC TARGET** channels to use as inputs to the TDC (Figure 13).

Click **Apply Changes** for the selections to be written into the ADF4030 registers. Click the **MEASURE TDC** button to obtain the phase delay measurement in the **TDC RESULT** dialog box expressed in ps.

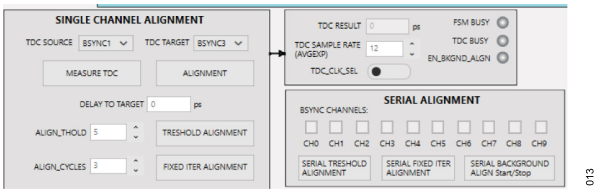

Figure 13. ACE GUI Alignment Section

The **TDC BUSY** green LED corresponds to Bit 4, TDC_BUSY, in Register 0x8F. It is on when the TDC is executing a conversion and is off when the TDC is not executing a conversion.

BUTTONS FOR VARIOUS SINGLE-CHANNEL ALIGNMENT PROCEDURES

Several buttons are used in the alignment procedures (see the BSYNC Channel Alignment section in the ADF4030 data sheet). Details are provided in the following paragraphs.

For the **ALIGNMENT** button (single-channel alignment in the data sheet), first select the **TDC SOURCE** and **TDC TARGET**. Next, click the **Apply Changes** button. Then, click the **ALIGNMENT** button.

For **DELAY ADJUST** (open-loop delay adjustment in the data sheet), select the **TDC TARGET** and click the **Apply Changes** button. Introduce the desired delay expressed in ps in the **DELAY TO TARGET** dialog box. Then, click the **DELAY ADJUST** button.

The **DELAY ADJUST With ALIGNMENT** button is the single-channel alignment with a time delay. **DELAY TO TARGET** delay is introduced into the ADF4030 through the TDC_OFFSETx and TDC_OFFSET_COM registers.

For the threshold alignment, select the **TDC SOURCE**, **TDC TARGET**, and click the **Apply Changes** button. Next, decide the **ALIGN_THOLD** alignment threshold, which the data sheet recommends to be set to 1, the minimum value (ALIGN_THOLD bits cleared to 0). Click the **Apply Changes** button again. Then click the **THRESHOLD ALIGNMENT** button.

For the **FIXED ITER ALIGNMENT** (fixed iteration alignment in the data sheet), select the **TDC SOURCE**, **TDC TARGET**, and then click the **Apply Changes** button. Decide the desired number of alignment cycles. The data sheet recommends to be anywhere between 1 and 8 cycles, meaning ALIGN_CYCLES bits between 0 and 7. Select the number **ALIGN_CYCLES** from the dropdown menu, and click the **Apply Changes** button again to save the settings. Then, click **Fixed ITER ALIGNMENT**.

MULTICHANNEL ALIGNMENT BUTTONS

Figure 14 presents the GUI section that deals with multichannel alignment procedures. Several details are provided in the following paragraphs.

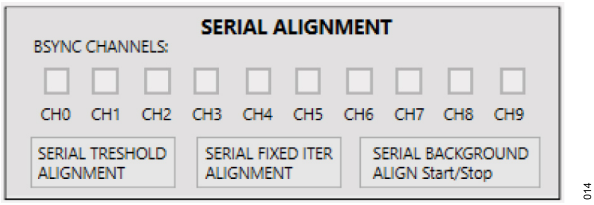

Figure 14. ACE GUI Multichannel Alignment Section

For the **SERIAL ALIGNMENT** dialog box (the serial alignment procedure with threshold iteration in the data sheet), first, select the **TDC SOURCE** channel and check the **BSYNC CHANNELS** that are to be aligned to the **TDC SOURCE**. The **TDC SOURCE** must be selected through the checkboxes if the channel is an outgoing clock. Then, decide and enter the alignment threshold in **ALIGN_THOLD** dropdown menu It is recommended to be set to 1, that is, the ALIGN_THOLD bits cleared to 0. Click **Apply Changes** for the settings to be written into the ADF4030. Next, click the **SERIALTHRESHOLD ALIGNMENT** button to start the procedure.

For the **SERIAL FIXED ITER ALIGNMENT** button (the serial alignment procedure with fixed number of iterations in the data sheet), select first the **TDC SOURCE** channel and check the **BSYNC CHANNELS** that are to be aligned to the **TDC SOURCE**. The **TDC SOURCE** must be selected through the checkboxes if the channel is an outgoing clock. Then, decide and choose from the **ALIGN_CYCLES** dropdown menu, the desired number of alignment cycles. The recommendation is for the alignment cycles to be anywhere between 1 and 8, meaning between ALIGN_CYCLES bits set between 0 and 7. Click **Apply Changes** for the settings to be written into the ADF4030. Then, click the **SERIAL FIXED ITER ALIGNMENT** button to start the procedure.

For the **SERIAL BACKGROUND ALIGN Start/Stop** button (the background serial alignment procedure in the data sheet), perform the same steps required for the serial alignment procedures outlined previously, only this time, when the **SERIAL BACKGROUND**

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ALIGN Start/Stop button is pressed, the alignment is done in the background, and the temperature measurement is also executed. Configure the temperature measurement first as presented in the data sheet.

CONTROL BLOCKS SECTION

Figure 15 presents the control blocks section of the ADF4030 evaluation software. By default, Bit 6, EN_DIGCLK, in Register 0x58 is set to 1. This means the **ENABLE DIGITAL CLOCK** checkbox is checked.

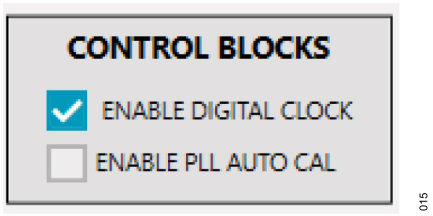


Figure 15. ACE Control Blocks Section

Bit 6, PLL_CAL_EN, in Register 0x5A is represented by the **ENABLE PLL AUTO CAL** checkbox. When the PLL parameters must be changed, introduce them into the GUI and check **ENABLE PLL AUTO CAL** checkbox. Then click **Apply Changes**. The ADF4030 is configured with the new parameters, and the PLL locks. Click the **CHECK LOCK STATUS** button in the **PLL/VCO** dialog box to verify that the **REF OK** green LED in the **REF IN CLOCK** dialog box and the green LED in the **PLL/VCO** dialog box are turned on.

MUXOUT/CMOS LEVEL BOX

The **MUXOUT/CMOS LEVEL** dialog box manages the MUXOUT1 and MUXOUT2 pins of the ADF4030. On the evaluation board, MUXOUT1 and MUXOUT2 are accessible at the J2 and J3 SMA connectors.

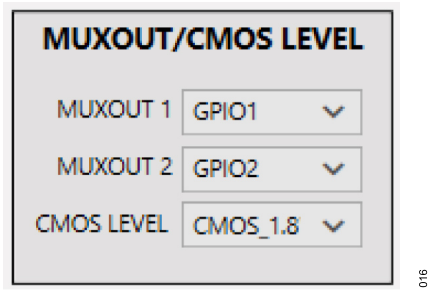


Figure 16. MUXOUT/CMOS Level Box

Select the desired **CMOS LEVEL** (**CMOS_1.8** or **CMOS_3.3**) and then select what signal to output at the **MUXOUT1** and **MUXOUT2** pins. See the CMOS Output Pin Logic High Control section in the ADF4030 data sheet for more details.

BSYNC TERMINATIONS BOX

Figure 17 shows the dialog box where the BSYNC terminations can be selected for every BSYNC channel. When a BSYNC channel is used to generate (that is transmit) clocks, three options are available as follows: differential voltage driver, differential current driver unterminated, or differential current driver terminated. As stated in the BSYNCx BIDIRECTIONAL Inputs and Outputs section, all BSYNC channels on the evaluation board are unterminated. BSYNC0, BSYNC1, BSYNC3, BSYNC5, and BSYNC7 are AC-coupled, while BSYNC2, BSYNC4, BSYNC6, BSYNC8, and BSYNC9 are DC-coupled. The interposer has three channels terminated with 50 Ω resistors to ground. Use Table 3 to select the appropriate driver mode depending on the evaluation board usage.

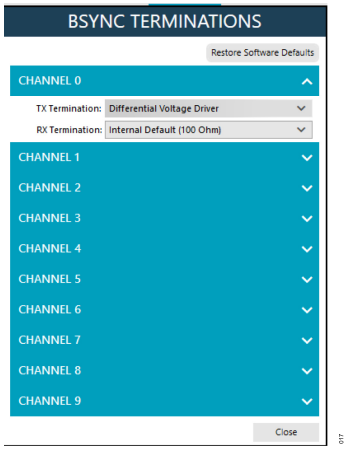


Figure 17. BSYNC Terminations Box

Table 3. BSYNC Transmit Configurations

Transmit Configuration	Required Terminations Outside ADF4030	Required Terminations at Receiver
Voltage Driver	None	100 Ω
Current Driver, Unterminated	100 Ω	50 Ω to ground
Current Driver, Terminated	None	50 Ω to ground

Use Table 4 to select the receive mode of the BSYNC channels.

Table 4. BSYNC Receive Configurations

Receive Configuration	Remarks
Internal 100 Ω	Use for incoming DC-coupled clocks on the BSYNC2, BSYNC4, BSYNC6, BSYNC8, or BSYNC9 channels.
External Termination Required	Not recommended.
AC-Coupled Termination	Use for incoming AC-coupled clocks. BSYNC0, BSYNC1, BSYNC3, BSYNC5, and BSYNC7 are AC-coupled on board. If AC coupling is placed outside evaluation board, BSYNC2, BSYNC4, BSYNC6, BSYNC8, and BSYNC9 may also be used
Grounded Common-Mode	Use for incoming DC-coupled HCSL clocks.

POWER DOWN BOX

Figure 18 presents the power down options as follow:

EVALUATION BOARD SOFTWARE

- When checked, the **PD ALL** checkbox sets Bit 7, PD_ALL, in Register 0x3C to 1, meaning the entire IC is powered down.
- When checked, the **PD PLL** checkbox sets Bit 6, PD_PLL, in Register 0x3C to 1, meaning the PLL is powered down.
- When checked, the **PD TDC** checkbox sets Bit 5, PD_TDC, in Register 0x3C to 1, meaning the TDC and the multiplexer at the TDC input are powered down.

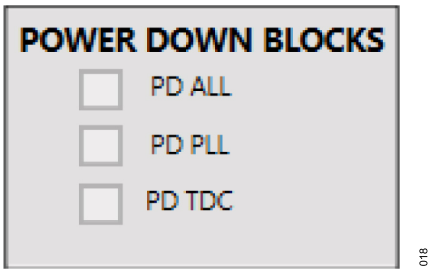


Figure 18. Power Down Box

CHIP TEMPERATURE BOX

When the **READ TEMP.** button is pressed (see Figure 19), the temperature is measured and visualized in the dialog box.

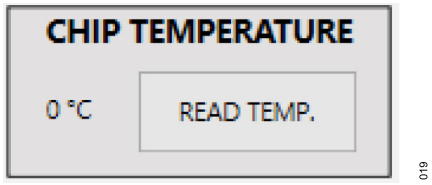


Figure 19. Chip Temperature Box

USING THE INTERPOSER BOARD

The interposer board provided in the evaluation kit gives access to all signals available at the twinax connectors of the EV-ADF4030SD1Z.

The interposer has multiple types of channels.

One type (see Figure 20) deals with the bidirectional BSYNC channels of the ADF4030. There are two identical such channels on the interposer board. Connect the EV-ADF4030SD1Z twinax connector to the interposer twinax connectors like P51. Use the J31 and J32 SMA connectors to capture or input single ended clocks. The balun may be used to transform a single-ended clock connected at J31, J32 or P54 into a differential clock going into the ADF4030 through the interposer.

Another type is in Figure 21. This one channel is identical with the BSYNC channels from Figure 20, but without the output twinax connector.

Table 5 presents what jumper settings are recommended when the BSYNC Channel 1 and BSYNC Channel 2 are configured as outputs or inputs. By default, the BSYNC channels are configured as outputs with the balun bypassed. The jumper settings also apply to BSYNC Channel 3.

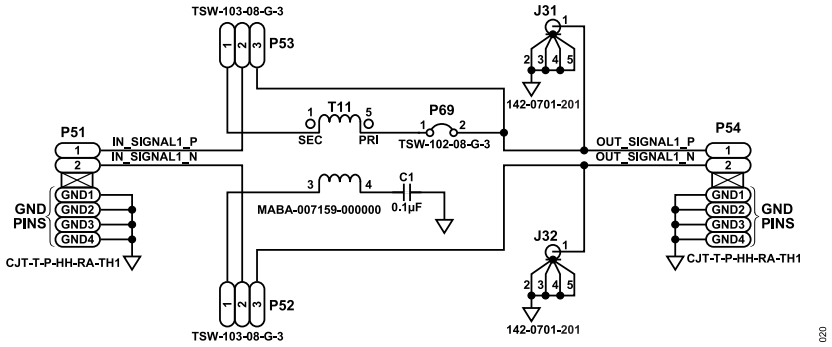


Figure 20. Interposer BSYNC OUT Channels 1 and 2

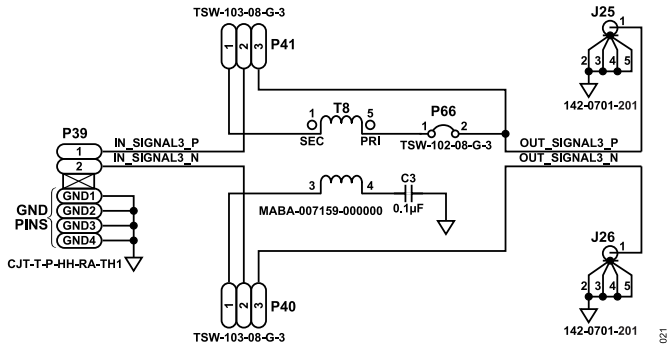


Figure 21. Interposer BSYNC OUT Channel 3

Table 5. Recommended Jumper Settings for BSYNC OUT Channels on the Interposer Board

Target	P53 Jumper	P52 Jumper	P69 Jumper	Use Case
BSYNC Output (Default)	Between Pin 2 and Pin 3	Between Pin 2 and Pin 3	Unplugged	Oscilloscope at J31 and J32
BSYNC Differential Input	Between Pin 2 and Pin 3	Between Pin 2 and Pin 3	Between Pin 2 and Pin 3	Differential input at J31 and J34 or P54
BSYNC Single Ended Input	Between Pin 1 and Pin 2	Between Pin 1 and Pin 2	Plugged	Single-ended input signal at J31

USING THE INTERPOSER BOARD

A schematic for a third type of channel is shown in Figure 22. It is similar to the channels from Figure 20 but without the jumpers and the balun. They also have 50 Ω resistors to ground on both P and N lines.

A fourth type of channel schematic is shown in Figure 23. These two channels may be used to access the P and N signals at the J7 and J8 SMA connectors.

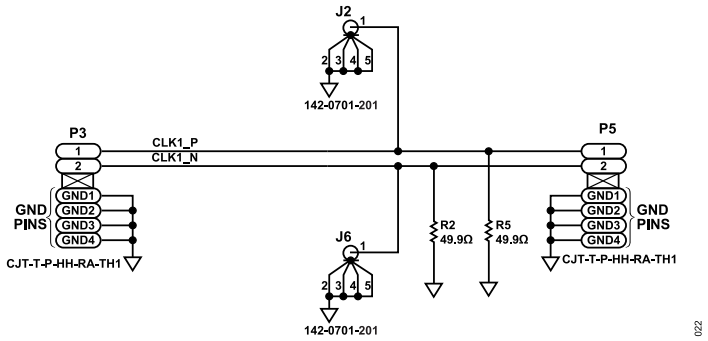


Figure 22. Interposer CLK Channels 1, 2, and 3

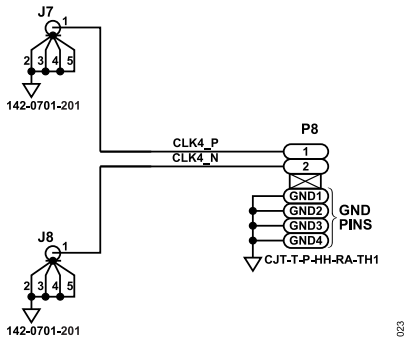


Figure 23. Interposer CLK Channels 4 and 5

TWO AND THREE ADF4030 ICS SYNCHRONIZATION DEMOS

This section describes how to install and execute the two and three ADF4030 ICs synchronization demos.

The demos contain the following:

- Two or three EV-ADF4030SD1Z evaluation boards with power supplies
- One interposer board used to connect the ADF4030 BSYNC clocks to an oscilloscope
- Three or five 11 in twinax cables
- One standard USB A to mini-B cable
- Two or three RF SMA male to SMA male cables to connect the AD9545 evaluation board outputs to the J1 inputs of the EV-ADF4030SD1Z

CREATING THE DEMO BENCH

Execute the following steps to create the hardware bench:

1. Plug the SDP K1 board underneath one EV-ADF4030SD1Z through the Arduino connectors. Call this board **ADF4030_EVB1**.
2. Set the ADDR3, ADDR2, ADDR1, and ADDR0 switches at S1 to the off position. This sets the SPI address of the ADF4030 populating ADF4030_EVB1 to 0000.
3. Set the REF_CLK S1 switch to on to enable providing a reference clock from J1 SMA connector to the ADF4030. Make sure the REFIN S1 switch is off. See the Reference Clock Input (REFIN) section for more details on these switches. This assumes a reference clock is provided from a signal generator at the J1 connector of ADF4030_EVB1.
4. Use the Arduino connectors of the ADF4030-EVB1 to connect the second evaluation board. Call this board **ADF4030_EVB2**.
5. Set the ADDR3, ADDR2, ADDR1, and ADDR0 switches at S1 to the off, off, off, and on positions, respectively. This sets the SPI address of the ADF4030 populating ADF4030_EVB2 to 0001, but any non 0000 SPI address can be used.
6. Set the REF_CLK S1 switch to on to enable providing a reference clock from J1 SMA connector to the ADF4030. Make sure REFIN S1 switch is off. This assumes a reference clock is provided from the same signal generator that is used with the ADF4030_EVB1 to J1 connector of ADF4030_EVB2.
7. Connect the eventual third EV-ADF4030SD1Z on top of the ADF4030_EVB2 using the Arduino connectors. Call this board **ADF4030_EVB3**.
8. Set the ADDR3, ADDR2, ADDR1, and ADDR0 switches at S1 to the off, off, on, and off positions, respectively. This sets the SPI address of the ADF4030 populating ADF4030_EVB3 to 0010, but any non 0000 and 0001 SPI address is acceptable. Using Address 0000 for EVB1 is recommended because writing Register 0x00 and Register 0x01 with this address makes the broadcast configuration for all ADF4030 ICs in the system use a 4-wire SPI. The addresses of the other two boards can be any non 0000 address.
9. Set the REF_CLK S1 switch to on to enable providing a reference clock at the J1 SMA connector to the ADF4030. Make sure the REFIN S1 switch is off. This assumes a reference clock from the same signal generator is provided and used with the ADF4030_EVB1 and the ADF4030_EVB2 to J1 connector of the ADF4030-EVB3.
10. Provide two (in case of the two ADF4030 ICs synchronization demo) or three (in case of three ADF4030 ICs synchronization demo) 100 MHz, 4 dBm clocks into the J1 SMA connector of each EV-ADF4030SD1Z from one common source. This ensures the reference clocks arriving at the ADF4030 ICs are frequency locked, and it prevents the BSYNC clocks of one ADF4030 to slew relative to the BSYNC clocks of another ADF4030. A 50 Ω load resistor to ground (R1) is populated on the evaluation board. The phase of these clocks arriving at the ADF4030 ICs does not matter, so the length of the cables connecting the source(s) to the boards does not matter. The demos are delivered with one AD9545 evaluation board. This board can be used to generate the 100 MHz clocks as follows:
    a. Supply the AD9545 evaluation board from a dedicated wall plugin. It has a 6 V, 2 A output. The AD9545 evaluation board schematic refers to an 8.5 V overprotection circuit that uses a 7.5 V Zener diode. The EV-ADF4030SD1Z wall plug has a 12 V, 2 A output. Do not use the ADF4030 wall plug to supply the AD9545 evaluation board.
    b. Provide a 100 MHz, 3 dBm clock at REFA_P or REFA_N input connectors. The AD9545 DPLL0 is configured to use any of the two inputs as reference. If this is not possible, the AD9545 DPLL0 generates the 100 MHz clocks in free run, so frequency, accuracy, and stability of the clocks depends on the crystal resonator that clocks the AD9545.
    c. Connect OUT0AP and OUT0BP outputs to the J1 SMA connector of each EV-ADF4030SD1Z. In case of the three ADF4030 synchronization demo, connect the OUT0CP output also. SMA male to SMA male cables have been provided for the setup (see Figure 27). The length of these connections does not matter. Additionally, using the N line of one or more outputs introduces a 180° phase shift in the reference clock relative to the clocks using the P line of the outputs. This can be used as well.
    d. The AD9545 evaluation board OUT0A, OUT0B, and OUT0C clocks are in CML format, 15 mA driver.
11. For the two ADF4030 sync demo, use the two provided 11 in twinax cables to connect the BSYNC4 terminal of each EV-ADF4030SD1Z to the CLK_1 and CLK_2 twinax connectors of the interposer (Figure 25). Note each P and N line of these channels has a 50 Ω to ground.
12. For the three ADF4030 sync demo, use the three provided 11 in twinax cables to connect the BSYNC2 terminal of each EV-ADF4030SD1Z to the CLK_1, CLK_2 , and CLK_3 twinax connectors of the interposer (see Figure 26). Note each P and N line of these channels has a 50 Ω to ground.

TWO AND THREE ADF4030 ICS SYNCHRONIZATION DEMOS

13. Connect the P output terminals of the interposer Channel J2, Channel J1, and Channel J9 to an oscilloscope using equal length SMA to BNC cables. Set the oscilloscope on 1 MΩ input impedance.
14. In case of the two ADF4030 sync demo, use one provided 11in twinax cable to connect ADF4030_EVB1 BSYNC6 terminal to the ADF4030_EVB2 BSYNC6 terminal. The length of this connection does not matter (Figure 25).
15. In case of the three ADF4030 sync demo, use two 11in twinax cables to connect ADF4030_EVB1 BSYNC4 and BSYNC6 terminals to the ADF4030_EVB2 BSYNC4 terminal and ADF4030_EVB3 BSYNC6 terminal, respectively. The length of these connections does not matter (see Figure 26).
16. Connect the standard USB A to mini-B cables to the SDP K1 boards. Do not connect them yet to the PC.

The description of the demo uses the BSYNC DC-coupled channels because DC coupling creates a more precise synchronization. However, AC-coupled channels can be used for this experiment as well with the parts in the script that identify the BSYNC channels used in the demo to be changed accordingly. On the ADF4030, the BSYNC0, BSYNC1, BSYNC3, BSYNC5, and BSYNC7 channels are AC-coupled, while the BSYNC2, BSYNC4, BSYNC6, BSYNC8, and BSYC9 channels are DC-coupled.

Note the following:

- The proposed reference clock architecture in Figure 27 is just one implementation example using the provided AD9545 evaluation board as the reference clock source. The system can be supplied from a signal generator at the J1 SMA connector of one board. Then, using the SMA and twinax connectors REF1_OUT, REF2_OUT, and REF3_OUT on the same board, the reference clock can fan out using LVPECL drivers to the J1 (SMA connector) or P1 (twinax connector) of the other boards. The possibilities of providing the reference clock to all boards are endless. An additional example is shown in Figure 24. Note the setting of the DIP switches.
- The reference clock and BSYNC output clocks values are 100 MHz by default. The ADF4030 python scripts provided with the demo allow full flexibility in selecting the clocks. See the Step-By-Step Demos Description section for more details.
- The connections between boards and to the interposer in Figure 25 and Figure 26 are suggestions. The ADF4030 python scripts provided with the demo allow full flexibility in selecting the connections. See the Step-By-Step Demos Description section for more details.

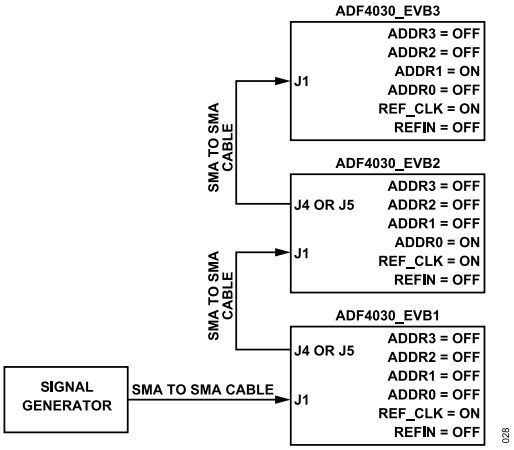


Figure 24. DIP Switch Settings and REFIN Connections for the EV-ADF4030SD1Z Evaluation Boards Using a Signal Generator

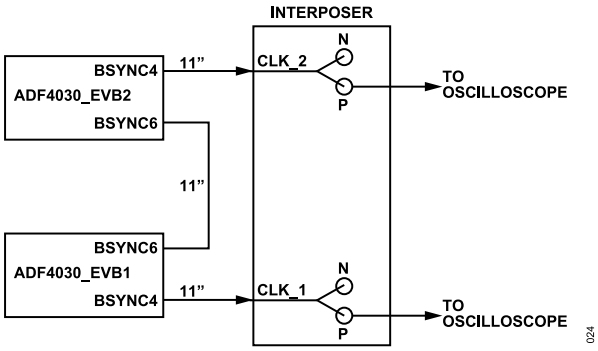


Figure 25. Two ADF4030 ICs Sync Demo Block Diagram

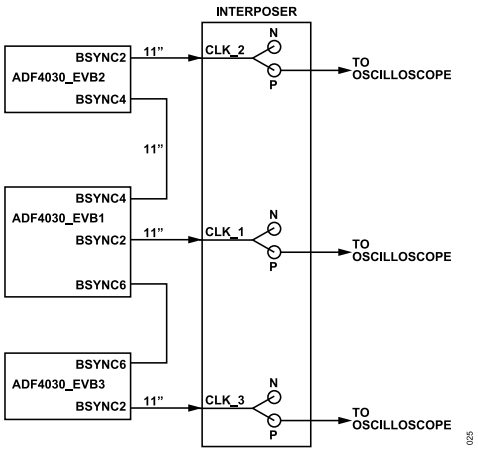


Figure 26. Three ADF4030 ICs Sync Demo Block Diagram

TWO AND THREE ADF4030 ICS SYNCHRONIZATION DEMOS

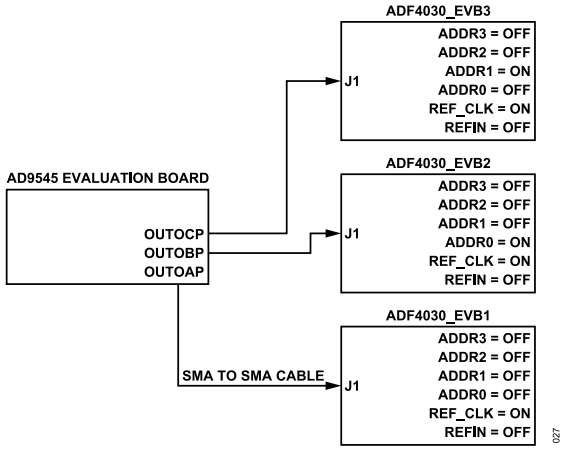


Figure 27. DIP Switch Settings and REFIN Connections for the EV-ADF4030SD1Z Evaluation Boards Using the Provided AD9545 Evaluation Board

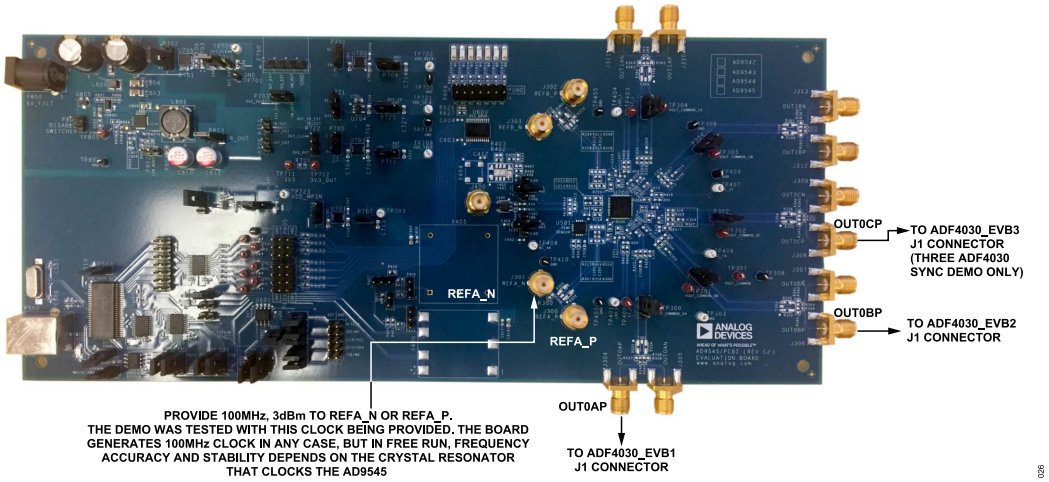


Figure 28. AD9545 Evaluation Board Connections

TWO AND THREE ADF4030 ICS SYNCHRONIZATION DEMOS

GOAL OF THE DEMOS

The ADF4030_EVB1 board generates a 100 MHz clock at a selected BSYNC channel connector. The goal of the demos is to make the other ADF4030_EVB2 and ADF4030_EVB3 boards generate 100 MHz clocks of the same phase with the clocks on ADF4030_EVB1. The clocks are generated at the selected BSYNC channels connectors. See the Step-By-Step Demos Description section for details on how to select various BSYNC channels used in the demos.

DEMOS SOFTWARE

1. Install the evaluation software and the ADF4030 plugin as presented in the Software Installation Procedures section.
2. Launch the ACE software. Click on the **Settings** button (Figure 29), then click **IPC Server** in the left menu pane. Make sure the **Server enabled** is checked, the ports have the **Number** 2357, and **Enabled** is checked (Figure 30).
3. Close ACE.

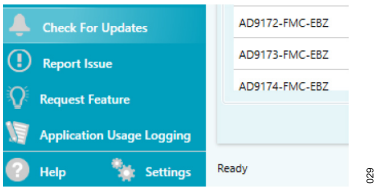


Figure 29. Settings Button on the Bottom Left Menu Pane in ACE

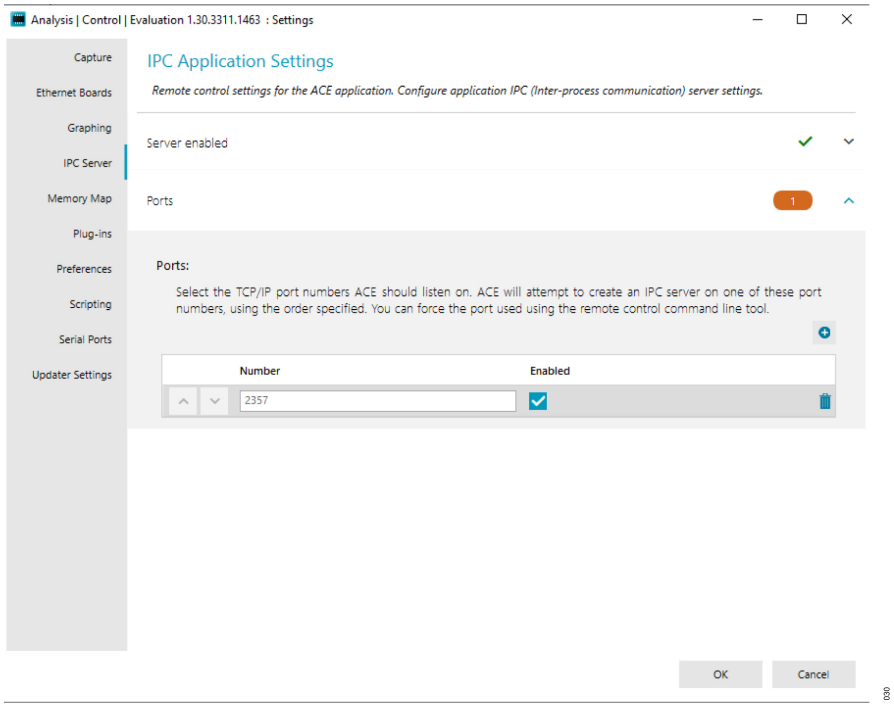


Figure 30. IPC Server Required Settings

TWO AND THREE ADF4030 ICS SYNCHRONIZATION DEMOS

STEP-BY-STEP DEMOS DESCRIPTION

Power up the AD9545 evaluation board by plugging the 6 V, 2 A AC/DC wall mount adapter into terminal P4 of the evaluation board. Make sure the provided wall mount adapter is used, as this board does not accept more than 8.5 V voltages (see Creating the Demo Bench). Important, never use the ADF4030 evaluation board wall mount adapter to power the AD9545 evaluation board.

Power up the EV-ADF4030SD1Z evaluation boards by plugging the 12 V, 2 A AC/DC wall mount adapters into the 12 V, P4 EV-ADF4030SD1Z connector of each board. Never use the ADF4030 adapters to power up the AD9545 evaluation board.

Connect the USB cables of the EV-ADF4030SD1Z evaluation boards to the PC.

Launch the ACE software. The attached hardware is shown as in Figure 8.

Double click the **ADF4030 Board** icon and the dialog box as shown in Figure 9 appears.

Go to **Tools** on the left side of the ACE menu pane and select **Script Manager** (see Figure 31).

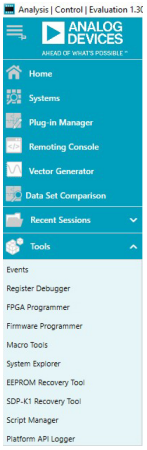


Figure 31. Script Manager Located in Tools Menu

Open the provided python scripts using the **Script Manager**. Select **Python 3** in the **IronPython** box above the python editor. Scroll down to the function called **ADF4030Demo** and enter the following demo settings:

1. REF_IN is the desired reference clock frequency applied to the ADF4030 ICs of the demo. Introduce the value expressed in Hz between 10 MHz and 250 MHz. By default, it is 100 MHz, that is REF_IN = 100e6
2. BSYNC_OUT is the desired BSYNC clock frequency that is to be synchronized. Introduce the value expressed in Hz. By default, it is 100 MHz, that is BSYNC_OUT = 100e6. Note there may be outputs that cannot be generated because the ADF4030 PLL has a VCO within 2.5 GHz ± 5% and the ODIV divider is an integer between 10 and 4095. In such cases, the script signals an error.
3. CHANNEL_ADF4030_1_to_2 represents the number of the BSYNC channels on both ADF4030_EVB1 and ADF4030_EVB2 that are connected together. By default, in the two ADF4030 synchronization demo, channel_ADF4030_1_to_2 = 6 (see Figure 25), meaning the BSYNC6 channel of the ADF4030_EVB1 is connected to the BSYNC6 channel of the ADF4030_EVB2. In the three ADF4030 synchronization demo, CHANNEL_ADF4030_1_to_2 = 4 (see Figure 26), meaning the BSYNC4 channel of the ADF4030_EVB1 is connected to the BSYNC4 channel of the ADF4030_EVB2.
4. CHANNEL_ADF4030_1_to_3 represents the number of the BSYNC channels on both ADF4030_EVB1 and ADF4030_EVB3 that are connected together in the three ADF4030 synchronization demo. By default, CHANNEL_ADF4030_1_to_3 = 6 (see Figure 26), meaning the BSYNC6 channel of the ADF4030_EVB1 is connected to the BSYNC6 channel of the ADF4030_EVB3.
5. CHANNEL_ADF4030_TO_OSC represents the number of the BSYNC channels on all of the ADF4030 ICs of the demos that are connected to the interposer and, ultimately, to the oscilloscope. By default, in the two ADF4030 synchronization demo, CHANNEL_ADF4030_TO_OSC = 4 (see Figure 25), meaning the BSYNC4 channels of both EV-ADF4030SD1Z boards are connected to the interposer. In the three ADF4030 synchronization demo, CHANNEL_ADF4030_TO_OSC = 2 (see Figure 26), meaning the BSYNC2 channels of all three EV-ADF4030SD1Z boards are connected to the interposer.
6. Set EVB1_ADDR, EVB2_ADDR, and EVB3_ADDR to the ADDR pins setting of various boards. It is recommended to set EVB1_ADDR to 0 because this ensures the SPI ports of all ADF4030 ICs in the system are set to 4-wire mode automatically.

INITIALIZE THE EV-ADF4030SD1Z EVALUATION BOARDS

Every EV-ADF4030SD1Z of the sync demos must be initialized. Execute the following steps:

1. Double-click the **ADF4030 Board** icon as shown in Figure 8.
2. Double-click the **ADF4030** icon (see Figure 9) to open the main control dialog box as shown in Figure 10.
3. In the top left of the user interface, the CHIP ADDRESS box indicates the address to identify the board to be initialized (Figure 32).
4. Select the address of the ADF4030_EVB1 first. Click the **Read All** button, then click the **Load Default Registers** button, and the **Apply Changes** button. The order of these operations is important to make sure the ADF4030 on EVB1 is initialized correctly. If nondefault REFIN = 100 MHz, BSYNC = 100 MHz values are pursued, change the ADF4030_EVB1 configuration

TWO AND THREE ADF4030 ICS SYNCHRONIZATION DEMOS

as desired. Click **Apply Changes** and then **CHECK LOCK STATUS**. Both the **REF OK** and **VCO LOCK** green LEDs must turn on. Either of the green LEDs failing to light signifies an error. Review the REFIN clock to ensure it is valid.

5. Select the address of the ADF4030_EVB2. Follow the exact operations from Step 4.
6. Select the address of the ADF4030_EVB3 (in case of the three ADF4030 ICs synchronization demo). Follow the exact operations from Step 4.

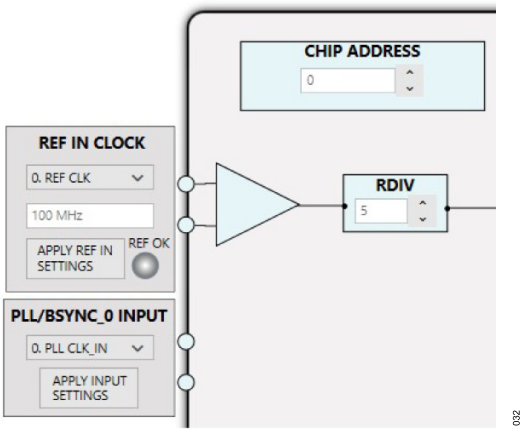


Figure 32. Chip Address Window is on the Top Left of the User Interface

EXECUTE THE PYTHON SCRIPT

Click the Play button (external). In several seconds, the script finishes the execution. On the oscilloscope, the BSYNC4 (in case of two ADF4030 sync demo) and BSYNC2 (in case of three ADF4030 sync demo) clocks created by all EV-ADF4030SD1Z evaluation boards are aligned. Figure 33 and Figure 34 present the results obtained after executing the two ADF4030 sync demo script. Executing the three ADF4030 sync demo provides similar results on three clocks.

The oscilloscope is set to average 1000 times both BSYNC4 clocks. The vertical scale of the averages is set to 10 mV/div (not 50 mV/div as in Figure 33). The offset is set to 150 mV, which is the same offset as in Figure 33. The time scale is reduced from 2 ns/div to 5 ps/div, and the alignment is measured to be under 1 ps.

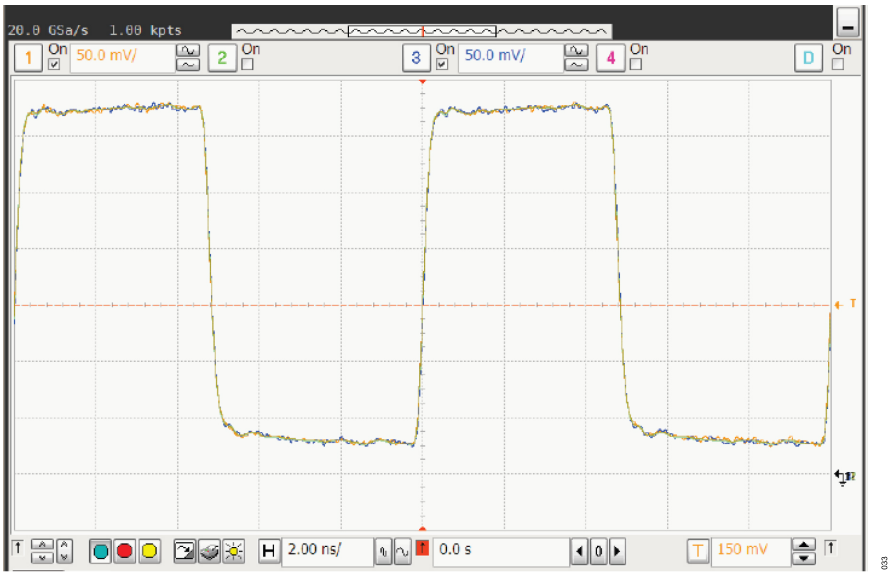


Figure 33. Two Aligned BSYNC4 Clocks after Two ADF4030 Sync Demo Scripts Were Executed (2 ns/div, 50 mV/div)

TWO AND THREE ADF4030 ICS SYNCHRONIZATION DEMOS

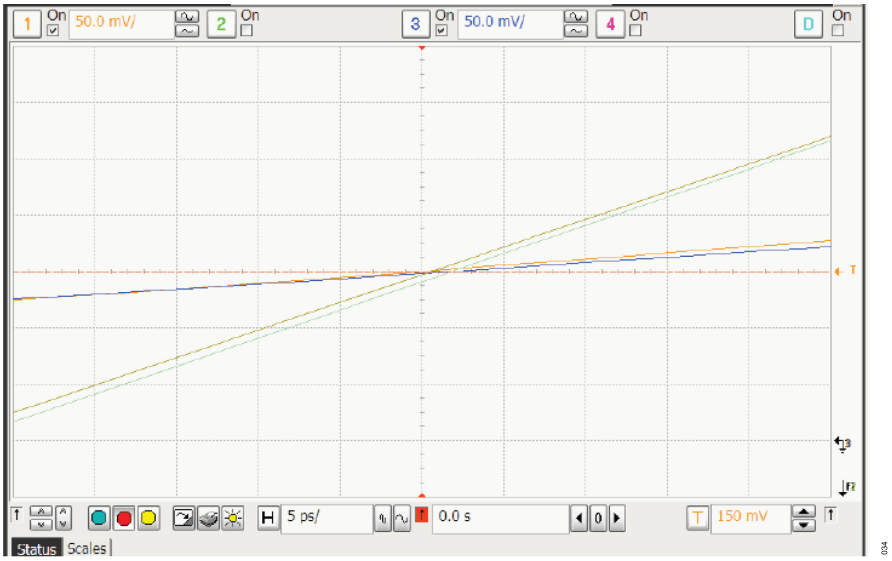


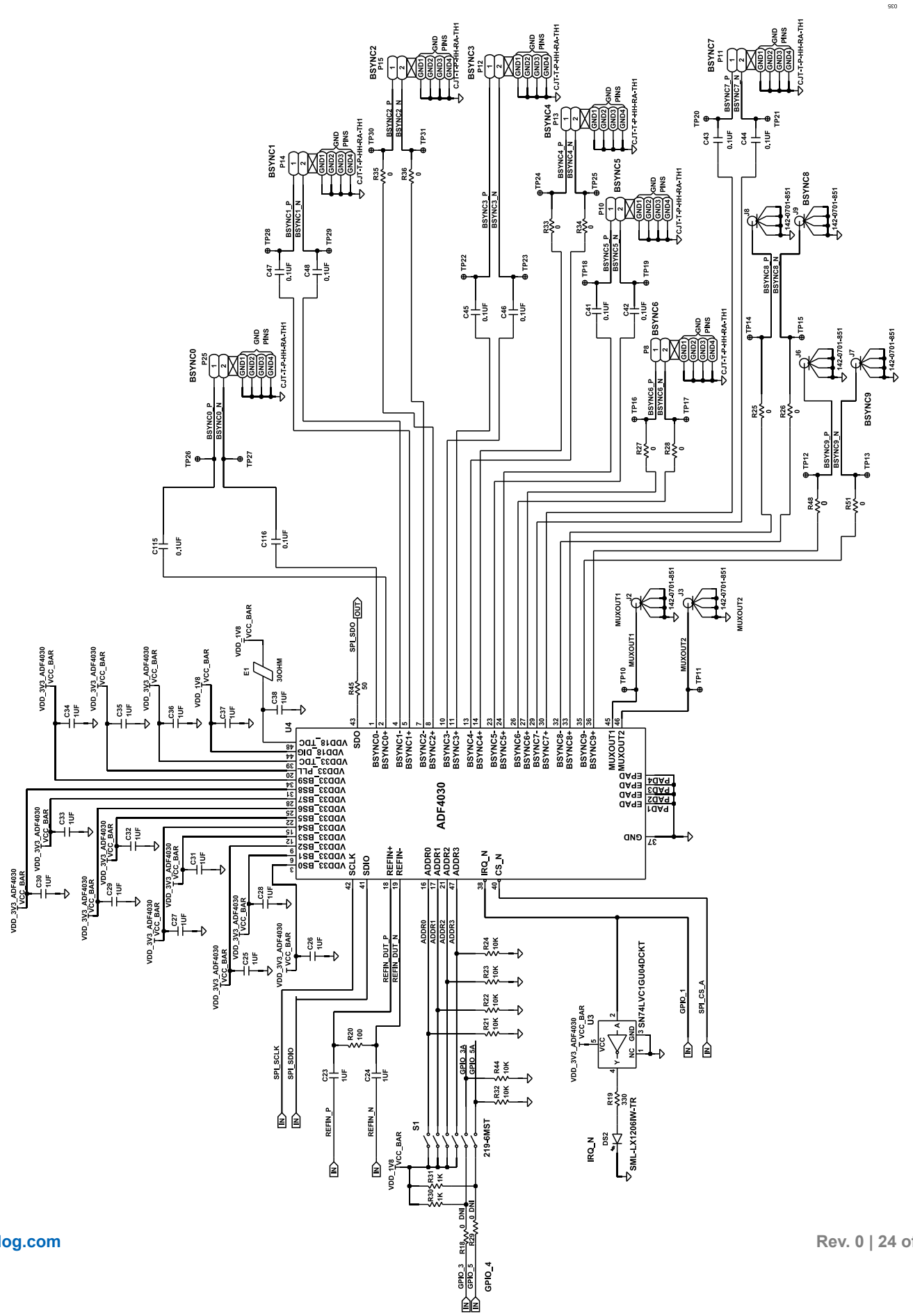
Figure 34. Averaged Clocks (Green and Brown Signals) of Two BSYNC4 Aligned Clocks Aligned to <1 ps

Note the messages printed on the bottom of the ACE screen as in the following table:

Table 6. Script Output Messages During Execution

Message	Comment
out_bsync 100000000.0	EVB1 BSYNC frequency as calculated by the script
out_bsync 100000000.0	EVB2 BSYNC frequency as calculated by the script
Set Direction: Board1.BSYNC6 → Board2.BSYNC6	EVB1 BSYNC6 transmits clock to EVB2 BSYNC6
TDC Meas Board1: BSYNC4 →BSYNC6 = 4379.696 ps	EVB1 BSYNC6 to BSYNC4 delay is 4379.696 ps
TDC Meas Board2: BSYNC6 → BSYNC4 = −314.755 ps	EVB2 BSYNC4 to BSYNC6 delay is −314.755 ps
Set Direction: Board2.BSYNC6 → Board1.BSYNC6	EVB2 BSYNC6 transmits clock to EVB1 BSYNC6
TDC Meas Board2: BSYNC6 → BSYNC4 = −3632.800 ps	EVB2 BSYNC4 to BSYNC6 delay is −3632.800 ps
TDC Meas Board1: BSYNC4 → BSYNC6 = 2869.188 ps	EVB1 BSYNC6 to BSYNC4 delay is 2869.188 ps
Set Direction: Board1.BSYNC6 → Board2.BSYNC6	EVB1 BSYNC6 transmits clock to EVB2 BSYNC6
Cable Delay = 2414.277 ps	Script estimates the trip delay of EVB1 BSYNC6 to EVB2 BSYNC6 is 2414.277 ps
Pin Alignment: Board1.BSYNC4-BSYNC6 = 2414.832 ps	−2414.832 ps phase offset in EVB1 BSYNC6 is introduced
Alignment Result: Board1.BSYNC4-BSYNC6 = 0.556 ps	EVB1 BSYNC6 to BSYNC4 delay is 0.556 ps
Pin Alignment: Board2.BSYNC6-BSYNC4 = 0.253 ps	EVB2 BSYNC4 to BSYNC6 delay is 0.253 ps
Alignment Result: Board2.BSYNC6-BSYNC4 = 0.253 ps	

EVALUATION BOARD SCHEMATICS AND ARTWORK



EVALUATION BOARD SCHEMATICS AND ARTWORK

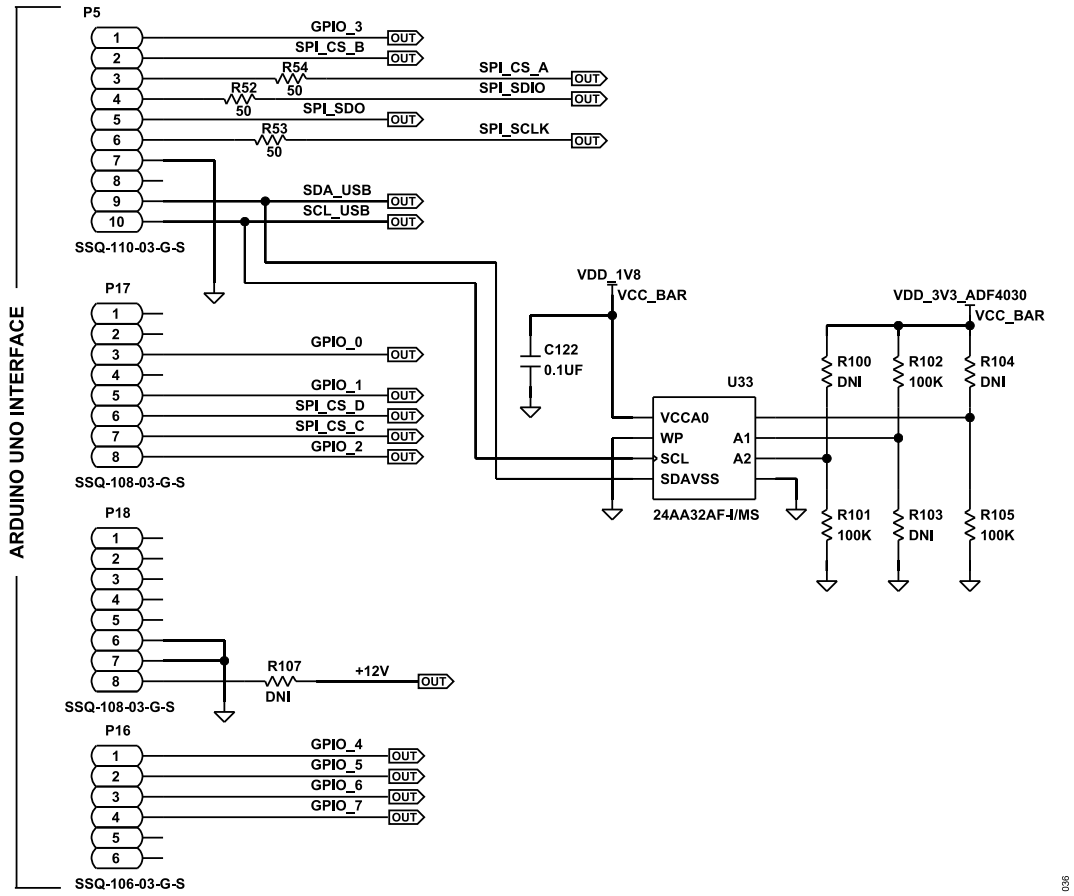


Figure 36. ADF4030 Evaluation Board: Arduino Connectors

EVALUATION BOARD SCHEMATICS AND ARTWORK

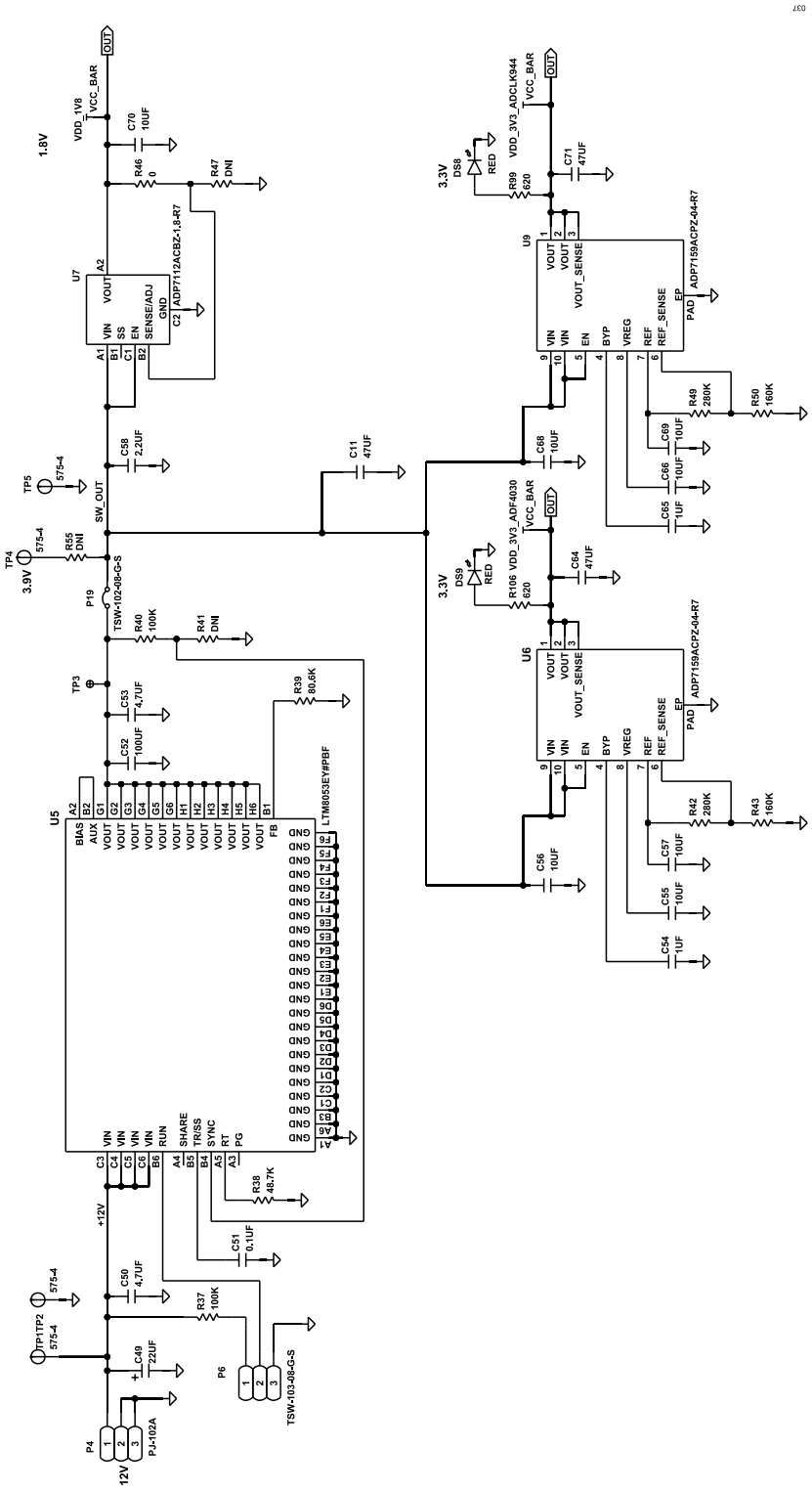


Figure 37. ADF4030 Evaluation Board: Power Supply Schematic

EVALUATION BOARD SCHEMATICS AND ARTWORK

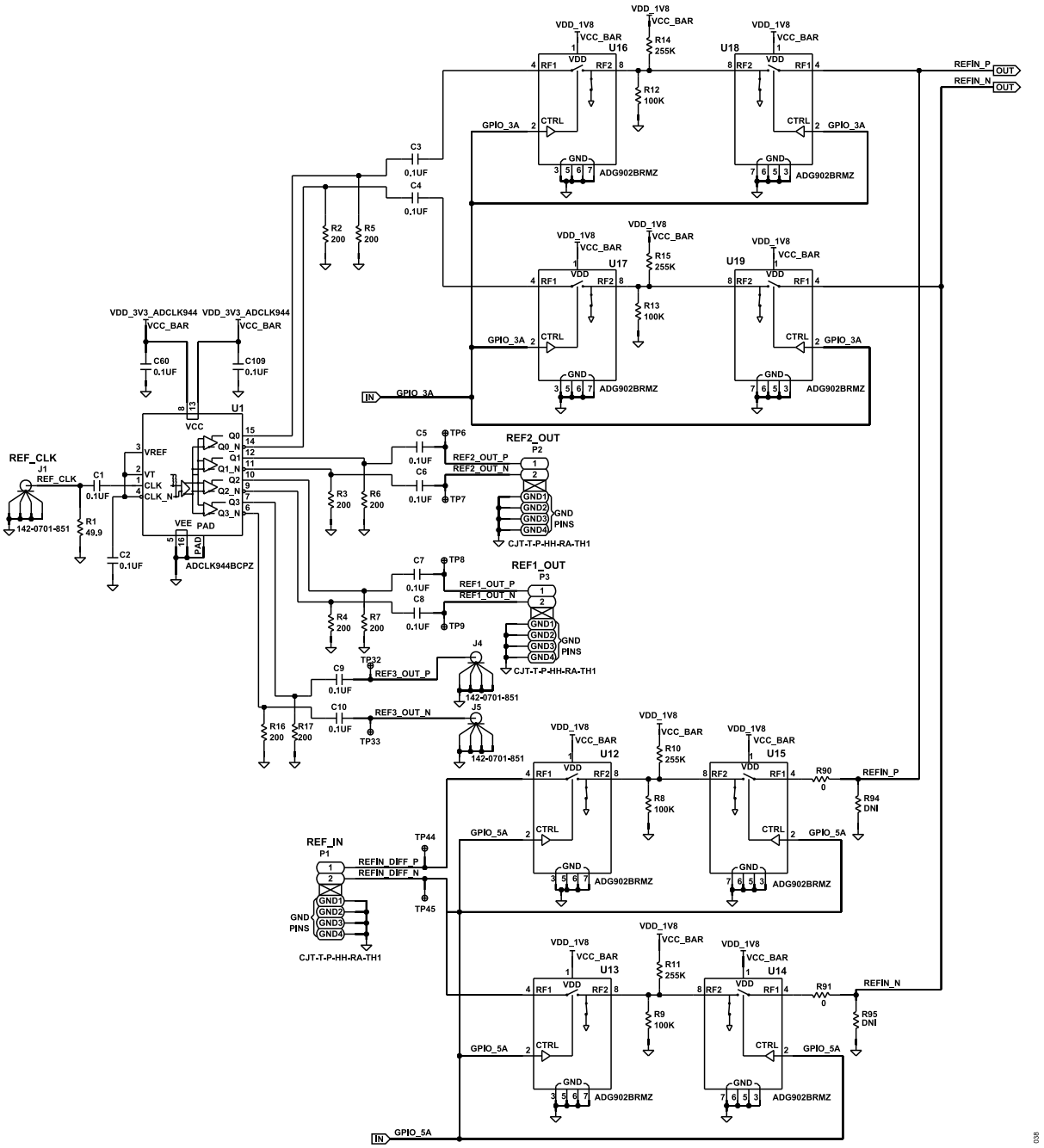


Figure 38. ADF4030 Evaluation Board: REFIN Schematic

EVALUATION BOARD SCHEMATICS AND ARTWORK

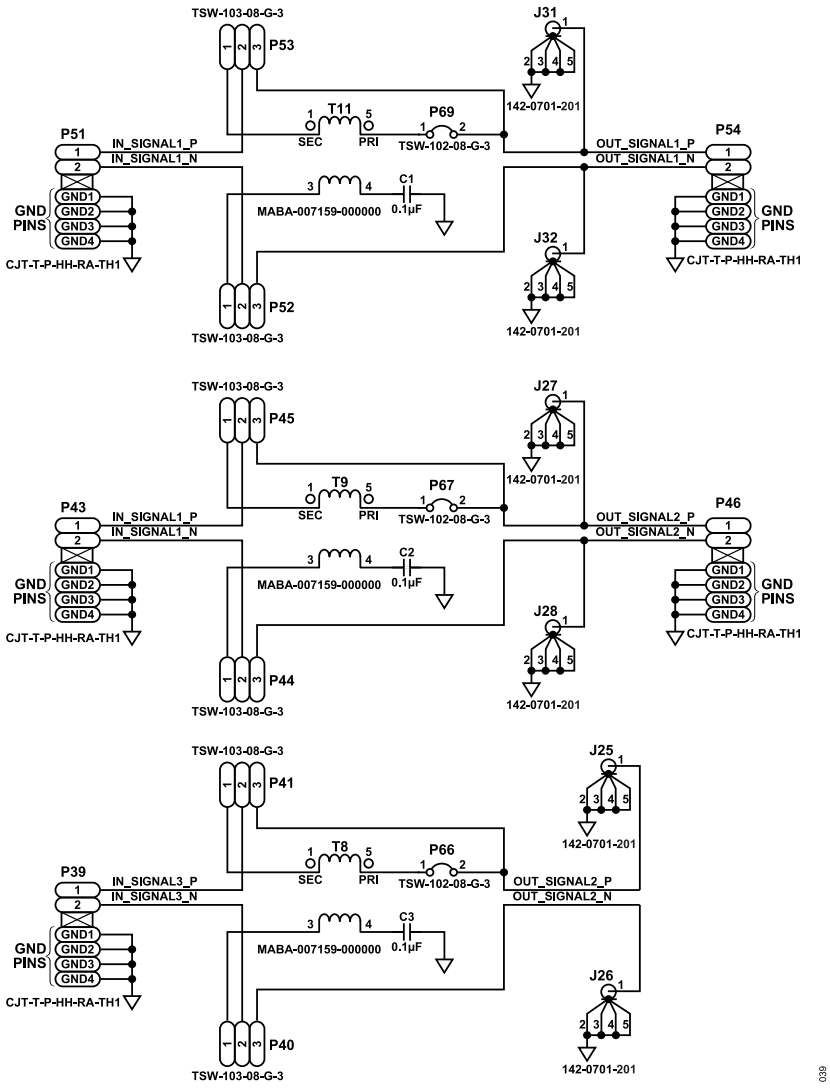


Figure 39. Interposer: BSYNC Channels Schematic

EVALUATION BOARD SCHEMATICS AND ARTWORK

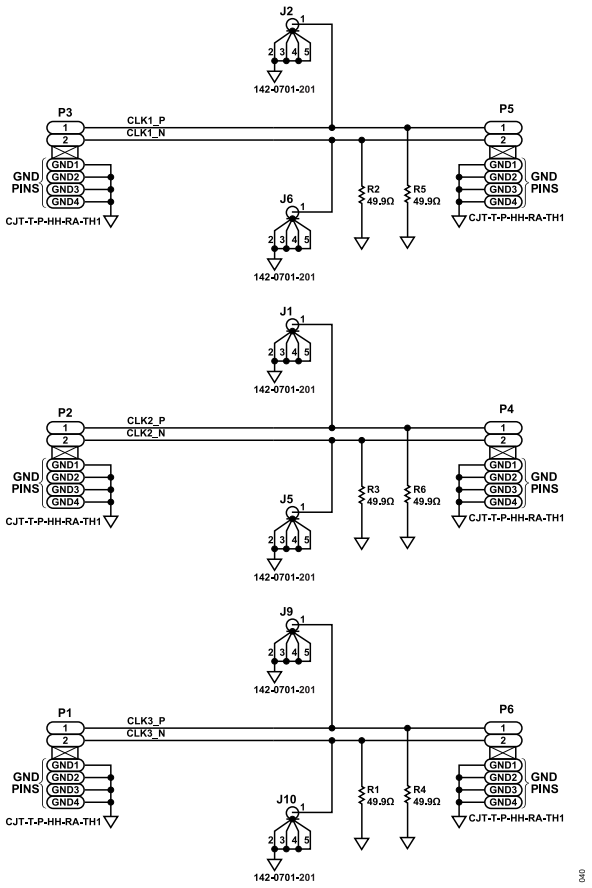


Figure 40. Interposer: CLK_1,2,3 Schematic

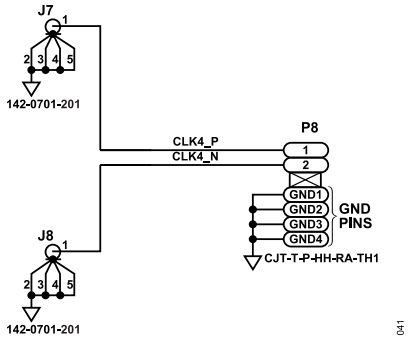


Figure 41. Interposer: CLK_4 Schematic

EVALUATION BOARD SCHEMATICS AND ARTWORK

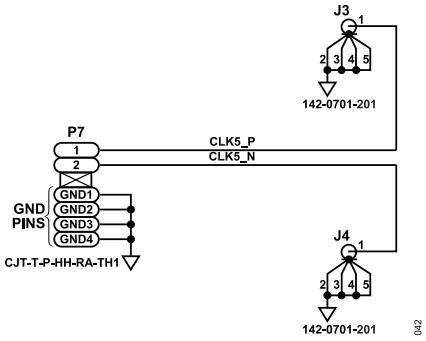


Figure 42. Interposer: CLK_5 Schematic

ORDERING INFORMATION

BILL OF MATERIALS

Qty	Designator	Description	Manufacturer	Part Number
24	C1, C2, C3, C4, C5, C6, C7, C8, C9, C10, C41, C42, C43, C44, C45, C46, C47, C48, C51, C60, C109, C115, C116, C122	Ceramic capacitors, 0.1 µF, 16 V, 10%, X7R, 0402	American Technical Ceramics	530L104KT16T
3	C11, C64, C71	Ceramic capacitors 47 µF, 6.3 V, 20%, X5R, 0603	Murata Manufacturing Co., Ltd.	GRM188R60J476ME15D
2	C23, C24	Ceramic capacitors 1 µF, 16 V, 10%, X5R, 0402	TAIYO YUDEN	EMK105BJ105KV-F
16	C25, C26, C27, C28, C29, C30,C31, C32, C33, C34, C35, C36, C37, C38, C54, C65	Ceramic capacitors 1 µF, 10 V, 10%, X5R, 0402	YAGEO	CC0402KRX5R6BB105
1	C49	Capacitor aluminum electrolytic, 22 µF, 63 V, 20%, 6.3 mm × 7.7 mm, AEC-Q200, 1.2 Ω ,120 MA, 2000 H	Panasonic	EEEFN1J220XP
2	C50, C53	Ceramic capacitors 4.7 µF, 50 V, 10%, X7R, 0805	Murata Manufacturing Co., Ltd.	GRM21BZ71H475KE15L
1	C52	Ceramic capacitor 100 µF, 6.3 V, 10%, X5R, 1206	Murata Manufacturing Co., Ltd.	GRM31CR60J107KEA8L
7	C55, C56, C57, C66, C68, C69, C70	Ceramic capacitors 10 µF, 10 V, 20%, X5R, 0402	Samsung	CL05A106MP5NUNC
1	C58	Ceramic capacitor 2.2 µF, 10 V, 10%, X5R, 0402	Murata Manufacturing Co., Ltd.	GRM155R61A225KE95D
3	DS2, DS8, DS9	LED, 635 nm, red, differential, 1206, surface-mount device (SMD)	Lumex	SML-LX1206IW-TR
1	E1	Inductor chip ferrite bead	Murata Manufacturing Co., Ltd.	BLM15AX300SN1D
9	J1, J2, J3, J4, J5, J6, J7, J8, J9	Connector (CONN)-PCB, SMA, 50 Ω, end launch jack receptacle, for high speed app use, ALT symbols	Cinch	142-0701-851
11	P1, P2, P3, P8, P10, P11, P12, P13, P14, P15, P25	CONN-PCB jack, right angle 0 Hz to 4 GHz 100 Ω circular twinax	Samtec	CJT-T-P-HH-RA-TH1
1	P16	CONN-PCB receptacle 25 mil square post, 2.54 mm pitch	Samtec	SSQ-106-03-G-S
2	P17, P18	CONN-PCB receptacle 25 mil square post 2.54 mm pitch	Samtec	SSQ-108-03-G-S
1	P19	CONN-PCB, header, 2 position	Samtec	TSW-102-08-G-S
1	P4	CONN-PCB, DC power jack, through-hole	CUI	PJ-102A
1	P5	CONN-PCB, receptacle, 25 mil, square post 2.54 mm pitch	Samtec	SSQ-110-03-G-S
1	P6	CONN-PCB, Berg-style header connector, straight, male, 3P	Samtec	TSW-103-08-G-S
1	R1	Resistor, SMD, 49.9 Ω, 1%, 1/10 W, 0402, AEC-Q200	Panasonic	ERJ-2RKF49R9X
4	R10, R11, R14, R15	Resistor SMD 255 KΩ 1%, 1/10 W, 0402, AEC-Q200	Panasonic	ERJ-2RKF2553X
9	R8, R9, R12, R13, R37, R40, R101, R102, R105	Resistor SMD 100 KΩ 1%, 1/16 W, 0402	MULTICOMP	MC 0.0625W 0402 1% 100K
2	R99, R106	Resistor SMD 620 Ω 5%, 1/10 W, 0402 AEC-Q200	Panasonic	ERJ-2GEJ621X
8	R2, R3, R4, R5, R6, R7, R16, R17	Resistor SMD 200 Ω 1%, 1/10 W 0402 AEC-Q200	Panasonic	ERJ-2RKF2000X
1	R19	Resistor SMD 330 Ω 5%, 1/10 W 0402 AEC-Q200	Panasonic	ERJ-2GEJ331X
1	R20	Resistor SMD 100 Ω 1%, 1/16 W 0402	Venkel	CR0402-16W-1000FPT
6	R21, R22, R23, R24, R32, R44	Resistor SMD 10K Ω 1%, 1/10 W 0402 AEC-Q200	Panasonic	ERJ-2RKF1002X
13	R25, R26, R27, R28, R33, R34, R35, R36, R46, R48, R51, R90, R91	Resistor SMD 0 Ω jumper, 1/10 W, 0402, AEC-Q200	Panasonic	ERJ-2GE0R00X
2	R30, R31	Resistor SMD 1 KΩ 1% 1/16 W, 0402, AEC-Q200	Vishay Intertechnology	CRCW04021K00FKED
1	R38	Resistor SMD 48.7 KΩ 1%, 1/10 W, 0402, AEC-Q200	Panasonic	ERJ-2RKF4872X
1	R39	Resistor SMD 80.6 KΩ 1%, 1/10 W, 0402, AEC-Q200	Panasonic	ERJ-2RKF8062X
2	R42, R49	Resistor SMD 280 KΩ 1%, 1/16 W, 0402, AEC-Q200	Vishay Intertechnology	CRCW0402280KFKED
2	R43, R50	Resistor SMD 160 KΩ, 1%, 1/10 W, 0402, AEC-Q200	Panasonic	ERJ-2RKF1603X
4	R45, R52, R53, R54	Resistor SMD 50 Ω 1%, ½ 0W, 0402, high frequency	Vishay Intertechnology	FC0402E50R0FST1
1	S1	6-position, SPST, DIP, autoplaceable	CTS Corporation	219-6MST

ORDERING INFORMATION

Qty	Designator	Description	Manufacturer	Part Number
4	TP1, TP2, TP4, TP5	CONN-PCB, banana jack	KEYSTONE ELECTRONICS	575-4
1	U1	2.5 V/3.3 V, four LVPECL outputs, SiGE clock fanout buffer	Analog Devices, Inc.	ADCLK944BCPZ-R7
8	U12, U13, U14, U15, U16, U17, U18, U19	1 Hz to 4.5 GHz, 40 dB off isolation at 1 Ghz, 17 dBm P1dB at 1 GHz SPST switch	Analog Devices	ADG902BRMZ
1	U3	IC-transistor-to-transistor (TTL) single inverter gate	Texas Instruments	SN74LVC1GU04DCKT
1	U33	IC-CMOS, 32 K, inter-ic bus (I^2C), serial EEPROM with quarter-array write protect	Microchip Technology	24AA32AF-I/MS
1	U4	10-channel precision synchronizer	Analog Devices	ADF4030
1	U5	40 V_{IN}, 3.5 A step-down silent switcher µModule regulator	Analog Devices	LTM8053EY#PBF
2	U6, U9	2 A ultra-low noise, high PSRR, RF linear regulator, 1.2 V to 3.3 V V_{OUT}	Analog Devices	ADP7159ACPZ-04-R7
1	U7	20 V, 200 mA, low noise, CMOS LDO linear regulator	Analog Devices	ADP7112ACBZ-1.8-R7
2		Socket, 2 position, 0.100 pitch, shunt connector, black, open top	Samtec	SNT-100-BK-G-H
2		Round aluminum standoff, 4-40 × 3/4	McMASTER-CARR	93330A437
2		Machine screw, pan head, Phillips with lock washer, 4-40, 1/4 in	McMASTER CARR	95345A023
9	R18, R29, R41, R55, R94, R95, R100, R103, R104	Resistor SMD, 0 Ω, jumper, 1/10 W, 0402, AEC-Q200	Panasonic	ERJ-2GE0R00X
1	R107	Resistor SMD, 0 Ω, 3 W, 2512	TE Connectivity	3522ZR
1	R47	Resistor SMD, 200 KΩ, 1%, 1/10 W 0402 AEC-Q200	Panasonic	ERJ-2RKF2003X

ESD Caution
ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.