SHARC+ Single Core High Performance DSP (Up to 1 GHz)

Preliminary Technical Data

ADSP-21560/21561/21564/21568

SYSTEM FEATURES

Enhanced SHARC+ high performance floating-point core
- **Up to 1 GHz**
- **5 Mb (640 kB) Level 1 (L1) SRAM memory with parity (optional ability to configure as cache)**
- **32-bit, 40-bit, and 64-bit floating-point support**
- **32-bit fixed point**
- **Byte, short word, word, long word addressed**

Powerful DMA system

On-chip memory protection

Integrated safety features

17 mm × 17 mm, 400-ball CSP_BGA (0.8 mm pitch), RoHS compliant

120-lead LQFP_EP (0.4 mm pitch), RoHS compliant

Low system power across automotive temperature range

3.3 V I/O with no power sequencing requirement

MEMORY

Large on-chip Level 2 (L2) SRAM with parity, up to 16 Mb (2 MB)

xSPI peripheral supports HyperBus connectivity to extend system memory

ADDITIONAL FEATURES

Security and Protection
- **Crypto hardware accelerators**
- **Fast secure boot with IP protection**

Enhanced FIR and IIR accelerators running up to 1 GHz

APPLICATIONS

Automotive: audio amplifier, head unit, ANC/RNC, rear seat entertainment, digital cockpit, ADAS

Consumer: speakers, sound bars, AVRs, conferencing systems, mixing consoles, microphone arrays, headphones

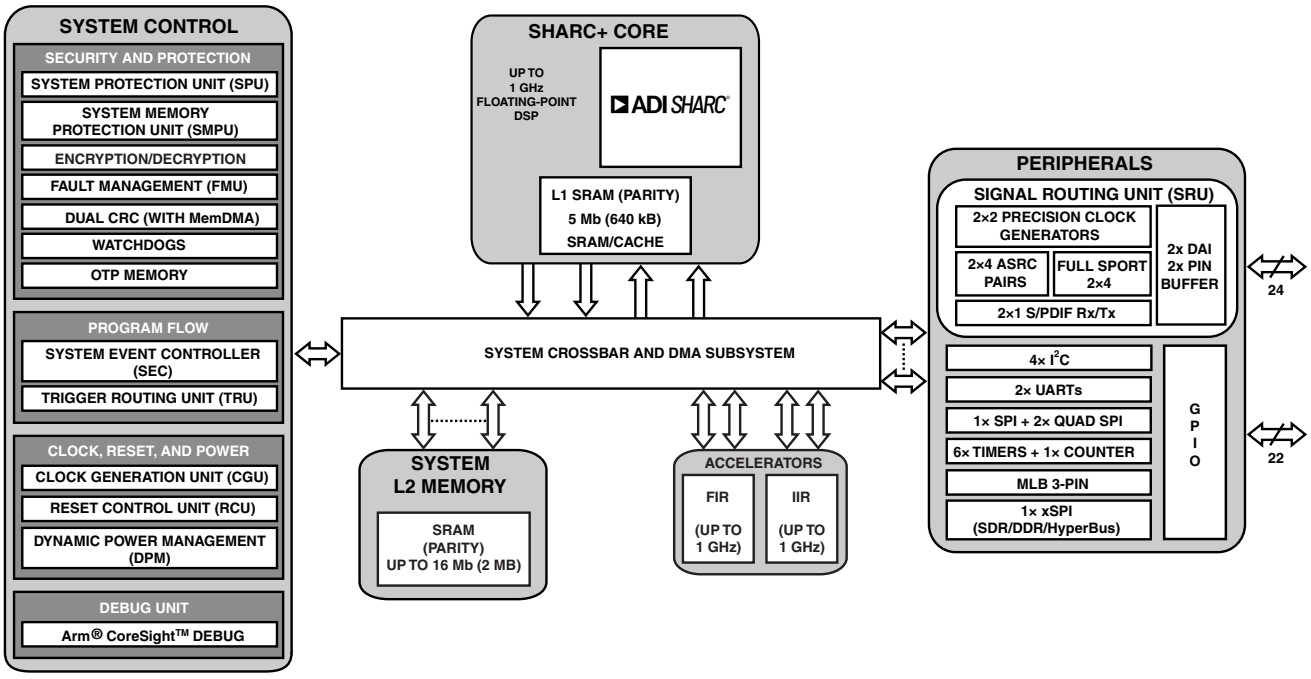

Figure 1. Processor Block Diagram

Rev. PrD **Document Feedback**

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TABLE OF CONTENTS

REVISION HISTORY

3/2025—Rev. PrC to Rev. PrD

Changed all processor speeds of 933 MHz to 1 GHz throughout data sheet.

Added Internal Timer Signal Routing 25

Added missing signals to ADSP-21560/21561/21564/21568 Designer Quick Reference 26

Changes to Preliminary Operating Conditions 30

Changes to Clock Operating Conditions 31

Changes to Preliminary Electrical Characteristics 33

Changes to $I_{DD\_INT\_TOT}$ equation in Total Internal Power Dissipation 35

Added specifications to Tables 16, 17, and 18 in Total Internal Power Dissipation 35

Changes to Clock Current 36

Changes to xSPI Port—Master Timing 55

Updated Figures 35 and 36 in Output Drive Currents 67

Updated Figures 40 and 41 in Capacitive Loading 68

Added model to Pre Release Products 81

GENERAL DESCRIPTION

Reaching speeds of up to 1 GHz, the ADSP-21560/21561/21564/21568 processors are members of the SHARC® family of products. The ADSP-21560/21561/21564/21568 processors are based on the SHARC+® single core. The ADSP-21560/21561/21564/21568 SHARC processors are members of the SIMD SHARC family of digital signal processors (DSPs) that feature Analog Devices, Inc., Super Harvard Architecture. These 32-bit/40-bit/64-bit floating-point processors are optimized for high performance audio/floating-point applications with large on-chip static random-access memory (SRAM), multiple internal buses that eliminate input/output (I/O) bottlenecks, and innovative digital audio interfaces (DAI).

The SHARC+ core includes cache enhancements and branch prediction, while maintaining instruction set compatibility to previous SHARC products.

By integrating a rich set of industry-leading system peripherals and memory (see Table 1), the SHARC+ processor is the platform of choice for applications that require programmability similar to reduced instruction set computing (RISC), multimedia support, and leading edge signal processing in one integrated package. These applications span a wide array of markets, including automotive, professional audio, and industrial-based applications that require high floating-point performance.

Table 1. Processor Features

Processor Feature	ADSP-21560	ADSP-21561	ADSP-21564	ADSP-21568
SHARC+ Core (MHz Maximum)[1]	600, 800	800, 1000	800, 1000	1000
SHARC L1 SRAM (kB)	640	640	640	640
System Memory				
L2 SRAM (kB)	1024	1536	2048	2048
HyperBus Support via xSPI	Yes	Yes	Yes	Yes
DAI (Includes SRU)	2	2	2	2
Full SPORTs	2 × 4	2 × 4	2 × 4	2 × 4
S/PDIF Rx/Tx	2 × 1	2 × 1	2 × 1	2 × 1
ASRCs	2 × 4	2 × 4	2 × 4	2 × 4
Precision Clock Generators	2 × 2	2 × 2	2 × 2	2 × 2
Buffers	2 × 12	2 × 12	2 × 12	2 × 12
Hardware Accelerators				
FIR/IIR	Yes	Yes	Yes	Yes
Security Crypto Engine	Yes	Yes	Yes	Yes
I^2C (TWI)	4	4	4	4
SPI	1	1	1	1
Quad SPI	2	2	2	2
xSPI	1	1	1	1
UARTs	2	2	2	2
General-Purpose Timer[2]	6	6	6	6
General-Purpose Counter	1	1	1	1
Watchdog Timer	2	2	2	2
MLB 3-pin	Automotive models only	Automotive models only	Automotive models only	Automotive models only
GPIO Ports	Port A to Port B	Port A to Port B	Port A to Port B	Port A to Port B
GPIO + DAI Pins	22 + 24	22 + 24	22 + 24	22 + 24
Package Options	120-lead LQFP_EP	120-lead LQFP_EP	120-lead LQFP_EP	400-ball CSP_BGA

[1] The values refer to different speed grades.
[2] Refer to Table 12 for internal timer signal routing.

SHARC PROCESSOR

The SHARC processor integrates a SHARC+ SIMD core, L1 memory crossbar, I-cache/D-cache controller, L1 memory blocks, and the requester/completer ports, as shown in Figure 2. The SHARC+ SIMD core block diagram is shown in Figure 3.

The SHARC processor supports a modified Harvard architecture in combination with a hierarchical memory structure. L1 memories typically operate at the full processor speed with little or no latency.

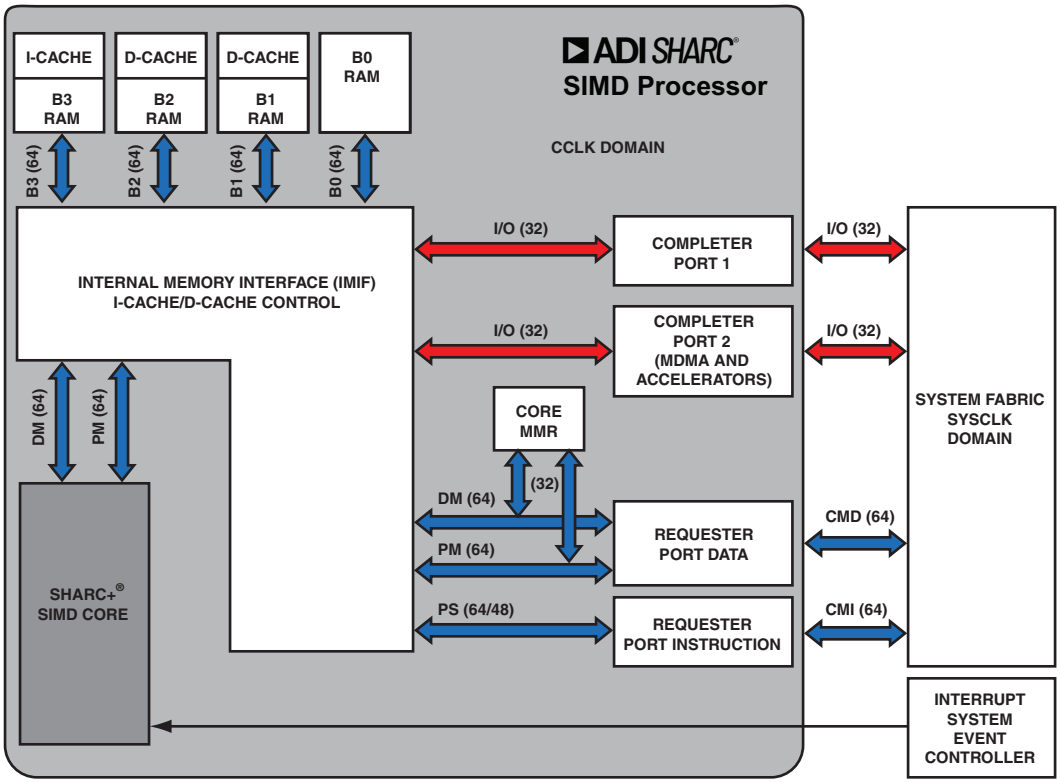

Figure 2. SHARC Processor Block Diagram

L1 Memory

Figure 4 shows the ADSP-21560/21561/21564/21568 memory map. The SHARC+ core has a tightly coupled 5 Mb L1 SRAM. The SHARC+ core can access code and data in a single cycle from this memory space.

In the SHARC+ core private address space, the core has L1 memory.

SHARC+ core memory-mapped register (CMMR) address space is 0x0000 0000 through 0x0003 FFFF in normal word (32-bit). Each block can be configured for different combinations of code and data storage. Of the 5 Mb SRAM, up to 1 Mb can be configured for data memory (DM), program memory (PM), and instruction cache each. Each memory block supports single-cycle, independent accesses by the core processor and I/O processor. The memory architecture, in combination with its separate on-chip buses, allows two data transfers from the core and one from the direct memory access (DMA) engine in a single cycle.

The SRAM of the processor can be configured as a maximum of 160k words of 32-bit data, 320k words of 16-bit data, 106.7k words of 48-bit instructions (or 40-bit data), or combinations of different word sizes up to 5 Mb. All of the memory can be accessed as 8-bit, 16-bit, 32-bit, 48-bit, or 64-bit words. Support of a 16-bit floating-point storage format doubles the amount of data that can be stored on chip.

Conversion between the 32-bit floating-point and 16-bit floating-point formats is performed in a single instruction. Whereas each memory block can store combinations of code and data, accesses are most efficient when one block stores data using the DM bus for transfers, and the other block stores instructions and data using the PM bus for transfers.

Using the DM and PM buses, with each bus dedicated to a memory block, assures single-cycle execution with two data transfers. In this case, the instruction must be available in the cache. The system configuration is flexible, but a typical configuration is 512 kb DM, 128 kb PM, and 128 kb of instruction

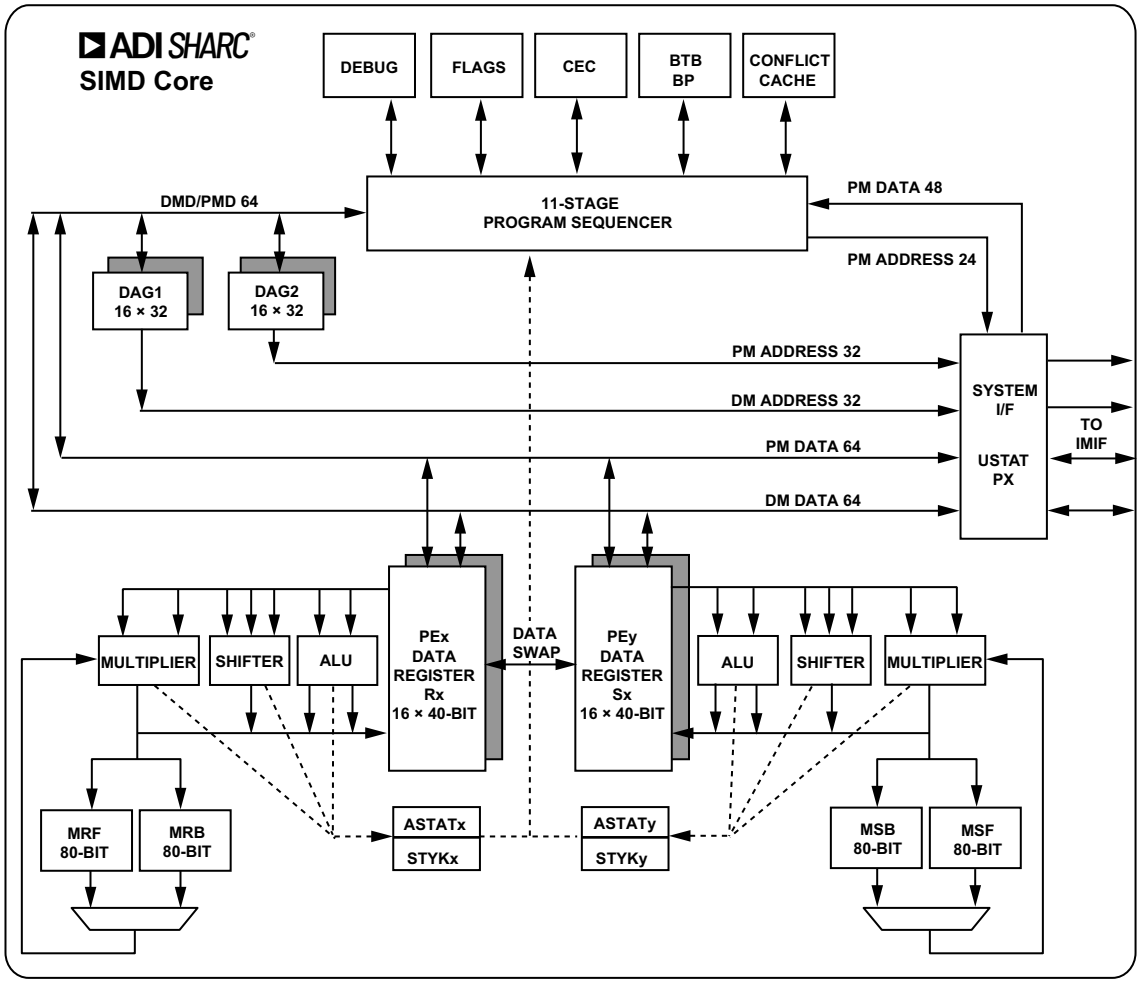

Figure 3. SHARC+ SIMD Core Block Diagram

cache, with the remaining L1 memory configured as SRAM. Each addressable memory space outside the L1 memory can be accessed either directly or via cache.

The memory map in Table 2 gives the L1 memory address space and shows multiple L1 memory blocks offering a configurable mix of SRAM and cache.

L1 Requester and Completer Ports

The SHARC+ core has two requester/completer ports to and from the system fabric. One requester port fetches instructions. The second requester port drives data to the system world. Completer Port 1 together with Completer Port 2 memory direct memory access (high speed MDMA) run conflict free access to the individual memory blocks. For the completer port addresses, refer to the L1 memory address map in Table 2.

L1 On-Chip Memory Bandwidth

The internal memory architecture allows programs to have four accesses at the same time to any of the four blocks, assuming no block conflicts. The total bandwidth is realized using both the DMD and PMD buses (2 × 64-bits CCLK speed and 2 × 32-bit SYSCLK speed).

Instruction and Data Cache

The ADSP-21560/21561/21564/21568 processors also include a traditional instruction cache (I-cache) and two data caches (D-caches, one each for PM/DM) with parity support for all caches. These caches support one instruction access and two data accesses over the DM and PM buses per CCLK cycle. The cache controllers automatically manage the configured L1 memory. The system can configure part of the L1 memory for automatic management by the cache controllers. The sizes of these caches are independently configurable from 0 to 128 kB each. The memory not managed by the cache controllers is directly addressable by the processors. The controllers ensure the data

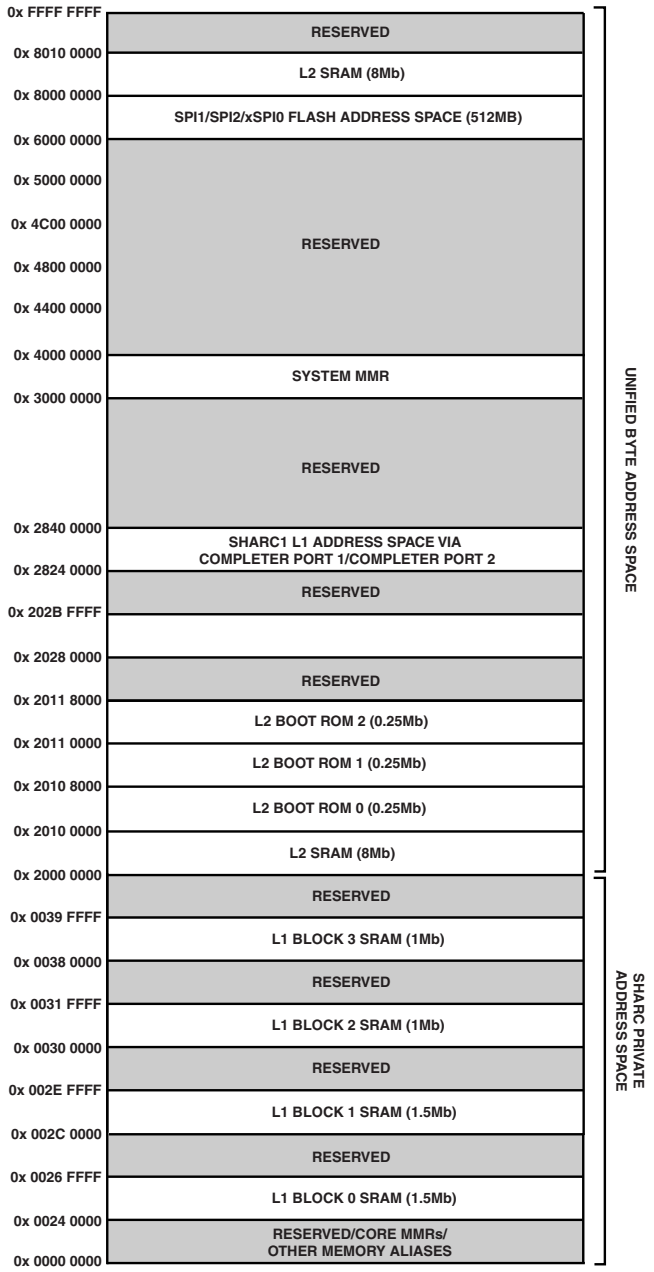

Figure 4. ADSP-21560/21561/21564/21568 Memory Map

coherence between the two data caches. The caches provide user controllable features such as full and partial locking, range bound invalidation, and flushing.

Core Memory-Mapped Registers (CMMR)

The core memory-mapped registers control the L1 instruction and data cache, branch target buffer (BTB), parity error, system control, debug, and monitor functions.

SHARC+ CORE ARCHITECTURE

The ADSP-21560/21561/21564/21568 processors are assembly code compatible with all previous SHARC processors featuring the SHARC or SHARC+ core, beginning with the first generation ADSP-2106x SHARC processors and including the ADSP-2116x, ADSP-2126x, ADSP-213xx, ADSP-214xx, and ADSP-SC5xx/ADSP-215xx processors.

The SIMD architecture featured on the ADSP-21560/21561/21564processors is identical to all previous SIMD SHARC processors, namely the ADSP-2116x, ADSP-2126x, ADSP-213xx, ADSP-214xx, and ADSP-SC5xx/ADSP-215xx processors, as shown in Figure 3 and as described in the following sections.

Single-Instruction, Multiple Data (SIMD) Computational Engine

The SHARC+ core contains two computational processing elements that operate as a single-instruction, multiple data (SIMD) engine.

The processing elements are referred to as PEx and PEy, each containing an arithmetic logic unit (ALU), multiplier, shifter, and register file. PEx is always active, and PEy is enabled by setting the PEYEN mode bit in the mode control register (MODE1).

SIMD mode allows the processors to execute the same instruction in both processing elements, but each processing element operates on different data. This architecture efficiently executes math intensive DSP algorithms. In addition to all the features of previous generation SHARC cores, the SHARC+ core also provides a new and simpler way to execute an instruction only on the PEy data register.

SIMD mode also doubles the bandwidth between memory and the processing elements, as required for sustained computational operation of two processing elements. When using the data address generators (DAGs) to transfer data in SIMD mode, two data values transfer with each memory or register file access.

Independent Parallel Computation Units

Within each processing element is a set of pipelined computational units. The computational units consist of a multiplier, an ALU, and a shifter. These units are arranged in parallel, maximizing computational throughput. These computational units support IEEE 32-bit single-precision floating-point; 40-bit extended-precision floating-point; IEEE 64-bit double-precision floating-point; and 32-bit fixed-point data formats.

A multifunction instruction set supports parallel execution of ALU and multiplier operations. In SIMD mode, the parallel ALU and multiplier operations occur in both processing elements per core.

All processing operations take one cycle to complete. For all floating-point operations, the processor takes two cycles to complete in case of data dependency. Double-precision floating-point data take two to six cycles to complete. The processor stalls for the appropriate number of cycles for an interlocked pipeline plus data dependency check.

Core Timer

The SHARC+ processor core includes an extra timer. This extra timer is clocked by the internal processor clock and is typically used as a system tick clock for generating periodic operating system interrupts.

Data Register File

Each processing element contains a general-purpose data register file. The register files transfer data between the computation units and the data buses, and store intermediate results. These 10-port, 32-register register files (16 primary, 16 secondary), combined with the enhanced Harvard architecture of the processor, allow unconstrained data flow between computation units and internal memory. The registers in the PEx data register file are referred to as R0–R15 and in the PEy data register file as S0–S15.

Context Switch

Many of the registers of the processor have secondary registers that can activate during interrupt servicing for a fast context switch. The data, DAG, and multiplier result registers have secondary registers. The primary registers are active at reset, whereas control bits in MODE1 activate the secondary registers.

Universal Registers

General-purpose tasks use the universal registers. The four universal status (USTAT) registers allow easy bit manipulations (set, clear, toggle, test, XOR) for all control and status peripheral registers.

The data bus exchange register (PX) permits data to pass between the 64-bit PM data bus and the 64-bit DM data bus or between the 40-bit register file and the PM or DM data bus. These registers contain hardware to handle the data width difference.

Data Address Generators (DAG) With Zero Overhead Hardware Circular Buffer Support

For indirect addressing and implementing circular data buffers in hardware, the ADSP-21560/21561/21564/21568 processors use two data address generators (DAGs). Circular buffers allow efficient programming of delay lines and other data structures required in digital signal processing and are commonly used in digital filters and fast Fourier transforms (FFT). The DAGs contain sufficient registers to allow the creation of up to 32 circular buffers (16 primary register sets and 16 secondary sets). The DAGs automatically handle address pointer wraparound, reduce overhead, increase performance, and simplify implementation. Circular buffers can start and end at any memory location.

Flexible Instruction Set Architecture (ISA)

The flexible instruction set architecture (ISA), a 48-bit instruction word, accommodates various parallel operations for concise programming. For example, the processors can conditionally execute a multiply, an add, and a subtract in both processing elements while branching and fetching up to four 32-bit values from memory—all in a single instruction.

Additionally, the double-precision floating-point instruction set is new to the SHARC+ core, as compared with the previous SHARC core.

Variable Instruction Set Architecture (VISA)

In addition to supporting the standard 48-bit instructions from previous SHARC core processors, the SHARC+ core processors support 16-bit and 32-bit opcodes for many instructions, formerly 48-bit in the ISA. This variable instruction set architecture (VISA) feature drops redundant or unused bits within the 48-bit instruction to create more efficient and compact code. The program sequencer supports fetching these 16-bit and 32-bit instructions from both internal and external memories. VISA is not an operating mode; rather, it is address dependent (refer to the ISA/VISA address spaces in Table 5). Finally, the processor allows jumps between ISA and VISA instruction fetches.

Single-Cycle Fetch of Instructional Four Operands

The ADSP-21560/21561/21564/21568 processors feature an enhanced Harvard architecture in which the DM bus transfers data and the PM bus transfers both instructions and data.

With the separate program memory bus, data memory buses, and on-chip instruction conflict cache, the processor can simultaneously fetch four operands (two over each data bus) and one instruction from the conflict cache in a single cycle.

Core Event Controller (CEC)

The SHARC+ core event controller (CEC) can be configured to service various interrupts generated by the core (including arithmetic and circular buffer instruction flow exceptions) and system event controller (SEC) events (peripheral interrupt request, debug or monitor, and software-raised), responding only to interrupts enabled in the IMASK register. The output of the SEC is forwarded to the CEC to respond directly to any enabled system interrupts. For all SEC channels, the processor automatically stacks the arithmetic status (ASTATx and ASTATy) registers and mode (MODE1) register in parallel with interrupt servicing.

Instruction Conflict Cache

The processors include a 32-entry instruction cache that enables three-bus operation for fetching an instruction and four data values. The cache is selective—only the instructions that require fetches conflict with the PM bus data access cache. This cache allows full speed execution of core looped operations, such as digital filter multiply accumulates and FFT butterfly processing. The conflict cache serves for bus conflicts within the SHARC+ core only.

Addressing Spaces

In addition to traditionally supported long word, normal word, extended precision word, and short word addressing aliases, the processors support byte addressing for the data and instruction accesses. The enhanced ISA/VISA provides new instructions for accessing all sizes of data from byte space, as well as converting word addresses to byte addresses and byte addresses to word addresses.

Branch Target Buffer (BTB)/Branch Predictor (BP)

Implementation of a hardware-based branch predictor (BP) and branch target buffer (BTB) reduce branch delay. The program sequencer supports efficient branching using the BTB for conditional and unconditional instructions.

SHARC Fabric

The FIR/IIR accelerators on the processors are integrated closely with the SHARC+ core with the help of a dedicated SHARC fabric and run at CCLK speed. This allows the FIR/IIR accelerator requester ports to directly access the SHARC L1 memory with reduced latency, as these accesses do not go through the main system fabric. These accesses are arbitrated between both the SHARC+ core completer ports.The SHARC+ core can also access the FIR/IIR accelerator MMR registers directly.

Additional Features

To enhance the reliability of the application, L1 data RAMs support parity error detection for every byte, and illegal opcodes are also detected (core interrupts flag both errors). Requester ports of the core also detect failed external accesses.

SYSTEM INFRASTRUCTURE

The following sections describe the system infrastructure of the ADSP-21560/21561/21564/21568 processors.

System L2 Memory

A system L2 SRAM memory of up to 16 Mb (2 MB) is available to the SHARC+ core and the system DMA channels (see Table 3). The L2 SRAM block is subdivided into up to eight banks to support concurrent access to the L2 memory ports. Memory accesses to the L2 memory space are multicycle accesses by the SHARC+ core.

The memory space is used for various situations including

- Accelerator and peripheral sources and destination memory to avoid accessing data in the external memory
- A location for DMA descriptors
- Storage for additional data for the SHARC+ core to avoid external memory latencies and reduce external memory bandwidth
- Storage for data coefficient tables cached by the SHARC+ core

See the System Memory Protection Unit (SMPU) section for options in limiting access by the core and DMA requesters.

One Time Programmable Memory (OTP)

The processors feature 7 kb of one time programmable (OTP) memory that is memory-map accessible. This memory can be programmed with custom keys and supports secure boot and secure operation.

I/O Memory Space

Mapped I/Os include SPI2 or xSPI0 memory address spaces (see Table 5).

SYSTEM MEMORY MAP

Table 2. L1 Block 0, Block 1, Block 2, and Block 3 SHARC+® Addressing Memory Map (Private Address Space)

Memory	Long Word (64 Bits)	Extended Precision/ ISA Code (48 Bits)	Normal Word (32 Bits)	Short Word/ VISA Code (16 Bits)	Byte Access (8 Bits)
L1 Block 0 SRAM (1.5 Mb)	0x00048000–0x0004DFFF	0x00090000–0x00097FFF	0x00090000–0x0009BFFF	0x00120000–0x00137FFF	0x00240000–0x0026FFFF
L1 Block 1 SRAM (1.5 Mb)	0x00058000–0x0005DFFF	0x000B0000–0x000B7FFF	0x000B0000–0x000BBFFF	0x00160000–0x00177FFF	0x002C0000–0x002EFFFF
L1 Block 2 SRAM (1 Mb)	0x00060000–0x00063FFF	0x000C0000–0x000C5554	0x000C0000–0x000C7FFF	0x00180000–0x0018FFFF	0x00300000–0x0031FFFF
L1 Block 3 SRAM (1 Mb)	0x00070000–0x00073FFF	0x000E0000–0x000E5554	0x000E0000–0x000E7FFF	0x001C0000–0x001CFFFF	0x00380000–0x0039FFFF

Table 3. L2 Memory Addressing Map

Memory[1]	Byte Address Space SHARC+ Data Access	Normal Word Address Space SHARC+ Data Address	VISA Address Space SHARC+ Instruction Fetch	ISA Address Space SHARC+ Instruction Fetch
L2 RAM (2 Mb)	0x200C0000–0x200FFFFF	0x08030000–0x0803FFFF	0x00BE0000–0x00BFFFFF	0x005E0000–0x005EAAAA
L2 RAM (4 Mb)	0x20080000–0x200FFFFF	0x08020000–0x0803FFFF	0x00BC0000–0x00BFFFFF	0x005D5556–0x005EAAAA
L2 RAM (8 Mb)	0x20000000–0x200FFFFF	0x08000000–0x0803FFFF	0x00B80000–0x00BFFFFF	0x005C0000–0x005EAAAA
L2 RAM (8 Mb)	0x80000000–0x800FFFFF	0x10000000–0x1003FFFF	0x00800000–0x0087FFFF	0x00400000–0x0042AAAA
L2 Boot ROM0	SHARC/DMA: 0x20100000–0x20107FFF	0x08040000–0x08041FFF	0x00B20000–0x00B23FFF	0x00580000–0x00581555
L2 Boot ROM1	0x20108000–0x2010FFFF	0x08042000–0x08043FFF	0x00B00000–0x00B03FFF	0x00500000–0x00501555
L2 Boot ROM2	0x20110000–0x20117FFF	0x08044000–0x08045FFF	0x00B40000–0x00B43FFF	0x00540000–0x00541555

[1] The L2 RAM blocks are subdivided into banks—the 8 Mb L2 models have eight banks, the 4 Mb models have four banks, and there are two banks for the 2 Mb models.

Table 4. SHARC+® L1 Memory Space

	Memory Block	Byte Address Space SHARC+	Normal Word Address Space SHARC+
L1 Memory Space Address via Completer 1/ Completer 2 Port	Block 0	0x28240000–0x2826FFFF	0x0A090000–0x0A09BFFF
	Block 1	0x282C0000–0x282EFFFF	0x0A0B0000–0x0A0BBFFF
	Block 2	0x28300000–0x2831FFFF	0x0A0C0000–0x0A0C7FFF
	Block 3	0x28380000–0x2839FFFF	0x0A0E0000–0x0A0E7FFF

Table 5. Memory Map of Mapped I/Os[1]

	Byte Address Space SHARC+ Data Access	Normal Word Address Space SHARC+ Data Access	VISA Address Space SHARC+ Instruction Fetch	ISA Address Space SHARC+ Instruction Fetch
SPI1/SPI2/xSPI0 Memory (512 MB)	0x60000000–0x600FFFFF	0x04000000–0x07FFFFFF	0x00F80000–0x00FFFFFF	0x00780000–0x007FFFFF
	0x60100000–0x602FFFFF		Not applicable	
	0x60300000–0x6FFFFFFF		Not applicable	Not applicable
	0x70000000–0x7FFFFFFF	Not applicable	Not applicable	Not applicable

[1] The SHARC+ VISA/ISA address space for instruction fetch and the normal word address space for data access do not cover the entire byte address space.

System Crossbars (SCBs)

The system crossbars (SCBs) are the fundamental building blocks of a switch fabric style for on-chip system bus interconnection. The SCBs connect system bus requesters to system bus completers, providing concurrent data transfer between multiple bus requesters and multiple bus completers. A hierarchical model—built from multiple SCBs—provides a power and area efficient system interconnection.

The SCBs provide the following features:

- Highly efficient, pipelined bus transfer protocol for sustained throughput
- Full-duplex bus operation for flexibility and reduced latency
- Concurrent bus transfer support to allow multiple bus requesters to access bus completers simultaneously
- Protection model (secure) support for selective bus interconnect protection

Direct Memory Access (DMA)

The processors use direct memory access (DMA) to transfer data within memory spaces or between a memory space and a peripheral. The processors can specify data transfer operations and return to normal processing while the fully integrated DMA controller carries out the data transfers independent of processor activity.

DMA transfers can occur between memory and a peripheral or between one memory and another memory. Each memory to memory DMA stream uses two channels: the source channel and the destination channel.

All DMA channels can transport data to and from all on-chip and off-chip memories. Programs can use two types of DMA transfers: descriptor-based or register-based. Register-based DMA allows the processors to program DMA control registers directly to initiate a DMA transfer. On completion, the DMA control registers automatically update with original setup values for continuous transfer. Descriptor-based DMA transfers require a set of parameters stored within memory to initiate a DMA sequence. Descriptor-based DMA transfers allow multiple DMA sequences to be chained together. Program a DMA channel to set up and start another DMA transfer automatically after the current sequence completes.

The DMA engine supports the following DMA operations:

- A single linear buffer that stops on completion
- A linear buffer with negative, positive, or zero stride length
- A circular autorefreshing buffer that interrupts when each buffer becomes full
- A similar circular buffer that interrupts on fractional buffers, such as at the halfway point
- The 1D DMA uses a set of identical ping pong buffers defined by a linked ring of two-word descriptor sets, each containing a link pointer and an address
- 1D and 2D fill block to initialize an array with constants
- 32-bit CRC signature of a block of memory or an MMR
- The 1D DMA uses a linked list of four-word descriptor sets containing a link pointer, an address, a length, and a configuration
- The 2D DMA uses an array of one-word descriptor sets, specifying only the base DMA address
- The 2D DMA uses a linked list of multiword descriptor sets, specifying all configurable parameters

Memory Direct Memory Access (MDMA)

The processor supports various memory direct memory access (MDMA) operations, including,

- Enhanced bandwidth MDMA channels with cyclic redundancy check (CRC) protection (32-bit bus width, run on SYSCLK)
- Enhanced bandwidth MDMA channel (32-bit bus width, runs on SYSCLK)
- Maximum bandwidth MDMA channel (64-bit bus width, runs on SYSCLK)

Extended Memory DMA

Extended memory DMA supports various operating modes, such as delay line (which allows processor reads and writes to external delay line buffers and to the external memory), with limited core interaction and scatter/gather DMA (writes to and from noncontiguous memory blocks).

Cyclic Redundancy Check (CRC) Protection

The cyclic redundancy check (CRC) protection modules allow system software to calculate the signature of code, data, or both in memory, the content of memory-mapped registers, or periodic communication message objects. Dedicated hardware circuitry compares the signature with precalculated values and triggers appropriate fault events.

For example, the system software initiates the signature calculation of the entire memory contents every 100 ms and compares this with expected, precalculated values. If a mismatch occurs, a fault condition is generated through the processor core or the trigger routing unit.

The CRC is a hardware module based on a CRC32 engine that computes the CRC value of the 32-bit data-words presented to it. The source channel of the memory to memory DMA (in memory scan mode) provides data. The data can be optionally forwarded to the destination channel (memory transfer mode). The main features of the CRC peripheral are as follows:

- Memory scan mode
- Memory transfer mode
- Data verify mode
- Data fill mode
- User-programmable CRC32 polynomial
- Bit and byte mirroring option (endianness)
- Fault and error interrupt mechanisms

  block

Event Handling

The processors provide event handling that supports both nesting and prioritization. Nesting allows multiple event service routines to be active simultaneously. Prioritization ensures that servicing a higher priority event takes precedence over servicing a lower priority event.

The processors provide support for four different types of events:

- An emulation event causes the processors to enter emulation mode, allowing command and control of the processors through the JTAG interface.
- A reset event resets the processors.
- An exception event occurs synchronously to program flow (in other words, the exception is taken before the instruction is allowed to complete). Conditions triggered by the SHARC+ core, such as data alignment (SIMD or long word) or compute violations (fixed or floating point) and illegal instructions, cause core exceptions. Conditions triggered by the SEC, such as error correcting code (ECC), parity, watchdog, or system clock, cause system exceptions.
- An interrupt event occurs asynchronously to program flow. Interrupts are caused by input signals, timers, and other peripherals, as well as by an explicit software instruction.

System Event Controller (SEC)

The SHARC+ core event controller receives interrupt requests from the system event controller (SEC). The SEC features include the following:

- Comprehensive system event source management, including interrupt enable, fault enable, priority, and source grouping
- A distributed programming model where each system event source control and all status fields are independent of each other
- Determinism where all system events have the same propagation delay and provide unique identification of a specific system event source
- A completer control port that provides access to all SEC registers for configuration, status, and interrupt and fault services
- Global locking that supports a register level protection model to prevent writes to locked registers
- Fault management including fault action configuration, time out, external indication, and system reset

Trigger Routing Unit (TRU)

The trigger routing unit (TRU) provides system level sequence control without core intervention. The TRU maps trigger generators to trigger receivers. Trigger receivers can be configured to respond to triggers in various ways. Common applications enabled by the TRU include,

- Automatically triggering the start of a DMA sequence after a sequence from another DMA channel completes
- Software triggering
- Synchronization of concurrent activities

SECURITY FEATURES

The following sections describe the security features of the ADSP-21560/21561/21564/21568 processors.

Cryptographic Hardware Accelerators

The ADSP-21560/21561/21564/21568 processors support standards-based hardware accelerated encryption, decryption, authentication, and true random number generation.

Support for the hardware accelerated cryptographic ciphers includes the following:

- AES in ECB, CBC, ICM, and CTR modes with 128-bit, 192-bit, and 256-bit keys
- DES in ECB and CBC mode with 56-bit key
- 3DES in ECB and CBC mode with 3x 56-bit key
- ARC4 in stateful, stateless mode, up to 128-bit key

Support for the hardware accelerated hash functions includes the following:

- SHA-1
- SHA-2 with 224-bit and 256-bit digests
- HMAC transforms for SHA-1 and SHA-2
- MD5

Public key accelerator (PKA) is available to offload computation intensive public key cryptography operations.

Both a hardware-based nondeterministic random number generator and pseudorandom number generator are available.

Secure boot is also available with 224-bit and 256-bit elliptic curve digital signatures ensuring integrity and authenticity of the boot stream. Optionally, ensuring confidentiality through AES-128 encryption is available.

Password protected secure debug is also available to allow only trusted users to access the system with debug tools.

CAUTION
This product includes security features that can be used to protect embedded nonvolatile memory contents and prevent execution of unauthorized code. When security is enabled on this device (either by the ordering party or the subsequent receiving parties), the ability of Analog Devices to conduct failure analysis on returned devices is limited. Contact Analog Devices for details on the failure analysis limitations for this device.

System Protection Unit (SPU)

The system protection unit (SPU) guards against accidental or unwanted access to an MMR space of the peripheral by providing a write protection mechanism. The user can choose and configure the protected peripherals as well as configure which of the three system MMR requesters (SHARC+ core, memory DMA, and Arm® CoreSight™ debug) the peripherals are guarded against.

The SPU is also part of the security infrastructure. Along with providing write protection functionality, the SPU is employed to define which resources in the system are secure or nonsecure as well as block access to secure resources from nonsecure requesters.

System Memory Protection Unit (SMPU)

The system memory protection unit (SMPU) provides memory protection against read and/or write transactions to defined regions of memory. There are SMPU units in the ADSP-21560/21561/21564/21568 processors for each memory space, except for SHARC L1 memory.

The SMPU is also part of the security infrastructure. It allows the user to protect against arbitrary read and/or write transactions and allows regions of memory to be defined as secure and prevent nonsecure requesters from accessing those memory regions.

SECURITY FEATURES DISCLAIMER

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SAFETY FEATURES

The ADSP-21560/21561/21564/21568 processors are designed to support functional safety applications. Whereas the level of safety is mainly dominated by the system concept, the following primitives are provided by the processors to build a robust safety concept.

Multiparity Bit Protected SHARC+ Core L1 Memories

In the SHARC+ core L1 memory space, whether SRAM or cache, multiple parity bits protect each word to detect the single event upsets that occur in all RAMs. Parity also protects the cache tags and BTB.

Parity Protected L2 Memories

Even parity protection is added to the whole of L2 memories. There is one parity bit for each 32-bit data, which is used to detect odd number of erroneous bits in the data retrieved from the memory.

Parity Protected Peripheral Memories

Parity protection is added to the following peripheral memories:

- ASRC
- IIR
- FIR
- CRYPTO
- MLB

Cyclic Redundancy Check (CRC) Protected Memories

Whereas parity bit and ECC protection mainly protect against random soft errors in L1 and L2 memory cells, the CRC engines can protect against systematic errors (pointer errors) and static content (instruction code) of L1 and L2 memories. The processors feature two CRC engines that are embedded in the memory to memory DMA controllers.

CRC checksums can be calculated or compared automatically during memory transfers. Alternatively, single or multiple memory regions can be continuously scrubbed by a single DMA work unit as per DMA descriptor chain instructions. The CRC engine also protects data loaded during the boot process.

Signal Watchdogs

The 10 general-purpose timers feature modes to monitor off-chip signals. The watchdog period mode monitors whether external signals toggle with a period within an expected range. The watchdog width mode monitors whether the pulse widths of external signals are within an expected range. Both modes help detect undesired toggling or lack of toggling of system level signals.

System Event Controller (SEC)

Besides system events, the system event controller (SEC) further supports fault management, including fault action configuration as timeout, internal indication by system interrupt, or external indication through the $\overline{\text{SYS\_FAULT}}$ pin and system reset.

Memory Error Controller (MEC)

The memory error controller (MEC) manages memory parity/ECC errors and warnings from the cores and peripherals and sends out interrupts and triggers.

PROCESSOR PERIPHERALS

The following sections describe the peripherals of the ADSP-21560/21561/21564/21568 processors.

Digital Audio Interface (DAI)

The processors support two digital audio interface (DAI) units. The DAI can connect various peripherals to any of the DAI pins.

The application code makes these connections using the signal routing unit (SRU), shown in Figure 1.

The SRU is a matrix routing unit (or group of multiplexers) that enables the peripherals provided by the DAI to interconnect under software control. This functionality allows easy use of the DAI associated peripherals for a wider variety of applications by using a larger set of algorithms than is possible with nonconfigurable signal paths.

The DAI includes the peripherals described in the following sections (SPORTs, ASRC, S/PDIF, and PCG). DAI Pin Buffer 20 and DAI Pin Buffer 19 can change the polarity of the input signals. Most signals of the peripherals belonging to different DAIs cannot be interconnected, with few exceptions.

The DAI_PINx pin buffers may also be used as GPIO pins. DAI input signals allow the triggering of interrupts on the rising edge, falling edge, or both.

See the ADSP-21560/21561/21564/21568 SHARC+ Processor Hardware Reference manual for complete information on the use of the DAIs and SRUs.

Serial Port (SPORT)

The processors feature eight synchronous serial ports (SPORTs), providing an inexpensive interface to a wide variety of digital and mixed-signal peripheral devices. These devices include Analog Devices AD19xx and ADAU19xx families of audio codecs, analog-to-digital converters (ADCs) and digital-to-analog converters (DACs). Two data lines, a clock, and a frame sync comprise a SPORT half. The data lines can be programmed to either transmit or receive data, and each SPORT half has a dedicated DMA channel.

An individual SPORT module consists of two independently configurable SPORT halves with identical functionality. Two bidirectional data lines—primary (0) and secondary (1)—are available per SPORT half and are configurable as either transmitters or receivers. Therefore, each SPORT half permits two unidirectional streams into or out of the same SPORT. This bidirectional functionality provides greater flexibility for serial communications. For full-duplex configuration, one half SPORT provides two transmit data signals, and the other half SPORT provides two receive data signals. The frame sync and clock are shared.

Serial ports operate in the following six modes:

- Standard DSP serial mode
- Multichannel time division multiplexing (TDM) mode
- I^2S mode
- Packed I^2S mode
- Left justified mode
- Right justified mode

Asynchronous Sample Rate Converter (ASRC)

The asynchronous sample rate converter (ASRC) contains eight ASRC blocks. The ASRC provides up to 140 dB signal-to-noise ratio (SNR). The ASRC block performs synchronous or asynchronous sample rate conversion across independent stereo channels, without using internal processor resources. The ASRC blocks can also be configured to operate together to convert multichannel audio data without phase mismatches. Finally, the ASRC can clean up audio data from jittery clock sources such as the S/PDIF receiver.

S/PDIF-Compatible Digital Audio Receiver/Transmitter

The Sony/Philips Digital Interface Format (S/PDIF) is a standard audio data transfer format that allows the transfer of digital audio signals from one device to another. There are two S/PDIF transmit/receive blocks on the processor. The digital audio interface carries three types of information: audio data, nonaudio data (compressed data), and timing information.

The S/PDIF interface supports one stereo channel or compressed audio streams. The S/PDIF transmitter and receiver are AES3 compatible and support the sample rate from 24 kHz to 192 kHz. The S/PDIF receiver supports professional jitter standards.

The S/PDIF receiver/transmitter has no separate DMA channels. The S/PDIF transmitter receives audio data in serial format and converts it into a biphase encoded signal. The serial data input to the transmitter can be formatted as left justified, I^2S, or right justified with word widths of 16, 18, 20, or 24 bits. The S/PDIF receiver converts a biphase encoded signal into I^2S serial format.The serial data, clock, and frame sync outputs/inputs from/to the S/PDIF receiver/transmitter are routed through the SRU. They can be connected to various peripherals, such as the SPORTs, external pins, and the precision clock generators (PCGs), and are controlled by the SRU control registers.

Precision Clock Generators (PCG)

The precision clock generators (PCG) consist of four units: Unit A and Unit B located in the DAI0 block, and Unit C and Unit D located in the DAI1 block. The PCG can generate a pair of signals (clock and frame sync) derived from a clock input signal (SCLK0, SYS_CLKIN0, or DAI pin buffer). Each unit can also output to the pin buffers of the opposite DAI unit. All units are identical in functionality and operate independently of each other. The two signals generated by each unit are normally used as a serial bit clock/frame sync pair.

Universal Asynchronous Receiver/Transmitter (UART) Ports

The processors provide full-duplex universal asynchronous receiver/transmitter (UART) ports, fully compatible with PC standard UARTs. Each UART port provides a simplified UART interface to other peripherals or hosts, supporting full-duplex, DMA supported, asynchronous transfers of serial data. A UART port includes support for five to eight data bits as well as no parity, even parity, or odd parity.

Optionally, an additional address bit can be transferred to interrupt only addressed nodes in multidrop bus (MDB) systems. A frame is terminated by a configurable number of stop bits.

The UART ports support automatic hardware flow control through the clear to send (CTS) input and request to send (RTS) output with programmable assertion first in, first out (FIFO) levels.

To help support the Local Interconnect Network (LIN) protocols, a special command causes the transmitter to queue a break command of programmable bit length into the transmit buffer. Similarly, the number of stop bits can be extended by a programmable interframe space.

Serial Peripheral Interface (SPI) Ports

The processors have three industry-standard SPI-compatible ports that allow the processors to communicate with multiple SPI-compatible devices.

The baseline SPI peripheral is a synchronous, 4-wire interface consisting of two data pins, one device select pin, and a gated clock pin. The two data pins allow full-duplex operation to other SPI-compatible devices. An extra two (optional) data pins are provided to support quad-SPI operation. Enhanced modes of operation, such as flow control, fast mode, and dual-I/O mode (DIOM), are also supported. DMA mode allows for transferring several words with minimal central processing unit (CPU) interaction.

With a range of configurable options, the SPI ports provide a glueless hardware interface with other SPI-compatible devices in master mode, slave mode, and multimaster environments. The SPI peripheral includes programmable baud rates, clock phase, and clock polarity. The peripheral can operate in a multimaster environment by interfacing with several other devices, acting as either a master device or a slave device. In a multimaster environment, the SPI peripheral uses open-drain outputs to avoid data bus contention. The flow control features enable slow slave devices to interface with fast master devices by providing an SPI ready pin (SPI_RDY), which flexibly controls the transfers.

The baud rate and clock phase and polarities of the SPI port are programmable. The port has integrated DMA channels for both transmit and receive data streams.

xSPI with Octal and HyperBus Support

The octal serial peripheral interface (xSPI0/HyperBus) port provides an increased external memory data bus width (up to eight bits in parallel). The xSPI0 port supports dual data rate (DDR) modes of operation, which enables the transfer of up to 16 bits of data each clock cycle. The xSPI0 port provides overall data throughput and performance improvement, including faster boot time.

Features of the xSPI0/HyperBus port include:

- Support for single-, dual-, quad-, or octal-I/O transfers
  - Can be interfaced with octal flash, octal RAM, HyperFlash, and HyperRAM devices
  - Can be interfaced with legacy flash devices including quad and SPINAND
- Auto-command engine and minicontroller
- Multithreading support
- Support for execute in place (XIP): continuous mode
- Programmable page and block sizes
- Programmable write protected regions
- Programmable memory timing
- Support for DDR commands
- Support for PHY mode of operation to enable high-speed transfers
- Support for DQS to increase robustness of data sampling at higher speeds

Timers

The processors include several timers that are described in the following sections.

General-Purpose (GP) Timers (TIMER)

There is one general-purpose (GP) timer unit, providing 10 general-purpose programmable timers. Each timer has an external pin that can be configured as PWM or timer output, as an input to clock the timer, or as a mechanism for measuring pulse widths and periods of external events. These timers can be synchronized to an external clock input on the TM_TMR[n] pins, an external TM_CLK input pin, or to the internal SCLK0.

These timer units can be used in conjunction with the UARTs to measure the width of the pulses in the data stream to provide a software autobaud detect function for the respective serial channels.

The GP timers can generate interrupts to the processor core, providing periodic events for synchronization to either the system clock or to external signals. Timer events can also trigger other peripherals via the TRU (for instance, to signal a fault). Each timer can also be started and stopped by any trigger generator without core intervention.

Watchdog Timer (WDT)

Two on-chip software watchdog timers (WDT) can be used by the SHARC+ core. A software watchdog can improve system availability by forcing the processors to a known state, via a general-purpose interrupt, or a fault, if the timer expires before being reset by software.

The programmer initializes the count value of the timer, enables the appropriate interrupt, then enables the timer. Thereafter, the software must reload the counter before it counts down to

zero from the programmed value, protecting the system from remaining in an unknown state where software that normally resets the timer stops running due to an external noise condition or software error.

General-Purpose Counters (CNT)

A 32-bit general-purpose counter (CNT) is provided that can operate in general-purpose up/down count modes and can sense 2-bit quadrature or binary codes as typically emitted by industrial drives or manual thumbwheels. Count direction is controlled by a level-sensitive input pin or by two edge detectors.

A third counter input can provide flexible zero marker support and can input the push button signal of thumbwheel devices. All three CNT0 pins have a programmable debouncing circuit.

Internal signals forwarded to a GP timer enable the timer to measure the intervals between count events. Boundary registers enable auto-zero operation or simple system warning by interrupts when programmed count values are exceeded.

Media Local Bus (MediaLB)

The automotive models have a MediaLB (MLB) device interface that allows the processors to function as a media local bus device. It includes support for 3-pin media local bus protocols. The MLB 3-pin configuration supports speeds up to 1024 × FS. The MLB also supports up to 64 logical channels with up to 468 bytes of data per MLB frame.

The MLB interface supports MOST25, MOST50, and MOST150 data rates and operates in device mode only.

2-Wire Controller Interface (TWI)

The processors include 2-wire interface (TWI) modules that provide a simple exchange method of control data between multiple devices. The TWI module is compatible with the widely used I^2C bus standard. The TWI module offers the capabilities of simultaneous controller and target operation and support for both 7-bit addressing and multimedia data arbitration. The TWI interface utilizes two pins for transferring clock (TWI_SCL) and data (TWI_SDA) and supports the protocol at speeds up to 400 kbps. The TWI interface pins are compatible with 3.3 V logic levels.

Additionally, the TWI module is fully compatible with serial camera control bus (SCCB) functionality for easier control of various CMOS camera sensor devices.

General-Purpose I/O (GPIO)

Each general-purpose port pin can be individually controlled by manipulating the port control, status, and interrupt registers:

- The GPIO direction control register specifies the direction of each individual GPIO pin as input or output.
- GPIO control and status registers have a write-one-to-modify mechanism that allows any combination of individual GPIO pins to be modified in a single instruction, without affecting the level of any other GPIO pins.
- GPIO interrupt mask registers allow each individual GPIO pin to function as an interrupt to the processors. GPIO pins defined as inputs can be configured to generate hardware interrupts, whereas output pins can be triggered by software interrupts.
- GPIO interrupt sensitivity registers specify whether individual pins are level or edge sensitive and specify, if edge sensitive, whether the rising edge or both the rising and falling edges of the signal are significant.

Pin Interrupts

Every port pin on the processors can request interrupts in either an edge sensitive or a level sensitive manner with programmable polarity. Interrupt functionality is decoupled from GPIO operation. Two system-level interrupt channels (PINT0–PINT1) are reserved for this purpose. Each of these interrupt channels can manage up to 32 interrupt pins. The assignment from pin to interrupt is not performed on a pin by pin basis. Rather, groups of eight pins (half ports) are flexibly assigned to interrupt channels.

Every pin interrupt channel features a special set of 32-bit memory-mapped registers that enable half port assignment and interrupt management. This functionality includes masking, identification, and clearing of requests. These registers also enable access to the respective pin states and use of the interrupt latches, regardless of whether the interrupt is masked. Most control registers feature multiple MMR address entries to write-one-to-set or write-one-to-clear them individually.

SYSTEM ACCELERATION

The following sections describe the system acceleration blocks of the ADSP-21560/21561/21564/21568 processors.

Finite Impulse Response (FIR) Accelerator

The finite impulse response (FIR) accelerator consists of a 1024 word coefficient memory, a 1024 word deep delay line for the data, and four multiplier-accumulator (MAC) units. A controller manages the accelerator. The FIR accelerator runs at the core clock frequency. The FIR accelerator can access all memory spaces and can run concurrently with the IIR accelerator on the processor.

Infinite Impulse Response (IIR) Accelerator

The infinite impulse response (IIR) accelerator consists of a 1440 word coefficient memory for storage of biquad coefficients, a data memory for storing the intermediate data, and one MAC unit. A controller manages the accelerator. The IIR accelerator runs at the core clock frequency. The IIR accelerator can access all memory spaces and run concurrently with the other accelerators on the processor.

In addition to operating at core clock, the FIR/IIR accelerators support various enhanced features, including the ability to halt the accelerator for dynamic queuing of unlimited FIR/IIR channels, selective interrupt generation for each channel, and trigger requester/completer support.

SYSTEM DESIGN

The following sections provide an introduction to system design features and power supply issues.

Clock Management

The processors provide three operating modes, each with a different performance and power profile. Control of clocking to each of the processor peripherals reduces power consumption. The processors do not support any low power operation modes. Control of clocking to each of the processor peripherals can reduce the power consumption.

Reset Control Unit (RCU)

Reset is the initial state of the whole processor, or the core, and is the result of a hardware or software triggered event. In this state, all control registers are set to default values and functional units are idle. Exiting a full system reset begins with the core ready to boot.

The reset control unit (RCU) controls how all the functional units enter and exit reset. Differences in functional requirements and clocking constraints define how reset signals are generated. Programs must guarantee that none of the reset functions put the system into an undefined state or cause resources to stall. This requirement is particularly important when the core resets (programs must ensure that there is no pending system activity involving the core when it is reset).

From a system perspective, reset is defined by both the reset target and the reset source.

The reset target is defined as the following:

- System reset—all functional units except the RCU are set to default states.
- Hardware reset—all functional units are set to default states without exception. History is lost.
- Core only reset—affects the core only. When in reset state, the core is not accessed by any bus requester.

The reset source is defined as the following:

- System reset—can be triggered by software (writing to the RCU_CTL register) or by another functional unit, such as the dynamic power management (DPM) unit or any of the SEC, TRU, or emulator inputs.
- Hardware reset—the $\overline{\text{SYS\_HWRST}}$ input signal asserts active (pulled down).
- Core only reset—affects only the core. The core is not accessed by any bus requester when in reset state.
- Trigger request (peripheral).

Clock Generation Unit (CGU)

The ADSP-21560/21561/21564/21568 processors support one PLL. The PLL is part of a clock generation unit (CGU). The CGU is driven externally by the same clock source, thus providing flexibility in determining the internal clocking frequencies for each clock domain.

Frequencies generated by the CGU are derived from a common multiplier with different divider values available for each output.

The CGU generates all on-chip clocks and synchronization signals. Multiplication factors are programmed to define the PLLCLK frequency.

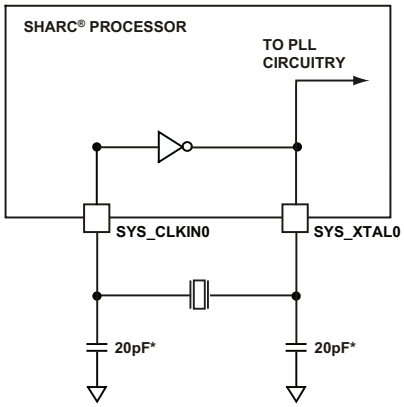
Programmable values divide the PLLCLK frequency to generate the core clock (CCLK), the system clocks, and the output clock (OCLK). For more information on clocking, see the ADSP-21560/21561/21564/21568 SHARC+ Processor Hardware Reference manual.

Writing to the CGU control registers does not affect the behavior of the PLL immediately. Registers are first programmed with a new value and the PLL logic executes the changes to ensure a smooth transition from the current conditions to the new conditions.

System Crystal Oscillator

The processor can be clocked by an external crystal (see Figure 5), a sine wave input, or a buffered, shaped clock derived from an external clock oscillator. If using an external clock, it must be compatible with the $V_{IHCLKIN}$ and $V_{ILCLKIN}$ specifications and must not be halted, changed, or operated below the specified frequency during normal operation (see the Preliminary Operating Conditions section). When using an external clock, the clock signal is connected to the SYS_CLKIN0 pin of the processor and the SYS_XTAL0 pin must be left unconnected. The external clock signal driving SYS_CLKIN0 must not exceed the internal (VDD_INT) voltage level. Alternatively, because the processor includes an on-chip oscillator circuit, an external crystal can be used.

For fundamental frequency operation, use the circuit shown in Figure 5. A parallel resonant, fundamental frequency, microprocessor grade crystal is connected across the SYS_CLKIN0 pin and the SYS_XTAL0 pin.



NOTE: VALUES MARKED WITH * MUST BE CUSTOMIZED, DEPENDING ON THE CRYSTAL AND LAYOUT. ANALYZE CAREFULLY. VALID FREQUENCY RANGE IS 20 MHz TO 30 MHz FOR SYS_CLKIN0.

Figure 5. External Crystal Connection

The two capacitors, shown in Figure 5, fine tune phase and amplitude of the sine frequency. The capacitor values shown in Figure 5 are typical values only. The capacitor values are dependent upon the load capacitance recommendations of the crystal manufacturer and the physical layout of the printed circuit board (PCB). The user must verify the customized values based on careful investigations on multiple devices over the required temperature range.

Clock Distribution Unit (CDU)

The clock generation unit provides output that feeds a clock distribution unit (CDU). The clock output CLKO0 and the clock generation unit outputs are connected to various targets. For more information, refer to the ADSP-21560/21561/21564/21568 SHARC+ Processor Hardware Reference manual.

Clock Out/External Clock

The SYS_CLKOUT output pin has programmable options to output divided down versions of the on-chip clocks. By default, the SYS_CLKOUT pin drives a buffered version of the SYS_ CLKIN0 input. Refer to the ADSP-21560/21561/21564/21568 SHARC+ Processor Hardware Reference manual to change the default mapping of clocks.

Booting

The processors have several mechanisms for automatically loading internal and external memory after a reset. The boot mode is defined by the SYS_BMODE[n] input pins. There are two categories of boot modes. In flash boot modes, the processors actively load data from serial memories. In external host boot modes, the processors receive data from external host devices.

The boot modes are shown in Table 6. These modes are implemented by the SYS_BMODE[n] bits of the reset configuration register and are sampled during power-on resets and software initiated resets.

Table 6. Boot Modes

SYS_BMODE[n] Setting	Boot Mode
000	No boot
001	SPI2 flash
010	SPI2 host
011	UART0 host
100	Reserved
101	xSPI0 flash
110	SPI1 flash
111	Reserved

In the ADSP-21560/21561/21564/21568 processors, the SHARC+ core controls the boot process, including loading all internal and external memory. The option for secure boot is available on all models.

Power Supplies

The processors have separate power supply connections for

- Internal (VDD_INT)
- External I/O (VDD_EXT)
- PLL and OTP high voltage power supplies (VDD_REF)

Power Management

As shown in Table 7, the processors support three different power domains, which maximizes flexibility while maintaining compliance with industry standards and conventions.

The power dissipated by a processor is largely a function of the clock frequency and the square of the operating voltage. For example, reducing the clock frequency by 25% results in a 25% reduction in dynamic power dissipation.

Table 7. Power Domains

Power Domain	V_{DD} Range
All Internal Logic	V_{DD_INT}
All Other I/O (Includes SYS, JTAG, and Ports Pins Except SYS_CLKIN0)	V_{DD_EXT}
SYS_CLKIN0	V_{DD_INT}
PLL, OTP	V_{DD_REF}

Power-Up

SYS_XTAL0 oscillations (SYS_CLKIN0) start when power is applied to the VDD_INT and VDD_EXT pins. The rising edge of $\overline{\text{SYS\_HWRST}}$ initiates the PLL locking sequence. The deassertion must apply only if all voltage supplies and SYS_CLKIN0 oscillations are valid (refer to the Power-Up Reset Timing section).

Target Board JTAG Emulator Connector

The Analog Devices DSP tools product line of JTAG emulators uses the IEEE 1149.1 JTAG test access port of the processors to monitor and control the target board processor during emulation. The Analog Devices DSP tools product line of JTAG emulators provides emulation at full processor speed, allowing inspection and modification of memory, registers, and processor stacks. The processor JTAG interface ensures the emulator does not affect target system loading or timing.

For information on JTAG emulator operation, see the appropriate emulator hardware user's guide at SHARC Processors Software and Tools.

SYSTEM DEBUG

The processors include a feature that allows easy system debug. This is described in the following section.

Debug Access Port (DAP)

The debug access port (DAP) provides IEEE 1149.1 JTAG interface support through the JTAG debug.

DEVELOPMENT TOOLS

Analog Devices supports its processors with a complete line of software and hardware development tools, including an integrated development environment, evaluation products, emulators, and a variety of software add-ins.

Integrated Development Environments (IDEs)

For C/C++ software writing and editing, code generation, and debug support, Analog Devices offers the CrossCore® Embedded Studio (CCES) integrated development environment (IDE).

CCES is based on the Eclipse framework. Supporting most Analog Devices processor families, CCES is the IDE of choice for processors, including multicore devices.

CCES seamlessly integrates available software add-ins to support real-time operating systems, file systems, TCP/IP stacks, USB stacks, algorithmic software modules, and evaluation hardware board support packages (BSPs). For more information, visit www.analog.com/cces.

EZ-KIT Evaluation System

For processor evaluation, Analog Devices provides EZ-KIT® evaluation systems, which are comprised of a System on Module (SOM) board and a SOM carrier board.

The SOM board (EV-21568-SOM) is small and low-cost, featuring the audio processor, QSPI flash memories, FTDI USB-to-UART, and USB power. SOM boards also include a JTAG debug connection such that they can be used standalone for debug/development using either the ADZS-ICE-2000 or ADZS-ICE-1000 in-circuit emulator (ICE).

The EV-SOMCRR-EZLITE SOM carrier board can be used in conjunction with the EV-21568-SOM and comes with a power supply and feature high-speed connectors for the SOM, a comprehensive set of peripherals, and an on-board emulator. The USB controller on the carrier board connects to the USB port of the user's PC, enabling CCES to emulate the on-board processor in-circuit. This permits users to download, execute, and debug programs, as well as in-circuit program the on-board flash memory device to store user-specific boot code, thus enabling standalone operation.

Each EZ-KIT purchased includes an evaluation license for CCES. The CCES evaluation license type restricts CCES features to specific evaluation systems. With the full CCES license type (sold separately), engineers can develop software for any of the CCES-supported evaluation boards (including the SOM when used standalone or when connected to a different carrier board) or any custom system designed around supported Analog Devices processors. The full CCES license type also enables higher-performance debug capabilities via JTAG using an ICE.

For further information, see:

- www.analog.com/cces
- www.analog.com/EV-21568-SOM
- www.analog.com/EV-SOMCRR-EZLITE

Software Add-Ins for CCES

Analog Devices offers software add-ins which seamlessly integrate with CCES to extend the capabilities and reduce development time. Add-ins include BSPs for evaluation hardware, various middleware packages, and algorithmic modules. Documentation, help, configuration dialogs, and coding examples present in these add-ins are viewable through the CCES IDE upon add-in installation.

Board Support Packages (BSPs) for Evaluation Hardware

Software support for the EZ-KIT evaluation systems is provided by software add-ins called board support packages (BSPs). The BSPs contain the required drivers, pertinent release notes, and select example code for the given evaluation hardware. A download link for a specific BSP is located on the web page for the associated SOM product.

Middleware Packages

Analog Devices offers middleware add-ins such as real-time operating systems, file systems, USB stacks, and TCP/IP stacks. For more information, see the Operating Systems and Middleware page.

Algorithmic Modules

To speed development, Analog Devices offers add-ins that perform popular audio and video processing algorithms. These are available for use with CCES. For more information, visit the Software page in the Resource Library.

Designing an Emulator-Compatible DSP Board (Target)

For embedded system test and debug, Analog Devices provides a family of emulators. On each JTAG DSP, Analog Devices supplies an IEEE 1149.1 JTAG test access port (TAP). In-circuit emulation is facilitated by use of this JTAG interface. The emulator accesses the internal features of the processor via the TAP, allowing the developer to load code, set breakpoints, and view variables, memory, and registers.

The processor must be halted to send data and commands, but after an operation is completed by the emulator, the DSP system is set to run at full speed with no impact on system timing. The emulators require the target board to include a header that supports connection of the JTAG port of the DSP to the emulator.

For details on target board design issues including mechanical layout, single processor connections, signal buffering, signal termination, and emulator pod logic, see Analog Devices JTAG Emulation Technical Reference (EE-68).

ADDITIONAL INFORMATION

This data sheet provides a general overview of the ADSP-21560/21561/21564/21568 architecture and functionality. For detailed information on the core architecture and instruction set, refer to the SHARC+ Core Programming Reference.

RELATED SIGNAL CHAINS

A signal chain is a series of signal conditioning electronic components that receive input (data acquired from sampling either real-time phenomena or from stored data) in tandem, with the output of one portion of the chain supplying input to the next. Signal chains are often used in signal processing applications to gather and process data or to apply system controls based on analysis of real-time phenomena.

Analog Devices eases signal processing system development by providing signal processing components that are designed to work together. See Reference Designs.

The application signal chains page at Circuits from the Lab® provides the following:

- Graphical circuit block diagram presentation of signal chains for a variety of circuit types and applications
- Drill down links for components in each chain to selection guides and application information
- Reference designs applying best practice design techniques

ADSP-21560/21561/21564/21568 DETAILED SIGNAL DESCRIPTIONS

Table 8 provides a detailed description of each pin.

Table 8. ADSP-21560/21561/21564/21568 Detailed Signal Descriptions

Signal Name	Direction	Description
C0_FLG[n]	InOut	**SHARC Core 0 Flag Pin.**
CNT_DG	Input	**Count Down and Gate.** Depending on the mode of operation, this input acts either as a count down signal or a gate signal. Count down—this input causes the GP counter to decrement. Gate—stops the GP counter from incrementing or decrementing.
CNT_UD	Input	**Count Up and Direction.** Depending on the mode of operation, this input acts either as a count up signal or a direction signal. Count up—this input causes the GP counter to increment. Direction—selects whether the GP counter is incrementing or decrementing.
CNT_ZM	Input	**Count Zero Marker.** Input that connects to the zero marker output of a rotary device or detects the pressing of a pushbutton.
DAI_PIN[nn]	InOut	**Pin n.** The digital applications interface (DAI0) connects various peripherals to any of the DAI0_PINxx pins. Programs make these connections using the signal routing unit (SRU).
JTG_TCK	Input	**JTAG Clock.** JTAG test access port clock.
JTG_TDI	Input	**JTAG Serial Data In.** JTAG test access port data input.
JTG_TDO	Output	**JTAG Serial Data Out.** JTAG test access port data output.
JTG_TMS	Input	**JTAG Mode Select.** JTAG test access port mode select.
$\overline{\text{JTG\_TRST}}$	Input	**JTAG Reset.** JTAG test access port reset.
MLB_CLK	InOut	**Single-Ended Clock.**
MLB_DAT	InOut	**Single-Ended Data.**
MLB_SIG	InOut	**Single-Ended Signal.**
P_[nn]	InOut	**Position n.** General-purpose input/output. See the ADSP-21560/21561/21564/21568 SHARC+ Processor Hardware Reference manual for programming information.
SPI_CLK	Output	**SPI Master Clock Output.** SPI master clock output.
SPI_D2	InOut	**Data 2.** Transfers serial data in quad modes.
SPI_D3	InOut	**Data 3.** Transfers serial data in quad modes. Open-drain when ODM mode is enabled.
SPI_MISO	InOut	**Master In, Slave Out.** Transfers serial data. Operates in the same direction as SPI_MOSI in dual and quad modes. Open-drain when ODM mode is enabled.
SPI_MOSI	InOut	**Master Out, Slave In.** Transfers serial data. Operates in the same direction as SPI_MISO in dual and quad modes. Open-drain when ODM mode is enabled.
SPI_RDY	InOut	**Ready.** Optional flow signal. Output in slave mode, input in master mode. This pin is three-stated by default.
$\overline{\text{SPI\_SEL[n]}}$	Output	**Slave Select Output n.** Used in master mode to enable the desired slave.
$\overline{\text{SPI\_SS}}$	Input	**Slave Select Input.** Slave mode—acts as the slave select input. Master mode—optionally serves as an error detection input for the SPI when there are multiple masters.
SPT_ACLK	InOut	**Channel A Clock.** Data and frame sync are driven or sampled with respect to this clock. This signal can be either internally or externally generated.
SPT_AD0	InOut	**Channel A Data 0.** Primary bidirectional data I/O. This signal can be configured as an output to transmit serial data or as an input to receive serial data.
SPT_AD1	InOut	**Channel A Data 1.** Secondary bidirectional data I/O. This signal can be configured as an output to transmit serial data or as an input to receive serial data.
SPT_AFS	InOut	**Channel A Frame Sync.** The frame sync pulse initiates shifting of serial data. This signal is either generated internally or externally.

Table 8. ADSP-21560/21561/21564/21568 Detailed Signal Descriptions (Continued)

Signal Name	Direction	Description
SPT_ATDV	Output	**Channel A Transmit Data Valid.** This signal is optional and only active when SPORT is configured in multichannel transmit mode. It is asserted during enabled slots.
SPT_BCLK	InOut	**Channel B Clock.** Data and frame sync are driven or sampled with respect to this clock. This signal can be either internally or externally generated.
SPT_BD0	InOut	**Channel B Data 0.** Primary bidirectional data I/O. This signal can be configured as an output to transmit serial data or as an input to receive serial data.
SPT_BD1	InOut	**Channel B Data 1.** Secondary bidirectional data I/O. This signal can be configured as an output to transmit serial data or as an input to receive serial data.
SPT_BFS	InOut	**Channel B Frame Sync.** The frame sync pulse initiates shifting of serial data. This signal is either generated internally or externally.
SPT_BTDV	Output	**Channel B Transmit Data Valid.** This signal is optional and only active when SPORT is configured in multichannel transmit mode. It is asserted during enabled slots.
SYS_BMODE[n]	Input	**Boot Mode Control n.** Selects the boot mode of the processor.
SYS_CLKIN0	Input	**Clock/Crystal Input.**
SYS_CLKOUT	Output	**Processor Clock Output.** Outputs internal clocks. Clocks may be divided down. See the ADSP-21560/21561/21564/21568 SHARC+ Processor Hardware Reference manual for more details.
SYS_FAULT	InOut	**Active, High, Fault Output.** Indicates internal faults or senses external faults depending on the operating mode.
$\overline{\text{SYS\_FAULT}}$	InOut	**Active, Low, Fault Output.** Indicates internal faults or senses external faults depending on the operating mode.
$\overline{\text{SYS\_HWRST}}$	Input	**Processor Hardware Reset Control.** Resets the device when asserted.
$\overline{\text{SYS\_RESOUT}}$	Output	**Reset Output.** Indicates the device is in the reset state.
SYS_XTAL0	Output	**Crystal Output.**
TM_ACI[n]	Input	**Alternate Capture Input n.** Provides an additional input for WIDCAP, WATCHDOG, and PININT modes.
TM_ACLK[n]	Input	**Alternate Clock n.** Provides an additional time base for an individual timer.
TM_CLK	Input	**Clock.** Provides an additional global time base for all GP timers.
TM_TMR[n]	InOut	**Timer n.** The main input/output signal for each timer.
TWI_SCL	InOut	**Serial Clock.** Clock output when master, clock input when slave.
TWI_SDA	InOut	**Serial Data.** Receives or transmits data.
$\overline{\text{UART\_CTS}}$	Input	**Clear to Send.** Flow control signal.
$\overline{\text{UART\_RTS}}$	Output	**Request to Send.** Flow control signal.
$\overline{\text{UART\_RX}}$	Input	**Receive.** Receives input. Typically connects to a transceiver that meets the electrical requirements of the device with which it is communicating.
$\overline{\text{UART\_TX}}$	Output	**Transmit.** Transmits output. Typically connects to a transceiver that meets the electrical requirements of the device with which it is communicating.
xSPI_CLK	Output	**SPI Master Clock Output.** SPI master clock output.
xSPI_D2	InOut	**Data 2.** Transfers serial data in quad and octal modes.
xSPI_D3	InOut	**Data 3.** Transfers serial data in quad and octal modes.
xSPI_D4	InOut	**Data 4.** Transfers serial data in octal mode.
xSPI_D5	InOut	**Data 5.** Transfers serial data in octal mode.
xSPI_D6	InOut	**Data 6.** Transfers serial data in octal mode.
xSPI_D7	InOut	**Data 7.** Transfers serial data in octal mode.
xSPI_MISO	InOut	**Master In, Slave Out.** Transfers serial data. Operates in the same direction as SPI_MOSI in dual and quad modes.
xSPI_MOSI	InOut	**Master Out, Slave In.** Transfers serial data. Operates in the same direction as SPI_MISO in dual and quad modes.
xSPI_RWDS	InOut	**Read/Write Data Strobe.** Strobe input for data read from external device and output mask signal for RAM write operations. This pin is three-stated by default.
$\overline{\text{xSPI\_SEL[n]}}$	Output	**Slave Select Output n.** Used in master mode to enable the desired slave. This pin is three-stated by default.

SIGNAL DESCRIPTIONS

The processor pin definitions are shown in Table 9. The columns in this table provide the following information:

- The signal name column includes the signal name for every pin and the GPIO multiplexed pin function, where applicable.
- The description column provides a descriptive name for each signal.
- The port column shows whether or not a signal is multiplexed with other signals on a general-purpose I/O port pin.
- The pin name column identifies the name of the package pin (at power on reset) on which the signal is located (if a single function pin) or is multiplexed (if a general-purpose I/O pin).
- The DAI pins and their associated signal routing units (SRUs) connect inputs and outputs of the DAI peripherals (SPORT, ASRC, S/PDIF, and PCG). See the Digital Audio Interface (DAI) chapter of the ADSP-21560/21561/21564/21568 SHARC+ Processor Hardware Reference manual for complete information on the use of the DAIs and SRUs.

Table 9. ADSP-21560/21561/21564/21568 Signal Descriptions

Signal Name	Description	Port	Pin Name
C0_FLG0	SHARC Core 0 Flag Pin	A	PA_12
C0_FLG1	SHARC Core 0 Flag Pin	A	PA_13
C0_FLG2	SHARC Core 0 Flag Pin	B	PB_03
C0_FLG3	SHARC Core 0 Flag Pin	B	PB_02
CNT0_DG	CNT0 Count Down and Gate	B	PB_05
CNT0_UD	CNT0 Count Up and Direction	B	PB_03
CNT0_ZM	CNT0 Count Zero Marker	B	PB_04
DAI0_PIN01	DAI0 Pin 1	Not Muxed	DAI0_PIN01
DAI0_PIN02	DAI0 Pin 2	Not Muxed	DAI0_PIN02
DAI0_PIN03	DAI0 Pin 3	Not Muxed	DAI0_PIN03
DAI0_PIN04	DAI0 Pin 4	Not Muxed	DAI0_PIN04
DAI0_PIN05	DAI0 Pin 5	Not Muxed	DAI0_PIN05
DAI0_PIN06	DAI0 Pin 6	Not Muxed	DAI0_PIN06
DAI0_PIN07	DAI0 Pin 7	Not Muxed	DAI0_PIN07
DAI0_PIN08	DAI0 Pin 8	Not Muxed	DAI0_PIN08
DAI0_PIN09	DAI0 Pin 9	Not Muxed	DAI0_PIN09
DAI0_PIN10	DAI0 Pin 10	Not Muxed	DAI0_PIN10
DAI0_PIN19	DAI0 Pin 19	Not Muxed	DAI0_PIN19
DAI0_PIN20	DAI0 Pin 20	Not Muxed	DAI0_PIN20
DAI1_PIN01	DAI1 Pin 1	Not Muxed	DAI1_PIN01
DAI1_PIN02	DAI1 Pin 2	Not Muxed	DAI1_PIN02
DAI1_PIN03	DAI1 Pin 3	Not Muxed	DAI1_PIN03
DAI1_PIN04	DAI1 Pin 4	Not Muxed	DAI1_PIN04
DAI1_PIN05	DAI1 Pin 5	Not Muxed	DAI1_PIN05
DAI1_PIN06	DAI1 Pin 6	Not Muxed	DAI1_PIN06
DAI1_PIN07	DAI1 Pin 7	Not Muxed	DAI1_PIN07
DAI1_PIN08	DAI1 Pin 8	Not Muxed	DAI1_PIN08
DAI1_PIN09	DAI1 Pin 9	Not Muxed	DAI1_PIN09
DAI1_PIN10	DAI1 Pin 10	Not Muxed	DAI1_PIN10
DAI1_PIN19	DAI1 Pin 19	Not Muxed	DAI1_PIN19
DAI1_PIN20	DAI1 Pin 20	Not Muxed	DAI1_PIN20
JTG_TCK	JTAG Clock	Not Muxed	JTG_TCK
JTG_TDI	JTAG Serial Data In	Not Muxed	JTG_TDI
JTG_TDO	JTAG Serial Data Out	Not Muxed	JTG_TDO
JTG_TMS	JTAG Mode Select	Not Muxed	JTG_TMS
$\overline{\text{JTG\_TRST}}$	JTAG Reset	Not Muxed	$\overline{\text{JTG\_TRST}}$

Table 9. ADSP-21560/21561/21564/21568 Signal Descriptions (Continued)

Signal Name	Description	Port	Pin Name
MLB0_CLK	MLB0 Single-Ended Clock	B	PB_02
MLB0_DAT	MLB0 Single-Ended Data	B	PB_00
MLB0_SIG	MLB0 Single-Ended Signal	B	PB_01
SPI0_CLK	SPI0 Clock	A	PA_06
SPI0_MISO	SPI0 Master In, Slave Out	A	PA_07
SPI0_MOSI	SPI0 Master Out, Slave In	A	PA_08
SPI0_RDY	SPI0 Ready	Not Muxed	SPI0_RDY
$\overline{\text{SPI0\_SEL1}}$	SPI0 Slave Select Output 1	A	PA_09
$\overline{\text{SPI0\_SEL2}}$	SPI0 Slave Select Output 2	B	PB_05
$\overline{\text{SPI0\_SS}}$	SPI0 Slave Select Input	A	PA_09
SPI1_CLK	SPI1 Clock	A	PA_10
SPI1_D2	SPI1 Data 2	A	PA_14
SPI1_D3	SPI1 Data 3	A	PA_15
SPI1_MISO	SPI1 Master In, Slave Out	A	PA_11
SPI1_MOSI	SPI1 Master Out, Slave In	A	PA_12
SPI1_RDY	SPI1 Ready	B	PB_04
$\overline{\text{SPI1\_SEL1}}$	SPI1 Slave Select Output 1	A	PA_13
$\overline{\text{SPI1\_SS}}$	SPI1 Slave Select Input	A	PA_13
SPI2_CLK	SPI2 Clock	A	PA_04
SPI2_D2	SPI2 Data 2	A	PA_02
SPI2_D3	SPI2 Data 3	A	PA_03
SPI2_MISO	SPI2 Master In, Slave Out	A	PA_00
SPI2_MOSI	SPI2 Master Out, Slave In	A	PA_01
SPI2_RDY	SPI2 Ready	B	PB_05
$\overline{\text{SPI2\_SEL1}}$	SPI2 Slave Select Output 1	A	PA_05
$\overline{\text{SPI2\_SEL2}}$	SPI2 Slave Select Output 2	B	PB_03
$\overline{\text{SPI2\_SS}}$	SPI2 Slave Select Input	A	PA_05
SYS_BMODE0	Boot Mode Control	Not Muxed	SYS_BMODE0
SYS_BMODE1	Boot Mode Control	Not Muxed	SYS_BMODE1
SYS_BMODE2	Boot Mode Control	Not Muxed	SYS_BMODE2
SYS_CLKIN0	Clock/Crystal Input	Not Muxed	SYS_CLKIN0
SYS_CLKOUT	Processor Clock Output	Not Muxed	SYS_CLKOUT
$\overline{\text{SYS\_FAULT}}$	Active-Low Fault Output	Not Muxed	$\overline{\text{SYS\_FAULT}}$
$\overline{\text{SYS\_HWRST}}$	Processor Hardware Reset Control	Not Muxed	$\overline{\text{SYS\_HWRST}}$
$\overline{\text{SYS\_RESOUT}}$	Reset Output	Not Muxed	$\overline{\text{SYS\_RESOUT}}$
SYS_XTAL0	Crystal Output	Not Muxed	SYS_XTAL0
TM0_ACI0	TIMER0 Alternate Capture Input 0	A	PA_07
TM0_ACI1	TIMER0 Alternate Capture Input 1	A	PA_14
TM0_ACI3	TIMER0 Alternate Capture Input 3	B	PB_00
TM0_ACI4	TIMER0 Alternate Capture Input 4	A	PA_11
TM0_ACLK1	TIMER0 Alternate Clock 1	A	PA_06
TM0_ACLK2	TIMER0 Alternate Clock 2	A	PA_08
TM0_ACLK3	TIMER0 Alternate Clock 3	A	PA_02
TM0_ACLK4	TIMER0 Alternate Clock 4	B	PB_02
TM0_CLK	TIMER0 Clock	B	PB_01
TM0_TMR0	TIMER0 Timer 0	A	PA_10
TM0_TMR1	TIMER0 Timer 1	A	PA_12
TM0_TMR2	TIMER0 Timer 2	A	PA_13

Table 9. ADSP-21560/21561/21564/21568 Signal Descriptions (Continued)

Signal Name	Description	Port	Pin Name
TM0_TMR3	TIMER0 Timer 3	B	PB_03
TM0_TMR4	TIMER0 Timer 4	B	PB_04
TM0_TMR5	TIMER0 Timer 5	B	PB_05
TWI0_SCL	TWI0 Serial Clock	A	PA_10
TWI0_SDA	TWI0 Serial Data	A	PA_11
TWI1_SCL	TWI1 Serial Clock	B	PB_00
TWI1_SDA	TWI1 Serial Data	B	PB_01
TWI2_SCL	TWI2 Serial Clock	A	PA_14
TWI2_SDA	TWI2 Serial Data	A	PA_15
TWI3_SCL	TWI3 Serial Clock	A	PA_02
TWI3_SDA	TWI3 Serial Data	A	PA_03
$\overline{\text{UART0\_CTS}}$	UART0 Clear to Send	A	PA_09
$\overline{\text{UART0\_RTS}}$	UART0 Request to Send	A	PA_08
$\overline{\text{UART0\_RX}}$	UART0 Receive	A	PA_07
$\overline{\text{UART0\_TX}}$	UART0 Transmit	A	PA_06
$\overline{\text{UART1\_CTS}}$	UART1 Clear to Send	B	PB_01
$\overline{\text{UART1\_RTS}}$	UART1 Request to Send	B	PB_00
$\overline{\text{UART1\_RX}}$	UART1 Receive	A	PA_14
$\overline{\text{UART1\_TX}}$	UART1 Transmit	A	PA_15
xSPI0_CLK	xSPI0 Clock	A	PA_04
xSPI0_D2	xSPI0 Data 2	A	PA_02
xSPI0_D3	xSPI0 Data 3	A	PA_03
xSPI0_D4	xSPI0 Data 4	A	PA_06
xSPI0_D5	xSPI0 Data 5	A	PA_07
xSPI0_D6	xSPI0 Data 6	A	PA_08
xSPI0_D7	xSPI0 Data 7	A	PA_09
xSPI0_MISO/D1	xSPI0 Master In, Slave Out	A	PA_00
xSPI0_MOSI/D0	xSPI0 Master Out, Slave In	A	PA_01
xSPI0_RWDS	xSPI0 Read/Write Data Strobe	Not Muxed	xSPI0_RWDS
$\overline{\text{xSPI0\_SEL1}}$	xSPI0 Slave Select Output 1	A	PA_05
$\overline{\text{xSPI0\_SEL2}}$	xSPI0 Slave Select Output 2	Not Muxed	$\overline{\text{xSPI0\_SEL2}}$

GPIO MULTIPLEXING

Table 10 and Table 11 identify the pin functions that are multiplexed on the general-purpose I/O pins.

Table 10. Signal Multiplexing for Port A

Signal Name	Multiplexed Function 0	Multiplexed Function 1	Multiplexed Function 2	Multiplexed Function Input Tap
PA_00	SPI2_MISO	xSPI0_MISO/D1		
PA_01	SPI2_MOSI	xSPI0_MOSI/D0		
PA_02	SPI2_D2	xSPI0_D2	TWI3_SCL	TM0_ACLK3
PA_03	SPI2_D3	xSPI0_D3	TWI3_SDA	
PA_04	SPI2_CLK	xSPI0_CLK		
PA_05	SPI2_SEL1	xSPI0_SEL1		SPI2_SS
PA_06	SPI0_CLK	UART0_TX	xSPI0_D4	TM0_ACLK1
PA_07	SPI0_MISO	UART0_RX	xSPI0_D5	TM0_ACI0
PA_08	SPI0_MOSI	UART0_RTS	xSPI0_D6	TM0_ACLK2
PA_09	SPI0_SEL1	UART0_CTS	xSPI0_D7	SPI0_SS
PA_10	TWI0_SCL	SPI1_CLK	TM0_TMR0	
PA_11	TWI0_SDA	SPI1_MISO		TM0_ACI4
PA_12	C0_FLG0	SPI1_MOSI	TM0_TMR1	
PA_13	C0_FLG1	SPI1_SEL1	TM0_TMR2	SPI1_SS
PA_14	TWI2_SCL	SPI1_D2	UART1_RX	TM0_ACI1
PA_15	TWI2_SDA	SPI1_D3	UART1_TX	

Table 11. Signal Multiplexing for Port B

Signal Name	Multiplexed Function 0	Multiplexed Function 1	Multiplexed Function 2	Multiplexed Function Input Tap
PB_00	MLB0_DAT	TWI1_SCL	UART1_RTS	TM0_ACI3
PB_01	MLB0_SIG	TWI1_SDA	UART1_CTS	TM0_CLK
PB_02	MLB0_CLK	C0_FLG3		TM0_ACLK4
PB_03	TM0_TMR3	C0_FLG2	SPI2_SEL2	CNT0_UD
PB_04	TM0_TMR4	SPI1_RDY		CNT0_ZM
PB_05	TM0_TMR5	SPI2_RDY	SPI0_SEL2	CNT0_DG

Table 12 shows the internal timer signal routing. This table applies to both the 400-ball CSP_BGA and 120-lead LQFP packages.

Table 12. Internal Timer Signal Routing

Timer Input Signal	Internal Source
TM0_ACLK0	SYS_CLKIN0
TM0_ACI5	DAI0_PB04_O
TM0_ACLK5	DAI0_PB03_O
TM0_ACI6	DAI1_PB04_O
TM0_ACLK6	DAI1_PB03_O
TM0_ACI7	CNT0_TO signal
TM0_ACLK7	SYS_CLKIN0
TM0_ACI8	DAI0_PB06_O
TM0_ACLK8	DAI0_PB05_O
TM0_ACI9	DAI1_PB06_O
TM0_ACLK9	DAI1_PB05_O

ADSP-21560/21561/21564/21568 DESIGNER QUICK REFERENCE

Table 13 provides a quick reference summary of pin related information for circuit board design. The columns in this table provide the following information:

- The signal name column includes the signal name for every pin and the GPIO multiplexed pin function, where applicable.
- The type column identifies the I/O type or supply type of the pin. The abbreviations used in this column are analog (a), supply (s), ground (g) and Input, Output, and InOut.
- The driver type column identifies the driver type used by the corresponding pin. The driver types are defined in the Output Drive Currents section of this data sheet.
- The internal termination column specifies the termination present after the processor is powered up (both during reset and after reset).
- The reset termination column specifies the termination present when the processor is in the reset state.
- The reset drive column specifies the active drive on the signal when the processor is in the reset state.
- The power domain column specifies the power supply domain in which the signal resides.
- The description and notes column identifies any special requirements or characteristics for a signal. These recommendations apply whether or not the hardware block associated with the signal is featured on the product. If no special requirements are listed, the signal can be left unconnected if it is not used. For multiplexed GPIO pins, this column identifies the functions available on the pin.

Table 13. ADSP-21560/21561/21564/21568 Designer Quick Reference

Signal Name	Type	Driver Type	Internal Termination	Reset Termination	Reset Drive	Power Domain	Description and Notes
DAI0_PIN01	InOut	A	Programmable pull-up/pull-down[1]	None	None	VDD_EXT	Desc: DAI0 Pin 1 Notes: See note[2]
DAI0_PIN02	InOut	A	Programmable pull-up/pull-down[1]	None	None	VDD_EXT	Desc: DAI0 Pin 2 Notes: See note[2]
DAI0_PIN03	InOut	A	Programmable pull-up/pull-down[1]	None	None	VDD_EXT	Desc: DAI0 Pin 3 Notes: See note[2]
DAI0_PIN04	InOut	A	Programmable pull-up/pull-down[1]	None	None	VDD_EXT	Desc: DAI0 Pin 4 Notes: See note[2]
DAI0_PIN05	InOut	A	Programmable pull-up/pull-down[1]	None	None	VDD_EXT	Desc: DAI0 Pin 5 Notes: See note[2]
DAI0_PIN06	InOut	A	Programmable pull-up/pull-down[1]	None	None	VDD_EXT	Desc: DAI0 Pin 6 Notes: See note[2]
DAI0_PIN07	InOut	A	Programmable pull-up/pull-down[1]	None	None	VDD_EXT	Desc: DAI0 Pin 7 Notes: See note[2]
DAI0_PIN08	InOut	A	Programmable pull-up/pull-down[1]	None	None	VDD_EXT	Desc: DAI0 Pin 8 Notes: See note[2]
DAI0_PIN09	InOut	A	Programmable pull-up/pull-down[1]	None	None	VDD_EXT	Desc: DAI0 Pin 9 Notes: See note[2]
DAI0_PIN10	InOut	A	Programmable pull-up/pull-down[1]	None	None	VDD_EXT	Desc: DAI0 Pin 10 Notes: See note[2]
DAI0_PIN19	InOut	A	Programmable pull-up/pull-down[1]	None	None	VDD_EXT	Desc: DAI0 Pin 19 Notes: See note[2]
DAI0_PIN20	InOut	A	Programmable pull-up/pull-down[1]	None	None	VDD_EXT	Desc: DAI0 Pin 20 Notes: See note[2]
DAI1_PIN01	InOut	A	Programmable pull-up/pull-down[1]	None	None	VDD_EXT	Desc: DAI1 Pin 1 Notes: See note[2]
DAI1_PIN02	InOut	A	Programmable pull-up/pull-down[1]	None	None	VDD_EXT	Desc: DAI1 Pin 2 Notes: See note[2]
DAI1_PIN03	InOut	A	Programmable pull-up/pull-down[1]	None	None	VDD_EXT	Desc: DAI1 Pin 3 Notes: See note[2]

Table 13. ADSP-21560/21561/21564/21568 Designer Quick Reference (Continued)

Signal Name	Type	Driver Type	Internal Termination	Reset Termination	Reset Drive	Power Domain	Description and Notes
DAI1_PIN04	InOut	A	Programmable pull-up/pull-down[1]	None	None	VDD_EXT	Desc: DAI1 Pin 4 Notes: See note[2]
DAI1_PIN05	InOut	A	Programmable pull-up/pull-down[1]	None	None	VDD_EXT	Desc: DAI1 Pin 5 Notes: See note[2]
DAI1_PIN06	InOut	A	Programmable pull-up/pull-down[1]	None	None	VDD_EXT	Desc: DAI1 Pin 6 Notes: See note[2]
DAI1_PIN07	InOut	A	Programmable pull-up/pull-down[1]	None	None	VDD_EXT	Desc: DAI1 Pin 7 Notes: See note[2]
DAI1_PIN08	InOut	A	Programmable pull-up/pull-down[1]	None	None	VDD_EXT	Desc: DAI1 Pin 8 Notes: See note[2]
DAI1_PIN09	InOut	A	Programmable pull-up/pull-down[1]	None	None	VDD_EXT	Desc: DAI1 Pin 9 Notes: See note[2]
DAI1_PIN10	InOut	A	Programmable pull-up/pull-down[1]	None	None	VDD_EXT	Desc: DAI1 Pin 10 Notes: See note[2]
DAI1_PIN19	InOut	A	Programmable pull-up/pull-down[1]	None	None	VDD_EXT	Desc: DAI1 Pin 19 Notes: See note[2]
DAI1_PIN20	InOut	A	Programmable pull-up/pull-down[1]	None	None	VDD_EXT	Desc: DAI1 Pin 20 Notes: See note[2]
GND	g		None	None	None		Desc: Ground Notes: No notes
JTG_TCK	Input		Pull-up	Pull-up	None	VDD_EXT	Desc: JTAG clock Notes: See note[2]
JTG_TDI	Input		Pull-up	Pull-up	None	VDD_EXT	Desc: JTAG serial data in Notes: See note[2]
JTG_TDO	Output	A	None	None	High-Z when $\overline{\text{JTG\_TRST}}$ is low, not affected by $\overline{\text{SYS\_HWRST}}$	VDD_EXT	Desc: JTAG serial data out Notes: No notes
JTG_TMS	InOut	A	Pull-up	Pull-up	None	VDD_EXT	Desc: JTAG mode select Notes: See note[2]
$\overline{\text{JTG\_TRST}}$	Input		Pull-down	Pull-down	None	VDD_EXT	Desc: JTAG reset Notes: See note[2]
PA_00	InOut	A	Programmable pull-up/pull-down[1]	None	None	VDD_EXT	Desc: Port A Position 0 Notes: See note[2]
PA_01	InOut	A	Programmable pull-up/pull-down[1]	None	None	VDD_EXT	Desc: Port A Position 1 Notes: See note[2]
PA_02	InOut	A	Programmable pull-up/pull-down[1]	None	None	VDD_EXT	Desc: Port A Position 2 Notes: See note[2]
PA_03	InOut	A	Programmable pull-up/pull-down[1]	None	None	VDD_EXT	Desc: Port A Position 3 Notes: See note[2]
PA_04	InOut	A	Programmable pull-up/pull-down[1]	None	None	VDD_EXT	Desc: Port A Position 4 Notes: See note[2]
PA_05	InOut	A	Programmable pull-up/pull-down[1]	None	None	VDD_EXT	Desc: Port A Position 5 Notes: See note[2]
PA_06	InOut	A	Programmable pull-up/pull-down[1]	None	None	VDD_EXT	Desc: Port A Position 6 Notes: See note[2]

Table 13. ADSP-21560/21561/21564/21568 Designer Quick Reference (Continued)

Signal Name	Type	Driver Type	Internal Termination	Reset Termination	Reset Drive	Power Domain	Description and Notes
PA_07	InOut	A	Programmable pull-up/pull-down[1]	None	None	VDD_EXT	Desc: Port A Position 7 Notes: See note[2]
PA_08	InOut	A	Programmable pull-up/pull-down[1]	None	None	VDD_EXT	Desc: Port A Position 8 Notes: See note[2]
PA_09	InOut	A	Programmable pull-up/pull-down[1]	None	None	VDD_EXT	Desc: Port A Position 9 Notes: See note[2]
PA_10	InOut	A	Programmable pull-up/pull-down[1]	None	None	VDD_EXT	Desc: Port A Position 10 Notes: See note[2]
PA_11	InOut	A	Programmable pull-up/pull-down[1]	None	None	VDD_EXT	Desc: Port A Position 11 Notes: See note[2]
PA_12	InOut	A	Programmable pull-up/pull-down[1]	None	None	VDD_EXT	Desc: Port A Position 12 Notes: See note[2]
PA_13	InOut	A	Programmable pull-up/pull-down[1]	None	None	VDD_EXT	Desc: Port A Position 13 Notes: See note[2]
PA_14	InOut	A	Programmable pull-up/pull-down[1]	None	None	VDD_EXT	Desc: Port A Position 14 Notes: See note[2]
PA_15	InOut	A	Programmable pull-up/pull-down[1]	None	None	VDD_EXT	Desc: Port A Position 15 Notes: See note[2]
PB_00	InOut	A	Programmable pull-up/pull-down[1]	None	None	VDD_EXT	Desc: Port B Position 0 Notes: See note[2]
PB_01	InOut	A	Programmable pull-up/pull-down[1]	None	None	VDD_EXT	Desc: Port B Position 1 Notes: See note[2]
PB_02	InOut	A	Programmable pull-up/pull-down[1]	None	None	VDD_EXT	Desc: Port B Position 2 Notes: See note[2]
PB_03	InOut	A	Programmable pull-up/pull-down[1]	None	None	VDD_EXT	Desc: Port B Position 3 Notes: See note[2]
PB_04	InOut	A	Programmable pull-up/pull-down[1]	None	None	VDD_EXT	Desc: Port B Position 4 Notes: See note[2]
PB_05	InOut	A	Programmable pull-up/pull-down[1]	None	None	VDD_EXT	Desc: Port B Position 5 Notes: See note[2]
SPI0_RDY	InOut	A	Programmable pull-up/pull-down[1]	None	None	VDD_EXT	Desc: SPI Ready Notes: See note[2]
SYS_BMODE0	Input	NA	None	None	None	VDD_EXT	Desc: Boot Mode Control 0 Notes: Cannot be left unconnected
SYS_BMODE1	Input	NA	None	None	None	VDD_EXT	Desc: Boot Mode Control 1 Notes: Cannot be left unconnected
SYS_BMODE2	Input	NA	Pull-down	None	None	VDD_EXT	Desc: Boot Mode Control 2 Notes: No notes
SYS_CLKIN0	a	NA	None	None	None	VDD_INT	Desc: Clock/crystal input Notes: Cannot be left unconnected
SYS_CLKOUT	a	A	None	None	None	VDD_EXT	Desc: Processor clock output Notes: No notes
$\overline{\text{SYS\_FAULT}}$	InOut	A	None	None	None	VDD_EXT	Desc: Active low fault output Notes: External pull-up required to keep signal in deasserted state
$\overline{\text{SYS\_HWRST}}$	Input	NA	None	None	None	VDD_EXT	Desc: Processor hardware reset control Notes: Cannot be left unconnected

Table 13. ADSP-21560/21561/21564/21568 Designer Quick Reference (Continued)

Signal Name	Type	Driver Type	Internal Termination	Reset Termination	Reset Drive	Power Domain	Description and Notes
$\overline{\text{SYS\_RESOUT}}$	Output	A	None	None	L	VDD_EXT	Desc: Reset output Notes: No notes
SYS_XTAL0	a	NA	None	None	None	VDD_INT	Desc: Crystal output Notes: Leave unconnected if an oscillator provides SYS_CLKIN0
VDD_EXT	s		None	None	None		Desc: External voltage domain Notes: No notes
VDD_INT	s		None	None	None		Desc: Internal voltage domain Notes: No notes
VDD_REF	s		None	None	None		Desc: External voltage reference Notes: No notes
xSPI_RWDS	InOut	A	Programmable pull-up/pull-down[1]	None	None	VDD_EXT	Desc: xSPI Read/Write Data Strobe Notes: See note[2]
$\overline{\text{xSPI\_SEL2}}$	Output	A	Programmable pull-up/pull-down[1]	None	None	VDD_EXT	Desc: xSPI Slave Select Output 2 Notes: See note[2]

[1] Disabled by default.

[2] When present, the internal pull-up/pull-down design holds the internal path from the pins at the expected logic levels. To pull up or pull down the external pads to the expected logic levels, use external resistors.

PRELIMINARY SPECIFICATIONS

Specifications are subject to change without notice. For information about product specifications, contact your Analog Devices, Inc., representative.

PRELIMINARY OPERATING CONDITIONS

All specifications and characteristics apply across the entire operating conditions range unless otherwise noted.

All specifications are subject to change without notice.

Parameter		Conditions	Min	Nominal	Max	Unit
V_{DD_INT}	Internal (Core) Supply Voltage	400 MHz ≤ CCLK ≤ 1 GHz	0.855	0.900	0.945	V
V_{DD_EXT}	External (I/O) Supply Voltage		3.13	3.30	3.47	V
V_{DD_REF}	High Voltage Supply of PLL and OTP		1.71	1.80	1.89	V
V_{IH}[1]	High Level Input Voltage	V_{DD_EXT} = 3.47 V	2.2			V
$V_{IHCLKIN}$[2]	High Level Clock Input Voltage	V_{DD_INT} = 0.945 V	0.68		V_{DD_INT}	V
V_{IL}[1]	Low Level Input Voltage	V_{DD_EXT} = 3.13 V			0.7	V
$V_{ILCLKIN}$[2]	Low Level Clock Input Voltage	V_{DD_INT} = 0.855 V	–0.30		+0.12	V
CONSUMER GRADE						
T_J	Junction Temperature 400-ball CSP_BGA		0		125	°C
T_J	Junction Temperature 120-Lead LQFP_EP		0		125	°C
INDUSTRIAL GRADE						
T_J	Junction Temperature 400-ball CSP_BGA		–40		+125	°C
T_J	Junction Temperature 120-Lead LQFP_EP		–40		+125	°C
AUTOMOTIVE GRADE[3]						
T_J	Junction Temperature 400-ball CSP_BGA		–40		+125	°C
T_J	Junction Temperature 120-Lead LQFP_EP		–40		+125	°C

[1] Parameter value applies to all input and bidirectional pins.
[2] Applies to SYS_CLKIN0 pin.
[3] Automotive application use profile only. Not supported for nonautomotive use. Contact Analog Devices for more information.

Clock Related Operating Conditions

Table 14 describes the core clock, system clock, and peripheral clock timing requirements. The data presented in the table applies to all speed grades except where noted.

Table 14. Clock Operating Conditions

All specifications are subject to change without notice.						
Parameter		**Conditions**	**Min**	**Typ**	**Max**	**Unit**
f_{CCLK}	Core Clock (CCLK) Frequency	$f_{CCLK} = 2 \times f_{SYSCLK}$	400		1000	MHz
f_{SYSCLK}	SYSCLK Frequency[1]		200.0		500	MHz
f_{SCLK0}	SCLK0 Frequency	$f_{SYSCLK} = N \times f_{SCLK0}$ where N = 2 or 4 or 6	30.000		125	MHz
f_{SCLK1}	SCLK1 Frequency	$f_{SYSCLK} \geq f_{SCLK1}$			333.3	MHz
f_{OCLK}	Output Clock (OCLK) Frequency[2]				125	MHz
$f_{SYS\_CLKOUTJ}$	SYS_CLKOUT Period Jitter[3, 4]			±1		%
$f_{SPTCLKPROG}$	Programmed SPT Clock When Transmitting Data and Frame Sync				62.5	MHz
$f_{SPTCLKPROG}$	Programmed SPT Clock When Receiving Data or Frame Sync				31.25	MHz
$f_{SPTCLKEXT}$	External SPT Clock When Receiving Data and Frame Sync	$f_{SPTCLKEXT} \leq f_{SCLK0}$			62.5	MHz
$f_{SPTCLKEXT}$	External SPT Clock Transmitting Data or Frame Sync	$f_{SPTCLKEXT} \leq f_{SCLK0}$			31.25	MHz
$f_{SPICLKPROG}$	Programmed SPI Clock When Transmitting Data	f_{SPICLK}:f_{SCLK0} ratio = 1:1			83.33	MHz
$f_{SPICLKPROG}$	Programmed SPI Clock When Receiving Data	f_{SPICLK}:f_{SCLK0} ratio = 1:1			83.33	MHz
$f_{SPICLKPROG}$	Programmed SPI Clock When Transmitting Data	f_{SPICLK}:f_{SCLK0} ratio = 1:2			62.5	MHz
$f_{SPICLKPROG}$	Programmed SPI Clock When Receiving Data	f_{SPICLK}:f_{SCLK0} ratio = 1:2			62.5	MHz
$f_{SPICLKEXT}$	External SPI Clock When Receiving Data	$f_{SPICLKEXT} \leq f_{CDU\_CLKO0}$			50	MHz
$f_{SPICLKEXT}$	External SPI Clock When Transmitting Data	$f_{SPICLKEXT} \leq f_{CDU\_CLKO0}$			50	MHz
$f_{xSPICLKPROG}$	Programmed xSPI Clock With Data Training and Without DQS[5]				125	MHz
$f_{xSPICLKPROG}$	Programmed xSPI Clock With Data Training and With DQS[5]				166.66	MHz
$f_{TMRCLKEXT}$	External Timer Clock (TMx_CLK)	$f_{TMRCLKEXT} \leq f_{SCLK0} / 4$			31.25	MHz

[1] When using MLB, there is a requirement that the f_{SYSCLK} value must be a minimum of 100 MHz for 3-pin mode and for all supported speeds.
[2] f_{OCLK} must not exceed f_{SCLK0} when selected as SYS_CLKOUT.
[3] SYS_CLKOUT jitter is dependent on the application system design including pin switching activity, board layout, and the jitter characteristics of the SYS_CLKIN source. Due to the dependency on these factors, the measured jitter may be higher or lower than this typical specification for each end application.
[4] The value in the Typ field is the percentage of the SYS_CLKOUT period.
[5] With offline PHY training methodology, the maximum programmed xSPI clock, which can be used without DQS and with DQS, is TBD MHz and TBD MHz respectively. For additional details, refer to xSPI PHY Configuration and Training (EE-TBD).

Table 15. Phase-Locked Loop (PLL) Operating Conditions

All specifications are subject to change without notice.				
Parameter		**Min**	**Max**	**Unit**
f_{PLLCLK}	PLL Clock Frequency	0.60	1.00	GHz

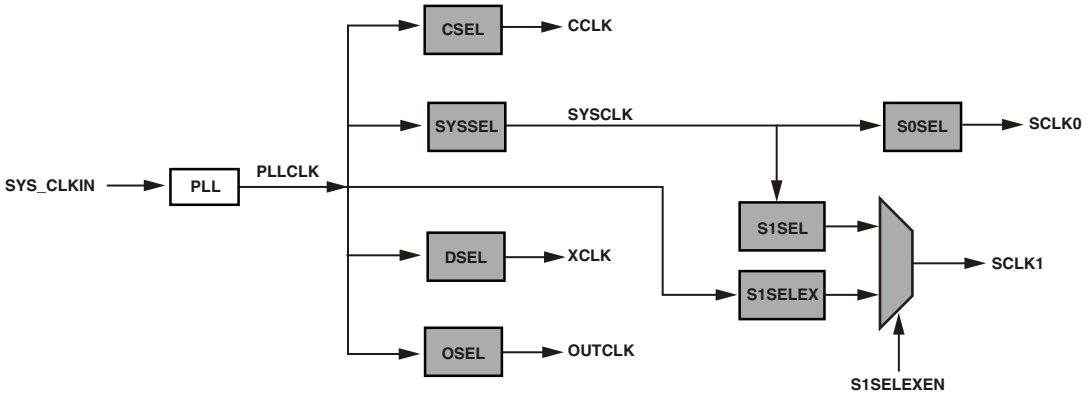


Figure 6. Clock Relationships and Divider Values

PRELIMINARY ELECTRICAL CHARACTERISTICS

All specifications and characteristics apply across the entire operating conditions range unless otherwise noted.

Parameter		Conditions	Min	Typ	Max	Unit
V_{OH}	High Level Output Voltage	V_{DD_EXT} = minimum, (I_{OH} = –2.0 mA, DS1), (I_{OH} = –4.0 mA, DS2)[1], (I_{OH} = –6.0 mA, DS3)[2]	2.4			V
V_{OL}	Low Level Output Voltage	V_{DD_EXT} = minimum, (I_{OL} = 2.0 mA, DS1), (I_{OL} = 4.0 mA, DS2)[1], (I_{OL} = 6.0 mA, DS3)[2]			0.4	V
V_{OH_XTAL}[3]	High Level Output Voltage	V_{DD_INT} = minimum, I_{OH} = –10.0 nA	0.58			V
V_{OL_XTAL}[3]	Low Level Output Voltage	V_{DD_INT} = minimum, I_{OL} = 10.0 nA			0.3	V
I_{IH}[4]	High Level Input Current	V_{DD_EXT} = maximum, V_{IN} = V_{DD_EXT} maximum			10	µA
I_{IL}[4]	Low Level Input Current	V_{DD_EXT} = maximum, V_{IN} = 0 V			10	µA
I_{IL_PU}[5]	Low Level Input Current Pull-Up	V_{DD_EXT} = maximum, V_{IN} = 0 V			250	µA
I_{IH_PD}[6]	High Level Input Current Pull-Down	V_{DD_EXT} = maximum, V_{IN} = V_{DD_EXT} maximum			250	µA
I_{OZH}[7]	Three-State Leakage Current	V_{DD_EXT} = maximum, V_{IN} = V_{DD_EXT} maximum			10	µA
I_{OZL}[7]	Three-State Leakage Current	V_{DD_EXT} = maximum, V_{IN} = 0 V			10	µA
C_{IN}[8]	Input Capacitance	T_J = 25°C			5	pF
I_{DD_IDLE}	V_{DD_INT} Current in Idle	f_{CCLK} = 1000 MHz ASF_{SHARC} = 0.39 f_{SYSCLK} = 500 MHz f_{SCLK0} = 125 MHz f_{SCLK1} = 250 MHz (Other clocks are disabled) No peripheral or DMA activity T_J = 25°C V_{DD_INT} = 0.9 V		410		mA
I_{DD_TYP}	V_{DD_INT} Current	f_{CCLK} = 1000 MHz ASF_{SHARC} = 1.0 f_{SYSCLK} = 500 MHz f_{SCLK0} = 125 MHz f_{SCLK1} = 250 MHz (Other clocks are disabled) DMA data rate = 328 MB/s T_J = 25°C V_{DD_INT} = 0.9 V		748		mA

Parameter		Conditions	Min	Typ	Max	Unit
I_{DD_IDLE}	V_{DD_INT} Current in Idle	f_{CCLK} = 800 MHz ASF_{SHARC} = 0.39 f_{SYSCLK} = 400 MHz f_{SCLK0} = 100 MHz f_{SCLK1} = 228.6 MHz (Other clocks are disabled) No peripheral or DMA activity T_J = 25°C V_{DD_INT} = 0.9 V		344		mA
I_{DD_TYP}	V_{DD_INT} Current	f_{CCLK} = 800 MHz ASF_{SHARC} = 1.0 f_{SYSCLK} = 400 MHz f_{SCLK0} = 100 MHz f_{SCLK1} = 228.6 MHz (Other clocks are disabled) DMA data rate = 328 MB/s T_J = 25°C V_{DD_INT} = 0.9 V		619		mA
I_{DD_IDLE}	V_{DD_INT} Current in Idle	f_{CCLK} = 600 MHz ASF_{SHARC} = 0.39 f_{SYSCLK} = 300 MHz f_{SCLK0} = 75 MHz f_{SCLK1} = 300 MHz (Other clocks are disabled) No peripheral or DMA activity T_J = 25°C V_{DD_INT} = 0.9 V		280		mA
I_{DD_TYP}	V_{DD_INT} Current	f_{CCLK} = 600 MHz ASF_{SHARC} = 1.0 f_{SYSCLK} = 300 MHz f_{SCLK0} = 75 MHz f_{SCLK1} = 300 MHz (Other clocks are disabled) DMA data rate = 328 MB/s T_J = 25°C V_{DD_INT} = 0.9 V		490		mA
I_{DD_INT}[9]	V_{DD_INT} Current	f_{CCLK} > 0 MHz $f_{SCLK0/1} \geq 0$ MHz			$I_{DD\_INT\_TOT}$ See equation in the Total Internal Power Dissipation section.	mA

[1] Applies to all output and bidirectional pins operating at less than or equal to 62.5 MHz, except SYS_XTAL0.
[2] Applies to all output and bidirectional pins operating above 62.5 MHz and less than or equal to 125 MHz.
[3] Applies to SYS_XTAL0 pin.
[4] Applies to input pins: SYS_BMODE2-0, SYS_CLKIN, and $\overline{\text{SYS\_HWRST}}$.
[5] Applies to input pins with internal pull-ups: JTG_TDI, JTG_TMS, and JTG_TCK.
[6] Applies to JTAG_TRST signal.
[7] Applies to signals: PA15 to PA0, PB5 to PB0, DAI0_PINx, DAI1_PINx, $\overline{\text{SYS\_FAULT}}$, and JTG_TDO.
[8] Applies to all signal pins.
[9] See Estimating Power for ADSP-21560/21561/21564/21568 SHARC+ Processors (EE-471) for further information.

Total Internal Power Dissipation

Total power dissipation has two components:

- Static, including leakage current
- Dynamic, due to transistor switching characteristics for each clock domain

Many operating conditions can also affect power dissipation, including temperature, voltage, operating frequency, and processor activity. The following equation describes the internal current consumption.

$$I_{DD\_INT\_TOT} = I_{DD\_INT\_STATIC} + I_{DD\_INT\_CCLK\_SHARC\_DYN} + I_{DD\_INT\_SYSCLK\_DYN} + I_{DD\_INT\_SCLK0\_DYN} + I_{DD\_INT\_SCLK1\_DYN} + I_{DD\_INT\_OCLK\_DYN} + I_{DD\_INT\_ACCL\_DYN} + I_{DD\_INT\_DMA\_DR\_DYN} + I_{DD\_INT\_XCLK\_DYN}$$

where $I_{DD\_INT\_XCLK\_DYN}$ is XCLK supplied to the xSPI block and $I_{DD\_INT\_STATIC}$ is the sole contributor to the static power dissipation component and is specified as a function of voltage (V_{DD_INT}) and junction temperature (T_J) in Table 16.

Table 16. Static Current—$I_{DD\_INT\_STATIC}$ (mA)

	Voltage (V_{DD_INT})		
T_J (°C)	**0.855 V**	**0.900 V**	**0.945 V**
–40	7	10	12
–20	15	19	24
–10	21	26	33
0	30	37	46
+10	42	51	63
+25	68	82	100
+40	109	129	154
+55	169	198	235
+70	257	300	352
+85	380	440	513
+100	561	644	746
+105	634	725	838
+115	808	924	1067
+125	1026	1171	1350

The other seven addends in the $I_{DD\_INT\_TOT}$ equation comprise the dynamic power dissipation component and fall into four broad categories: application dependent currents, clock currents, currents from high speed peripheral operation, and data transmission currents.

Application Dependent Current

The application dependent currents include the dynamic current in the core clock domain of the SHARC+ core, as well as the dynamic current in the accelerator block.

Dynamic current consumed by the core is subject to an activity scaling factor (ASF) that represents application code running on the processor core (see Table 17). The ASF is combined with the CCLK frequency and V_{DD_INT} dependent dynamic current data in Table 18 to calculate this portion of the total dynamic power dissipation component.

$$I_{DD\_INT\_CCLK\_SHARC\_DYN} = \text{Table 18} \times ASF_{SHARC}$$

Table 17. Activity Scaling Factors for the SHARC+® Core (ASF_{SHARC})

I_{DD_INT} Power Vector	**ASF**
$I_{DD\text{-}LS}$	0.23
$I_{DD\text{-}IDLE}$	0.39
$I_{DD\text{-}NOP}$	0.62
$I_{DD\text{-}TYP\_3070}$	0.78
$I_{DD\text{-}TYP\_5050}$	0.89
$I_{DD\text{-}TYP\_7030}$	1.0
$I_{DD\text{-}PEAK\_100}$	1.1

Table 18. Dynamic Current for SHARC+®Core (mA, with ASF = 1.00)

	Voltage (V_{DD_INT})		
f_{CCLK} (MHz)	**0.855 V**	**0.900 V**	**0.945 V**
400	199	210	220
450	224	236	247
500	249	262	275
550	274	288	302
600	299	314	330
650	323	340	357
700	348	367	385
750	373	393	412
800	398	419	440
850	423	445	467
900	448	471	495
950	473	498	522
1000	498	524	550

Clock Current

The dynamic clock currents provide the total power dissipated by all transistors switching in the clock paths. The power dissipated by each clock domain is dependent on voltage (V_{DD_INT}), operating frequency, and a unique scaling factor.

$I_{DD\_INT\_SYSCLK\_DYN}$ (mA) = 0.254 × f_{SYSCLK} (MHz) × V_{DD_INT} (V)

$I_{DD\_INT\_SCLK0\_DYN}$ (mA) = 0.066 × f_{SCLK0} (MHz) × V_{DD_INT} (V)

$I_{DD\_INT\_SCLK1\_DYN}$ (mA) = 0.008 × f_{SCLK1} (MHz) × V_{DD_INT} (V)

$I_{DD\_INT\_OCLK\_DYN}$ (mA) = 0.026 × f_{OCLK} (MHz) × V_{DD_INT} (V)

$I_{DD\_INT\_XCLK\_DYN}$ (mA) = 0.021 × f_{XCLK} (MHz) × V_{DD_INT} (V)

Data Transmission Current

The data transmission current represents the power dissipated when moving data throughout the system via DMA. This current is proportional to the data rate. Refer to the power calculator available with Estimating Power for ADSP-21560/21561/21564/21568 SHARC+ Processors (EE-471) to estimate $I_{DD\_INT\_DMA\_DR\_DYN}$ based on the bandwidth of the data transfer.

ABSOLUTE MAXIMUM RATINGS

Stresses at or above those listed in Table 19 may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Table 19. Absolute Maximum Ratings

Parameter	Rating
Internal (Core) Supply Voltage (V_{DD_INT})	–0.3 V to +0.945 V
External (I/O) Supply Voltage (V_{DD_EXT})	–0.3 V to +3.47 V
High Voltage Supply of PLL and OTP (V_{DD_REF})	–0.3 V to +1.89 V
SYS_CLKIN0 Input Voltage[1]	–0.3 V to V_{DD_INT}
Digital Input Voltage[1, 2]	–0.3 V to +3.47 V
TWI Input Voltage[1, 3]	–0.3 V to +3.47 V
Output Voltage Swing	–0.3 V to V_{DD_EXT} +0.5 V
I_{OH}/I_{OL} Current per Signal[2]	6 mA (maximum)
Storage Temperature Range	–65°C to +150°C
Junction Temperature While Biased	125°C

[1] Applies only when the related power supply (VDD_INT, VDD_EXT) is within specification. When the power supply is below specification, the range is the voltage being applied to that power domain ± 0.2 V.

[2] Applies to 100% transient duty cycle.

[3] Applies to TWI_SCL and TWI_SDA.

Table 20. Maximum Duty Cycle for Input Transient Voltage for V_{DD_INT} and V_{DD_EXT}

V_{DD_INT} (V)[1]	V_{DD_EXT} (V)[1]	Maximum Duty Cycle[2]
0.945	3.470	100%

[1] The individual values cannot be combined for analysis of a single instance of overshoot or undershoot. The worst case observed value must fall within one of the voltages specified and the total duration of the overshoot or undershoot (exceeding the 100% case) must be less than or equal to the corresponding duty cycle.

[2] Duty cycle refers to the percentage of time the signal exceeds the value for the 100% case. This is equivalent to the measured duration of a single instance of overshoot or undershoot as a percentage of the period of occurrence.

Table 21. Maximum Duty Cycle for Input Transient Voltage

3.3 V V_{IN} Max (V)[1]	1.8 V V_{IN} Max (V)[1]	Maximum Duty Cycle[2]
3.47	1.89	100%

[1] The individual values cannot be combined for analysis of a single instance of overshoot or undershoot. The worst case observed value must fall within one of the voltages specified and the total duration of the overshoot or undershoot (exceeding the 100% case) must be less than or equal to the corresponding duty cycle.

[2] Duty cycle refers to the percentage of time the signal exceeds the value for the 100% case. This is equivalent to the measured duration of a single instance of overshoot or undershoot as a percentage of the period of occurrence.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PRELIMINARY TIMING SPECIFICATIONS

All specifications and characteristics apply across the entire operating conditions range unless otherwise noted.

Power-Up Reset Timing

Table 22 and Figure 7 show the relationship between power supply startup and processor reset timing, as relating to the clock generation unit (CGU) and the reset control unit (RCU).

In Figure 7, the $V_{DD\_SUPPLIES}$ are V_{DD_INT}, V_{DD_EXT}, and V_{DD_REF}.

Table 22. Power-Up Reset Timing

All specifications are subject to change without notice.				
Parameter		**Min**	**Max**	**Unit**
Timing Requirements				
$t_{RST\_IN\_PWR}$	$\overline{\text{SYS\_HWRST}}$ Deasserted after $V_{DD\_SUPPLIES}$ (V_{DD_INT}, V_{DD_EXT}, V_{DD_REF}) and SYS_CLKIN0 are Stable and Within Specification	11 × t_{CKIN}		ns
t_{PWR_UP}	$V_{DD\_SUPPLIES}$ Power Ramp Up	10		µs
t_{PWR_DOWN}	$V_{DD\_SUPPLIES}$ Power Ramp Down	10		µs

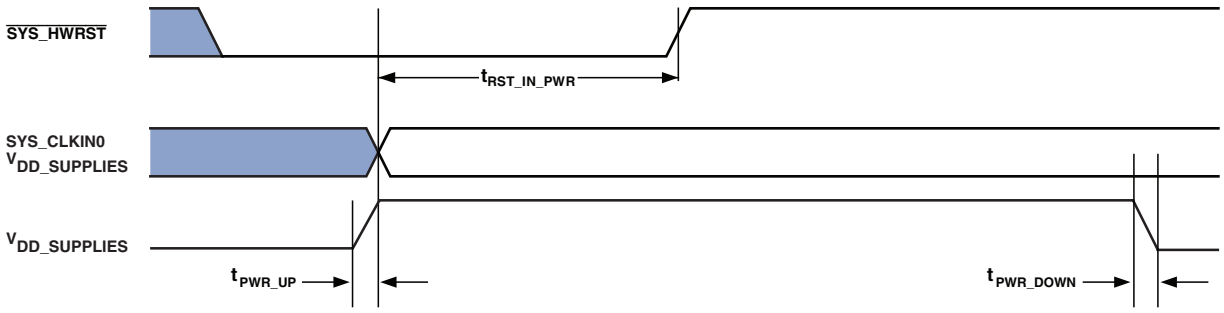


Figure 7. Power-Up Reset Timing

Clock and Reset Timing

Table 23 and Figure 8 describe clock and reset operations related to the CGU and RCU. Per the CCLK, SYSCLK, SCLKx, and OCLK timing specifications in Table 14 (Clock Operating Conditions), combinations of SYS_CLKIN0 and clock multipliers must not select clock rates in excess of the maximum instruction rate of the processor.

Table 23. Clock and Reset Timing

All specifications are subject to change without notice.				
Parameter		**Min**	**Max**	**Unit**
Timing Requirements				
f_{CKIN}	SYS_CLKIN0 Frequency (Crystal)[1, 2]	20	30	MHz
	SYS_CLKIN0 Frequency (External SYS_CLKIN0)[1, 2]	20	30	MHz
t_{CKINL}	SYS_CLKIN0 Low Pulse[1]	16.67		ns
t_{CKINH}	SYS_CLKIN0 High Pulse[1]	16.67		ns
t_{WRST}	$\overline{\text{RESET}}$ Asserted Pulse Width Low[3]	11 × t_{CKIN}		ns

[1] Applies to PLL bypass mode and PLL nonbypass mode.
[2] The t_{CKIN} period (see Figure 8) equals $1/f_{CKIN}$.
[3] Applies after power-up sequence is complete. See Table 22 and Figure 7 for power-up reset timing.

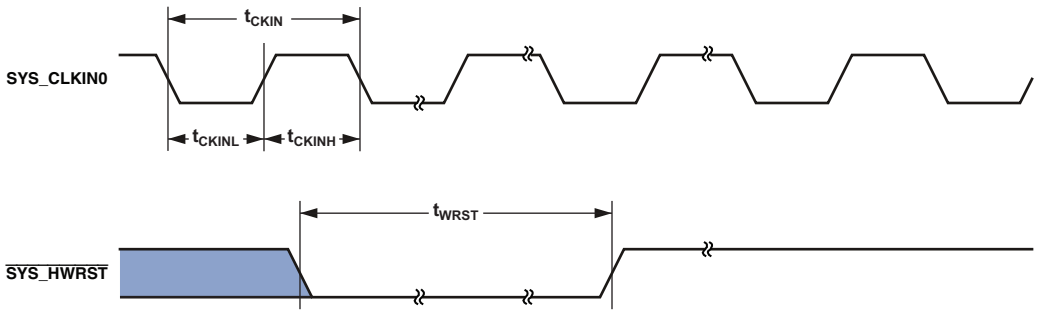


Figure 8. Clock and Reset Timing

Serial Ports (SPORTs)

To determine whether a device is compatible with the SPORT at clock speed n, the following specifications must be confirmed: frame sync delay and frame sync setup and hold; data delay and data setup and hold; and serial clock (SPTx_CLK) width. In Figure 9, either the rising edge or the falling edge of SPTx_A/BCLK (external or internal) can be used as the active sampling edge.

When externally generated, the SPORT clock is called $f_{SPTCLKEXT}$:

$$t_{SPTCLKEXT} = \frac{1}{f_{SPTCLKEXT}}$$

When internally generated, the programmed SPORT clock ($f_{SPTCLKPROG}$) frequency in megahertz is set by the following equation:

$$f_{SPTCLKPROG} = \frac{f_{SCLK0}}{(CLKDIV + 1)}$$

$$t_{SPTCLKPROG} = \frac{1}{f_{SPTCLKPROG}}$$

where *CLKDIV* is a field in the SPORT_DIV register that can be set from 0 to 65,535.

Table 24. SPORTs—External Clock[1]

All specifications are subject to change without notice.				
Parameter		**Min**	**Max**	**Unit**
Timing Requirements				
t_{SFSE}	Frame Sync Setup Before SPTx_CLK (Externally Generated Frame Sync in Either Transmit or Receive Mode)[2]	2		ns
t_{HFSE}	Frame Sync Hold After SPTx_CLK (Externally Generated Frame Sync in Either Transmit or Receive Mode)[2]	3		ns
t_{SDRE}	Receive Data Setup Before Receive SPTx_CLK[2]	2		ns
t_{HDRE}	Receive Data Hold After SPTx_CLK[2]	3		ns
$t_{SPTCLKW}$	SPTx_CLK Width[3]	$0.5 \times t_{SPTCLKEXT} - 1.5$		ns
t_{SPTCLK}	SPTx_CLK Period[3]	$t_{SPTCLKEXT} - 1.5$		ns
Switching Characteristics				
t_{DFSE}	Frame Sync Delay After SPTx_CLK (Internally Generated Frame Sync in Either Transmit or Receive Mode)[4]		11	ns
t_{HOFSE}	Frame Sync Hold After SPTx_CLK (Internally Generated Frame Sync in Either Transmit or Receive Mode)[4]	2		ns
t_{DDTE}	Transmit Data Delay After Transmit SPTx_CLK[4]		11	ns
t_{HDTE}	Transmit Data Hold After Transmit SPTx_CLK[4]	2		ns

[1] Specifications apply to all four SPORTs.
[2] Referenced to sample edge.
[3] This specification indicates the minimum instantaneous width or period that can be tolerated due to duty cycle variation or jitter on the ideal maximum external SPTx_CLK. For the external SPTx_CLK ideal maximum frequency, see the $f_{SPTCLKEXT}$ specification in Table 14.
[4] Referenced to drive edge.

Table 25. SPORTs—Internal Clock[1]

All specifications are subject to change without notice.				
Parameter		**Min**	**Max**	**Unit**
Timing Requirements				
t_{SFSI}	Frame Sync Setup Before SPTx_CLK (Externally Generated Frame Sync in Either Transmit or Receive Mode)[2]	12		ns
t_{HFSI}	Frame Sync Hold After SPTx_CLK (Externally Generated Frame Sync in Either Transmit or Receive Mode)[2]	–0.5		ns
t_{SDRI}	Receive Data Setup Before SPTx_CLK[2]	3.4		ns
t_{HDRI}	Receive Data Hold After SPTx_CLK[2]	2		ns
Switching Characteristics				
t_{DFSI}	Frame Sync Delay After SPTx_CLK (Internally Generated Frame Sync in Transmit or Receive Mode)[3]		3.5	ns
t_{HOFSI}	Frame Sync Hold After SPTx_CLK (Internally Generated Frame Sync in Transmit or Receive Mode)[3]	–3		ns
t_{DDTI}	Transmit Data Delay After SPTx_CLK[3]		3.5	ns
t_{HDTI}	Transmit Data Hold After SPTx_CLK[3]	–3		ns
$t_{SPTCLKIW}$	SPTx_CLK Width[4]	$0.5 \times t_{SPTCLKPROG} - 2$		ns
$t_{SPTCLKWI}$	SPTx_CLK Period[4]	$t_{SPTCLKPROG} - 1.5$		ns

[1] Specifications apply to all four SPORTs.
[2] Referenced to the sample edge.
[3] Referenced to drive edge.
[4] See Table 14 for details on the minimum period that can be programmed for $f_{SPTCLKPROG}$.

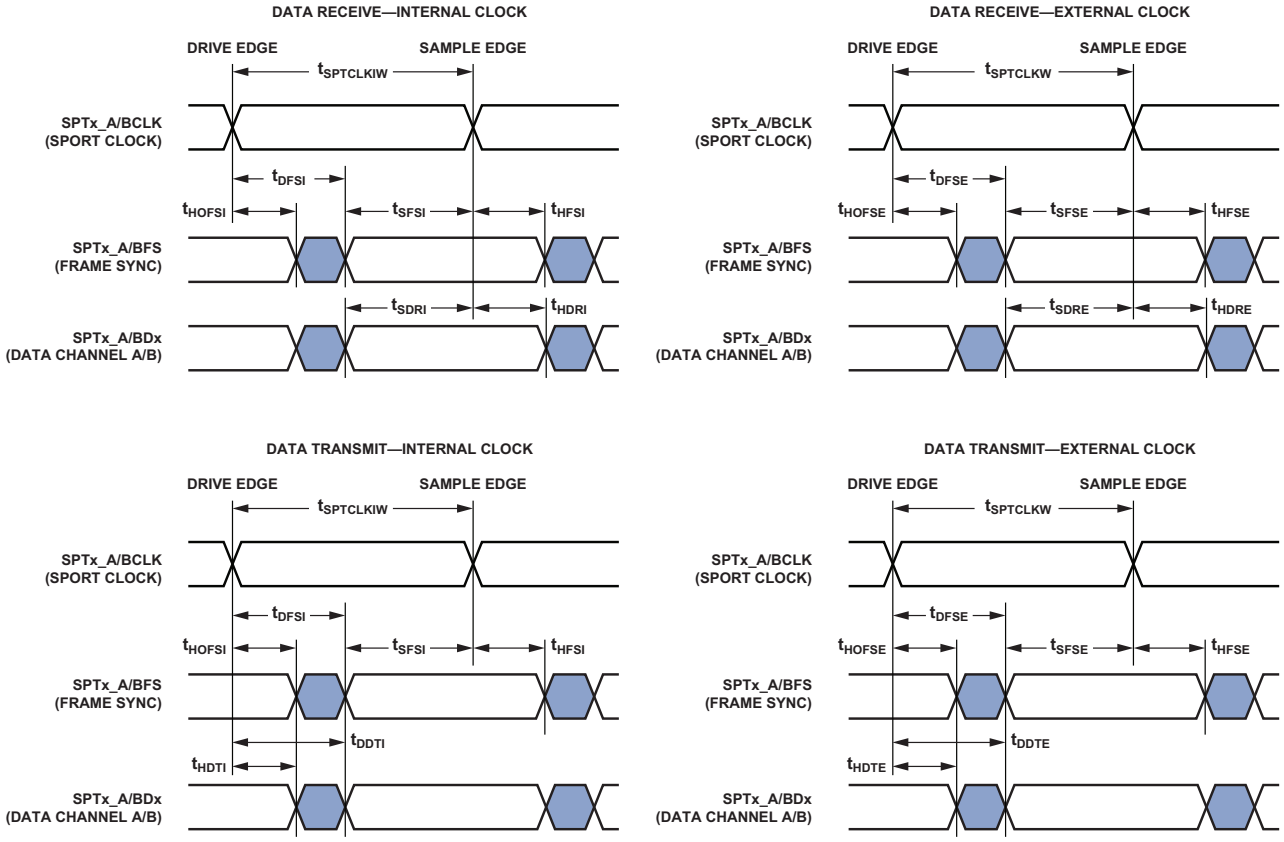


Figure 9. SPORTs

Table 26. SPORTs—Enable and Three-State[1]

All specifications are subject to change without notice.				
Parameter		**Min**	**Max**	**Unit**
Switching Characteristics				
t_{DDTEN}	Data Enable From External Transmit SPTx_CLK[2]	1		ns
t_{DDTTE}	Data Disable From External Transmit SPTx_CLK[2]		14	ns
t_{DDTIN}	Data Enable From Internal Transmit SPTx_CLK[2]	–2.5		ns
t_{DDTTI}	Data Disable From Internal Transmit SPTx_CLK[2]		2.8	ns

[1] Specifications apply to all four SPORTs.
[2] Referenced to drive edge.

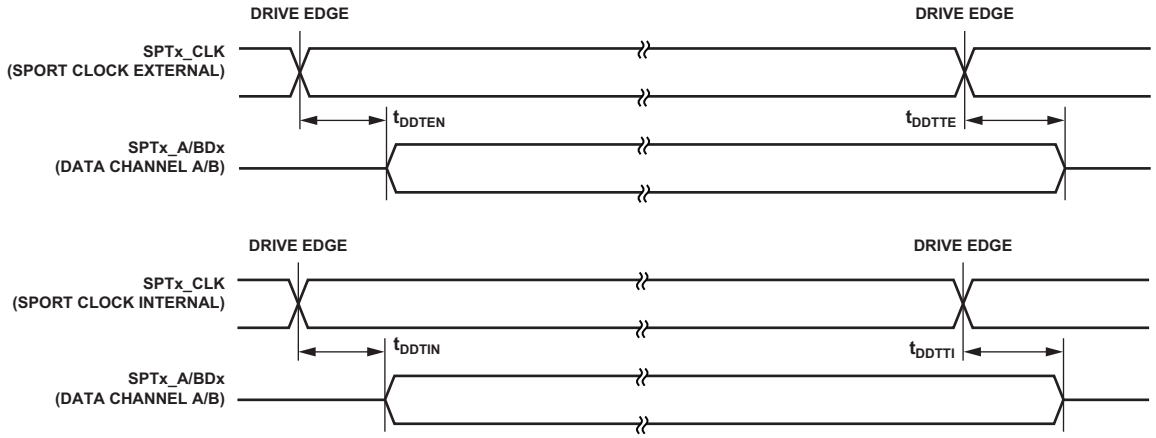


Figure 10. SPORTs—Enable and Three-State

The SPTx_TDV output signal becomes active in SPORT multichannel mode. During transmit slots (enabled with active channel selection registers) the SPTx_TDV is asserted for communication with external devices.

Table 27. SPORTs—Transmit Data Valid (TDV)[1]

All specifications are subject to change without notice.				
Parameter		**Min**	**Max**	**Unit**
Switching Characteristics				
t_{DRDVEN}	Data Valid Enable Delay From Drive Edge of External Clock[2]	2		ns
t_{DFDVEN}	Data Valid Disable Delay From Drive Edge of External Clock[2]		14	ns
t_{DRDVIN}	Data Valid Enable Delay From Drive Edge of Internal Clock[2]	–2.5		ns
t_{DFDVIN}	Data Valid Disable Delay From Drive Edge of Internal Clock[2]		3.5	ns

[1] Specifications apply to all four SPORTs.
[2] Referenced to drive edge.

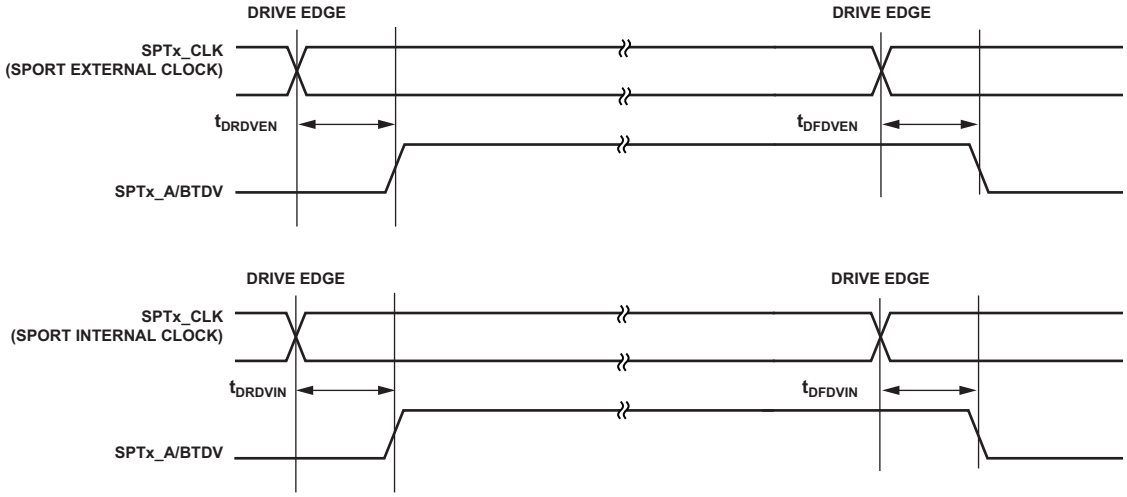


Figure 11. SPORTs—Transmit Data Valid Internal and External Clock

Table 28. SPORTs—External Late Frame Sync[1]

All specifications are subject to change without notice.				
Parameter		**Min**	**Max**	**Unit**
Switching Characteristics				
$t_{DDTLFSE}$	Data Delay From Late External Transmit Frame Sync or External Receive Frame Sync with SPORT_MCTL_A/B bits MCE = 1, MFD = 0[2]		14	ns
$t_{DDTENFS}$	Data Enable for SPORT_MCTL_A/B bits MCE = 1, MFD = 0[2]	0.5		ns

[1] Specifications apply to all four SPORTs.
[2] The $t_{DDTLFSE}$ and $t_{DDTENFS}$ parameters apply to left justified as well as standard serial mode and MCE = 1, MFD = 0.

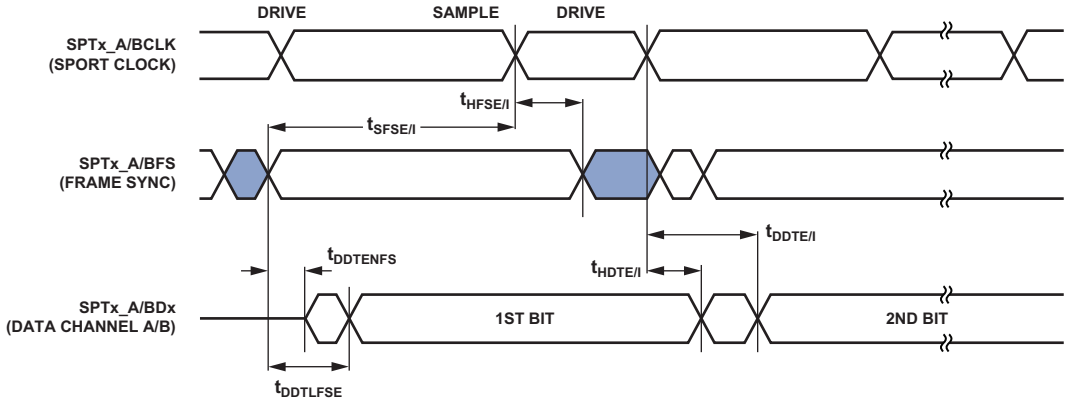


Figure 12. External Late Frame Sync

Asynchronous Sample Rate Converter (ASRC)—Serial Input Port

The ASRC input signals are routed from the DAI0_PINx pins using the SRU. Therefore, the timing specifications provided in Table 29 are valid at the DAI0_PINx pins.

Table 29. ASRC, Serial Input Port

All specifications are subject to change without notice.				
Parameter		**Min**	**Max**	**Unit**
Timing Requirements				
t_{SRCSFS}[1]	Frame Sync Setup Before Serial Clock Rising Edge	4		ns
t_{SRCHFS}[1]	Frame Sync Hold After Serial Clock Rising Edge	5.5		ns
t_{SRCSD}[1]	Data Setup Before Serial Clock Rising Edge	4		ns
t_{SRCHD}[1]	Data Hold After Serial Clock Rising Edge	5.5		ns
$t_{SRCCLKW}$	Clock Width	$t_{SCLK0} - 1$		ns
t_{SRCCLK}	Clock Period	$2 \times t_{SCLK0}$		ns

[1] The serial clock, data, and frame sync signals can originate from any of the DAI pins. The serial clock and frame sync signals can also originate via PCG or SPORTs. The input of the PCG can be either CLKIN or any of the DAI pins.

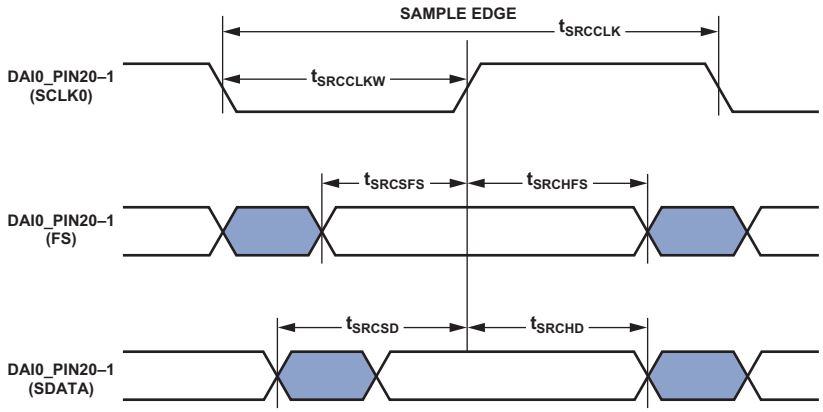


Figure 13. ASRC Serial Input Port Timing

Asynchronous Sample Rate Converter (ASRC)—Serial Output Port

For the serial output port, the frame sync is an input and it must meet setup and hold times with regard to SCLK0 on the output port. The serial data output has a hold time and delay specification with regard to the serial clock. The serial clock rising edge is the sampling edge, and the falling edge is the drive edge.

Table 30. ASRC, Serial Output Port

All specifications are subject to change without notice.				
Parameter		**Min**	**Max**	**Unit**
Timing Requirements				
t_{SRCSFS}[1]	Frame Sync Setup Before Serial Clock Rising Edge	4		ns
t_{SRCHFS}[1]	Frame Sync Hold After Serial Clock Rising Edge	5.5		ns
$t_{SRCCLKW}$	Clock Width	$t_{SCLK0} - 1$		ns
t_{SRCCLK}	Clock Period	$2 \times t_{SCLK0}$		ns
Switching Characteristics				
t_{SRCTDD}[1]	Transmit Data Delay After Serial Clock Falling Edge		13	ns
t_{SRCTDH}[1]	Transmit Data Hold After Serial Clock Falling Edge	1		ns

[1] The serial clock, data, and frame sync signals can originate from any of the DAI pins. The serial clock and frame sync signals can also originate via PCG or SPORTs. The input of the PCG can be either CLKIN, SCLK0, or any of the DAI pins.

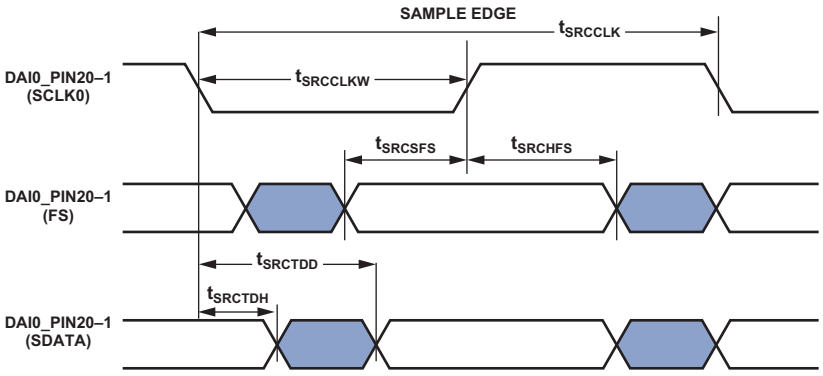


Figure 14. ASRC Serial Output Port Timing

SPI Port—Master Timing

SPI0, SPI1, and SPI2

Table 31 and Figure 15 describe the SPI port master operations.

When internally generated, the programmed SPI clock ($f_{SPICLKPROG}$) frequency in megahertz is set by the following equation:

$$f_{SPICLKPROG} = \frac{f_{CDU\_CLKO6}}{(BAUD + 1)}$$

$$t_{SPICLKPROG} = \frac{1}{f_{SPICLKPROG}}$$

where *BAUD* is a field in the SPIx_CLK register that can be set from 0 to 65,535.

Note that

- In dual-mode data transmit, the SPIx_MISO signal is also an output.
- In quad-mode data transmit, the SPIx_MISO, SPIx_D2, and SPIx_D3 signals are also outputs.
- In dual-mode data receive, the SPIx_MOSI signal is also an input.
- In quad-mode data receive, the SPIx_MOSI, SPIx_D2, and SPIx_D3 signals are also inputs.
- Quad mode is supported by SPI1 and SPI2.
- CPHA is a configuration bit in the SPI_CTL register.

Table 31. SPI Port—Master Timing[1]

All specifications are subject to change without notice.				
Parameter		**Min**	**Max**	**Unit**
Timing Requirements				
t_{SSPIDM}	Data Input Valid to SPIx_CLK Edge (Data Input Setup)	3.5		ns
t_{HSPIDM}	SPIx_CLK Sampling Edge to Data Input Invalid	2		ns
Switching Characteristics				
t_{SDSCIM}	$\overline{\text{SPIx\_SEL}}$ Low to First SPI_CLK Edge for CPHA = 1[2]	$t_{SPICLKPROG}$ – 5		ns
	$\overline{\text{SPIx\_SEL}}$ Low to First SPI_CLK Edge for CPHA = 0[2]	1.5 × $t_{SPICLKPROG}$ – 5		ns
t_{SPICHM}	SPIx_CLK High Period[3]	0.5 × $t_{SPICLKPROG}$ – 1.5		ns
t_{SPICLM}	SPIx_CLK Low Period[3]	0.5 × $t_{SPICLKPROG}$ – 1.5		ns
t_{SPICLK}	SPIx_CLK Period[3]	$t_{SPICLKPROG}$ – 1.5		ns
t_{HDSM}	Last SPIx_CLK Edge to $\overline{\text{SPIx\_SEL}}$ High for CPHA = 1[2]	1.5 × $t_{SPICLKPROG}$ – 5		ns
	Last SPIx_CLK Edge to $\overline{\text{SPIx\_SEL}}$ High for CPHA = 0[2]	$t_{SPICLKPROG}$ – 5		ns
t_{SPITDM}	Sequential Transfer Delay[2, 4]	$t_{SPICLKPROG}$ – 1.5		ns
$t_{DDSPIDM}$	SPIx_CLK Edge to Data Out Valid (Data Out Delay)		2.7	ns
$t_{HDSPIDM}$	SPIx_CLK Edge to Data Out Invalid (Data Out Hold)	–3.75		ns

[1] All specifications apply to SPI0, SPI1, and SPI2.
[2] Specification assumes the LEADX and LAGX bits in the SPI_DLY register are 1.
[3] See Table 14 for details on the minimum period that can be programmed for $t_{SPICLKPROG}$.
[4] Applies to sequential mode with STOP ≥ 1.

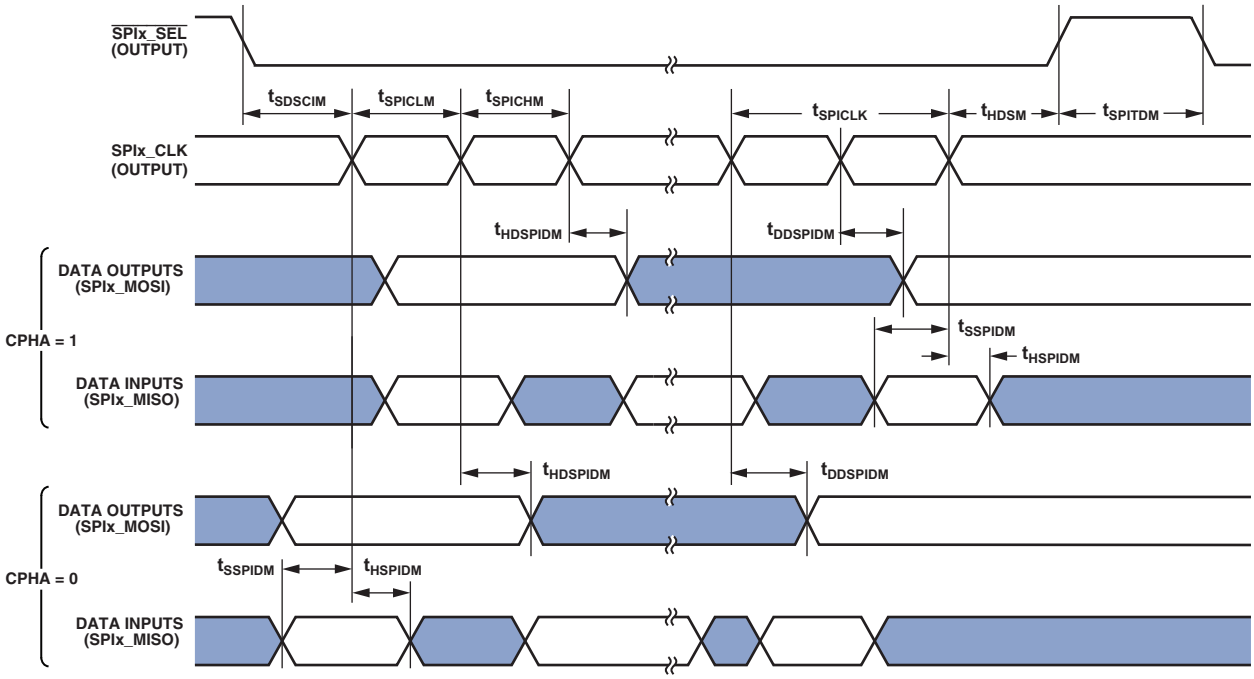


Figure 15. SPI Port—Master Timing

SPI Port—Slave Timing

SPI0, SPI1, and SPI2

Table 32 and Figure 16 describe SPI port slave operations. Note that

- In dual-mode data transmit, the SPIx_MOSI signal is also an output.
- In quad-mode data transmit, the SPIx_MOSI, SPIx_D2, and SPIx_D3 signals are also outputs.
- In dual-mode data receive, the SPIx_MISO signal is also an input.
- In quad-mode data receive, the SPIx_MISO, SPIx_D2, and SPIx_D3 signals are also inputs.
- In SPI slave mode, the SPI clock is supplied externally and is called $f_{SPICLKEXT}$:

$$t_{SPICLKEXT} = \frac{1}{f_{SPICLKEXT}}$$

- Quad mode is supported by SPI1 and SPI2.
- CPHA is a configuration bit in the SPI_CTL register.

Table 32. SPI Port—Slave Timing[1]

All specifications are subject to change without notice.				
Parameter		**Min**	**Max**	**Unit**
Timing Requirements				
t_{SPICHS}	SPIx_CLK High Period[2]	0.5 × $t_{SPICLKEXT}$ – 1.5		ns
t_{SPICLS}	SPIx_CLK Low Period[2]	0.5 × $t_{SPICLKEXT}$ – 1.5		ns
t_{SPICLK}	SPIx_CLK Period[2]	$t_{SPICLKEXT}$ – 1.5		ns
t_{HDS}	Last SPIx_CLK Edge to $\overline{\text{SPIx\_SS}}$ Not Asserted	5		ns
t_{SPITDS}	Sequential Transfer Delay	$t_{SPICLKEXT}$ – 1.5		ns
t_{SDSCI}	$\overline{\text{SPIx\_SS}}$ Assertion to First SPIx_CLK Edge	11.7		ns
t_{SSPID}	Data Input Valid to SPIx_CLK Edge (Data Input Setup)	2		ns
t_{HSPID}	SPIx_CLK Sampling Edge to Data Input Invalid	1.6		ns
Switching Characteristics				
t_{DSOE}	$\overline{\text{SPIx\_SS}}$ Assertion to Data Out Active	0	14.12	ns
t_{DSDHI}	$\overline{\text{SPIx\_SS}}$ Deassertion to Data High Impedance	0	12.6	ns
t_{DDSPID}	SPIx_CLK Edge to Data Out Valid (Data Out Delay)		14.16	ns
t_{HDSPID}	SPIx_CLK Edge to Data Out Invalid (Data Out Hold)	1.5		ns

[1] All specifications apply to SPI0, SPI1, and SPI2.
[2] This specification indicates the minimum instantaneous width or period that can be tolerated due to duty cycle variation or jitter on the external SPIx_CLK. For the external SPIx_CLK ideal maximum frequency, see the $f_{SPICLKTEXT}$ specification in Table 14.

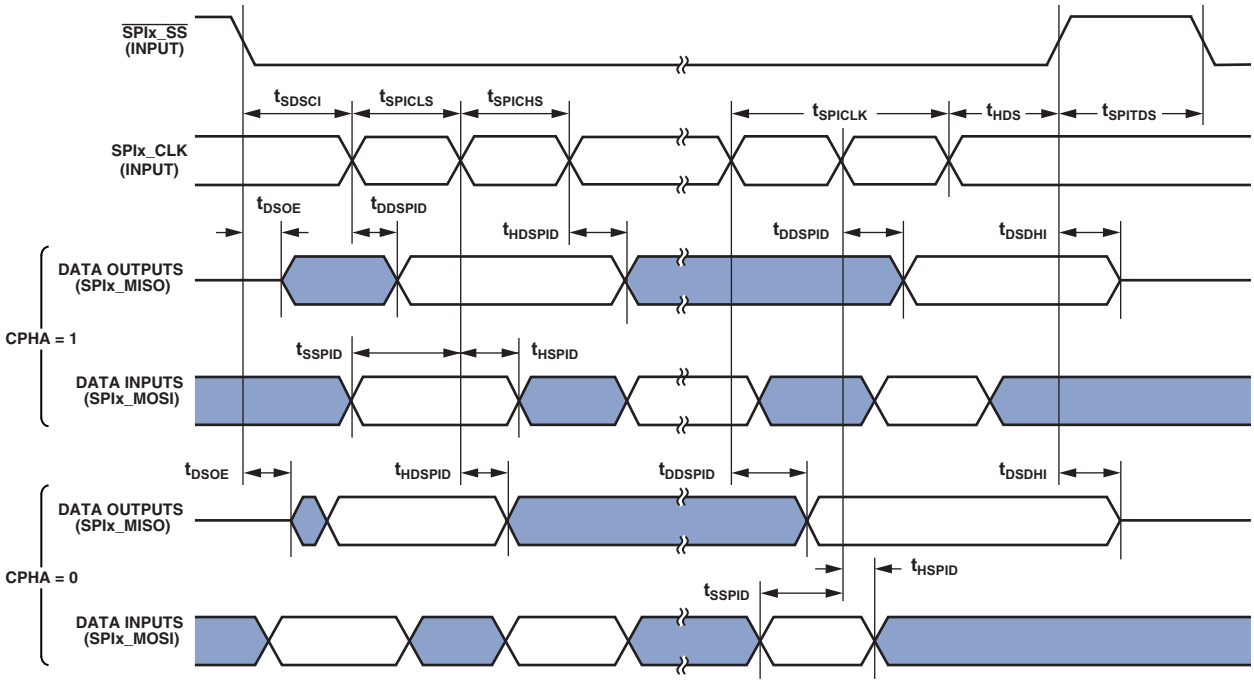


Figure 16. SPI Port—Slave Timing

SPI Port—SPIx_RDY Slave Timing

SPIx_RDY provides flow control. CPOL, CPHA, and FCCH are configuration bits in the SPIx_CTL register.

Table 33. SPI Port—SPIx_RDY Slave Timing[1]

All specifications are subject to change without notice.				
Parameter	**Conditions**	**Min**	**Max**	**Unit**
Switching Characteristic				
$t_{DSPISCKRDYS}$ SPIx_RDY Deassertion From Last Valid Input SPIx_CLK Edge	FCCH = 0	$3 \times t_{CDU\_CLKO0}$	$4 \times t_{CDU\_CLKO0} + 10$	ns
	FCCH = 1	$4 \times t_{CDU\_CLKO0}$	$5 \times t_{CDU\_CLKO0} + 10$	ns

[1] All specifications apply to all three SPIs.

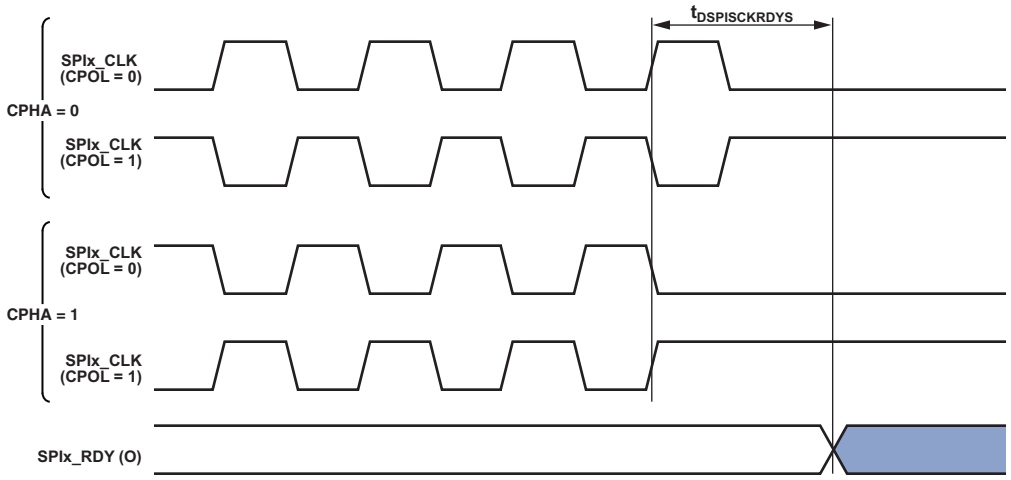


Figure 17. SPIx_RDY Deassertion from Valid Input SPIx_CLK Edge in Slave Mode

SPI Port—Open Drain Mode (ODM) Timing

In Figure 18 and Figure 19, the outputs can be SPIx_MOSI, SPIx_MISO, SPIx_D2, and/or SPIx_D3, depending on the mode of operation. CPOL and CPHA are configuration bits in the SPI_CTL register.

Table 34. SPI Port—ODM Master Mode Timing[1]

All specifications are subject to change without notice.				
Parameter		**Min**	**Max**	**Unit**
Switching Characteristics				
$t_{HDSPIODMM}$	SPIx_CLK Edge to High Impedance From Data Out Valid	–1.5		ns
$t_{DDSPIODMM}$	SPIx_CLK Edge to Data Out Valid From High Impedance		6	ns

[1] All specifications apply to all three SPIs.

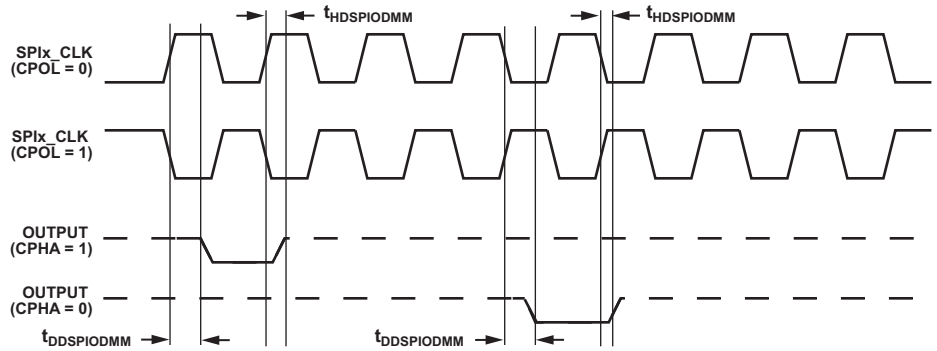


Figure 18. ODM Master Mode

Table 35. SPI Port—ODM Slave Mode[1]

All specifications subject to change without notice.				
Parameter		**Min**	**Max**	**Unit**
Timing Requirements				
$t_{HDSPIODMS}$	SPIx_CLK Edge to High Impedance From Data Out Valid	0		ns
$t_{DDSPIODMS}$	SPIx_CLK Edge to Data Out Valid From High Impedance		11	ns

[1] All specifications apply to all three SPIs.

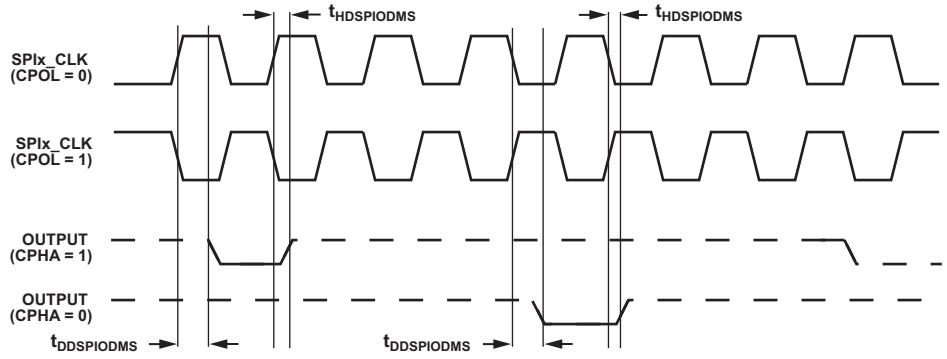


Figure 19. ODM Slave Mode

SPI Port—SPIx_RDY Master Timing

SPIx_RDY is used to provide flow control. CPOL and CPHA are configuration bits in the SPIx_CTL register, whereas LEADX, LAGX, and STOP are configuration bits in the SPIx_DLY register.

Table 36. SPI Port—SPIx_RDY Master Timing[1]

All specifications are subject to change without notice.					
Parameter		**Conditions**	**Min**	**Max**	**Unit**
Timing Requirement					
$t_{SRDYSCKM}$	Setup Time for SPIx_RDY Deassertion Before Last Valid Data SPIx_CLK Edge		$(2+2\times BAUD^{2})\times t_{CDU\_CLKO0}+11$		ns
Switching Characteristic					
$t_{DRDYSCKM}$[3]	Assertion of SPIx_RDY to First SPIx_CLK Edge of Next Transfer	BAUD = 0, CPHA = 0	$4.5\times t_{CDU\_CLKO0}$	$5.5\times t_{CDU\_CLKO0}+11$	ns
		BAUD = 0, CPHA = 1	$4\times t_{CDU\_CLKO0}$	$5\times t_{CDU\_CLKO0}+11$	ns
		BAUD > 0, CPHA = 0	$(1+1.5\times BAUD^{2})\times t_{CDU\_CLKO0}$	$(2+2.5\times BAUD^{2})\times t_{CDU\_CLKO0}+11$	ns
		BAUD > 0, CPHA = 1	$(1+1\times BAUD^{2})\times t_{CDU\_CLKO0}$	$(2+2\times BAUD^{2})\times t_{CDU\_CLKO0}+11$	ns

[1] All specifications apply to all three SPIs.
[2] BAUD value is set using the SPIx_CLK.BAUD bits. BAUD value = SPIx_CLK.BAUD bits + 1.
[3] Specification assumes the LEADX, LAGX, and STOP bits in the SPI_DLY register are zero.

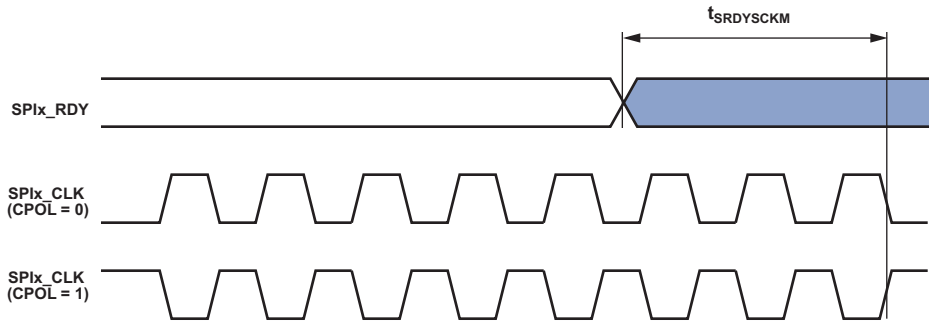


Figure 20. SPIx_RDY Setup Before SPIx_CLK

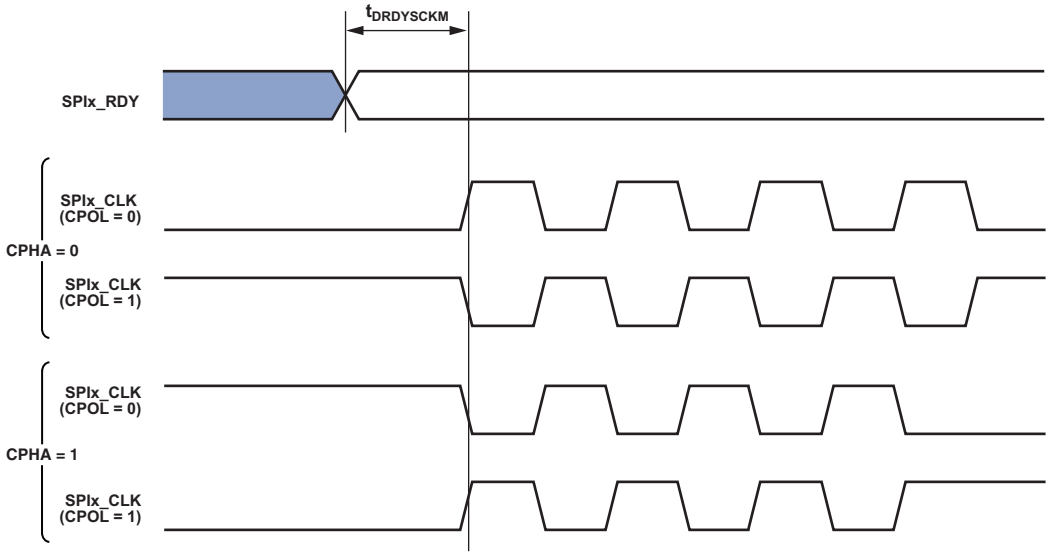


Figure 21. SPIx_CLK Switching Diagram after SPIx_RDY Assertion

xSPI Port—Master Timing

xSPI

Table 37 and Figure 22 describe the xSPI port master operations. Slave mode is not supported for xSPI.

When internally generated, the programmed xSPI clock ($f_{xSPICLKPROG}$) frequency in megahertz is set by the following equations:

$$f_{SYSCLK} = f_{CDU\_CLKO10}$$

$$f_{xSPICLKPROG} = \frac{f_{SYSCLK}}{PRG\_MBD}$$

$$t_{xSPICLKPROG} = \frac{1}{f_{xSPICLKPROG}}$$

where *PRG_MBD* is the master mode baud rate divisor.

Note that

- In dual-mode data transmit, the xSPI_MISO signal is also an output.
- In quad-mode data transmit, the xSPI_MISO, xSPI_D2, and xSPI_D3 signals are also outputs.
- In octal-mode data transmit, the xSPI_MISO, xSPI_D2, xSPI_D3, xSPI_D4, xSPI_D5, xSPI_D6, and xSPI_D7 signals are also outputs.
- In dual-mode data receive, the xSPI_MOSI signal is also an input.
- In quad-mode data receive, the xSPI_MOSI, xSPI_D2, and xSPI_D3 signals are also inputs.
- In octal-mode data receive, the xSPI_MISO, xSPI_D2, xSPI_D3, xSPI_D4, xSPI_D5, xSPI_D6, and xSPI_D7 signals are also outputs.

Table 37. xSPI Port—Master Timing[1]

All specifications are subject to change without notice.				
Parameter		**Min**	**Max**	**Unit**
Timing Requirements				
t_{SSPIDM}	Data Input Valid to xSPI_CLK (Data Input Setup) Sampling Edge (DQS)[2]	–1.1		ns
t_{HSPIDM}	xSPI_CLK Sampling Edge (Data Input Hold) to Data Input Invalid (DQS)[2]	3.1		ns
t_{SSPIDM}	Data Input Valid to xSPI_CLK (Data Input Setup) Sampling Edge (PHY CLK)[3]	–3.8		ns
t_{HSPIDM}	xSPI_CLK Sampling Edge (Data Input Hold) to Data Input Invalid (PHY CLK)[3]	7		ns
Switching Characteristics[4]				
t_{SDSCIM}	$\overline{\text{xSPI\_SEL}}$ Low to First xSPI_CLK Edge[5, 6]	PRG_CSSOT × $t_{xSPICLKPROG}$ – 2		ns
t_{SPICHM}	xSPI_CLK High Period[6]	0.45 × $t_{xSPICLKPROG}$		ns
t_{SPICLM}	xSPI_CLK Low Period[6]	0.45 × $t_{xSPICLKPROG}$		ns
t_{SPICLK}	xSPI_CLK Period[6]	$t_{xSPICLKPROG}$ – 0.8		ns
t_{HDSM}	Last xSPI_CLK Edge to $\overline{\text{xSPI\_SEL}}$ High for Mode = 0[6, 7, 8]	PRG_CSEOT × $t_{xSPICLKPROG}$ – 5		ns

Table 37. xSPI Port—Master Timing[1] (Continued)

All specifications are subject to change without notice.			
Parameter	**Min**	**Max**	**Unit**
$t_{DDSPIDM}$ xSPI_CLK Edge to Data Out Valid to Driving Edge (Data Out Delay)		3	ns
$t_{HDSPIDM}$ xSPI_CLK Edge to Data Out Invalid to Driving Edge (Data Out Hold)	1		ns

[1] All specifications apply to xSPI only.
[2] t_{SSPIDM} and t_{HSPIDM} specifications are characterized in DQS mode at 166.66 MHz for TX_RX_DLL = 0x00002C2B, RD_DEL_SEL_9, and DQS is sampling.
[3] t_{SSPIDM} and t_{HSPIDM} specifications are characterized in LOOPBACK mode at 125 MHz for TX_RX_DLL = 0x00002C5F, RD_DEL_SEL_5, and PHY CLK is sampling.
[4] All switching parameters are characterized at 166.66 MHz for TX_RX_DLL = 0x00002335, RD_DEL_SEL_5 and at 125 MHz for TX_RX_DLL = 0x00003035, RD_DEL_SEL_5.
[5] PRG_CSSOT = chip select start of transfer (defined in xSPI_DLY[7:0]).
[6] See Table 14 for details on the minimum period that can be programmed for $t_{xSPICLKPROG}$.
[7] PRG_CSEOT = chip select end of transfer (defined in xSPI_DLY[15:8]).
[8] Mode = SPI Clock Mode Select (defined in xSPI_CTL[0]).

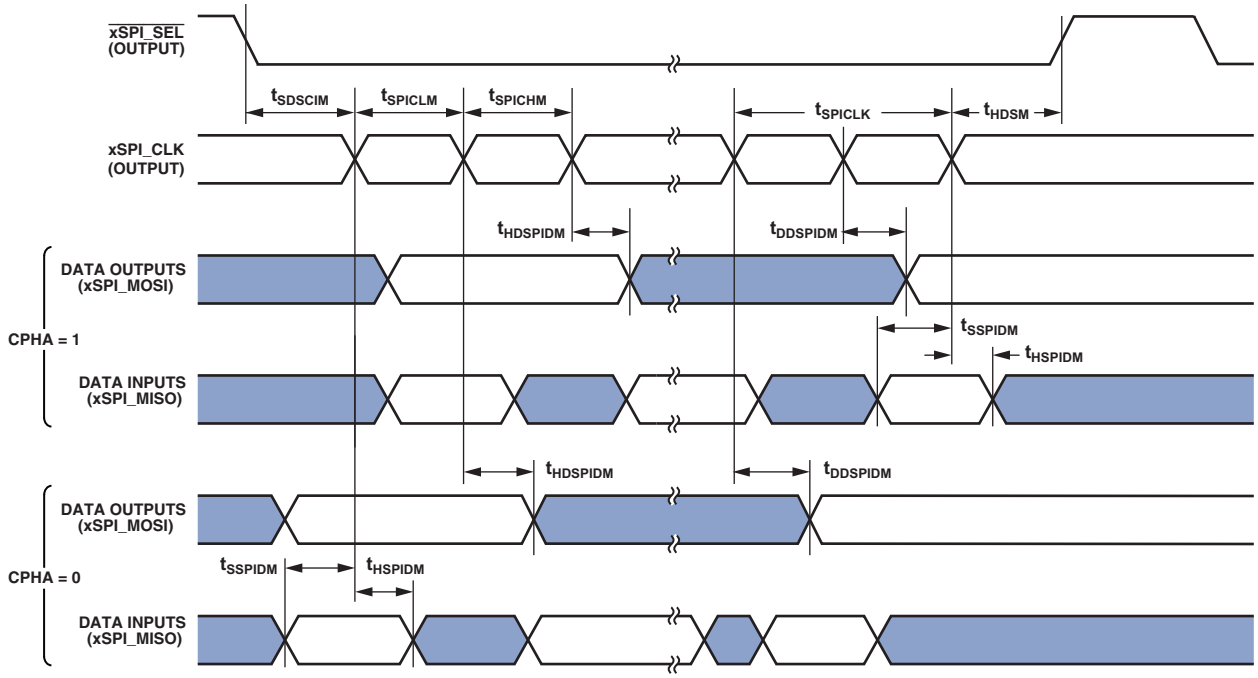


Figure 22. xSPI Port—Master Timing

xSPI With Data Training

I/O timing requirements and switching characteristics are not applicable when xSPI is used with data training. See xSPI PHY Configuration and Training (EE-TBD) for additional information.

When xSPI is used with data training, the programmed xSPI clock ($f_{xSPICLKPROG}$) frequency in megahertz (MHz) is set by the following equation:

$$f_{xSPICLKPROG} = f_{CDU\_CLKO10}$$

Precision Clock Generator (PCG) (Direct Pin Routing)

This timing is only valid when the SRU is configured such that the precision clock generator (PCG) takes inputs directly from the DAI pins (via pin buffers) and sends outputs directly to the DAI pins. For the other cases, where the PCG inputs and outputs are not directly routed to/from DAI pins (via pin buffers), there is no timing data available. All timing parameters and switching characteristics apply to external DAI pins (DAI0_PINx).

Table 38. PCG (Direct Pin Routing)

All specifications are subject to change without notice.				
Parameter		**Min**	**Max**	**Unit**
Timing Requirements				
t_{PCGIP}	Input Clock Period	$t_{SCLK0} \times 2$		ns
t_{STRIG}	PCG Trigger Setup Before Falling Edge of PCG Input Clock	4.5		ns
t_{HTRIG}	PCG Trigger Hold After Falling Edge of PCG Input Clock	3		ns
Switching Characteristics				
t_{DPCGIO}	PCG Output Clock and Frame Sync Active Edge Delay After PCG Input Clock	2	10	ns
$t_{DTRIGCLK}$	PCG Output Clock Delay After PCG Trigger	$2 + (2.5 \times t_{PCGIP})$	$13.5 + (2.5 \times t_{PCGIP})$	ns
$t_{DTRIGFS}$[1]	PCG Frame Sync Delay After PCG Trigger	$2.5 + ((2.5 + D - PH) \times t_{PCGIP})$	$13.5 + ((2.5 + D - PH) \times t_{PCGIP})$	ns
t_{PCGOW}[2]	Output Clock Period	$2 \times t_{PCGIP} - 1$		ns

[1] D = FSxDIV, PH = FSxPHASE. For more information, see the ADSP-21560/21561/21564/21568 SHARC+ Processor Hardware Reference.
[2] Normal mode of operation.

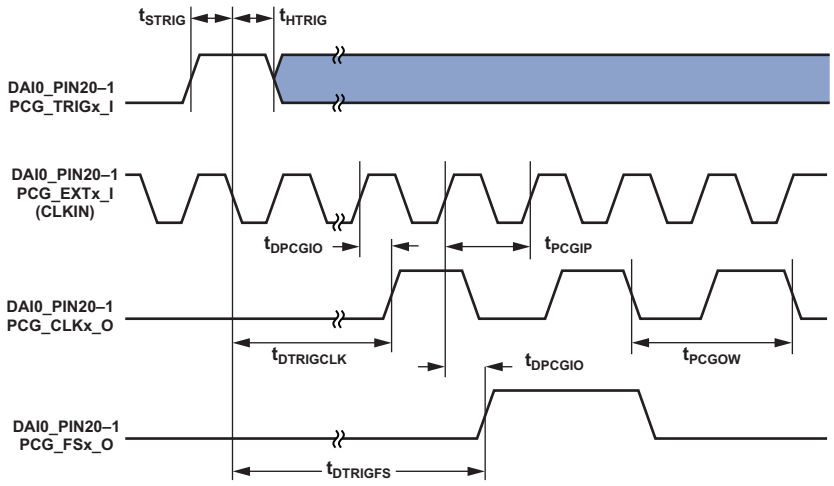


Figure 23. PCG (Direct Pin Routing)

General-Purpose IO Port Timing

Table 39 and Figure 24 describe I/O timing, related to the general-purpose ports (PORT).

Table 39. General-Purpose Port Timing

All specifications are subject to change without notice.				
Parameter		**Min**	**Max**	**Unit**
Timing Requirement				
t_{WFI}	General-Purpose Port Pin Input Pulse Width	$2 \times t_{SCLK0} - 1.5$		ns

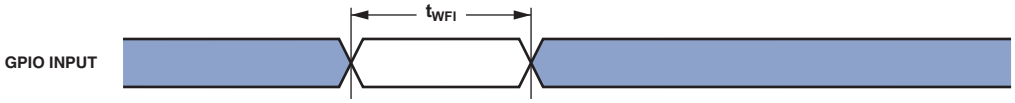


Figure 24. General-Purpose Port Timing

General-Purpose I/O Timer Cycle Timing

Table 40, Table 41, and Figure 25 describe timer expired operations related to the general-purpose timer (TIMER0). The width value is the timer period assigned in the TMx_TMRn_WIDTH register and can range from 1 to $2^{32} - 1$. When externally generated, the TMx_CLK clock is called $f_{TMRCLKEXT}$:

$$t_{TMRCLKEXT} = \frac{1}{f_{TMRCLKEXT}}$$

Table 40. Timer Cycle Timing—Internal Mode

All specifications are subject to change without notice.				
Parameter		**Min**	**Max**	**Unit**
Timing Requirements				
t_{WL}	Timer Pulse Width Input Low (Measured In SCLK0 Cycles)[1]	$2 \times t_{SCLK0}$		ns
t_{WH}	Timer Pulse Width Input High (Measured In SCLK0 Cycles)[1]	$2 \times t_{SCLK0}$		ns
Switching Characteristic				
t_{HTO}	Timer Pulse Width Output (Measured In SCLK0 Cycles)[2]	$t_{SCLK0} \times$ WIDTH – 1.7	$t_{SCLK0} \times$ WIDTH + 1.5	ns

[1] The minimum pulse width applies for timer signals in width capture and external clock modes.
[2] WIDTH refers to the value in the TMRx_WIDTH register (it can vary from 2 to $2^{32} - 1$).

Table 41. Timer Cycle Timing—External Mode

All specifications are subject to change without notice.				
Parameter		**Min**	**Max**	**Unit**
Timing Requirements				
t_{WL}	Timer Pulse Width Input Low (Measured In EXT_CLK Cycles)[1]	$2 \times t_{EXT\_CLK}$		ns
t_{WH}	Timer Pulse Width Input High (Measured In EXT_CLK Cycles)[1]	$2 \times t_{EXT\_CLK}$		ns
t_{EXT_CLK}	Timer External Clock Period[2]	$t_{TMRCLKEXT}$		ns
Switching Characteristic				
t_{HTO}	Timer Pulse Width Output (Measured In EXT_CLK Cycles)[3]	$t_{EXT\_CLK} \times$ WIDTH – 1.5	$t_{EXT\_CLK} \times$ WIDTH + 1.5	ns

[1] The minimum pulse width applies for timer signals in width capture and external clock modes.
[2] This specification indicates the minimum instantaneous width or period that can be tolerated due to duty cycle variation or jitter on the external TMR_CLK. For the external TMR_CLK maximum frequency, see the $f_{TMRCLKEXT}$ specification in Table 14.
[3] WIDTH refers to the value in the TMRx_WIDTH register (it can vary from 1 to $2^{32} - 1$).

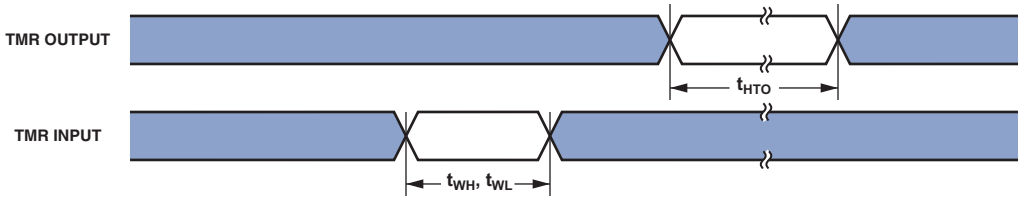


Figure 25. Timer Cycle Timing

DAIx Pin to DAIx Pin Direct Routing (DAI0 Block and DAI1 Block)

Table 42 and Figure 26 describe I/O timing related to the digital audio interface (DAI) for direct pin connections only (for example, DAIx_PB01_I to DAIx_PB02_O).

Table 42. DAI Pin to DAI Pin Routing

All specifications are subject to change without notice.				
Parameter		**Min**	**Max**	**Unit**
Switching Characteristic				
t_{DPIO}	Delay DAI Pin Input Valid to DAI Output Valid	1.5	12	ns

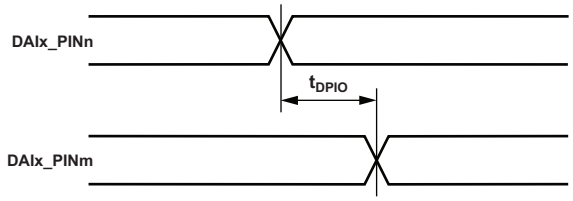


Figure 26. DAI Pin to DAI Pin Direct Routing

Up/Down Counter/Rotary Encoder Timing

Table 43 and Figure 27 describe timing related to the general-purpose counter (CNT).

Table 43. Up/Down Counter/Rotary Encoder Timing

All specifications are subject to change without notice.				
Parameter		**Min**	**Max**	**Unit**
Timing Requirement				
t_{WCOUNT}	Up/Down Counter/Rotary Encoder Input Pulse Width	$2 \times t_{SCLK0}$		ns

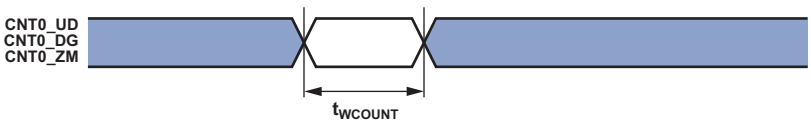


Figure 27. Up/Down Counter/Rotary Encoder Timing

Universal Asynchronous Receiver-Transmitter (UART) Ports—Receive and Transmit Timing

The UART ports receive and transmit operations are described in the ADSP-21560/21561/21564/21568 SHARC+ Processor Hardware Reference manual.

Sony/Philips Digital Interface (S/PDIF) Transmitter

Serial data input to the S/PDIF transmitter can be formatted as left justified, I^2S, or right justified with word widths of 16, 18, 20, or 24 bits. The following sections provide timing for the transmitter.

S/PDIF Transmitter Serial Input Waveforms

Table 44 and Figure 28 show the right justified mode. Frame sync is high for the left channel and low for the right channel. Data is valid on the rising edge of the serial clock. The MSB is delayed the minimum in 24-bit output mode or the maximum in 16-bit output mode from a frame sync transition, so that when there are 64 serial clock periods per frame sync period, the LSB of the data is right justified to the next frame sync transition.

Table 44. S/PDIF Transmitter Right Justified Mode

All specifications are subject to change without notice.			
Parameter	**Conditions**	**Nominal**	**Unit**
Timing Requirement			
t_{RJD} Frame Sync to MSB Delay in Right Justified Mode	16-bit word mode	16	SCLK0
	18-bit word mode	14	SCLK0
	20-bit word mode	12	SCLK0
	24-bit word mode	8	SCLK0

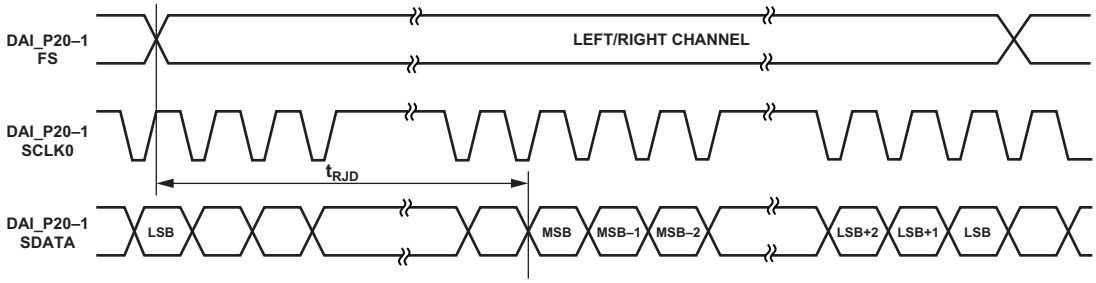


Figure 28. Right Justified Mode

Table 45 and Figure 29 show the default I²S justified mode. The frame sync is low for the left channel and high for the right channel. Data is valid on the rising edge of the serial clock. The MSB is left justified to the frame sync transition but with a delay.

Table 45. S/PDIF Transmitter I²S Mode

All specifications are subject to change without notice.			
Parameter		**Nominal**	**Unit**
Timing Requirement			
t_{I2SD}	Frame Sync to MSB Delay in I²S Mode	1	SCLK0

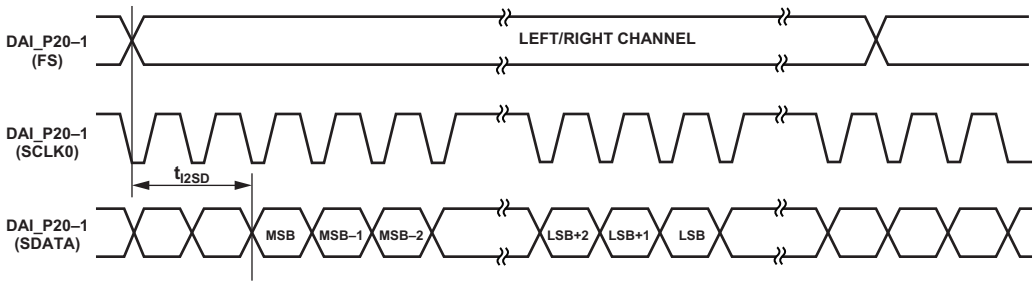


Figure 29. I²S Justified Mode

Table 46 and Figure 30 show the left justified mode. The frame sync is high for the left channel and low for the right channel. Data is valid on the rising edge of the serial clock. The MSB is left justified to the frame sync transition with no delay.

Table 46. S/PDIF Transmitter Left Justified Mode

All specifications are subject to change without notice.			
Parameter		**Nominal**	**Unit**
Timing Requirement			
t_{LJD}	Frame Sync to MSB Delay in Left Justified Mode	0	SCLK0

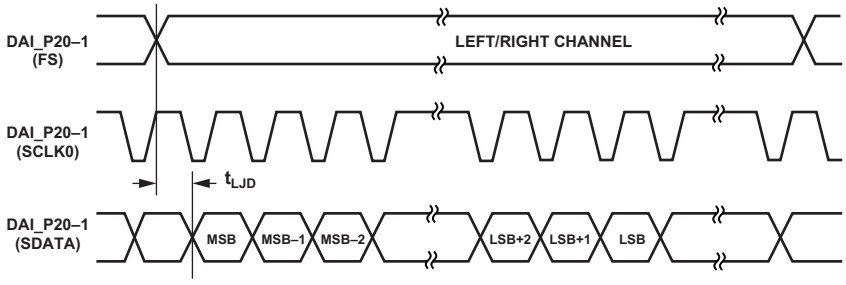


Figure 30. Left Justified Mode

S/PDIF Transmitter Input Data Timing

The timing requirements for the S/PDIF transmitter are given in Table 47. Input signals are routed to the DAI0_PINx pins using the SRU. Therefore, the timing specifications provided below are valid at the DAI0_PINx pins.

Table 47. S/PDIF Transmitter Input Data Timing

All specifications are subject to change without notice.				
Parameter		**Min**	**Max**	**Unit**
Timing Requirements				
t_{SISFS}[1]	Frame Sync Setup Before Serial Clock Rising Edge	3.4		ns
t_{SIHFS}[1]	Frame Sync Hold After Serial Clock Rising Edge	3		ns
t_{SISD}[1]	Data Setup Before Serial Clock Rising Edge	3		ns
t_{SIHD}[1]	Data Hold After Serial Clock Rising Edge	3		ns
$t_{SITXCLKW}$	Transmit Clock Width	9		ns
$t_{SITXCLK}$	Transmit Clock Period	20		ns
$t_{SISCLKW}$	Clock Width	36		ns
t_{SISCLK}	Clock Period	80		ns

[1] The serial clock, data, and frame sync signals can come from any of the DAI pins. The serial clock and frame sync signals can also come via PCG or SPORTs. The input of the PCG can be either CLKIN or any of the DAI pins.

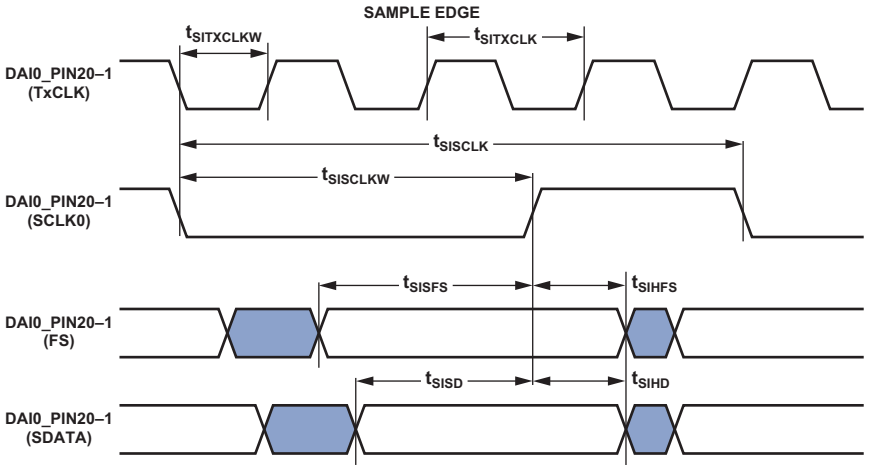


Figure 31. S/PDIF Transmitter Input Timing

Oversampling Clock (TxCLK) Switching Characteristics

The S/PDIF transmitter requires an oversampling clock input. This high frequency clock (TxCLK) input is divided down to generate the internal biphase clock.

Table 48. Oversampling Clock (TxCLK) Switching Characteristics

All specifications are subject to change without notice.			
Parameter		**Max**	**Unit**
Switching Characteristics			
f_{TXCLK_384}	Frequency for TxCLK = 384 × Frame Sync	Oversampling ratio × frame sync ≤ $1/t_{SITXCLK}$	MHz
f_{TXCLK_256}	Frequency for TxCLK = 256 × Frame Sync	49.2	MHz
f_{FS}	Frame Rate (FS)	192.0	kHz

S/PDIF Receiver

The following section describes timing as it relates to the S/PDIF receiver.

Internal Digital PLL Mode

In the internal digital PLL mode, the internal digital PLL generates the 512 × FS clock.

Table 49. S/PDIF Receiver Internal Digital PLL Mode Timing

All specifications are subject to change without notice.				
Parameter		**Min**	**Max**	**Unit**
Switching Characteristics				
t_{DFSI}	Frame Sync Delay After Serial Clock		5	ns
t_{HOFSI}	Frame Sync Hold After Serial Clock	–2		ns
t_{DDTI}	Transmit Data Delay After Serial Clock		5	ns
t_{HDTI}	Transmit Data Hold After Serial Clock	–2		ns

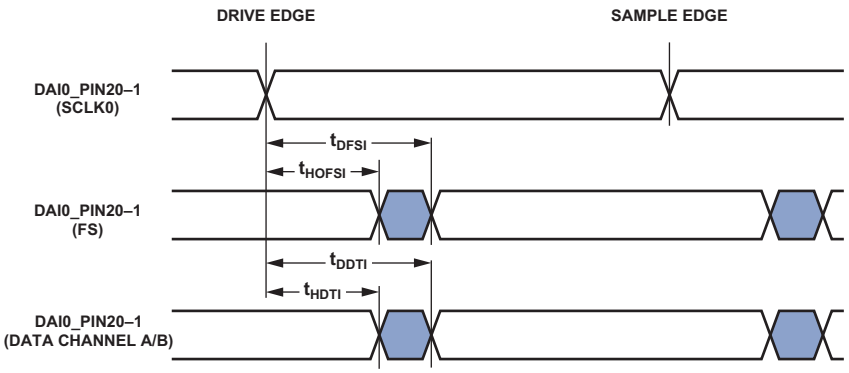


Figure 32. S/PDIF Receiver Internal Digital PLL Mode Timing

MediaLB (MLB)

All the numbers shown in Table 50 are applicable for all MLB speed modes (1024 FS, 512 FS, and 256 FS) for the 3-pin protocol, unless otherwise specified. Refer to the *Media Local Bus Specification Version 4.2* for more details.

Table 50. 3-Pin MLB Interface Specifications

All specifications are subject to change without notice.					
Parameter		**Min**	**Typ**	**Max**	**Unit**
t_{MLBCLK}	MLB Clock Period				
	1024 FS		20.3		ns
	512 FS		40		ns
	256 FS		81		ns
t_{MCKL}	MLBCLK Low Time				
	1024 FS	6.1			ns
	512 FS	14			ns
	256 FS	30			ns
t_{MCKH}	MLBCLK High Time				
	1024 FS	9.3			ns
	512 FS	14			ns
	256 FS	30			ns
t_{MCKR}	MLBCLK Rise Time (V_{IL} to V_{IH})				
	1024 FS			1	ns
	512 FS/256 FS			3	ns
t_{MCKF}	MLBCLK Fall Time (V_{IH} to V_{IL})				
	1024 FS			1	ns
	512 FS/256 FS			3	ns
t_{MPWV}[1]	MLBCLK Pulse Width Variation				
	1024 FS			0.7	nspp
	512 FS/256			2.0	nspp
t_{DSMCF}	DAT/SIG Input Setup Time	1			ns
t_{DHMCF}	DAT/SIG Input Hold Time	2			ns
t_{MCFDZ}	DAT/SIG Output Time to Three-State	0		15	ns
t_{MCDRV}	DAT/SIG Output Data Delay From MLBCLK Rising Edge			8	ns
t_{MDZH}[2]	Bus Hold Time				
	1024 FS	2			ns
	512 FS/256	4			ns
C_{MLB}	DAT/SIG Pin Load				
	1024 FS			40	pf
	512 FS/256			60	pf

[1] Pulse width variation is measured at 1.25 V by triggering on one edge of MLBCLK and measuring the spread on the other edge, measured in nanoseconds peak-to-peak.

[2] Board designs must ensure the high impedance bus does not leave the logic state of the final driven bit for this time period. Therefore, coupling must be minimized while meeting the maximum capacitive load listed.

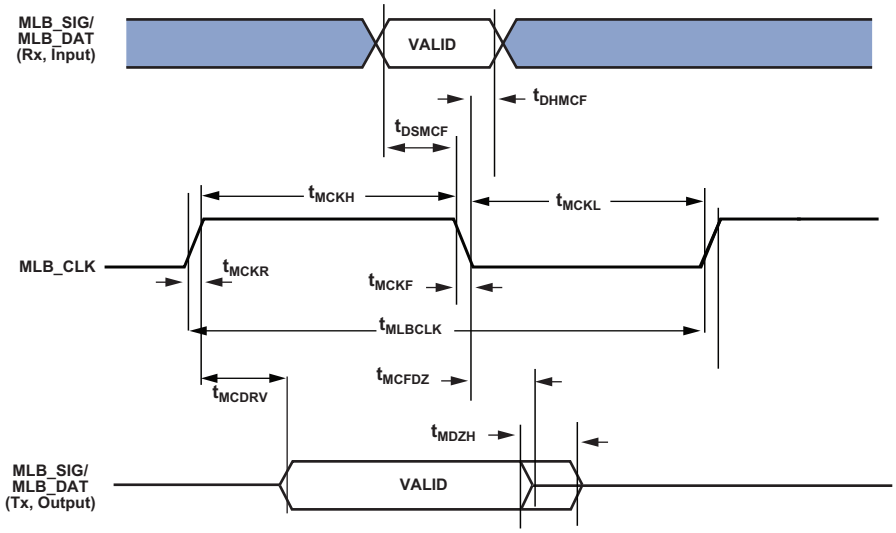


Figure 33. MLB Timing (3-Pin Interface)

Debug Interface (JTAG Emulation Port) Timing

Table 51 and Figure 34 provide I/O timing related to the debug interface (JTAG emulator port).

Table 51. JTAG Emulation Port Timing

All specifications are subject to change without notice.				
Parameter		**Min**	**Max**	**Unit**
Timing Requirements				
t_{TCK}	JTG_TCK Period	20		ns
t_{STAP}	JTG_TDI, JTG_TMS Setup Before JTG_TCK High	4		ns
t_{HTAP}	JTG_TDI, JTG_TMS Hold After JTG_TCK High	4		ns
t_{SSYS}	System Inputs Setup Before JTG_TCK High[1]	4		ns
t_{HSYS}	System Inputs Hold After JTG_TCK High[1]	4		ns
t_{TRSTW}	$\overline{\text{JTG\_TRST}}$ Pulse Width (Measured in JTG_TCK Cycles)[2]	4		T_{CK}
Switching Characteristics				
t_{DTDO}	JTG_TDO Delay From JTG_TCK Low		12	ns
t_{DSYS}	System Outputs Delay After JTG_TCK Low[3]		17	ns

[1] System Inputs = DAI0_PIN20-19, DAI0_PIN12-1, DAI1_PIN20-19, DAI1_PIN12-1, PA_15-0, PB_15-0, PC_7-0, SYS_BMODE2-0, $\overline{\text{SYS\_FAULT}}$.
[2] 50 MHz maximum.
[3] System Outputs = PA_15-0, PB_5-0, SYS_CLKOUT, $\overline{\text{SYS\_FAULT}}$, $\overline{\text{SYS\_RESOUT}}$.

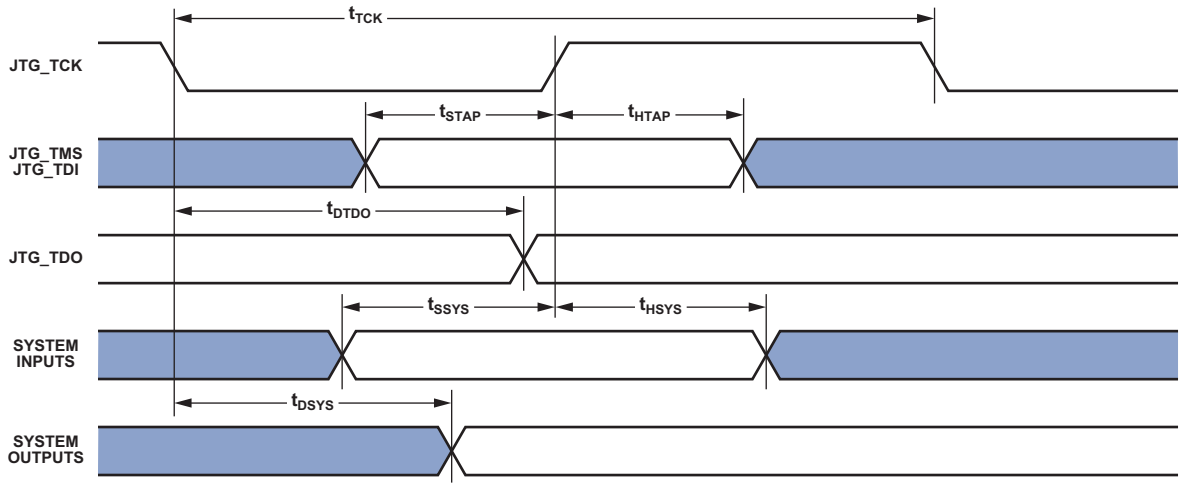


Figure 34. JTAG Port Timing

OUTPUT DRIVE CURRENTS

Figure 35 and Figure 36 show typical current voltage characteristics for the output drivers of the ADSP-21560/21561/21564/21568 processors. The curves represent the current drive capability of the output drivers as a function of output voltage.

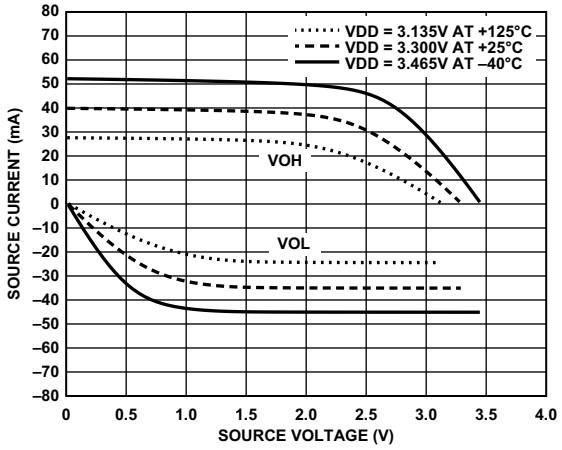


Figure 35. Driver Type A Current for All Pins Operating at Less Than or Equal to 62.5 MHz (3.3 V V_{DD_EXT})

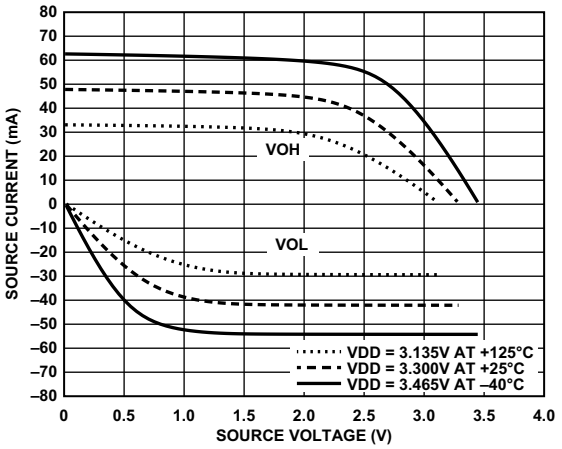


Figure 36. Driver Type A Current for All Pins Operating Above 62.5 MHz and Less Than or Equal to166.66 MHz (3.3 V V_{DD_EXT})

TEST CONDITIONS

All timing parameters appearing in this data sheet were measured under the conditions described in this section. Figure 37 shows the measurement point for ac measurements (except output enable/disable). The measurement point, V_{MEAS}, is $V_{DD\_EXT}/2$ for V_{DD_EXT} (nominal) = 3.3 V.

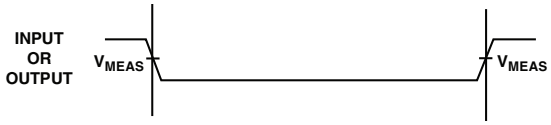


Figure 37. Voltage Reference Levels for AC Measurements (Except Output Enable/Disable)

Output Enable Time Measurement

Output pins are considered enabled when they make a transition from a high impedance state to the point when they start driving.

The output enable time, t_{ENA}, is the interval from the point when a reference signal reaches a high or low voltage level to the point when the output starts driving, as shown on the right side of Figure 38. If multiple pins are enabled, the measurement value is that of the first pin to start driving.

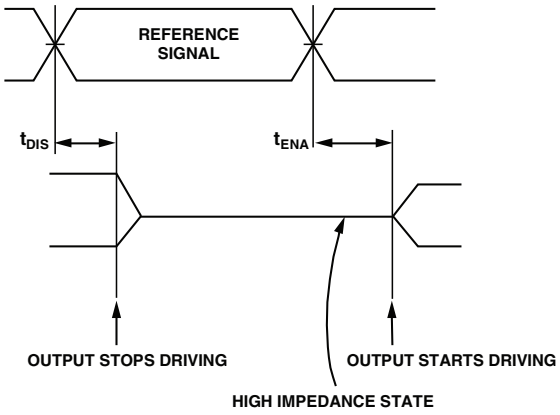


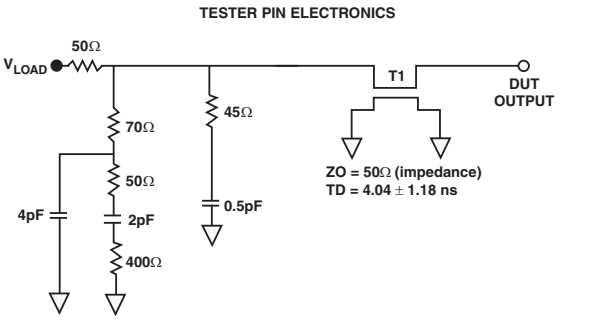
Figure 38. Output Enable/Disable

Output Disable Time Measurement

Output pins are considered disabled when they stop driving, enter a high impedance state, and start to decay from the output high or low voltage. The output disable time, t_{DIS}, is the interval from when a reference signal reaches a high or low voltage level to the point when the output stops driving, as shown on the left side of Figure 38).

Capacitive Loading

Output delays and holds are based on standard capacitive loads of an average of 6 pF on all pins (see Figure 39). V_{LOAD} is equal to $V_{DD\_EXT}/2$. Figure 40 and Figure 41 show how output rise time varies with capacitance. The delay and hold specifications given must be derated by a factor derived from these figures. The graphs in Figure 40 and Figure 41 cannot be linear outside the ranges shown.



NOTES:
THE WORST-CASE TRANSMISSION LINE DELAY IS SHOWN AND CAN BE USED FOR THE OUTPUT TIMING ANALYSIS TO REFLECT THE TRANSMISSION LINE EFFECT AND MUST BE CONSIDERED. THE TRANSMISSION LINE (TD) IS FOR LOAD ONLY AND DOES NOT AFFECT THE DATA SHEET TIMING SPECIFICATIONS.

ANALOG DEVICES RECOMMENDS USING THE IBIS MODEL TIMING FOR A GIVEN SYSTEM REQUIREMENT. IF NECESSARY, THE SYSTEM CAN INCORPORATE EXTERNAL DRIVERS TO COMPENSATE FOR ANY TIMING DIFFERENCES.

Figure 39. Equivalent Device Loading for AC Measurements (Includes All Fixtures)

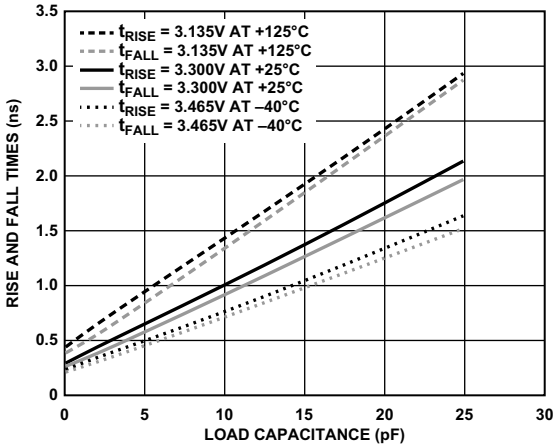


Figure 40. Driver Type A Rise and Fall Times (10% to 90%) vs. Load Capacitance for All Pins Operating Above 62.5 MHz and Less Than or Equal to 166.66 MHz

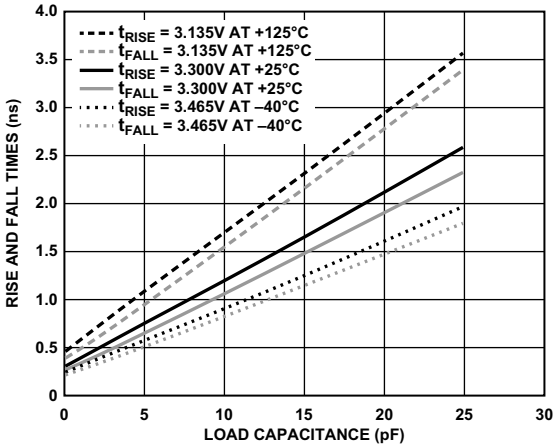


Figure 41. Driver Type A Rise and Fall Times (10% to 90%) vs. Load Capacitance for All Pins Operating at Less Than or Equal to 62.5 MHz

ENVIRONMENTAL CONDITIONS

The ADSP-21560/21561/21564/21568 processors are rated for performance over the temperature range specified in the Preliminary Operating Conditions section.

Application system thermal simulation is required for accurate temperature analysis. The thermal simulation must account for all specific 3D system design features, including, but not limited to other heat sources, use of heat sinks, use of thermal interface materials, and the system enclosure details. Thermal models of the package are available from Analog Devices under the Tools and Simulations tab of the product web page. The thermal model(s) are compatible with all major thermal simulation tools.

The use of JEDEC θ_{JA}, θ_{JC}, or Ψ_{JT} thermal parameters for application system thermal estimates is not recommended as indicated in the JEDEC51 specifications:

> "This methodology is not meant to and will not predict the performance of a package in an application-specific environment."

ADSP-21568 400-BALL CSP_BGA BALL ASSIGNMENTS

The ADSP-21568 400-Ball CSP_BGA Ball Assignments (Numerical by Ball Number) table lists the 400-ball CSP_BGA package by ball number.

The ADSP-21568 400-Ball CSP_BGA Ball Assignments (Alphabetical by Pin Name) table lists the 400-ball CSP_BGA package by pin name.

ADSP-21568 400-BALL CSP_BGA BALL ASSIGNMENTS (NUMERICAL BY BALL NUMBER)

Ball No.	Pin Name	Ball No.	Pin Name	Ball No.	Pin Name	Ball No.	Pin Name
A01	GND	C01	DNC	E01	DNC	G01	DNC
A02	DNC	C02	DNC	E02	DNC	G02	DNC
A03	DNC	C03	GND	E03	GND	G03	GND
A04	DNC	C04	GND	E04	VDD_INT	G04	VDD_INT
A05	DNC	C05	GND	E05	VDD_INT	G05	VDD_INT
A06	DNC	C06	GND	E06	VDD_INT	G06	DNC
A07	PB_00	C07	PB_03	E07	VDD_INT	G07	DNC
A08	SYS_BMODE2	C08	PB_05	E08	VDD_INT	G08	DNC
A09	$\overline{\text{SYS\_HWRST}}$	C09	PB_01	E09	VDD_INT	G09	DNC
A10	$\overline{\text{JTG\_TRST}}$	C10	$\overline{\text{SYS\_RESOUT}}$	E10	VDD_INT	G10	DNC
A11	$\overline{\text{SYS\_FAULT}}$	C11	JTG_TDO	E11	VDD_INT	G11	DNC
A12	DNC	C12	JTG_TMS	E12	VDD_INT	G12	DNC
A13	DNC	C13	JTG_TDI	E13	VDD_INT	G13	DNC
A14	DNC	C14	GND	E14	VDD_INT	G14	DNC
A15	DNC	C15	GND	E15	VDD_INT	G15	DNC
A16	DNC	C16	GND	E16	VDD_INT	G16	VDD_INT
A17	DNC	C17	GND	E17	VDD_INT	G17	VDD_INT
A18	DNC	C18	GND	E18	GND	G18	GND
A19	DNC	C19	DNC	E19	DNC	G19	DNC
A20	GND	C20	DNC	E20	DNC	G20	DNC
B01	GND	D01	DNC	F01	DNC	H01	DNC
B02	GND	D02	GND	F02	DNC	H02	GND
B03	DNC	D03	DNC	F03	GND	H03	GND
B04	DNC	D04	GND	F04	VDD_INT	H04	VDD_INT
B05	DNC	D05	GND	F05	VDD_INT	H05	VDD_INT
B06	DNC	D06	GND	F06	DNC	H06	DNC
B07	PB_04	D07	GND	F07	DNC	H07	DNC
B08	PB_02	D08	VDD_EXT	F08	DNC	H08	GND
B09	SYS_BMODE1	D09	VDD_EXT	F09	DNC	H09	GND
B10	SYS_BMODE0	D10	VDD_EXT	F10	DNC	H10	GND
B11	JTG_TCK	D11	VDD_EXT	F11	DNC	H11	GND
B12	DNC	D12	GND	F12	DNC	H12	GND
B13	DNC	D13	GND	F13	DNC	H13	GND
B14	DNC	D14	GND	F14	DNC	H14	DNC
B15	DNC	D15	GND	F15	DNC	H15	DNC
B16	DNC	D16	GND	F16	VDD_INT	H16	VDD_INT
B17	DNC	D17	GND	F17	VDD_INT	H17	VDD_INT
B18	DNC	D18	GND	F18	GND	H18	GND
B19	GND	D19	DNC	F19	DNC	H19	DNC
B20	DNC	D20	DNC	F20	DNC	H20	DNC

Ball No.	Pin Name	Ball No.	Pin Name	Ball No.	Pin Name	Ball No.	Pin Name
J01	DNC	L09	GND	N17	GND	T05	VDD_EXT
J02	DNC	L10	GND	N18	GND	T06	DNC
J03	GND	L11	GND	N19	DNC	T07	DNC
J04	DNC	L12	GND	N20	DNC	T08	DNC
J05	VDD_INT	L13	GND	P01	GND	T09	DNC
J06	DNC	L14	VDD_INT	P02	PA_02	T10	VDD_REF
J07	DNC	L15	VDD_INT	P03	PA_01	T11	VDD_REF
J08	GND	L16	GND	P04	VDD_EXT	T12	VDD_REF
J09	GND	L17	GND	P05	VDD_REF	T13	VDD_REF
J10	GND	L18	DNC	P06	VDD_INT	T14	VDD_REF
J11	GND	L19	DNC	P07	VDD_INT	T15	VDD_REF
J12	GND	L20	DNC	P08	VDD_INT	T16	VDD_EXT
J13	GND	M01	GND	P09	VDD_INT	T17	GND
J14	VDD_INT	M02	GND	P10	VDD_INT	T18	DAI1_PIN09
J15	VDD_INT	M03	SYS_CLKOUT	P11	VDD_INT	T19	DAI1_PIN06
J16	VDD_INT	M04	VDD_EXT	P12	VDD_INT	T20	DAI1_PIN04
J17	VDD_INT	M05	VDD_INT	P13	VDD_INT	U01	GND
J18	GND	M06	VDD_INT	P14	VDD_INT	U02	PA_10
J19	DNC	M07	VDD_INT	P15	VDD_REF	U03	PA_08
J20	DNC	M08	GND	P16	VDD_EXT	U04	GND
K01	GND	M09	GND	P17	GND	U05	GND
K02	GND	M10	GND	P18	DAI1_PIN02	U06	VDD_EXT
K03	GND	M11	GND	P19	GND	U07	VDD_EXT
K04	VDD_EXT	M12	GND	P20	GND	U08	VDD_EXT
K05	VDD_INT	M13	GND	R01	PA_04	U09	VDD_EXT
K06	VDD_INT	M14	VDD_INT	R02	GND	U10	VDD_EXT
K07	DNC	M15	VDD_REF	R03	PA_03	U11	VDD_EXT
K08	GND	M16	VDD_EXT	R04	VDD_EXT	U12	VDD_EXT
K09	GND	M17	GND	R05	VDD_REF	U13	VDD_EXT
K10	GND	M18	GND	R06	VDD_INT	U14	VDD_EXT
K11	GND	M19	DNC	R07	VDD_INT	U15	VDD_EXT
K12	GND	M20	DNC	R08	VDD_INT	U16	GND
K13	GND	N01	SYS_CLKIN0	R09	VDD_INT	U17	GND
K14	VDD_INT	N02	GND	R10	VDD_INT	U18	DAI1_PIN10
K15	VDD_INT	N03	PA_00	R11	VDD_INT	U19	DAI1_PIN07
K16	VDD_INT	N04	VDD_EXT	R12	VDD_INT	U20	DAI1_PIN05
K17	GND	N05	DNC	R13	VDD_INT	V01	PA_07
K18	GND	N06	VDD_INT	R14	VDD_INT	V02	PA_09
K19	GND	N07	VDD_INT	R15	VDD_REF	V03	GND
K20	GND	N08	GND	R16	VDD_EXT	V04	GND
L01	SYS_XTAL0	N09	GND	R17	GND	V05	DNC
L02	GND	N10	GND	R18	DAI1_PIN03	V06	DNC
L03	GND	N11	GND	R19	DAI1_PIN08	V07	DNC
L04	VDD_EXT	N12	GND	R20	DAI1_PIN01	V08	PA_11
L05	VDD_INT	N13	GND	T01	GND	V09	DAI0_PIN02
L06	VDD_INT	N14	VDD_INT	T02	PA_05	V10	DAI0_PIN06
L07	VDD_INT	N15	VDD_REF	T03	PA_06	V11	DAI0_PIN09
L08	GND	N16	VDD_EXT	T04	GND	V12	DAI0_PIN20

Ball No.	Pin Name
V13	DNC
V14	DNC
V15	GND
V16	GND
V17	DAI1_PIN19
V18	GND
V19	DNC
V20	DNC
W01	GND
W02	GND
W03	xSPI_RWDS
W04	SPI0_RDY
W05	DNC
W06	PA_12
W07	PA_14
W08	PA_15
W09	DAI0_PIN03
W10	DAI0_PIN05
W11	DAI0_PIN08
W12	DNC
W13	DAI0_PIN19
W14	DNC
W15	DNC
W16	DNC
W17	DNC
W18	DAI1_PIN20
W19	GND
W20	GND
Y01	GND
Y02	GND
Y03	DNC
Y04	$\overline{\text{xSPI\_SEL2}}$
Y05	GND
Y06	PA_13
Y07	GND
Y08	DAI0_PIN01
Y09	DAI0_PIN04
Y10	DAI0_PIN07
Y11	DAI0_PIN10
Y12	DNC
Y13	GND
Y14	DNC
Y15	DNC
Y16	GND
Y17	DNC
Y18	DNC
Y19	GND
Y20	GND

ADSP-21568 400-BALL CSP_BGA BALL ASSIGNMENTS (ALPHABETICAL BY PIN NAME)

Pin Name	Ball No.	Pin Name	Ball No.	Pin Name	Ball No.	Pin Name	Ball No.
DAI0_PIN01	Y08	DNC	B17	DNC	H14	GND	B02
DAI0_PIN02	V09	DNC	B18	DNC	H15	GND	B19
DAI0_PIN03	W09	DNC	B20	DNC	H19	GND	C03
DAI0_PIN04	Y09	DNC	C01	DNC	H20	GND	C04
DAI0_PIN05	W10	DNC	C02	DNC	J01	GND	C05
DAI0_PIN06	V10	DNC	C19	DNC	J02	GND	C06
DAI0_PIN07	Y10	DNC	C20	DNC	J04	GND	C14
DAI0_PIN08	W11	DNC	D01	DNC	J06	GND	C15
DAI0_PIN09	V11	DNC	D03	DNC	J07	GND	C16
DAI0_PIN10	Y11	DNC	D19	DNC	J19	GND	C17
DAI0_PIN19	W13	DNC	D20	DNC	J20	GND	C18
DAI0_PIN20	V12	DNC	E01	DNC	K07	GND	D02
DAI1_PIN01	R20	DNC	E02	DNC	L18	GND	D04
DAI1_PIN02	P18	DNC	E19	DNC	L19	GND	D05
DAI1_PIN03	R18	DNC	E20	DNC	L20	GND	D06
DAI1_PIN04	T20	DNC	F01	DNC	M19	GND	D07
DAI1_PIN05	U20	DNC	F02	DNC	M20	GND	D12
DAI1_PIN06	T19	DNC	F06	DNC	N05	GND	D13
DAI1_PIN07	U19	DNC	F07	DNC	N19	GND	D14
DAI1_PIN08	R19	DNC	F08	DNC	N20	GND	D15
DAI1_PIN09	T18	DNC	F09	DNC	T06	GND	D16
DAI1_PIN10	U18	DNC	F10	DNC	T07	GND	D17
DAI1_PIN19	V17	DNC	F11	DNC	T08	GND	D18
DAI1_PIN20	W18	DNC	F12	DNC	T09	GND	E03
DNC	A02	DNC	F13	DNC	V05	GND	E18
DNC	A03	DNC	F14	DNC	V06	GND	F03
DNC	A04	DNC	F15	DNC	V07	GND	F18
DNC	A05	DNC	F19	DNC	V13	GND	G03
DNC	A06	DNC	F20	DNC	V14	GND	G18
DNC	A12	DNC	G01	DNC	V19	GND	H02
DNC	A13	DNC	G02	DNC	V20	GND	H03
DNC	A14	DNC	G06	DNC	W05	GND	H08
DNC	A15	DNC	G07	DNC	W12	GND	H09
DNC	A16	DNC	G08	DNC	W14	GND	H10
DNC	A17	DNC	G09	DNC	W15	GND	H11
DNC	A18	DNC	G10	DNC	W16	GND	H12
DNC	A19	DNC	G11	DNC	W17	GND	H13
DNC	B03	DNC	G12	DNC	Y03	GND	H18
DNC	B04	DNC	G13	DNC	Y12	GND	J03
DNC	B05	DNC	G14	DNC	Y14	GND	J08
DNC	B06	DNC	G15	DNC	Y15	GND	J09
DNC	B12	DNC	G19	DNC	Y17	GND	J10
DNC	B13	DNC	G20	DNC	Y18	GND	J11
DNC	B14	DNC	H01	GND	A01	GND	J12
DNC	B15	DNC	H06	GND	A20	GND	J13
DNC	B16	DNC	H07	GND	B01	GND	J18

Pin Name	Ball No.	Pin Name	Ball No.	Pin Name	Ball No.	Pin Name	Ball No.
GND	K01	GND	T01	PB_02	B08	VDD_INT	E12
GND	K02	GND	T04	PB_03	C07	VDD_INT	E13
GND	K03	GND	T17	PB_04	B07	VDD_INT	E14
GND	K08	GND	U01	PB_05	C08	VDD_INT	E15
GND	K09	GND	U04	SPI0_RDY	W04	VDD_INT	E16
GND	K10	GND	U05	SYS_BMODE0	B10	VDD_INT	E17
GND	K11	GND	U16	SYS_BMODE1	B09	VDD_INT	F04
GND	K12	GND	U17	SYS_BMODE2	A08	VDD_INT	F05
GND	K13	GND	V03	SYS_CLKIN0	N01	VDD_INT	F16
GND	K17	GND	V04	SYS_CLKOUT	M03	VDD_INT	F17
GND	K18	GND	V15	$\overline{\text{SYS\_FAULT}}$	A11	VDD_INT	G04
GND	K19	GND	V16	$\overline{\text{SYS\_HWRST}}$	A09	VDD_INT	G05
GND	K20	GND	V18	$\overline{\text{SYS\_RESOUT}}$	C10	VDD_INT	G16
GND	L02	GND	W01	SYS_XTAL0	L01	VDD_INT	G17
GND	L03	GND	W02	VDD_EXT	D08	VDD_INT	H04
GND	L08	GND	W19	VDD_EXT	D09	VDD_INT	H05
GND	L09	GND	W20	VDD_EXT	D10	VDD_INT	H16
GND	L10	GND	Y01	VDD_EXT	D11	VDD_INT	H17
GND	L11	GND	Y02	VDD_EXT	K04	VDD_INT	J05
GND	L12	GND	Y05	VDD_EXT	L04	VDD_INT	J14
GND	L13	GND	Y07	VDD_EXT	M04	VDD_INT	J15
GND	L16	GND	Y13	VDD_EXT	M16	VDD_INT	J16
GND	L17	GND	Y16	VDD_EXT	N04	VDD_INT	J17
GND	M01	GND	Y19	VDD_EXT	N16	VDD_INT	K05
GND	M02	GND	Y20	VDD_EXT	P04	VDD_INT	K06
GND	M08	JTG_TCK	B11	VDD_EXT	P16	VDD_INT	K14
GND	M09	JTG_TDI	C13	VDD_EXT	R04	VDD_INT	K15
GND	M10	JTG_TDO	C11	VDD_EXT	R16	VDD_INT	K16
GND	M11	JTG_TMS	C12	VDD_EXT	T05	VDD_INT	L05
GND	M12	$\overline{\text{JTG\_TRST}}$	A10	VDD_EXT	T16	VDD_INT	L06
GND	M13	PA_00	N03	VDD_EXT	U06	VDD_INT	L07
GND	M17	PA_01	P03	VDD_EXT	U07	VDD_INT	L14
GND	M18	PA_02	P02	VDD_EXT	U08	VDD_INT	L15
GND	N02	PA_03	R03	VDD_EXT	U09	VDD_INT	M05
GND	N08	PA_04	R01	VDD_EXT	U10	VDD_INT	M06
GND	N09	PA_05	T02	VDD_EXT	U11	VDD_INT	M07
GND	N10	PA_06	T03	VDD_EXT	U12	VDD_INT	M14
GND	N11	PA_07	V01	VDD_EXT	U13	VDD_INT	N06
GND	N12	PA_08	U03	VDD_EXT	U14	VDD_INT	N07
GND	N13	PA_09	V02	VDD_EXT	U15	VDD_INT	N14
GND	N17	PA_10	U02	VDD_INT	E04	VDD_INT	P06
GND	N18	PA_11	V08	VDD_INT	E05	VDD_INT	P07
GND	P01	PA_12	W06	VDD_INT	E06	VDD_INT	P08
GND	P17	PA_13	Y06	VDD_INT	E07	VDD_INT	P09
GND	P19	PA_14	W07	VDD_INT	E08	VDD_INT	P10
GND	P20	PA_15	W08	VDD_INT	E09	VDD_INT	P11
GND	R02	PB_00	A07	VDD_INT	E10	VDD_INT	P12
GND	R17	PB_01	C09	VDD_INT	E11	VDD_INT	P13

Pin Name	Ball No.
VDD_INT	P14
VDD_INT	R06
VDD_INT	R07
VDD_INT	R08
VDD_INT	R09
VDD_INT	R10
VDD_INT	R11
VDD_INT	R12
VDD_INT	R13
VDD_INT	R14
VDD_REF	M15
VDD_REF	N15
VDD_REF	P05
VDD_REF	P15
VDD_REF	R05
VDD_REF	R15
VDD_REF	T10
VDD_REF	T11
VDD_REF	T12
VDD_REF	T13
VDD_REF	T14
VDD_REF	T15
xSPI_RWDS	W03
$\overline{\text{xSPI\_SEL2}}$	Y04

CONFIGURATION OF THE 400-BALL CSP_BGA

Figure 42 shows an overview of signal placement on the 400-ball CSP_BGA.

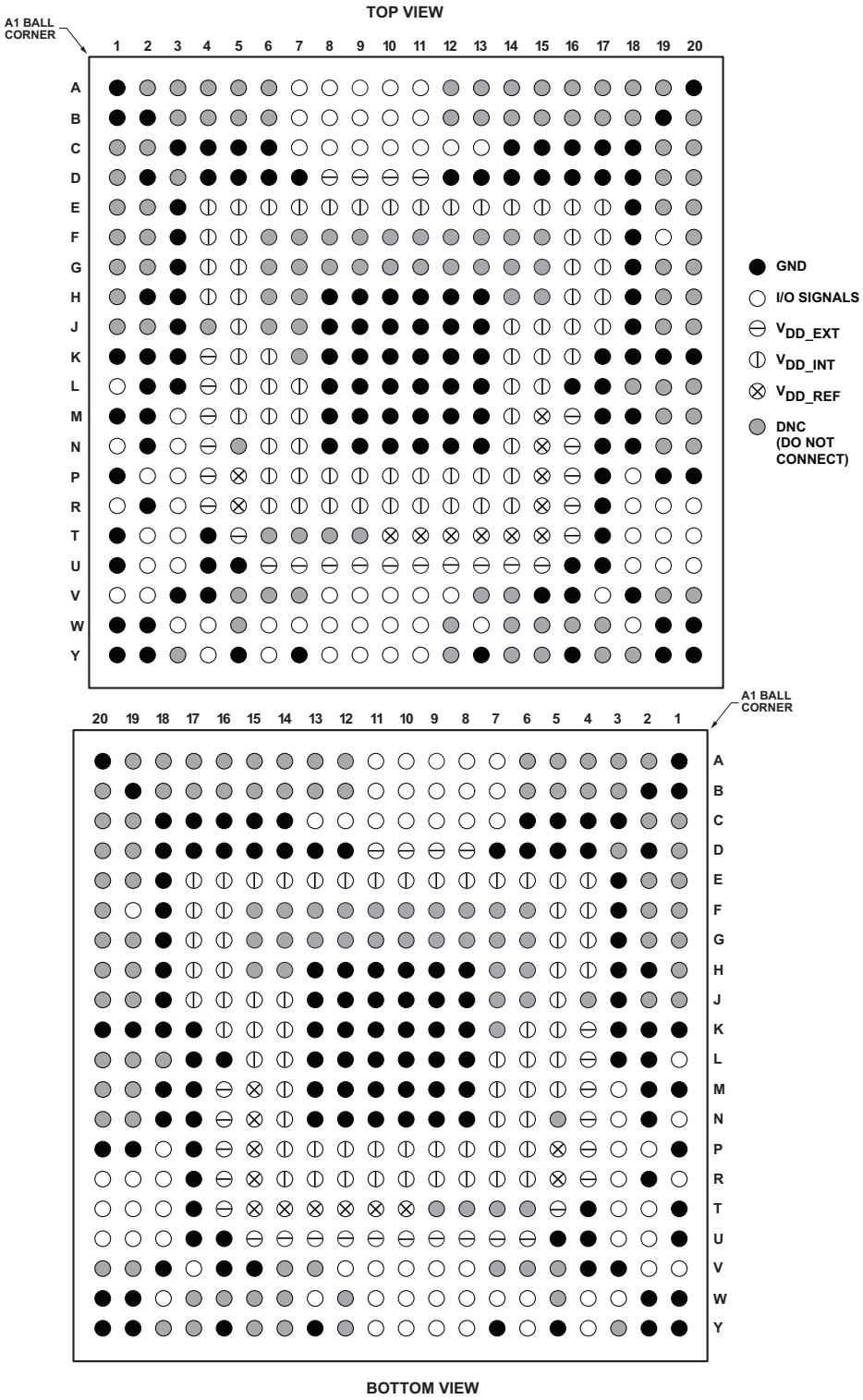


Figure 42. 400-Ball CSP_BGA Configuration

ADSP-21560/21561/21564 120-LEAD LQFP LEAD ASSIGNMENTS

The ADSP-21560/21561/21564 120-Lead LQFP Lead Assignments (Numerical by Lead Number) table lists the 120-lead LQFP package by lead number.

The ADSP-21560/21561/21564 120-Lead Assignments (Alphabetical by Pin Name) table lists the 120-lead LQFP package by pin name.

ADSP-21560/21561/21564 120-LEAD LQFP LEAD ASSIGNMENTS (NUMERICAL BY LEAD NUMBER)

Lead No.	Pin Name[1, 2]	Lead No.	Pin Name[1, 2]	Lead No.	Pin Name[1, 2]	Lead No.	Pin Name[1, 2]
01	VDD_INT	41	DAI0_PIN01	81	GND	121[3]	GND
02	GND	42	DAI0_PIN02	82	SYS_BMODE2		
03	VDD_INT	43	DAI0_PIN03	83	DNC		
04	VDD_INT	44	VDD_INT	84	SPI0_RDY		
05	SYS_CLKIN0	45	VDD_INT	85	DNC		
06	SYS_XTAL0	46	DAI0_PIN04	86	GND		
07	VDD_REF	47	DAI0_PIN05	87	VDD_INT		
08	VDD_INT	48	DAI0_PIN06	88	VDD_INT		
09	xSPI_RWDS	49	DAI0_PIN07	89	VDD_INT		
10	SYS_CLKOUT	50	VDD_EXT	90	GND		
11	DNC	51	DNC	91	VDD_INT		
12	VDD_EXT	52	DAI0_PIN08	92	GND		
13	VDD_INT	53	DAI0_PIN09	93	VDD_INT		
14	PA_00	54	DAI0_PIN10	94	VDD_INT		
15	PA_01	55	DAI0_PIN19	95	VDD_INT		
16	PA_02	56	DAI0_PIN20	96	JTG_TDI		
17	DNC	57	VDD_INT	97	JTG_TCK		
18	PA_03	58	GND	98	JTG_TMS		
19	PA_04	59	VDD_INT	99	JTG_TDO		
20	PA_05	60	VDD_INT	100	DNC		
21	PA_06	61	VDD_INT	101	VDD_EXT		
22	VDD_INT	62	GND	102	$\overline{\text{SYS\_FAULT}}$		
23	$\overline{\text{xSPI\_SEL2}}$	63	DAI1_PIN20	103	$\overline{\text{JTG\_TRST}}$		
24	VDD_EXT	64	DAI1_PIN19	104	$\overline{\text{SYS\_HWRST}}$		
25	PA_07	65	DAI1_PIN10	105	SYS_BMODE0		
26	PA_08	66	DAI1_PIN09	106	SYS_BMODE1		
27	PA_09	67	DNC	107	$\overline{\text{SYS\_RESOUT}}$		
28	PA_10	68	VDD_EXT	108	PB_00		
29	VDD_INT	69	VDD_INT	109	PB_01		
30	GND	70	DAI1_PIN08	110	VDD_INT		
31	GND	71	DAI1_PIN07	111	VDD_EXT		
32	VDD_INT	72	DAI1_PIN06	112	DNC		
33	VDD_INT	73	DAI1_PIN05	113	PB_02		
34	PA_11	74	DAI1_PIN04	114	PB_03		
35	PA_12	75	DAI1_PIN03	115	PB_04		
36	PA_13	76	DAI1_PIN02	116	PB_05		
37	PA_14	77	DAI1_PIN01	117	VDD_INT		
38	VDD_EXT	78	VDD_EXT	118	VDD_INT		
39	DNC	79	VDD_REF	119	VDD_INT		
40	PA_15	80	VDD_INT	120	GND		

[1]DNC = Do not make any electrical connection to this pin.
[2]Pin 09, Pin 23, and Pin 84 are three-stated by default.
[3]Pin 121 is the GND supply (see Figure 44) for the processor; this pad must connect to GND.

ADSP-21560/21561/21564 120-LEAD LQFP LEAD ASSIGNMENTS (ALPHABETICAL BY PIN NAME)

Pin Name[1, 2]	Lead No.	Pin Name[1, 2]	Lead No.	Pin Name[1, 2]	Lead No.
DAI0_PIN01	41	JTG_TDO	99	VDD_INT	08
DAI0_PIN02	42	JTG_TMS	98	VDD_INT	13
DAI0_PIN03	43	$\overline{\text{JTG\_TRST}}$	103	VDD_INT	22
DAI0_PIN04	46	PA_00	14	VDD_INT	29
DAI0_PIN05	47	PA_01	15	VDD_INT	32
DAI0_PIN06	48	PA_02	16	VDD_INT	33
DAI0_PIN07	49	PA_03	18	VDD_INT	44
DAI0_PIN08	52	PA_04	19	VDD_INT	45
DAI0_PIN09	53	PA_05	20	VDD_INT	57
DAI0_PIN10	54	PA_06	21	VDD_INT	59
DAI0_PIN19	55	PA_07	25	VDD_INT	60
DAI0_PIN20	56	PA_08	26	VDD_INT	61
DAI1_PIN01	77	PA_09	27	VDD_INT	69
DAI1_PIN02	76	PA_10	28	VDD_INT	80
DAI1_PIN03	75	PA_11	34	VDD_INT	87
DAI1_PIN04	74	PA_12	35	VDD_INT	88
DAI1_PIN05	73	PA_13	36	VDD_INT	89
DAI1_PIN06	72	PA_14	37	VDD_INT	91
DAI1_PIN07	71	PA_15	40	VDD_INT	93
DAI1_PIN08	70	PB_00	108	VDD_INT	94
DAI1_PIN09	66	PB_01	109	VDD_INT	95
DAI1_PIN10	65	PB_02	113	VDD_INT	110
DAI1_PIN19	64	PB_03	114	VDD_INT	117
DAI1_PIN20	63	PB_04	115	VDD_INT	118
DNC	11	PB_05	116	VDD_INT	119
DNC	17	SPI0_RDY	84	VDD_REF	07
DNC	39	SYS_BMODE0	105	VDD_REF	79
DNC	51	SYS_BMODE1	106	xSPI_RWDS	09
DNC	67	SYS_BMODE2	82	$\overline{\text{xSPI\_SEL2}}$	23
DNC	83	SYS_CLKIN0	05		
DNC	85	SYS_CLKOUT	10		
DNC	100	$\overline{\text{SYS\_FAULT}}$	102		
DNC	112	$\overline{\text{SYS\_HWRST}}$	104		
GND	02	$\overline{\text{SYS\_RESOUT}}$	107		
GND	30	SYS_XTAL0	06		
GND	31	VDD_EXT	12		
GND	58	VDD_EXT	24		
GND	62	VDD_EXT	38		
GND	81	VDD_EXT	50		
GND	86	VDD_EXT	68		
GND	90	VDD_EXT	78		
GND	92	VDD_EXT	101		
GND	120	VDD_EXT	111		
GND	121[3]	VDD_INT	01		
JTG_TCK	97	VDD_INT	03		
JTG_TDI	96	VDD_INT	04		

[1]DNC = Do not make any electrical connection to this pin.
[2]Pin 09, Pin 23, and Pin 84 are three-stated by default.
[3]Pin 121 is the GND supply (see Figure 44) for the processor; this pad must connect to GND.

CONFIGURATION OF THE 120-LEAD LQFP LEAD CONFIGURATION

Figure 43 shows the top view of the 120-lead LQFP lead configuration and Figure 44 shows the bottom view of the 120-lead LQFP lead configuration.

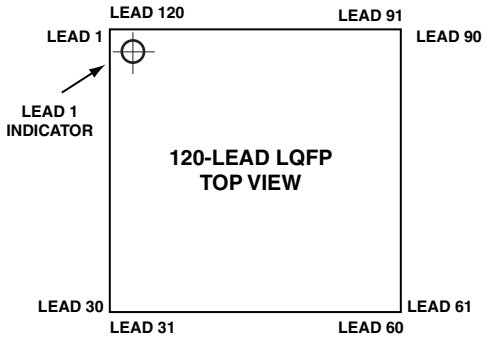


Figure 43. 120-Lead LQFP Lead Configuration (Top View)

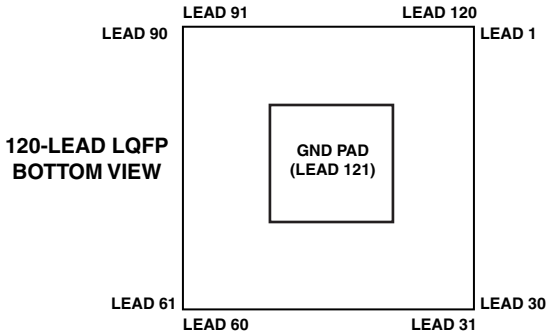


Figure 44. 120-Lead LQFP Lead Configuration (Bottom View)

OUTLINE DIMENSIONS

Dimensions in Figure 45 (for the 400-ball CSP_BGA) and Figure 46 (for the 120-lead LQFP) are shown in millimeters.

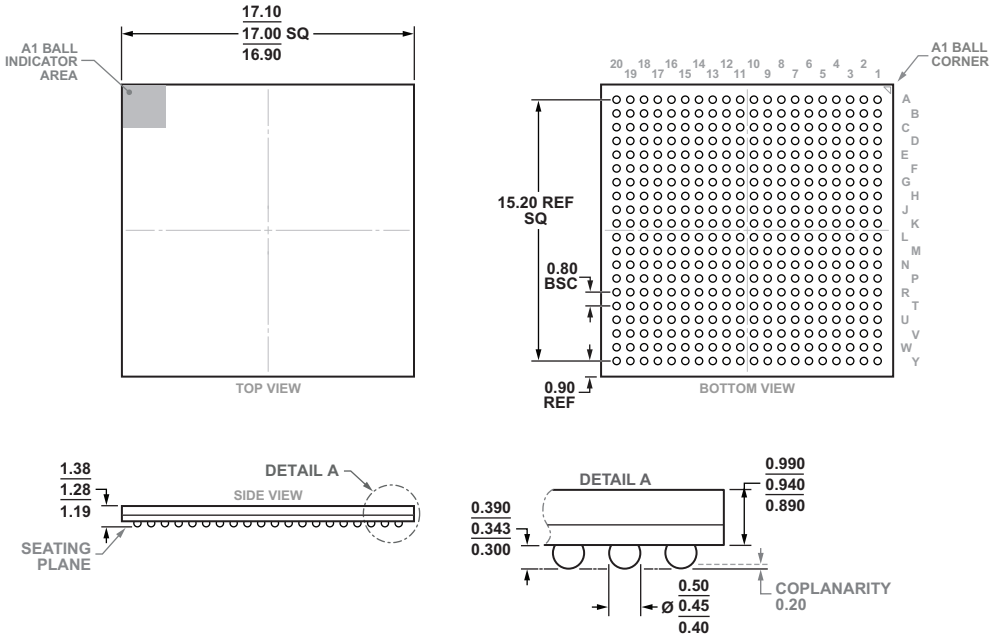
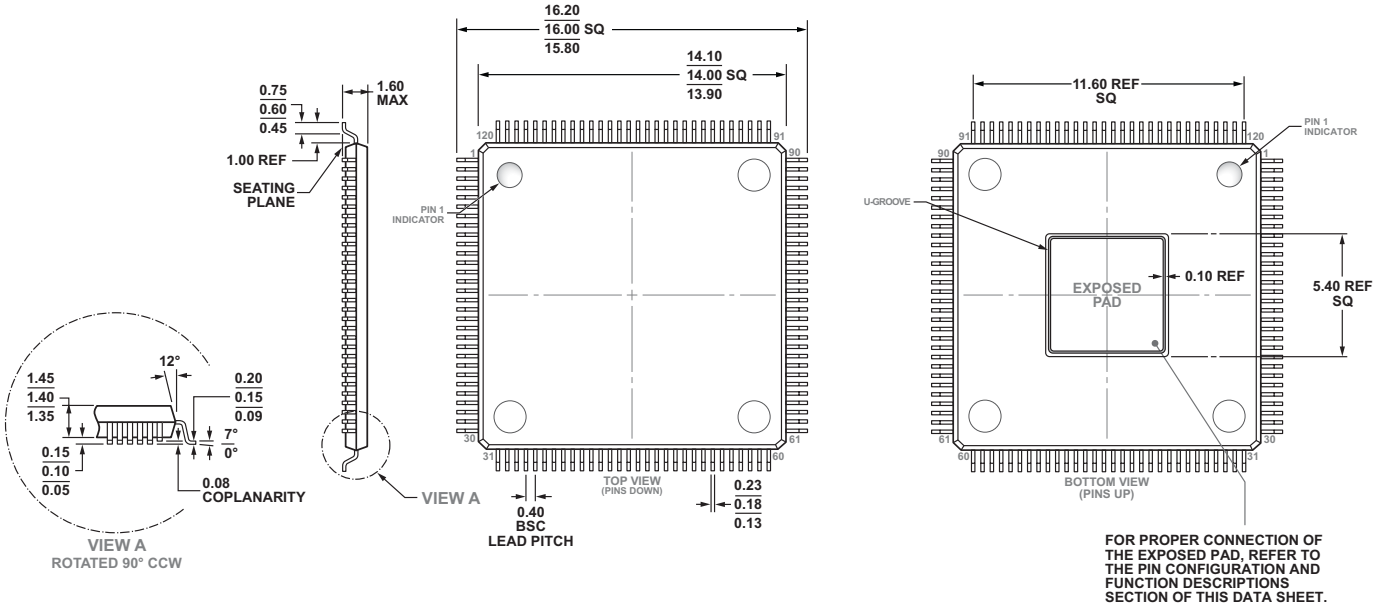


Figure 45. 400-Ball Chip Scale Package Ball Grid Array [CSP_BGA]
(BC-400-3)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MS-026-BEE-HD

Figure 46. 120-Lead Low Profile Quad Flat Package, Exposed Pad [LQFP]
(SW-120-4)
Dimensions shown in millimeters

SURFACE-MOUNT DESIGN

Table 52 is provided as an aid to PCB design. For industry-standard design recommendations, refer to IPC-7351, *Generic Requirements for Surface-Mount Design and Land Pattern Standard*.

Table 52. CSP_BGA Data for Use with Surface-Mount Design

Package	Package Ball Attach Type	Package Solder Mask Opening	Package Ball Pad Size
BC-400-3	Solder Mask Defined	0.4 mm Diameter	0.5 mm Diameter

PLANNED AUTOMOTIVE PRODUCTION PRODUCTS

Model[1, 2]	Processor Instruction Rate (Max)	L2 SRAM	Temperature Range[3]	Package Description	Package Option
ADSP-21560WCSWZ6	600 MHz	1 MB	–40°C to +125°C	120-Lead LQFP_EP, Exposed Pad	SW-120-4
ADSP-21560WCSWZ6RL	600 MHz	1 MB	–40°C to +125°C	120-Lead LQFP_EP, Exposed Pad	SW-120-4
ADSP-21560WCSWZ8	800 MHz	1 MB	–40°C to +125°C	120-Lead LQFP_EP, Exposed Pad	SW-120-4
ADSP-21560WCSWZ8RL	800 MHz	1 MB	–40°C to +125°C	120-Lead LQFP_EP, Exposed Pad	SW-120-4
ADSP-21561WCSWZ8	800 MHz	1.5 MB	–40°C to +125°C	120-Lead LQFP_EP, Exposed Pad	SW-120-4
ADSP-21561WCSWZ8RL	800 MHz	1.5 MB	–40°C to +125°C	120-Lead LQFP_EP, Exposed Pad	SW-120-4
ADSP-21561WCSWZ10	1 GHz	1.5 MB	–40°C to +125°C	120-Lead LQFP_EP, Exposed Pad	SW-120-4
ADSP21561WCSWZ10RL	1 GHz	1.5 MB	–40°C to +125°C	120-Lead LQFP_EP, Exposed Pad	SW-120-4
ADSP-21564WCSWZ8	800 MHz	2 MB	–40°C to +125°C	120-Lead LQFP_EP, Exposed Pad	SW-120-4
ADSP-21564WCSWZ8RL	800 MHz	2 MB	–40°C to +125°C	120-Lead LQFP_EP, Exposed Pad	SW-120-4
ADSP-21564WCSWZ10	1 GHz	2 MB	–40°C to +125°C	120-Lead LQFP_EP, Exposed Pad	SW-120-4
ADSP21564WCSWZ10RL	1 GHz	2 MB	–40°C to +125°C	120-Lead LQFP_EP, Exposed Pad	SW-120-4
ADSP-21568WCBCZ10	1 GHz	2 MB	–40°C to +125°C	400-Ball CSP_BGA	BC-400-3
ADSP21568WCBCZ10RL	1 GHz	2 MB	–40°C to +125°C	400-Ball CSP_BGA	BC-400-3

[1] Z =RoHS compliant part.
[2] RL = Supplied on Tape and Reel.
[3] Referenced temperature is junction temperature. See Preliminary Operating Conditions for junction temperature (T_J) specification.

PLANNED PRODUCTION PRODUCTS

Model[1]	Processor Instruction Rate (Max)	L2 SRAM	Temperature Range[2]	Package Description	Package Option
ADSP-21560KSWZ8	800 MHz	1 MB	0°C to 125°C	120-Lead LQFP_EP, Exposed Pad	SW-120-4
ADSP-21561KSWZ8	800 MHz	1.5 MB	0°C to 125°C	120-Lead LQFP_EP, Exposed Pad	SW-120-4
ADSP-21561KSWZ10	1 GHz	1.5 MB	0°C to 125°C	120-Lead LQFP_EP, Exposed Pad	SW-120-4
ADSP-21564KSWZ8	800 MHz	2 MB	0°C to 125°C	120-Lead LQFP_EP, Exposed Pad	SW-120-4
ADSP-21564KSWZ10	1 GHz	2 MB	0°C to 125°C	120-Lead LQFP_EP, Exposed Pad	SW-120-4
ADSP-21568KBCZ10	1 GHz	2 MB	0°C to 125°C	400-Ball CSP_BGA	BC-400-3

[1] Z =RoHS compliant part.
[2] Referenced temperature is junction temperature. See Preliminary Operating Conditions for junction temperature (T_J) specification.

PRE RELEASE PRODUCTS

Model[1]	Processor Instruction Rate (Max)	Temperature Range[2, 3]	Package Description	Package Option
ADSP-21560-SWZENG	800 MHz	N/A	120-Lead LQFP_EP, Exposed Pad	SW-120-4
ADSP-21564-SWZENG	1 GHz	N/A	120-Lead LQFP_EP, Exposed Pad	SW-120-4
ADSP-21568-BCZENG	1 GHz	N/A	Pad 400-Ball CSP_BGA	BC-400-3

[1] Z =RoHS compliant part.
[2] Referenced temperature is junction temperature. See Preliminary Operating Conditions for junction temperature (T_J) specification.
[3] N/A means not applicable.

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).