ADPL20502

600mV to 5.5V Input, 2A Boost Converter with True Shutdown

FEATURES

- 500nA Quiescent Supply Current from Output
- Output Short-Circuit Protection
- True Shutdown Mode
  - 1nA Shutdown Current
  - Output Disconnects from Input
  - No Reverse-Current with Any Voltage on V_{OUT}
- 96% Peak Efficiency, 90% or Higher at 500µA
- Typical 800mA Output Current at 5.0V (V_{IN} = 3.0V)
- 600mV to 5.5V Input Range, Up to 5.35V in Regulation
- 900mV Minimum Startup Voltage
- Single Resistor-Adjustable Output Voltage
  - 2.3V to 5.2V Output Voltage Range with 100mV Steps
  - 5.5V Output Voltage Setting Available
- 2A Peak Inductor Current Limit
- Thermal Shutdown Protection
- Multiple Package Options
  - 1.58mm x 0.89mm, 0.4mm Pitch, 6-Bump (3 x 2) WLP
  - 2mm x 2mm, 8-Pin TDFN
- -40°C to +125°C Operating Temperature Range

GENERAL DESCRIPTION

The **ADPL20502®** is a boost converter capable of delivering a peak inductor current up to 2A with True Shutdown™, cycle-by-cycle inductor current limit, short circuit, and thermal protection. During shutdown, only 1nA is drawn from the input pin. The ADPL20502 offers ultra-low quiescent current, small total solution size, and operates at a high efficiency throughout the load and line range. The ADPL20502 is ideal for battery-powered applications where long battery life is a must and high efficiency is required at all power levels.

The ADPL20502 utilizes an adjustable on-time, pulse-frequency modulation (PFM) control scheme that consumes ultra-low quiescent current. The ADPL20502 features True Shutdown mode where the output disconnects from the input with no forward or reverse-current. This saves precious energy from the battery for systems that dynamically turn on and off by having the ability to startup into a precharged output capacitor.

The ADPL20502 is offered in a space-saving and cost effective 1.58mm x 0.89mm, 6-bump WLP (3 x 2, 0.4mm pitch) and 8-pin, 2mm x 2mm TDFN packages. The operating temperature range is from -40°C to +125°C.

APPLICATIONS

- Consumer: WiFi Module, Near-Band IoT, Wearable audio
- Industrial: Emergency Lighting, IoT Sensors
- Medical: Clinical Instrumentation

SIMPLIFIED APPLICATION DIAGRAM

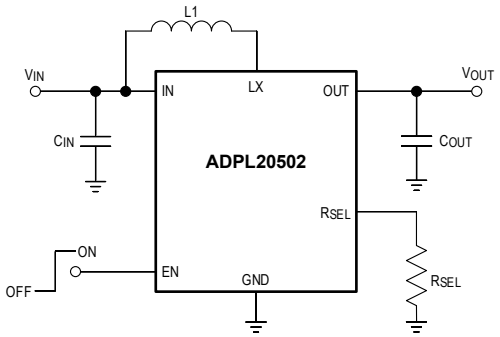

Figure 1. Simplified Application Diagram

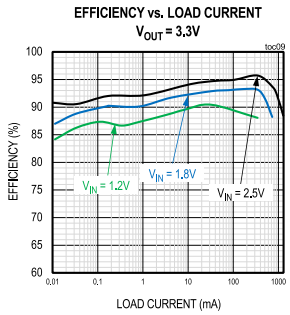

Figure 2. Efficiency vs. Load Current (Figure 5 Circuit)

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REVISION HISTORY

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	12/23	Initial Release	-

SPECIFICATIONS

Table 1. Electrical Characteristics

(V_{IN} = 1.5V, R_{SEL} = 191kΩ, V_{OUT} = 3.3V, T_J = -40°C to +125°C, typical values are at T_J = +25°C, C_{IN} = 22µF, C_{OUT} = 22µF, unless otherwise noted.) (1)

PARAMETER	SYMBOL	CONDITIONS/COMMENTS		MIN	TYP	MAX	UNITS
Minimum Input Voltage	V_{IN_MIN}	Runs from output after startup, I_{OUT} = 1mA			600		mV
Input Voltage Range	V_{IN}	Guaranteed by LX Maximum On-Time, $V_{OUT} > V_{IN}$ + 150mV while in regulation		0.95		5.5	V
Minimum Startup Input Voltage	V_{IN_START}	$R_L \geq 3k\Omega$, *Typical Application Circuit*, T_J = +25°C			0.9	0.95	V
Output Voltage Range	V_{OUT_RANGE}	See . For $V_{IN} < V_{OUT}$ target. (2)		2.3		5.5	V
Output Accuracy, LPM	V_{ACC_LPM}	V_{OUT} Falling (3)		-1.2		+1.2	%
Output Accuracy, ULPM	V_{ACC_ULPM}	V_{OUT} Rising, when LX stops switching (4)		+1.5	+2.7	+4.6	%
DC Load Regulation	ACC_{LOAD}	Load from 20mA to I_{OUT} at 80% of Peak Inductor Current			-1.2		%
DC Line Regulation	ACC_{LINE}	Duty Cycle varied from 25% to Maximum			-1.2		%
Input Shutdown Current	I_{SD_IN}	V_{EN} = 0V, V_{OUT} = 0V, T_J = +25°C			1	120	nA
Quiescent Supply Current Into IN	I_{Q_IN}	$V_{EN} = V_{IN}$, not switching, V_{OUT} = 105% of target voltage, T_J = +25°C, R_{SEL} = Open			15		nA
Quiescent Supply Current Into OUT	I_{Q_OUT}	$V_{EN} = V_{IN}$, not switching, V_{OUT} = 105% of target voltage, T_J = +25°C, R_{SEL} = Open			500	800	nA
Maximum LX On-Time	t_{ONMAX}	T_J = -40°C to +125°C		1.0	1.75	2.2	µs
LX On-Time in CCM	$t_{ON\_1.2V}$	V_{IN} = 1.2V	T_J = +25°C	580	620	660	ns
			T_J = -40°C to +125°C	500	620	740	
	$t_{ON\_3.0V}$	V_{IN} = 3.0V	T_J = +25°C	240	300	360	
LX Maximum Duty Cycle	DC	R_{SEL} = 10kΩ, V_{IN} = 1.2V, T_J = +25°C (5)		80	86		%
		R_{SEL} = 10kΩ, V_{IN} = 1.2V (5)		74	86		
		R_{SEL} = 191kΩ, V_{IN} = 3.0V (5)		65	75		
LX Leakage Current	I_{LEAK_LX}	$V_{LX} = V_{IN}$ = 5.5V, $V_{OUT} = V_{EN}$ = 0V	T_J = +25°C		1	100	nA
IN Current Limit	I_{IN_PT}	$V_{IN} = V_{EN}$ = 3.3V, V_{OUT} = 2.3V			1.1		A
	I_{PEAK_LX}	V_{OUT} = 3.3V, (6)	T_J = +25°C	1.9	2.0	2.1	A

(V_{IN} = 1.5V, R_{SEL} = 191kΩ, V_{OUT} = 3.3V, T_J = -40°C to +125°C, typical values are at T_J = +25°C, C_{IN} = 22µF, C_{OUT} = 22µF, unless otherwise noted.) ([1])

PARAMETER	SYMBOL	CONDITIONS/COMMENTS		MIN	TYP	MAX	UNITS
Inductor Peak Current Limit		V_{OUT} = 3.3V	T_J = -40°C to +125°C	1.8	2.0	2.2	
High-Side R_{DSON}	R_{DS_H}	V_{OUT} = 3.3V			105	175	mΩ
Low-Side R_{DSON}	R_{DS_L}	V_{OUT} = 3.3V			55	100	mΩ
Zero Crossing Threshold	I_{ZX_LX}	([6])		25	50	75	mA
Soft Start Rate	t_{SS_RATE}	Target V_{OUT} = 5.0V			3		V/ms
Enable Input Leakage	I_{LEAK_EN}	T_J = +25°C, V_{EN} = 5.5V			0.3	100	nA
Enable Voltage Threshold	V_{EN_IH}	V_{EN} Rising, LX begins switching			0.6	0.95	V
	V_{EN_IL}	V_{EN} Falling, LX stops switching		0.15	0.55		
Required Select Resistor Accuracy	ACC_{RSEL}	Note: Use the resistor from *Table 4*.		-1		+1	%
Select Resistor Detection Time	t_{RSEL}	C_{RSEL} < 2pF ([7])		240	600	1320	µs
Thermal Shutdown Threshold	T_{SHUT}	OUT disabled	T_J Rising		165		°C
			T_J Falling		150		

1 Limits over the specified operating temperature and supply voltage range are guaranteed by design and characterization, and production tested at room temperature only.

2 Guaranteed by the Required Select Resistor Accuracy parameter.

3 Output Accuracy in Low-Power mode when $I_{OUT} > I_{OUT\_TRANSITION}$ and inductor current is not in Continuous Conduction mode. This accuracy does not include load, line, or ripple.

4 Output Accuracy in Ultra-Low-Power mode when $I_{OUT} < I_{OUT\_TRANSITION}$. This accuracy does not include load, line, or ripple.

5 Guaranteed by measuring LX frequency and duty cycle. Maximum duty cycle is a function of input voltage since LX on time varies with V_{IN}.

6 This is static measurement. The actual peak current limit depends on V_{IN} and L due to propagation delays.

7 This is the time required to acquire the R_{SEL} value. This time adds to the startup time.

ABSOLUTE MAXIMUM RATINGS

Table 2. Absolute Maximum Ratings

PARAMETER	RATING
IN, EN, RSEL, OUT to GND	-0.3V to +6V
LX RMS Current	$-1.6A_{RMS}$ to $+1.6A_{RMS}$
IN RMS Current	$-0.8A_{RMS}$ to $+0.8A_{RMS}$
LX to GND	-0.3V to (V_{OUT} + 0.3V) ([1])
Output Short-Circuit Duration	Continuous
Continuous Power Dissipation - WLP (T_A = +70°C) (Derate 10.51mW/°C above +70°C)	840mW
Continuous Power Dissipation - TDFN (T_A = +70°C) (Derate 11.7mW/°C above 70°C)	937.9mW
Operating Junction Temperature Range	-40°C to +125°C
Maximum Junction Temperature	+150°C
Storage Temperature Range	-65°C to +150°C

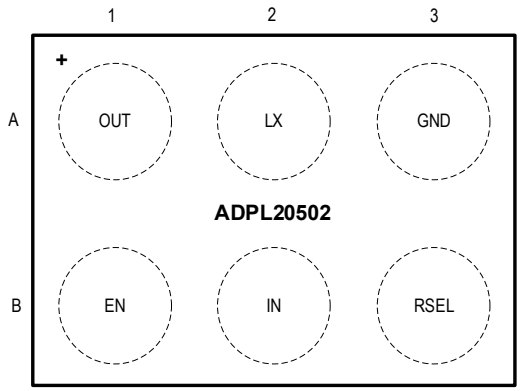
[1] LX pin has internal clamps to GND and OUT. These diodes may be forward biased during switching transitions. During these transitions, the max LX current should be within the Max RMS Current rating for safe operation.

Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

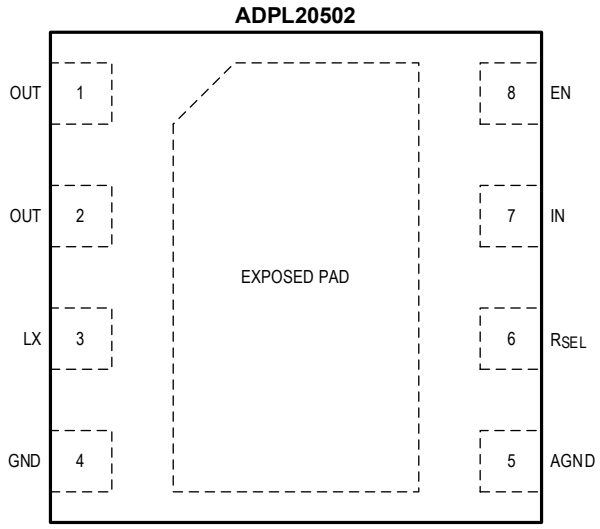
Pin Configurations

WLP



TOP VIEW

TDFN



TOP VIEW

Pin Descriptions

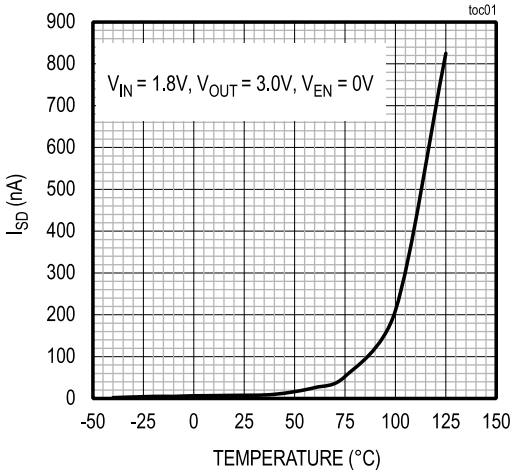
Table 3. Pin Descriptions

PIN		NAME	DESCRIPTION
WLP	TDFN		
A1	1, 2	OUT	Output Pins. Connect a 22µF X7R ceramic capacitor to ground.
A2	3	LX	Switching Node. Connect a 1.0µH inductor from LX to IN.
A3	4	GND	Power Ground Pin. Connect to GND. In the TDFN package, applications connect to the exposed pad (EP) externally in the PCB layout at a single point.
—	5	AGND	Analog Ground Pin. Connect to the EP externally in the PCB layout at a single point.
B3	6	RSEL	Output Voltage Select Pin. Connect a resistor from RSEL to GND based on the desired output voltage. See *Table 4*. RSEL floats in shutdown. Care must be taken that the total capacitance on this pin should be less than 2pF. See *PCB Layout Guidelines* for more information.
B2	7	IN	Input Pin. Connect a 22µF X7R ceramic capacitor to ground. Depending on the specific application requirements, more capacitance may be needed.
B1	8	EN	Enable Input Pin. Force this pin to larger than 0.6V to enable the boost converter. Force this pin below 0.55V to disable the part and enter the True Shutdown mode.
—	EP	EP	Exposed Pad. Connect the EP to GND. Functionally connected to AGND. Connect the GND and AGND pins to EP externally in the PCB layout with short traces under the device.

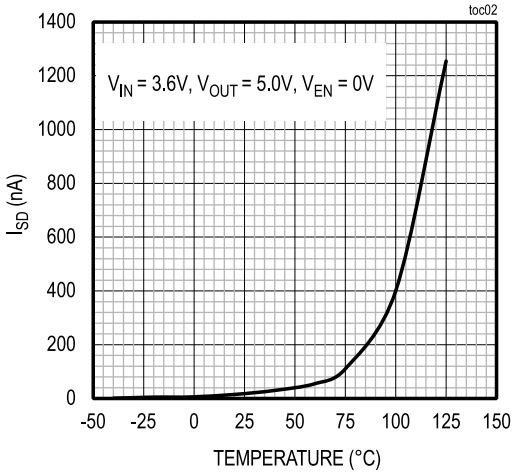
TYPICAL OPERATING CHARACTERISTICS

(ADPL20502AANT+, IN = 1.5V, OUT = 3.3V, L = 1.0µH, C_{IN} = 22µF, C_{OUT} = 22µF, T_A = +25°C, unless otherwise noted.)

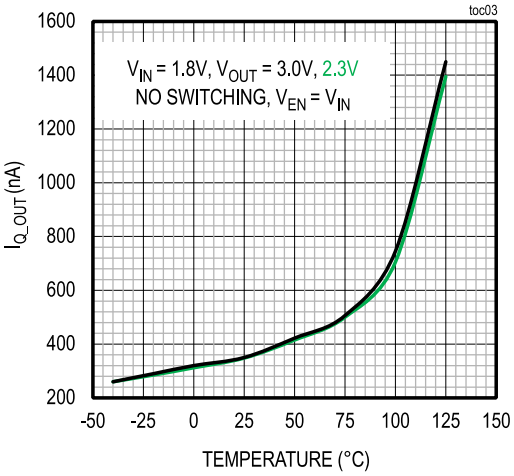
TOTAL SYSTEM SHUTDOWN CURRENT vs.TEMPERATURE



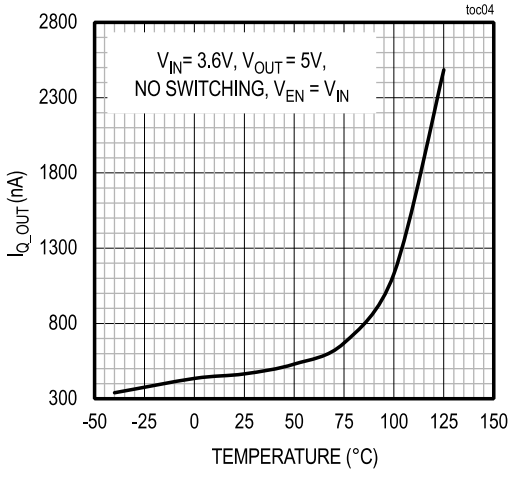
TOTAL SYSTEM SHUTDOWN CURRENT vs.TEMPERATURE



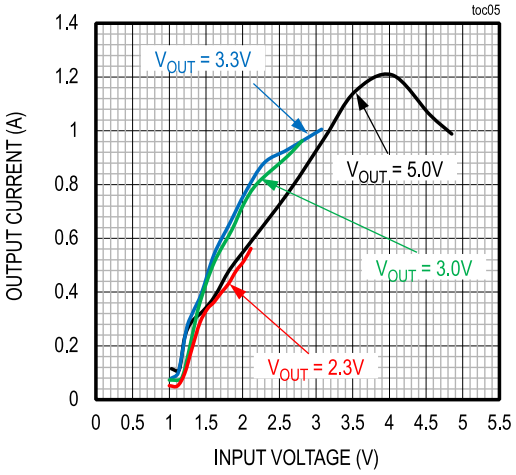
QUIESCENT SUPPLY CURRENT INTO OUT PIN vs.TEMPERATURE



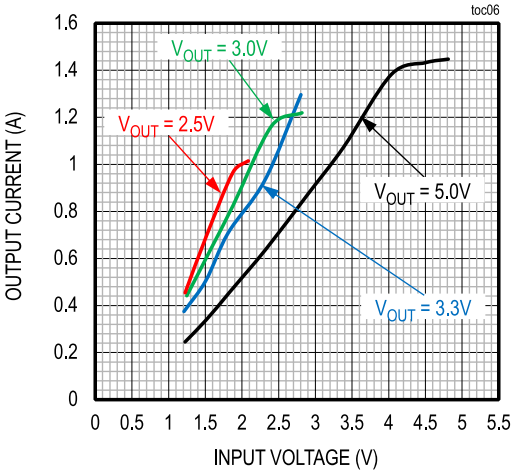
QUIESCENT CURRENT INTO OUT PIN vs.TEMPERATURE



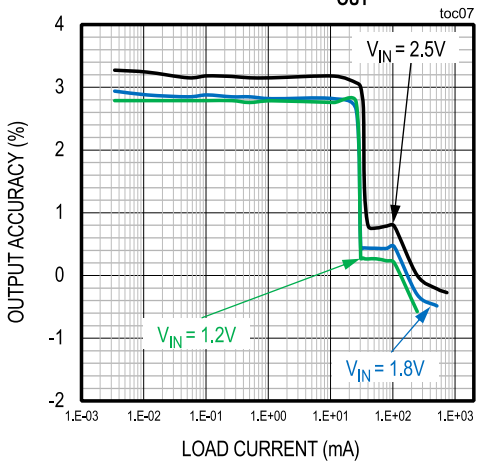
MAXIMUM OUTPUT CURRENT DURING STARTUP vs. INPUT VOLTAGE



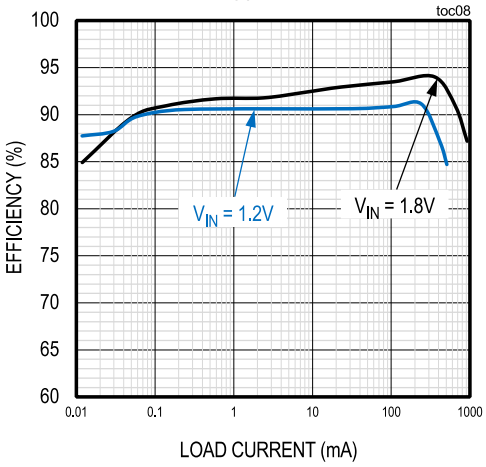
MAXIMUM OUTPUT CURRENT AT STEADY STATE vs. INPUT VOLTAGE



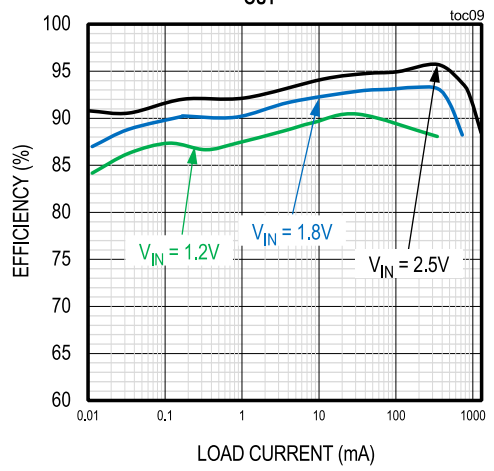
OUTPUT VOLTAGE ACCURACY vs. LOAD CURRENT AT V_{OUT} = 3.3V



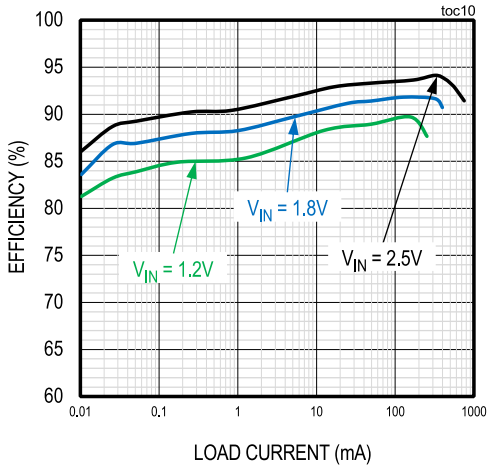
EFFICIENCY vs. LOAD CURRENT V_{OUT} = 2.3V



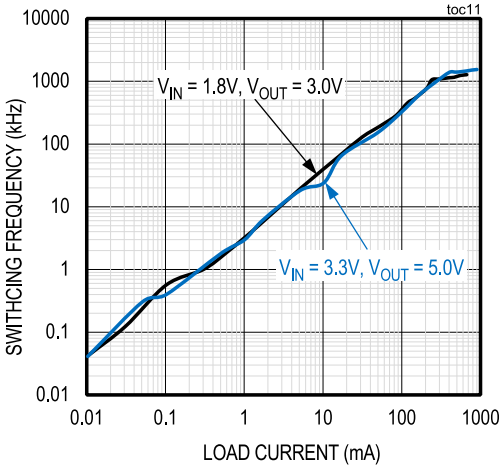
EFFICIENCY vs. LOAD CURRENT
V_{OUT} = 3.3V



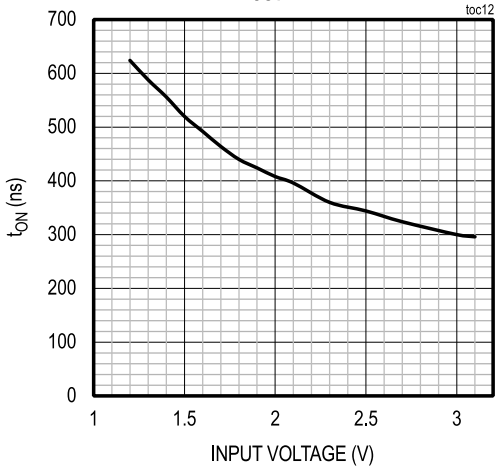
EFFICIENCY vs. LOAD CURRENT
VOUT = 5.0V



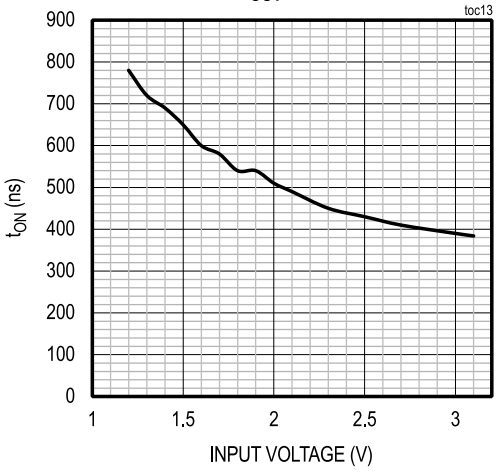
SWITCHING FREQUENCY vs.
LOAD CURRENT



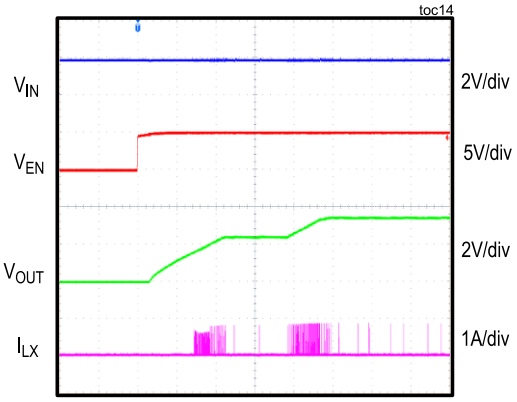
ON-TIME vs. INPUT VOLTAGE IN CCM
V_{OUT} = 3.3V



ON-TIME vs. INPUT VOLTAGE IN DCM
V_{OUT} = 3.3V

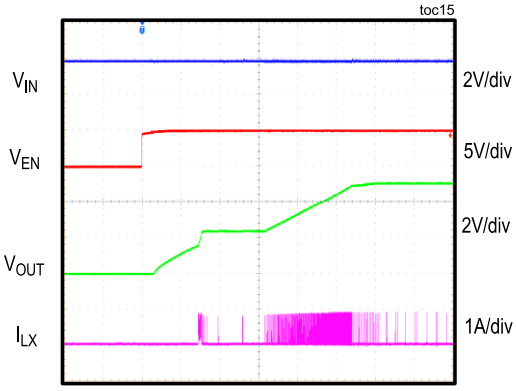


STARTUP



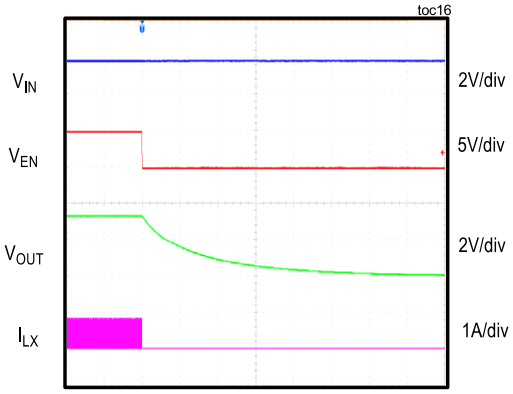
V_{IN} = 1.8V, V_{OUT} = 3.3V, R_{LOAD} = 3kΩ
400µs/div

STARTUP



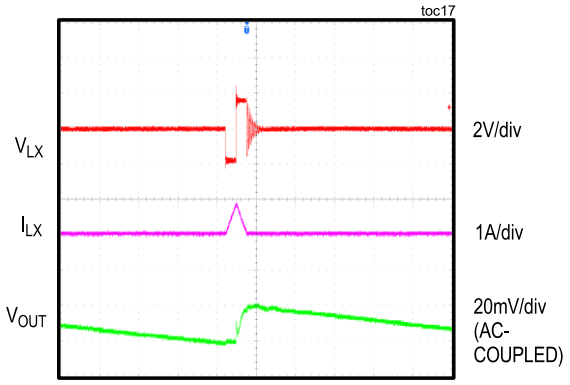
V_{IN} = 1.8V, V_{OUT} = 5.0V, R_{LOAD} = 3kΩ
400µs/div

POWERDOWN



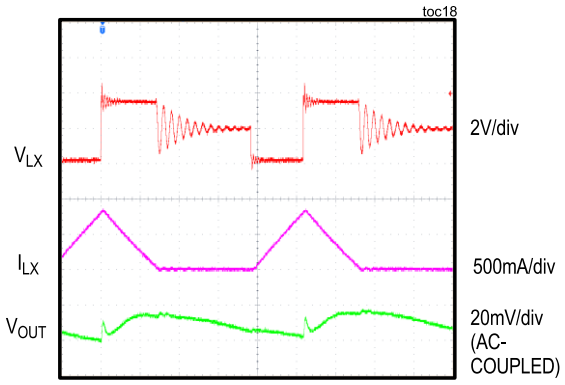
V_{IN} = 1.8V, V_{OUT} = 3.3V, R_{LOAD} = 3kΩ
40ms/div

ULTRA LIGHT-LOAD SWITCHING



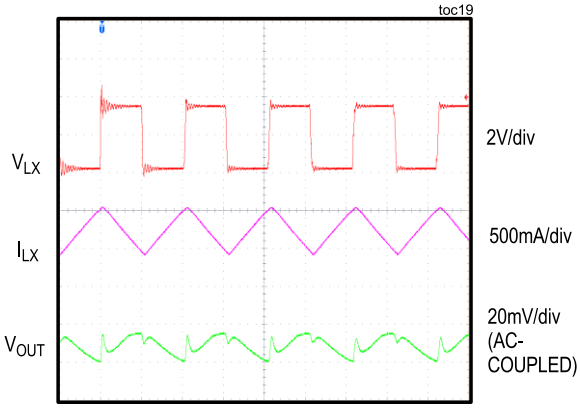
V_{IN} = 1.8V, V_{OUT} = 3.3V, I_{OUT} = 10mA
2µs/div

LIGHT-LOAD SWITCHING



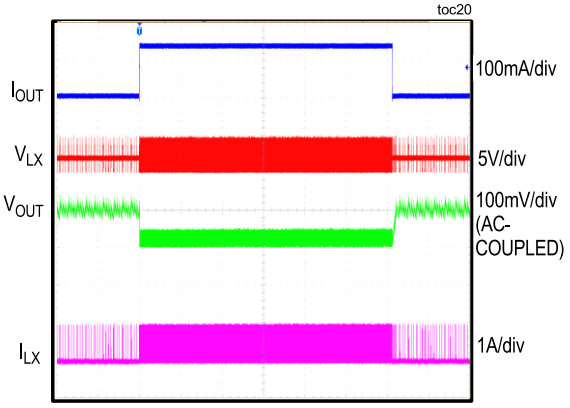
V_{IN} = 1.8V, V_{OUT} = 3.3V, I_{OUT} = 100mA
400ns/div

HIGH LOAD SWITCHING

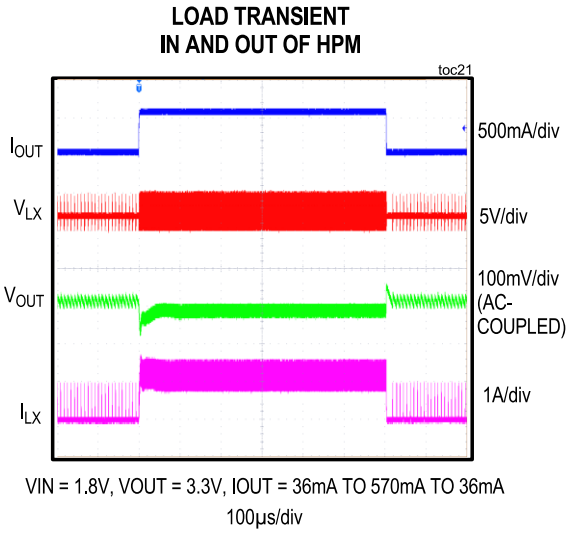


V_{IN} = 1.8V, V_{OUT} = 3.3V, I_{OUT} = 350mA
400ns/div

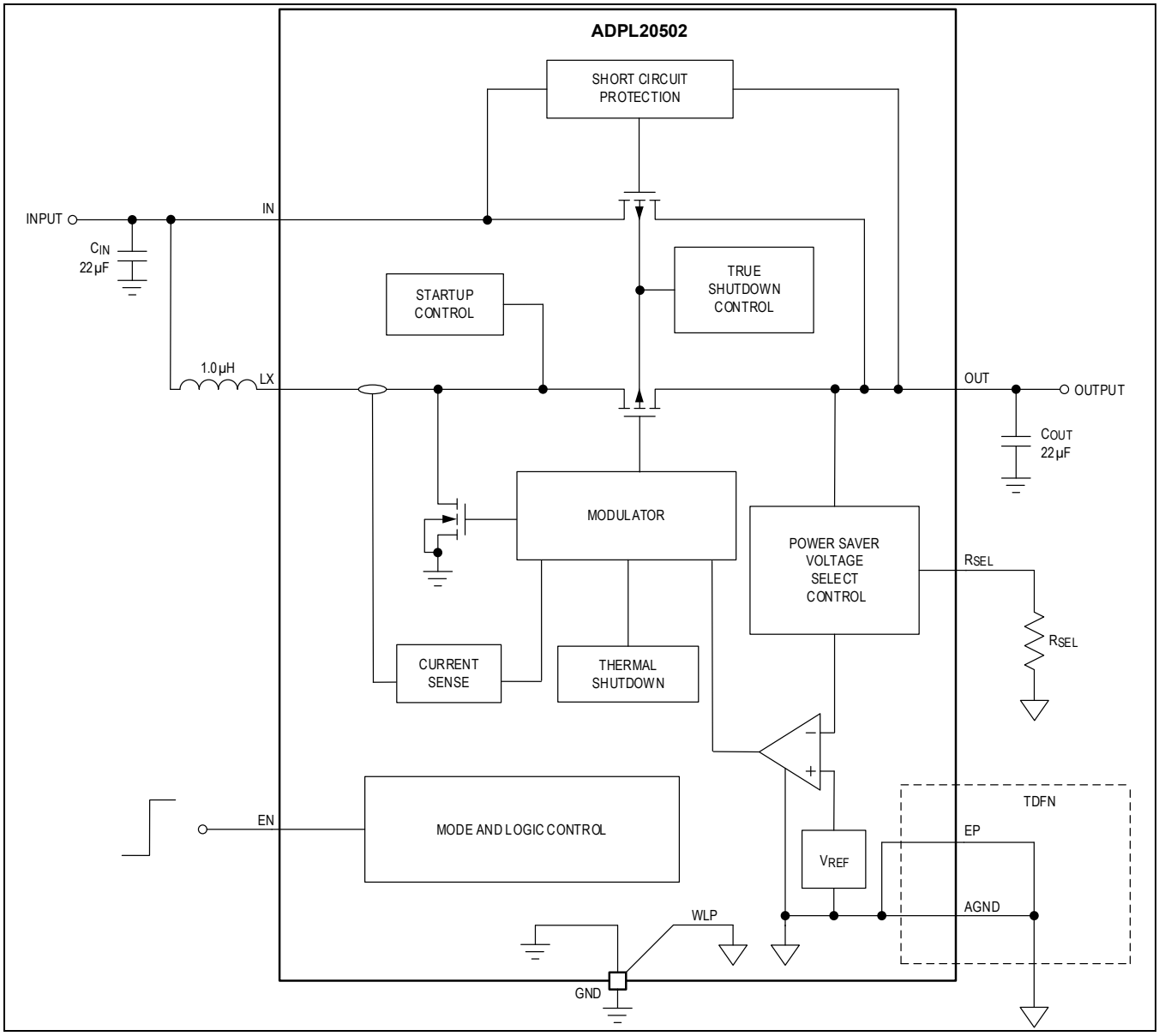
LOAD TRANSIENT IN AND OUT OF LPM



V_{IN} = 1.8V, V_{OUT} = 3.3V, I_{OUT} = 10mA TO 120mA TO 10mA
800µs/div


LOAD TRANSIENT
IN AND OUT OF HPM
toc21
IOUT
VLX
VOUT
ILX
500mA/div
5V/div
100mV/div
(AC-
COUPLED)
1A/div
VIN = 1.8V, VOUT = 3.3V, IOUT = 36mA TO 570mA TO 36mA
100µs/div

FUNCTIONAL DIAGRAMS



DETAILED DESCRIPTION

The ADPL20502 is an ultra-low I_Q synchronous step-up converter optimized for battery-powered systems requiring long battery running time, high efficiency across wide load range, and small solution size. The device can operate across a wide input voltage ranging from 0.6V to 5.5V. The ADPL20502 consumes only 500nA of current, output referred while in regulation. The output voltage is programmed in the range between 2.3V to 5.2V with 100mV resolution using a single resistor connected from the RSEL pin to ground. 5.4V and 5.5V output target levels are available. However, the device does not support ultra-low-power mode when the target output voltage is either 5.4V or 5.5V.

The ADPL20502 utilizes an adaptive on-time PFM control scheme that allows ultra-low quiescent current and high efficiency over a wide output current range. The peak inductor current is set by on-time or by cycle-by-cycle 2A current limit. The device provides the True Shutdown feature where the load is completely disconnected from the input minimizing leakage current. The ADPL20502 features short-circuit and thermal protection.

Control Scheme

The ADPL20502 boost converter is controlled by a unique, adaptive on-time pulse frequency modulation scheme that allows very high-efficiency operation across full load current range. The ADPL20502 automatically switches between the Ultra-Low-Power mode (ULPM), Low-Power mode (LPM) and High-Power mode (HPM) of operation, depending on the load current. *Figure 3* and *Figure 4* show typical waveforms while in each mode. On-time is a function of V_{IN} with typical performance shown in *Typical Operating Characteristics*.

The output voltage is regulated 2.7% higher while in ULPM (V_{ACC_ULPM}). This reduces the effective skip frequency, significantly improving the system's efficiency. In addition, operating marginally above the regulation threshold, the device has an excellent transient response when a large load transient event occurs. The device will typically be in ULPM when the system is in standby state. Once the output voltage exceeds the ULPM regulation level, the device will go into sleep mode, consuming very low quiescent current. It will wake up to resume switching when the output voltage falls below the threshold. While in this mode, the device will regulate output while consuming only 500nA of current. Such a low current consumption translates into great performance, achieving 90% efficiency at 10µA load current.

The ADPL20502 will transition to LPM once the load current is high enough that it forces the device to switch faster than 17µs. The load current level at which this transition happens is a function on the operating condition and component selection. The user can calculate the value of the load current where ULPM transitions to LPM using the equation below:

$$I_{OUT\_TRANSITION} = \left(\frac{(t_{ON})^2}{2 \times L}\right) \times \left(\frac{V_{IN}}{\frac{V_{OUT}}{V_{IN}} - 1}\right) \times \left(\frac{n}{17\mu s}\right)$$

For example, for V_{IN} = 1.2V, V_{OUT} = 3V and L = 1.0µH, assuming 85% efficiency the UPLM to LPM transition current happens at approximately 11.3mA.

The ADPL20502 enters HPM when the inductor current transitions from DCM to CCM. The inductor current ripple will be reduced in the CCM operation in order to assure proper mode transitions. The voltage is regulated by an error amplifier that compares the output voltage to the internal reference and adjusts inductor current accordingly achieving great load regulation performance of 1.2%.

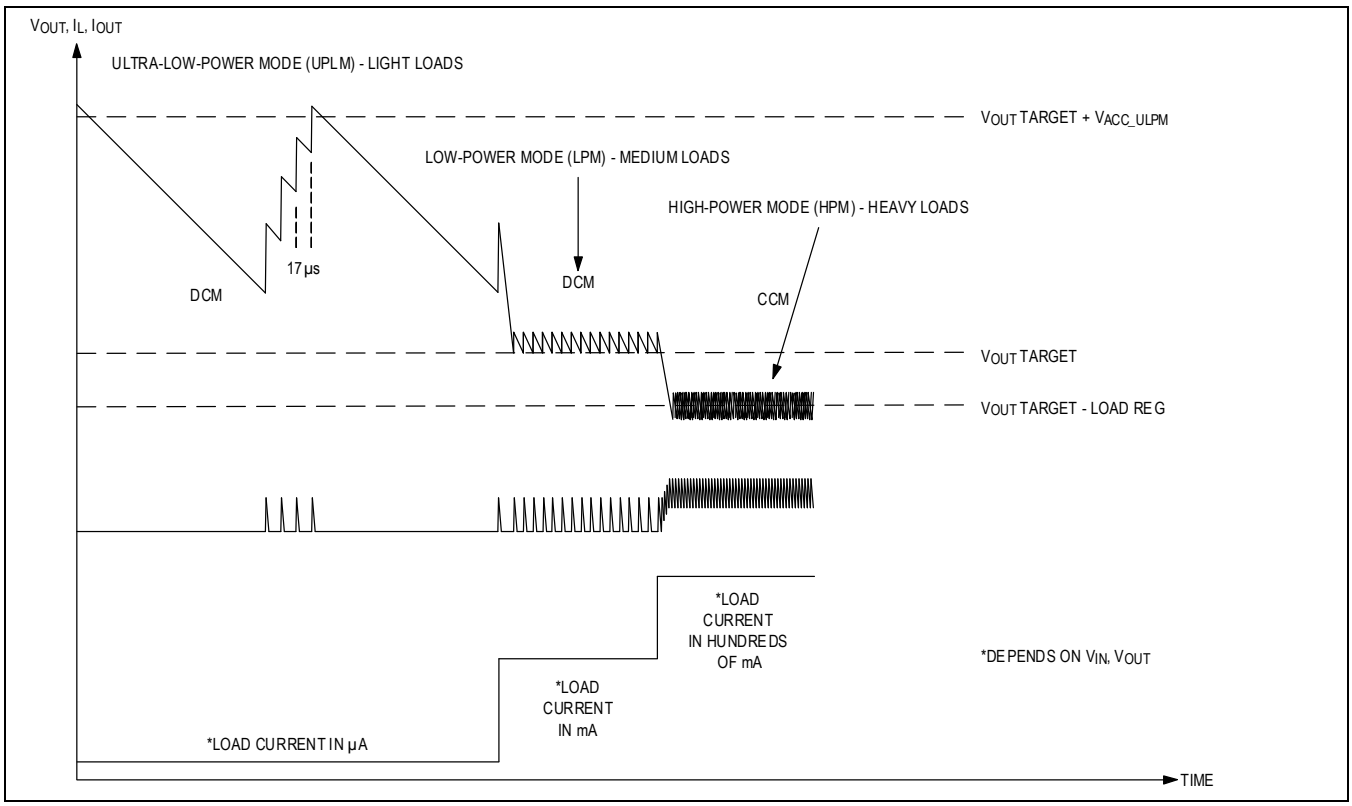


Figure 3. ULPM, LPM, HPM Transition Waveforms

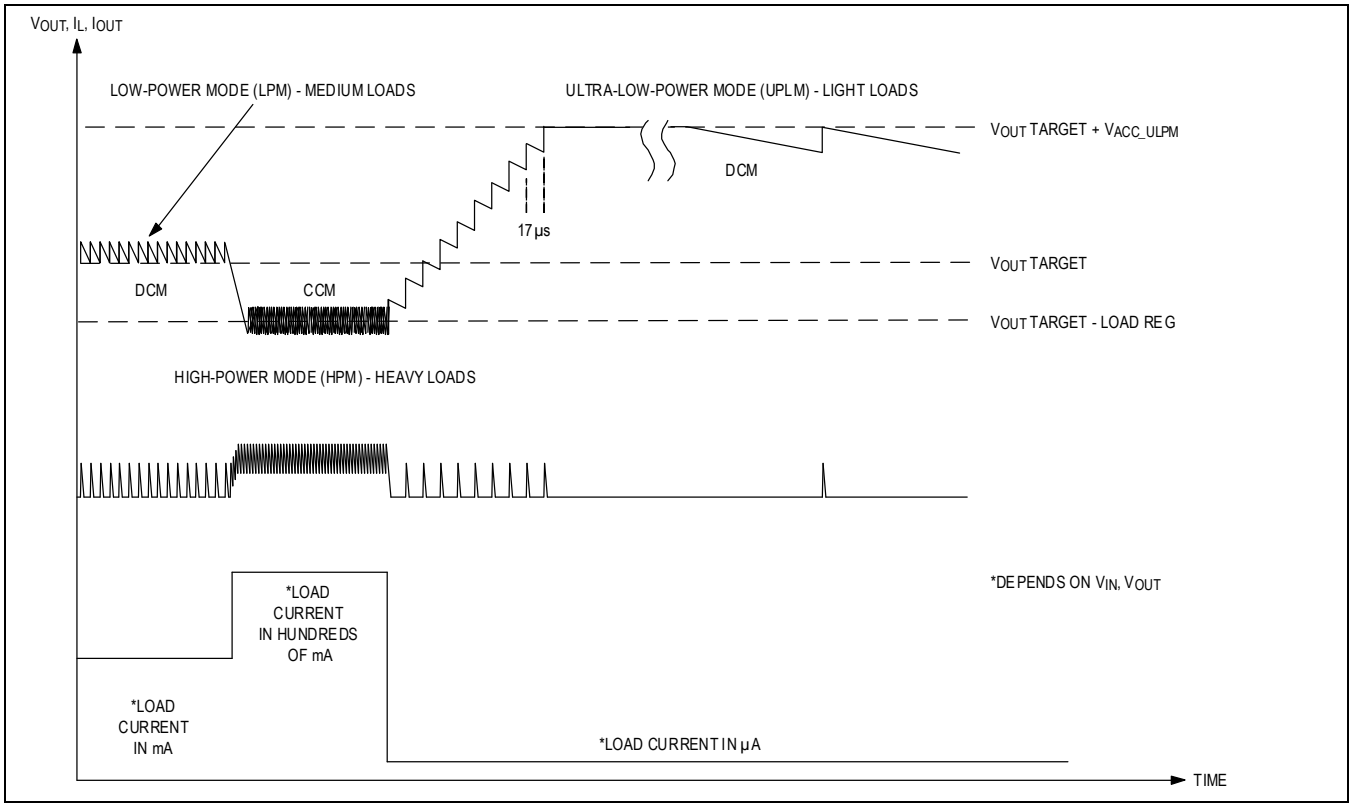


Figure 4. LPM, HPM, ULPM Transition Waveforms

Output Voltage Selection

The ADPL20502 has a unique single resistor output selection method where one can select 32 different voltage selections from 2.3V to 5.5V, as shown in *Table 4*.

At startup, the ADPL20502 sources up to 200µA during the select resistor detection time, typically for 600µs (tRSEL), to read the R_{SEL} value.

Care must be taken that the total capacitance on this pin should be less than 2pF. See *PCB Layout Guidelines* for more information.

The R_{SEL} output voltage selection method has many benefits:

- In conventional boost converters, current is drawn from output continuously through a feedback resistor-divider. In the ADPL20502, 200µA current is drawn from output only during startup, which helps to increase efficiency at light loads.
- Lower cost and smaller size, since only one resistor is needed versus the two resistors needed in typical feedback connections.
- The R_{SEL} feature allows customers to stock just one part in their inventory system and use it in multiple projects with different output voltages just by changing a single standard 1% resistor.
- The R_{SEL} feature allows much higher internal feedback resistors instead of lower impedance external feedback resistors to enable for ultra-low-power applications.

Select the R_{SEL} resistor value by choosing the desired output voltage in the *Table 4*.

Table 4. R_{SEL} Selection Table

TARGET OUTPUT VOLTAGE VOUT (V)	RSEL STANDARD RESISTOR 1% (kΩ)
2.3	OPEN
2.4	909
2.5	768
2.6	634
2.7	536
2.8	452
2.9	383
3.0	324
3.1	267
3.2	226
3.3	191
3.4	162
3.5	133
3.6	113
3.7	95.3
3.8	80.6
3.9	66.5
4.0	56.2
4.1	47.5
4.2	40.2
4.3	34.0

4.4	28.0
4.5	23.7
4.6	20.0
4.7	16.9
4.8	14.0
4.9	11.8
5.0	10.0
5.1	8.45
5.2	7.15
5.4*	4.99
5.5*	SHORT TO GROUND

* Indicates ULPM disabled.

Fixed-Output Voltage Version

In applications where board space is at a premium, contact a Maxim Integrated representative to order fixed-output versions that don't require the R_{SEL} resistor to program the output voltage. The RSEL pin must be left floating for fixed output versions. The output voltage can be preprogrammed in the range from 2.3V to 5.2V with 100mV resolution. 5.3V, 5.4V, and 5.5V output target levels are available. The output target levels programmed to 5.3V, 5.4V, and 5.5V will have the ULPM disabled.

Features

Enable

The ADPL20502 includes an enable input pin (EN). Connect EN pin to IN pin or drive it to more than 0.6V (V_{EN_IH}) for normal operation. When EN pin goes below 0.55V (V_{EN_IL}), ADPL20502 enters True Shutdown mode. The device will consume 1nA (ISD_IN) of current from V_{IN} while in this mode.

In shutdown, the output is truly disconnected from the input. In conventional boost circuits, the body diode of the synchronous rectifier is forward biased in shutdown and allows current flow from the battery to the output. If the load cannot be shut down, a load switch is required to avoid depleting the battery during the shutdown. A proprietary design in the ADPL20502 allows the synchronous rectifier to provide True Shutdown with no additional components. True Shutdown on the ADPL20502 allows the output to be biased at any voltage or grounded without consuming any current from IN or OUT pins other than pin leakage currents.

Soft-Start Control

After the EN pin goes above its raising threshold (V_{EN_IH}), the ADPL20502 begins the startup.

When the output capacitor is fully discharged prior to the device being enabled, the startup follows the below steps:

When V_{IN} is at its final level, for example, 3V, the ADPL20502 ramps the output to the level where V_{OUT} starts approaching $V_{IN,}$ at which point switching is enabled. It then acquires the RSEL pin voltage level to determine the output target level. Then, the output is ramped up to its target voltage level, for example, 5.0V following a 3V/ms slew rate. This controls the amount of inrush current into the output capacitor.

The ADPL20502 starts with a 0.9V input voltage and a load resistance of 3kΩ or larger. Enabling the device when V_{IN} is between 0.9V and 2.0V will be load current limited. If the load current is heavy such that it does not allow the ADPL20502 to charge the output above 1.5V, the device cannot reach its output target level until V_{IN} is increased or the load current is reduced.

The ADPL20502 initiates a controlled soft start when supply voltage is applied at high dV/dt rate, for example, during installation of a fresh battery. While in regulation, if V_{IN} steps abruptly above V_{OUT} for more than 1V, the device resets. In this case, output voltage droop will be a function of the load current, output capacitance, and time required for soft-start to complete, which is typically 1.6ms.

For maximum load conditions during soft start, see the *Typical Operating Characteristics* section.

Short-Circuit Protection

The ADPL20502 is protected from an output short-circuit condition by current and thermal overload circuits. If the output voltage is detected 1V lower than the input voltage during operation, the ADPL20502 enters the short-circuit protection mode. Once the short-circuit event is detected, the synchronous rectifier and its body diode are disconnected from the output, and the short-circuit protection block gets engaged. The short-circuit current (I_{IN_PT}) is limited to 1.1A. Under this condition, the part will heat up due to high power dissipation in the short-circuit protection device, and likely enter thermal shutdown.

Thermal Shutdown

The ADPL20502 features thermal shutdown. The converter and short circuit protection device turn off when the junction temperature exceeds +165°C. Once the device cools by 15°C, the converter will resume operation. If the fault condition is not removed, the regulator will cycle on and off.

Design Procedure

Inductor Selection

It is recommended to use a 1.0µH inductor. This inductor value provides the best size and efficiency trade-off in most applications.

Input Capacitor

Input capacitors reduce current peaks from the input supply and increase efficiency. For the input capacitor, choose a ceramic capacitor because they have the lowest equivalent series resistance (ESR), smallest size, and lowest cost. Other capacitor types can be used as well but will have larger ESR. The biggest downside of ceramic capacitors is their capacitance derating with higher DC bias and, because of this, at minimum a standard 22µF ceramic capacitor is recommended at the input for all applications. For applications which use batteries that have a high source impedance greater than 1Ω, more capacitance may be needed. A good starting point is to use the same capacitance value at the input as well as output. In applications where V_{IN} is approaching V_{OUT}, more input capacitance will be required to minimize input voltage ripple.

At a minimum, a standard 22µF X7R ceramic capacitor is recommended for all applications. Due to DC bias effects the effective capacitance can be 80% lower than the nominal capacitor value. The capacitor data sheet needs to be consulted for proper DC bias, AC ripple, and temperature capacitance derating.

Output Capacitor

A 22µF ceramic capacitor is recommended for all applications. The output capacitor (C_{OUT}) is required to keep the output voltage ripple small and to ensure loop stability. C_{OUT} must have low impedance at the switching frequency. Ceramic capacitors are recommended due to their small size and low ESR. Make sure the minimum effective capacitance is 11µF over temperature, DC bias, and AC ripple capacitor data sheet specifications. Capacitors with X7R temperature characteristics typically perform well. In applications where V_{IN} is approaching V_{OUT}, more output capacitance is required to minimize the output voltage ripple.

PCB Layout Guidelines

Careful PCB layout is important, especially in DC-DC converters. Poor layout can affect the IC performance, causing electromagnetic interference (EMI) and electromagnetic compatibility (EMC) issues, ground bounce, and voltage drops, etc. Poor layout can also affect regulation and stability.

A good layout is implemented using the following rules:

- Place the inductor, input capacitor, and output capacitor close to the IC using short traces. These components carry high switching currents, and long traces act like antennas. The output capacitor placement is the most important in the PCB layout and make sure it is placed directly next to the IC. The inductor and input capacitor placement are secondary to the output capacitor's placement but should remain close to the IC.
- The connection from the bottom plate of the output capacitor and the ground pin of the device must be extremely short, as should be that of the input capacitor.
- Similarly, the top plate of output capacitor and the OUT pin of the device must be short as well.
- Minimize the surface area used for LX since this is the noisiest node.
- Keep the main power path from IN, LX, OUT, and GND as tight and short as possible.
- Route the output voltage path away from the inductor and LX_ switching node to minimize noise and magnetic interference.
- Maximize the size of the ground metal on the component side to help with thermal dissipation. Use a ground plane with several vias connecting to the component-side ground to further reduce noise interference on sensitive circuit nodes.

- Lastly, the trace used for RSEL should neither be too long nor should produce a capacitance of more than 2pF.

It is recommended to consult the **ADPL20502 Evaluation board layout**.

Thermal Considerations

In most applications, the IC does not dissipate much heat due to its high efficiency. But in applications where the IC runs at high ambient temperature with heavy loads, the heat dissipated may cause the temperature to exceed +125°C or the maximum junction temperature of the part. If the junction temperature reaches approximately +165°C (TJ Rising), the thermal-overload protection is activated. The maximum power dissipation depends on the thermal resistance of the IC package and the application circuit board.

The power dissipated (PD) in the device is:

$$P_D = P_{IN} - P_{OUT} - P_{IND}$$

where P_{IND} is power dissipated in the inductor that includes DC, AC, and core losses; P_{OUT} is power delivered to the load.

The maximum allowed power dissipation is:

$$P_{D\_MAX} = \frac{T_{JMAX} - T_A}{\theta_{JA}}$$

where (T_{JMAX} - T_A) is the temperature difference between the ADPL20502 maximum rated junction temperature (+125°C) and the surrounding ambient temperature, and θ_{JA} is the thermal resistance of the junction through the package, PCB, copper traces, and other materials to the surrounding ambient temperature.

TYPICAL APPLICATION CIRCUIT

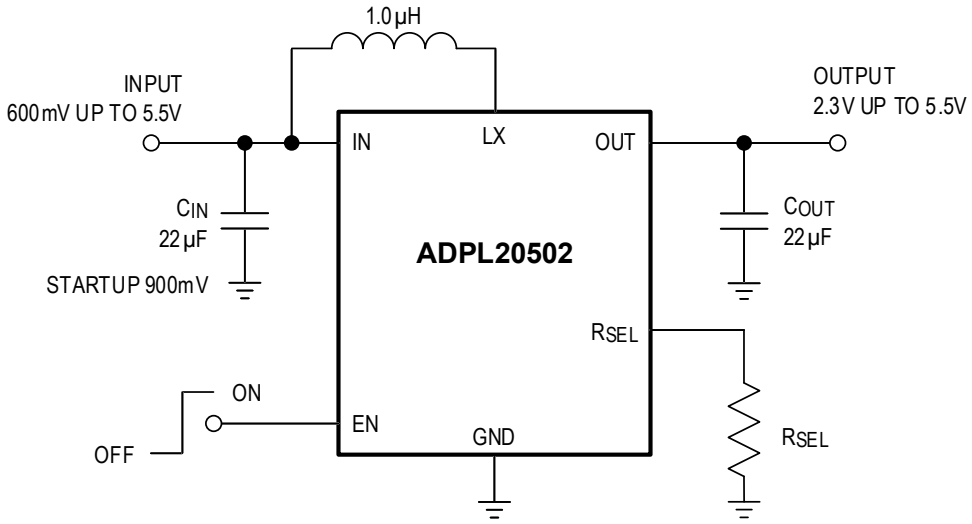


Figure 5. Typical Application Circuit

OUTLINE DIMENSIONS

Table 5. Thermal Resistance of 8 TDFN-EP

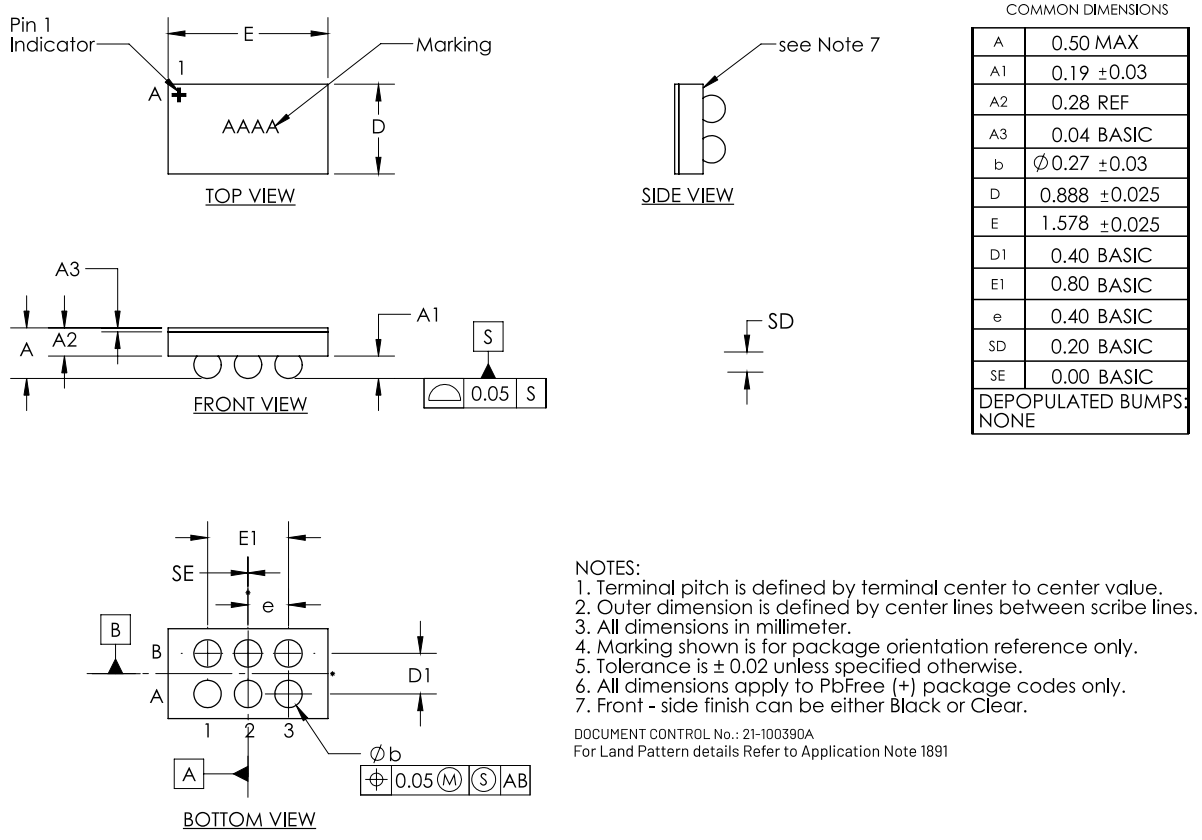
Thermal Resistance, Four-Layer Board [9]	
Junction-to-Ambient (θ_{JA})	85.3°C/W
Junction-to-Case Thermal Resistance (θ_{JC})	8.9°C/W

Table 6. Thermal Resistance of 6-bump WLP

Thermal Resistance, Four-Layer Board [9]	
Junction-to-Ambient (θ_{JA})	95.15°C/W
Junction-to-Case Thermal Resistance (θ_{JC})	N/A

[9] Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board.

PACKAGE OUTLINE 6-Bumps
THIN WLP, 0.4mm PITCH



COMMON DIMENSIONS

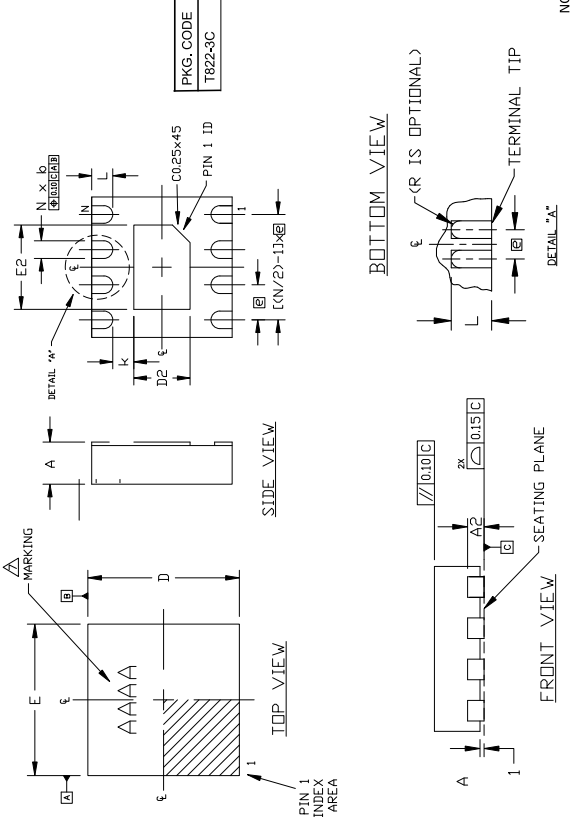
A	0.50 MAX
A1	0.19 ±0.03
A2	0.28 REF
A3	0.04 BASIC
b	∅0.27 ±0.03
D	0.888 ±0.025
E	1.578 ±0.025
D1	0.40 BASIC
E1	0.80 BASIC
e	0.40 BASIC
SD	0.20 BASIC
SE	0.00 BASIC
DEPOPULATED BUMPS: NONE	

NOTES:
1. Terminal pitch is defined by terminal center to center value.
2. Outer dimension is defined by center lines between scribe lines.
3. All dimensions in millimeter.
4. Marking shown is for package orientation reference only.
5. Tolerance is ± 0.02 unless specified otherwise.
6. All dimensions apply to PbFree (+) package codes only.
7. Front - side finish can be either Black or Clear.

DOCUMENT CONTROL No.: 21-100390A
For Land Pattern details Refer to Application Note 1891

- DRAWING NOT TO SCALE -

PACKAGE OUTLINE 8L TDFN
EXPOSED PAD, 2mm x 2mm



PKG. CODE	N	D2	E2	e	b	r	[(N/2)-1] x e
T822-3C	8	0.80±0.10	1.20±0.10	0.50 TYP.	0.25±0.05	0.125	1.50 REF

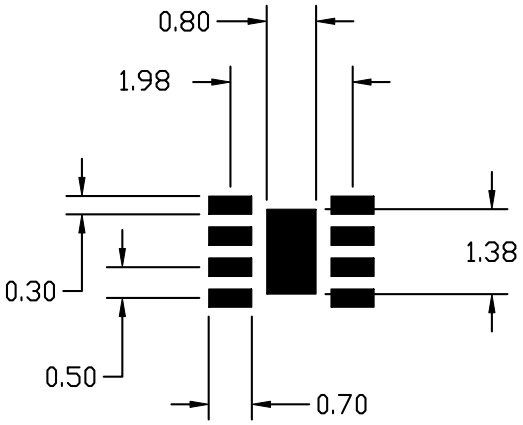
COMMON DIMENSIONS			
SYMBOL	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
D	1.90	2.00	2.10
E	1.90	2.00	2.10
A1	0.00	-	0.05
L	0.20	0.30	0.40
k		0.25 MIN.	
A2		0.20 REF.	

NOTES:
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. WARPAGE SHALL NOT EXCEED 0.08mm.
3. PACKAGE LENGTH/PACKAGE WIDTH ARE CONSIDERED AS SPECIAL CHARACTERISTIC(S).
4. COMPLIES TO JEDEC MO229 EXCEPT D2 AND E2 DIMENSIONS.
5. "N" IS THE TOTAL NUMBER OF LEADS.
6. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
7. △ MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
8. MATERIAL MUST BE COMPLIANT WITH MAXIM SPECIFICATION 10-0131 FOR SUBSTANCE CONTENT, MUST BE Eu ROHS COMPLIANT WITHOUT EXEMPTION AND PB-FREE

DOCUMENT CONTROL NO: 21-0168M

-DRAWING NOT TO SCALE-

PACKAGE LAND PATTERN
8L TDFN, 2mm x 2mm



PKG. CODE
[T822-3C]

NOTES:
1. REFERENCE PKG. OUTLINE: 21-0168
2. LAND PATTERN COMPLIES TO: IPC7351A.
3. TOLERANCE: +/- 0.02 MM.
4. ALL DIMENSIONS APPLY TO BOTH LEADED (-) AND PbFREE (+) PKG. CODES.
5. ALL DIMENSIONS IN MM.

-DRAWING NOT TO SCALE-

DOCUMENT CONTROL NO.- 90-0065E

This document (including dimensions notes & specs) is a recoomendation based on typical circuit baord manufaturing parameters. Since land pattern design depend on many factors unknown to Analog (eg. user's board manufacturing specs), user must determine sutability for use. This document is subject to change without notice. Contact technical support at https://www.analog.com/en/support/technical-support

ORDERING GUIDE

Table 7. Ordering Guide

PART NUMBER	TEMPERATURE RANGE	PIN-PACKAGE
ADPL20502AANT+	-40°C to +125°C	6-bump WLP
ADPL20502AATA+	-40°C to +125°C	8-pin TDFN

+Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape and reel.