CMOS, ±5 V/+5 V, 4 Ω, Single SPDT Switches

FEATURES

- 6.6 Ω (maximum) on resistance
- 0.8 Ω (maximum) on-resistance flatness
- 2.7 V to 5.5 V single supply
- ±2.7 V to ±5.5 V dual supply
- Rail-to-rail operation
- 8-lead SOT-23, 8-lead MSOP
- Typical power consumption (<0.1 µW)
- TTL-/CMOS-compatible inputs

APPLICATIONS

- Automatic test equipment
- Power routing
- Communication systems
- Data acquisition systems
- Sample-and-hold systems
- Avionics
- Relay replacement
- Battery-powered systems

GENERAL DESCRIPTION

The ADG619 is a monolithic CMOS single-pole double-throw (SPDT) switch. Each switch conducts equally well in both directions when the device is on.

The ADG619 offers a low on resistance of 4 Ω, which is matched to within 0.7 Ω between channels. These switches also provide low power dissipation, yet result in high switching speeds. The ADG619 exhibits break-before-make switching action, thus preventing momentary shorting when switching channels.

The ADG619 is available in an 8-lead SOT-23 and an 8-lead MSOP.

FUNCTIONAL BLOCK DIAGRAM

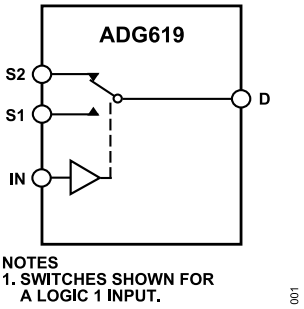

Figure 1.

PRODUCT HIGHLIGHTS

1. Low on resistance (R_{ON}): 4 Ω typical.
2. Dual ±2.7 V to ±5.5 V or single 2.7 V to 5.5 V supplies.
3. Low power dissipation.
4. Fast t_{ON}/t_{OFF}.
5. Tiny, 8-lead SOT-23 and 8-lead MSOP.

Table 1. Truth Table for the ADG619

IN	Switch S1	Switch S2
0	On	Off
1	Off	On

TABLE OF CONTENTS

REVISION HISTORY

4/2025—Rev. C to Rev. D

Deleted ADG620 (Universal) ... 1
Change to Features Section ... 1
Changes to General Description Section ... 1
Changes to Table 2 ... 3
Changes to Table 3 ... 4
Deleted Figure 20; Renumbered Sequentially ... 10
Changes to Ordering Guide ... 12

SPECIFICATIONS

DUAL SUPPLY

V_{DD} = +5 V ± 10%, V_{SS} = −5 V ± 10%, GND = 0 V. All specifications −40°C to +85°C, unless otherwise noted.

Table 2.

Parameter	B Version[1] +25°C	B Version[1] −40°C to +85°C	Unit	Test Conditions/Comments
ANALOG SWITCH				
Analog Signal Range		V_{SS} to V_{DD}	V	V_{DD} = +4.5 V, V_{SS} = −4.5 V
On Resistance (R_{ON})	4		Ω typ	V_S = ±4.5 V, I_{DS} = −10 mA; see Figure 15
	6.6	8.6	Ω max	
R_{ON} Match Between Channels (ΔR_{ON})	0.7		Ω typ	V_S = ±4.5 V, I_{DS} = −10 mA
	1.2	1.45	Ω max	
On-Resistance Flatness ($R_{FLAT (ON)}$)	0.7	0.8	Ω typ	V_S = ±3.3 V, I_{DS} = −10 mA
	1.5	1.6	Ω max	
LEAKAGE CURRENTS				V_{DD} = +5.5 V, V_{SS} = −5.5 V
Source Off Leakage, I_S (Off)	±0.01		nA typ	V_S = ±4.5 V, V_D = ∓ 4.5 V; see Figure 17
	±0.25	±1	nA max	
Channel On Leakage, I_D, I_S (On)	±0.01		nA typ	V_S = V_D = ±4.5 V; see Figure 17
	±0.25	±1	nA max	
DIGITAL INPUTS				
Input High Voltage, V_{INH}		2.4	V min	
Input Low Voltage, V_{INL}		0.8	V max	
Input Current, I_{INL} or I_{INH}	0.005		μA typ	V_{IN} = V_{INL} or V_{INH}
		±0.1	μA max	
Digital Input Capacitance, C_{IN}	2		pF typ	
DYNAMIC CHARACTERISTICS[2]				
t_{ON}	80		ns typ	R_L = 300 Ω, C_L = 35 pF
	120	155	ns max	V_S = 3.3 V; see Figure 18
t_{OFF}	45		ns typ	R_L = 300 Ω, C_L = 35 pF
	75	90	ns max	V_S = 3.3 V; see Figure 18
Break-Before-Make Time Delay, t_{BBM}	40		ns typ	R_L = 300 Ω, C_L = 35 pF
		10	ns min	V_{S1} = V_{S2} = 3.3 V; see Figure 19
Charge Injection	110		pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 1 nF; see Figure 20
Off Isolation	−67		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 21
Channel-to-Channel Crosstalk	−67		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 22
Bandwidth −3 dB	190		MHz typ	R_L = 50 Ω, C_L = 5 pF; see Figure 23
C_S (Off)	25		pF typ	f = 1 MHz
C_D, C_S (On)	95		pF typ	f = 1 MHz
POWER REQUIREMENTS				V_{DD} = +5.5 V, V_{SS} = −5.5 V
I_{DD}	0.001		μA typ	Digital inputs = 0 V or 5.5 V
		1.0	μA max	
I_{SS}	0.001		μA typ	Digital inputs = 0 V or 5.5 V
		1.0	μA max	

[1] Temperature range for B version is −40°C to +85°C.

[2] Guaranteed by design, not subject to production test.

SPECIFICATIONS

SINGLE SUPPLY

V_{DD} = 5 V ± 10%, V_{SS} = 0 V, GND = 0 V. All specifications −40°C to +85°C, unless otherwise noted.

Table 3.

Parameter	B Version[1] +25°C	B Version[1] −40°C to +85°C	Unit	Test Conditions/Comments
ANALOG SWITCH				
Analog Signal Range		0 V to V_{DD}	V	V_{DD} = 4.5 V, V_{SS} = 0 V
On Resistance (R_{ON})	7		Ω typ	V_S = 0 V to 4.5 V, I_{DS} = −10 mA; see Figure 15
	11	13.5	Ω max	
R_{ON} Match Between Channels (ΔR_{ON})	0.8		Ω typ	V_S = 0 V to 4.5 V, I_{DS} = −10mA
	1.2	1.45	Ω max	
On-Resistance Flatness ($R_{FLAT (ON)}$)	0.5	0.5	Ω typ	V_S = 1.5 V to 3.3 V, I_{DS} = −10 mA
		1.5	Ω max	
LEAKAGE CURRENTS				V_{DD} = 5.5 V
Source Off Leakage, I_S (Off)	±0.01		nA typ	V_S = 1 V/4.5 V, V_D = 4.5 V/1 V; see Figure 17
	±0.25	±1	nA max	
Channel On Leakage, I_D, I_S (On)	±0.01		nA typ	V_S = V_D = 1 V/4.5 V; see Figure 17
	±0.25	±1	nA max	
DIGITAL INPUTS				
Input High Voltage, V_{INH}		2.4	V min	
Input Low Voltage, V_{INL}		0.8	V max	
Input Current, I_{INL} or I_{INH}	0.005		μA typ	V_{IN} = V_{INL} or V_{INH}
		±0.1	μA max	
Digital Input Capacitance, C_{IN}	2		pF typ	
DYNAMIC CHARACTERISTICS[2]				
t_{ON}	120		ns typ	R_L = 300 Ω, C_L = 35 pF
	220	280	ns max	V_S = 3.3 V; see Figure 18
t_{OFF}	50		ns typ	R_L = 300 Ω, C_L = 35 pF
	75	110	ns max	V_S = 3.3 V; see Figure 18
Break-Before-Make Time Delay, t_{BBM}	70		ns typ	R_L = 300 Ω, C_L = 35 pF
		10	ns min	V_{S1} = V_{S2} = 3.3 V; see Figure 19
Charge Injection	6		pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 1 nF; see Figure 20
Off Isolation	−67		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 21
Channel-to-Channel Crosstalk	−67		dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 22
Bandwidth −3 dB	190		MHz typ	R_L = 50 Ω, C_L = 5 pF; see Figure 23
C_S (OFF)	25		pF typ	f = 1 MHz
C_D, C_S (ON)	95		pF typ	f = 1 MHz
POWER REQUIREMENTS				V_{DD} = 5.5 V
I_{DD}	0.001		μA typ	Digital inputs = 0 V or 5.5 V
		1.0	μA max	

[1] Temperature range for B version is −40°C to +85°C.

[2] Guaranteed by design, not subject to production test.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 4.

Parameter	Rating
V_{DD} to V_{SS}	13 V
V_{DD} to GND	−0.3 V to +6.5 V
V_{SS} to GND	+0.3 V to −6.5 V
Analog Inputs[1]	V_{SS} − 0.3 V to V_{DD} + 0.3 V
Digital Inputs[1]	−0.3 V to V_{DD} + 0.3 V or 30 mA (whichever occurs first)
Peak Current, S or D	100 mA (pulsed at 1 ms, 10% duty cycle maximum)
Continuous Current, S or D	50 mA
Operating Temperature Range	
Industrial (B Version)	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
MSOP	
θ_{JA} Thermal Impedance	206°C/W
θ_{JC} Thermal Impedance	44°C/W
SOT-23	
θ_{JA} Thermal Impedance	229.6°C/W
θ_{JC} Thermal Impedance	91.99°C/W
Lead Temperature, Soldering(10 sec)	300°C
IR Reflow, Peak Temperature	220°C

[1] Overvoltages at IN, S, or D are clamped by internal diodes. Current should be limited to the maximum ratings given.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Only one absolute maximum rating may be applied at a time.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

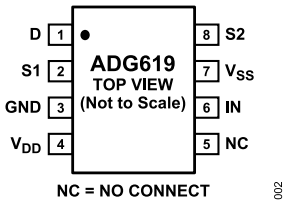

Figure 2. 8-Lead SOT-23 (RJ-8)

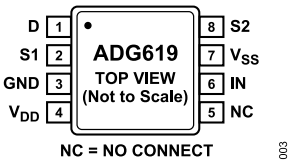

Figure 3. 8-Lead MSOP (RM-8)

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	D	Drain Terminal. Can be an input or output.
2	S1	Source Terminal. Can be an input or output.
3	GND	Ground (0 V) Reference.
4	V_{DD}	Most Positive Power Supply.
5	NC	No Connect. Not internally connected.
6	IN	Logic Control Input.
7	V_{SS}	Most Negative Power Supply. This pin is only used in dual-supply applications and should be tied to ground in single-supply applications.
8	S2	Source Terminal. Can be an input or output.

TYPICAL PERFORMANCE CHARACTERISTICS

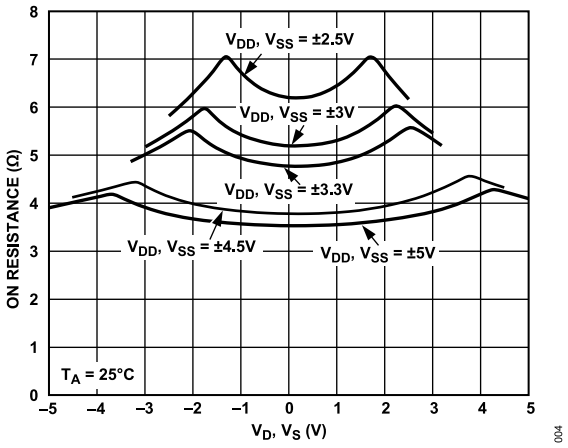

Figure 4. On Resistance vs. V_D, V_S (Dual Supply)

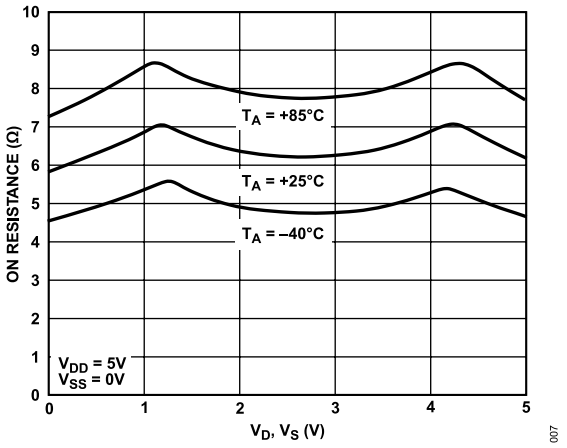

Figure 7. On Resistance vs. V_D, V_S for Different Temperatures (Single Supply)

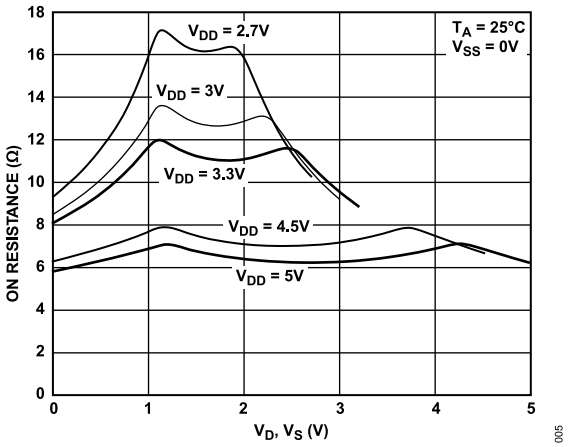

Figure 5. On Resistance vs. V_D, V_S (Single Supply)

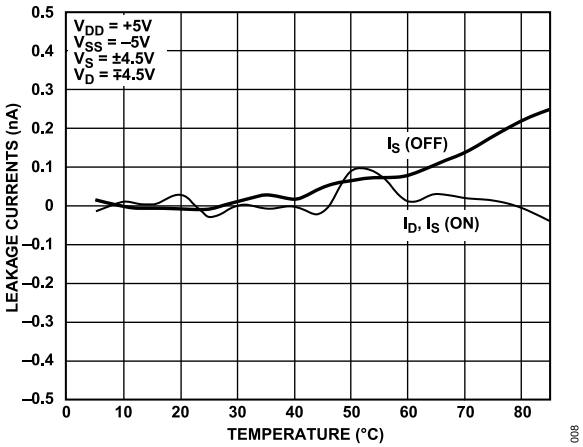

Figure 8. Leakage Currents vs. Temperature (Dual Supply)

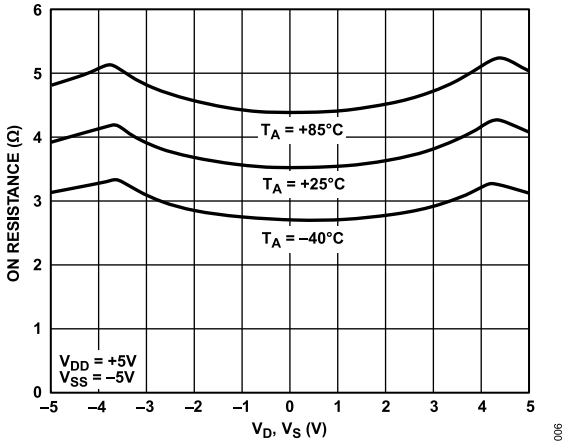

Figure 6. On Resistance vs. V_D, V_S for Different Temperatures (Dual Supply)

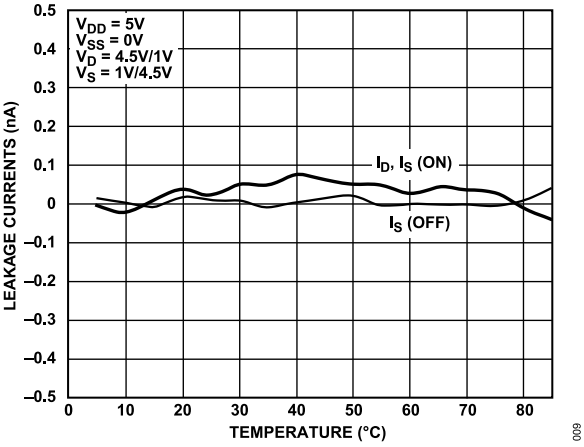

Figure 9. Leakage Currents vs. Temperature (Single Supply)

TYPICAL PERFORMANCE CHARACTERISTICS

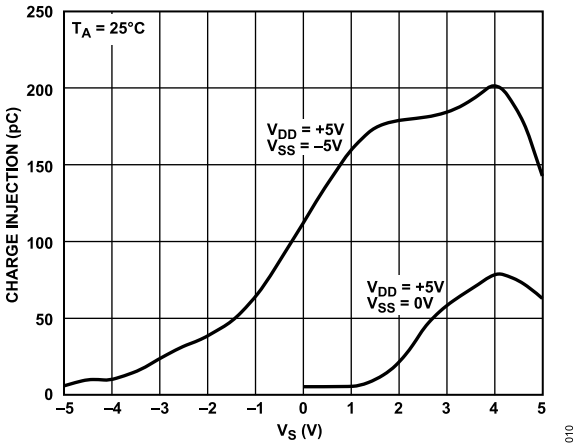

Figure 10. Charge Injection vs. Source Voltage

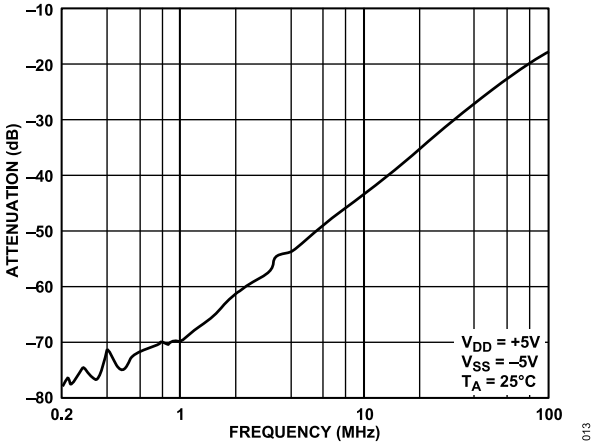

Figure 13. Crosstalk vs. Frequency

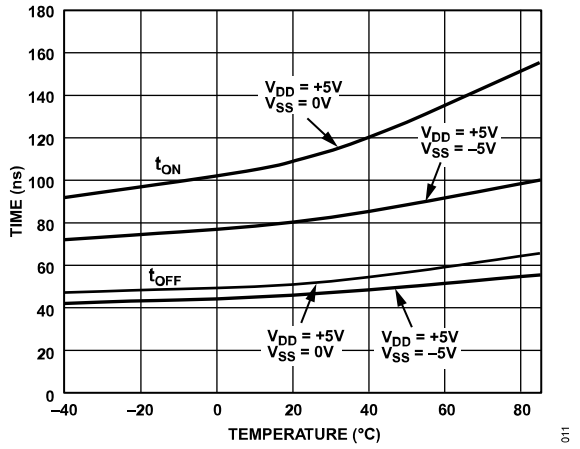

Figure 11. t_{ON}/t_{OFF} Times vs. Temperatures

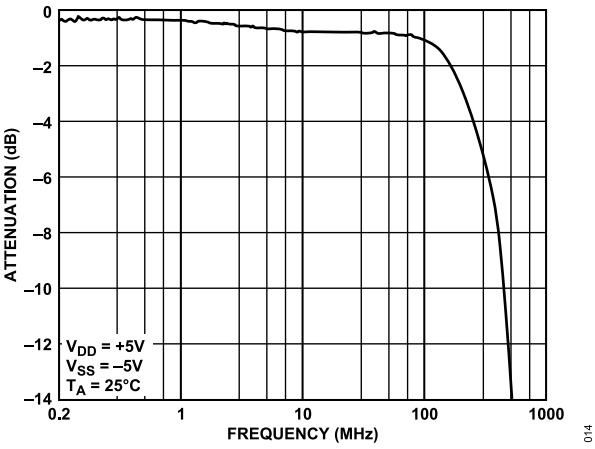

Figure 14. On Response vs. Frequency

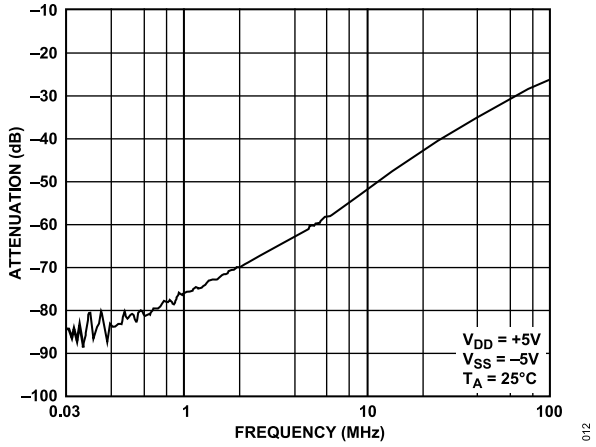

Figure 12. Off Isolation vs. Frequency

TERMINOLOGY

I_{DD}

Positive supply current.

I_{SS}

Negative supply current.

R_{ON}

Ohmic resistance between D and S terminals.

ΔR_{ON}

On resistance match between any two channels.

$R_{FLAT (ON)}$

Flatness is defined as the difference between the maximum and minimum value of on resistance as measured over the specified analog signal range.

I_S (Off)

Source leakage current with the switch off.

I_D, I_S (On)

Channel leakage current with the switch on.

V_D, V_S

Analog voltage on Terminal D and Terminal S.

V_{INL}

Maximum input voltage for Logic 0.

V_{INH}

Minimum input voltage for Logic 1.

I_{INL}, I_{INH}

Input current of the digital input.

C_S (Off)

Off switch source capacitance.

C_D, C_S (On)

On switch capacitance.

t_{ON}

Delay between applying the digital control input and the output switching on.

t_{OFF}

Delay between applying the digital control input and the output switching off.

t_{MBB}

On time is measured between the 80% points of both switches, when switching from one address state to another.

t_{BBM}

Off time or on time is measured between the 90% points of both switches, when switching from one address state to another.

Charge Injection

A measure of the glitch impulse transferred from the digital input to the analog output during switching.

Crosstalk

A measure of unwanted signal coupled through from one channel to another as a result of parasitic capacitance.

Off Isolation

A measure of unwanted signal coupling through an off switch.

Bandwidth

The frequency response of the on switch.

Insertion Loss

The loss due to the on resistance of the switch.

TEST CIRCUITS

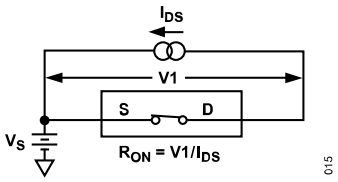

Figure 15. On Resistance

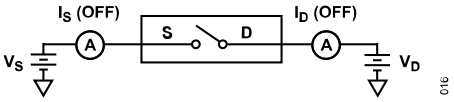

Figure 16. Off Leakage

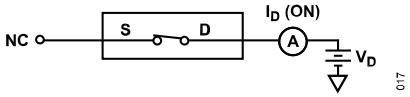

Figure 17. On Leakage

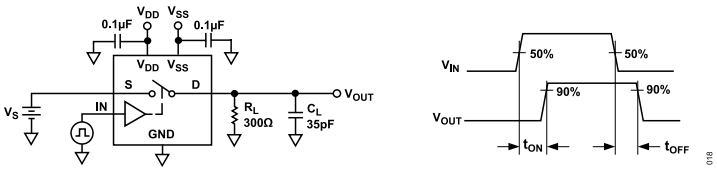

Figure 18. Switching Times

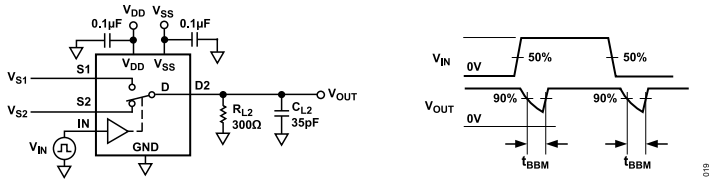

Figure 19. Break-Before-Make Time Delay, t_{BBM}

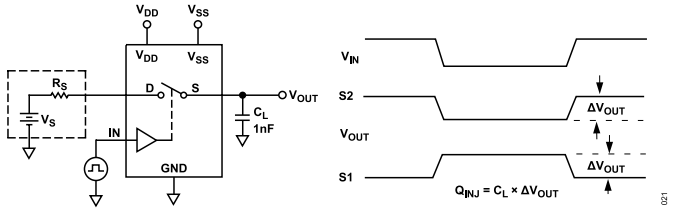

Figure 20. Charge Injection

TEST CIRCUITS

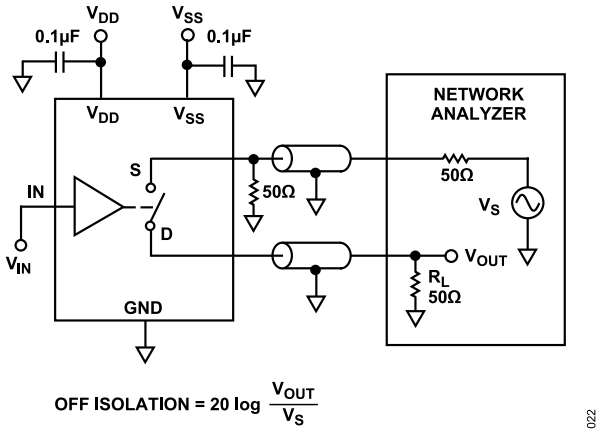

Figure 21. Off Isolation

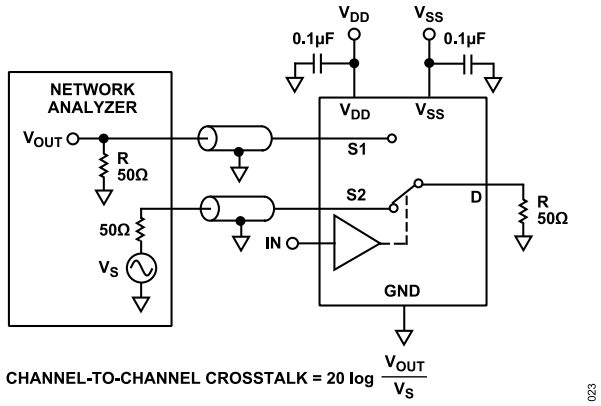

Figure 22. Channel-to-Channel Crosstalk

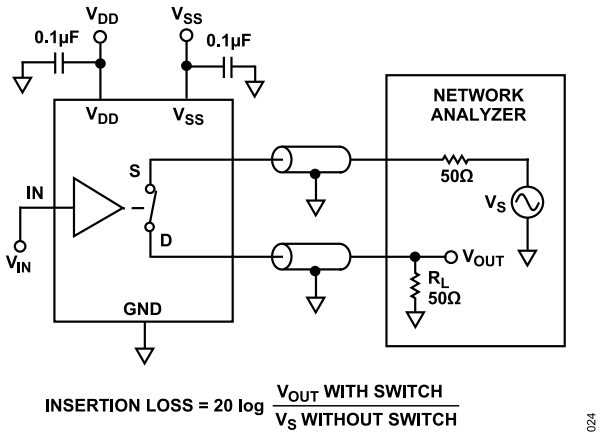

Figure 23. Bandwidth

OUTLINE DIMENSIONS

Package Drawing (Option)	Package Type	Package Description
RM-8	MSOP	8-Lead Mini Small Outline Package
RJ-8	SOT-23	8-Lead Small Outline Transistor Package

For the latest package outline information and land patterns (footprints), go to Package Index.

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Packing Quantity	Package Option	Marking Code[2]
ADG619BRMZ	−40°C to +85°C	8-Lead Mini Small Outline Package (MSOP)	Tube, 50	RM-8	SCC
ADG619BRMZ-REEL	−40°C to +85°C	8-Lead Mini Small Outline Package (MSOP)	Reel, 3000	RM-8	SCC
ADG619BRMZ-REEL7	−40°C to +85°C	8-Lead Mini Small Outline Package (MSOP)	Reel, 1000	RM-8	SCC
ADG619BRTZ-REEL	−40°C to +85°C	8-Lead Small Outline Transistor Package (SOT-23)	Reel, 10000	RJ-8	SCC
ADG619BRTZ-REEL7	−40°C to +85°C	8-Lead Small Outline Transistor Package (SOT-23)	Reel, 3000	RJ-8	SCC
ADG619BRTZ-500RL7	−40°C to +85°C	8-Lead Small Outline Transistor Package (SOT-23)	Reel, 500	RJ-8	SCC

[1] Z = RoHS Compliant Part.

[2] Marking code on SOT-23 and MSOP is limited to three characters due to space constraints.