

Silicon Carbide (SiC) Cascode JFET - EliteSiC, Power N-Channel, TO247-3, 1200 V, 80 mohm

UJ3C120080K3S

Description

This SiC FET device is based on a unique ‘cascode’ circuit configuration, in which a normally-on SiC JFET is co-packaged with a Si MOSFET to produce a normally-off SiC FET device. The device’s standard gate-drive characteristics allows for a true “drop-in replacement” to Si IGBTs, Si FETs, SiC MOSFETs or Si super-junction devices. Available in the TO247-3 package, this device exhibits ultra-low gate charge and exceptional reverse recovery characteristics, making it ideal for switching inductive loads, and any application requiring standard gate drive.

Features

- Typical On-resistance $R_{DS(on),typ}$: 80 m Ω
- Maximum Operating Temperature of 175 °C
- Excellent Reverse Recovery
- Low Gate Charge
- Low Intrinsic Capacitance
- ESD Protected: HBM Class 2 and CDM Class C3
- This Device is Pb-Free, Halogen Free and is RoHS Compliant

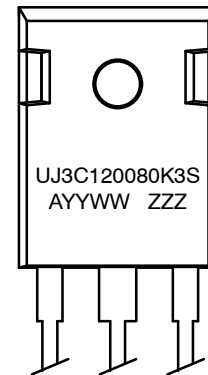
Typical Applications

- EV Charging
- PV Inverters
- Switch Mode Power Supplies
- Power Factor Correction Modules
- Motor Drives
- Induction Heating



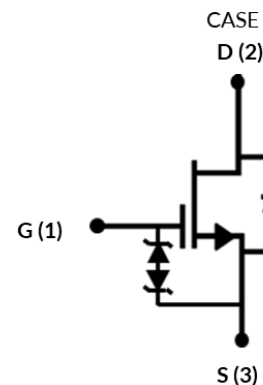
TO247-3 15.90x20.96x5.03, 5.44P
CASE 340AK

MARKING DIAGRAM



UJ3C120080K3S = Specific Device Code
A = Assembly Location
YY = Year
WW = Work Week
ZZZ = Lot ID

PIN CONNECTIONS



ORDERING INFORMATION

See detailed ordering and shipping information on page 8 of this data sheet.

UJ3C120080K3S

MAXIMUM RATINGS

Parameter	Symbol	Test Conditions	Value	Unit
Drain-source Voltage	V_{DS}		1200	V
Gate-source Voltage	V_{GS}	DC	-25 to +25	V
Continuous Drain Current (Note 1)	I_D	$T_C = 25\text{ }^{\circ}\text{C}$	33	A
		$T_C = 100\text{ }^{\circ}\text{C}$	24	A
Pulsed Drain Current (Note 2)	I_{DM}	$T_C = 25\text{ }^{\circ}\text{C}$	77	A
Single Pulsed Avalanche Energy (Note 3)	E_{AS}	$L = 15\text{ mH}$, $I_{AS} = 2.8\text{ A}$	58.5	mJ
Power Dissipation	P_{tot}	$T_C = 25\text{ }^{\circ}\text{C}$	254.2	W
Maximum Junction Temperature	$T_{J,max}$		175	$^{\circ}\text{C}$
Operating and Storage Temperature	T_J , T_{STG}		-55 to 175	$^{\circ}\text{C}$
Max. Lead Temperature for Soldering, 1/8" from Case for 5 Seconds	T_L		250	$^{\circ}\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Limited by $T_{J,max}$.
2. Pulse width t_p limited by $T_{J,max}$.
3. Starting $T_J = 25\text{ }^{\circ}\text{C}$.

THERMAL CHARACTERISTICS

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$		-	0.45	0.59	$^{\circ}\text{C/W}$

ELECTRICAL CHARACTERISTICS ($T_J = +25\text{ }^{\circ}\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
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TYPICAL PERFORMANCE – STATIC

Drain-source Breakdown Voltage	BV _{DS}	V _{GS} = 0 V, I _D = 1 mA		1200	–	–	V
Total Drain Leakage Current	I _{DSS}	V _{DS} = 1200 V, V _{GS} = 0 V, T _J = 25 °C		–	10	75	μA
		V _{DS} = 1200 V, V _{GS} = 0 V, T _J = 175°C		–	50	–	
Total Gate Leakage Current	I _{GSS}	V _{DS} = 0 V, T _J = 25 °C, V _{GS} = –20 V/ +20 V		–	6	±20	μA
Drain-source On-resistance	R _{DS(on)}	V _{GS} = 12 V, I _D = 20 A	T _J = 25 °C	–	80	100	mΩ
			T _J = 125 °C	–	130	–	
			T _J = 175 °C	–	172	–	
Gate Threshold Voltage	V _{G(th)}	V _{DS} = 5 V, I _D = 10 mA		4	5	6	V
Gate Resistance	R _G	f = 1 MHz, open drain		–	4.5	–	Ω

TYPICAL PERFORMANCE – REVERSE DIODE

Diode Continuous Forward Current (Note 4)	I_S	$T_C = 25\text{ }^{\circ}\text{C}$	-	-	33	A
Diode Pulse Current (Note 5)	$I_{S,pulse}$	$T_C = 25\text{ }^{\circ}\text{C}$	-	-	77	A
Forward Voltage	V_{FSD}	$V_{GS} = 0\text{ V}$, $I_S = 10\text{ A}$, $T_J = 25\text{ }^{\circ}\text{C}$	-	1.5	2	V
		$V_{GS} = 0\text{ V}$, $I_S = 10\text{ A}$, $T_J = 175\text{ }^{\circ}\text{C}$	-	2	-	
Reverse Recovery Charge	Q_{rr}	$V_{DS} = 800\text{ V}$, $I_S = 20\text{ A}$, $V_{GS} = 0\text{ V}$, $R_{G_EXT} = 10\text{ }\Omega$, $di/dt = 2200\text{ A}/\mu\text{s}$, $T_J = 150\text{ }^{\circ}\text{C}$	-	180	-	nC
Reverse Recovery Time	t_{rr}		-	30	-	ns

UJ3C120080K3S

ELECTRICAL CHARACTERISTICS ($T_J = +25\text{ }^{\circ}\text{C}$ unless otherwise specified) (continued)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
TYPICAL PERFORMANCE – DYNAMIC						
Input Capacitance	C_{iss}	$V_{DS} = 100\text{ V}, V_{GS} = 0\text{ V},$ $f = 100\text{ kHz}$	–	1500	–	pF
Output Capacitance	C_{oss}		–	100	–	
Reverse Transfer Capacitance	C_{rss}		–	2.1	–	
Effective Output Capacitance, Energy Related	$C_{oss(er)}$	$V_{DS} = 0\text{ V to } 800\text{ V}, V_{GS} = 0\text{ V}$	–	59	–	pF
Effective Output Capacitance, Time Related	$C_{oss(tr)}$		–	136	–	pF
C_{oss} Stored Energy	E_{oss}	$V_{DS} = 800\text{ V}, V_{GS} = 0\text{ V}$	–	19	–	μJ
Total Gate Charge	Q_G	$V_{DS} = 800\text{ V}, I_D = 20\text{ A},$ $V_{GS} = -5\text{ V to } 15\text{ V}$	–	51	–	nC
Gate-drain Charge	Q_{GD}		–	11	–	
Gate-source Charge	Q_{GS}		–	19	–	
Turn-on Delay Time	$t_{d(on)}$	$V_{DS} = 800\text{ V}, I_D = 20\text{ A},$ Gate Driver = $-5\text{ V to } +15\text{ V},$ Turn-on $R_{G_EXT} = 1\text{ }\Omega,$ Turn-off $R_{G_EXT} = 20\text{ }\Omega,$ Inductive Load, FWD: UJ2D1215T, $T_J = 150\text{ }^{\circ}\text{C}$	–	22	–	ns
Rise Time	t_r		–	14	–	
Turn-off Delay Time	$t_{d(off)}$		–	61	–	
Fall Time	t_f		–	14	–	
Turn-on Energy	E_{ON}		–	260	–	μJ
Turn-off Energy	E_{OFF}		–	108	–	
Total Switching Energy	E_{TOTAL}		–	368	–	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Limited by $T_{J,max}$.

5. Pulse width t_p limited by $T_{J,max}$.

TYPICAL PERFORMANCE DIAGRAMS

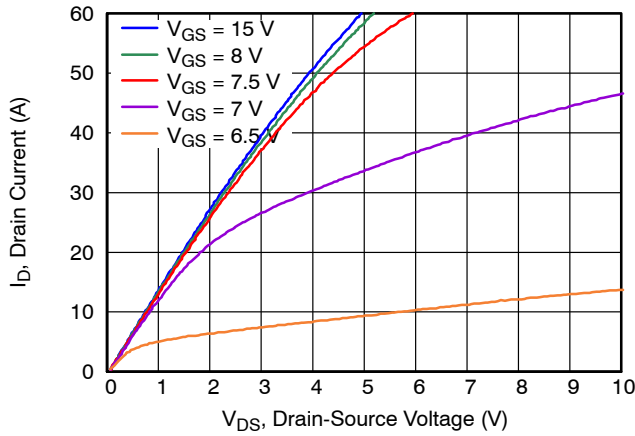


Figure 1. Typical Output Characteristics at $T_J = -55\text{ }^{\circ}\text{C}$, $t_p < 250\text{ }\mu\text{s}$

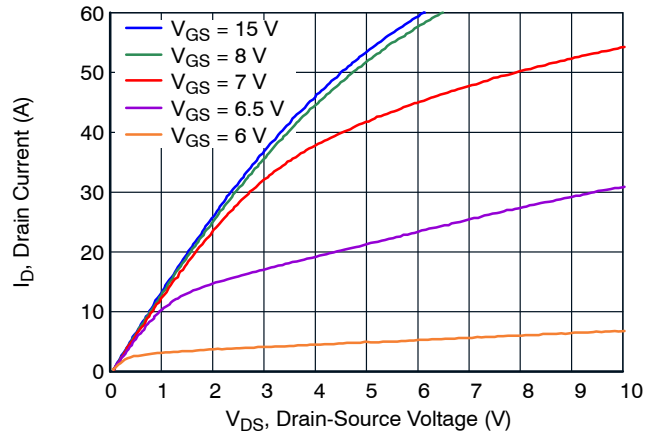


Figure 2. Typical Output Characteristics at $T_J = 25\text{ }^{\circ}\text{C}$, $t_p < 250\text{ }\mu\text{s}$

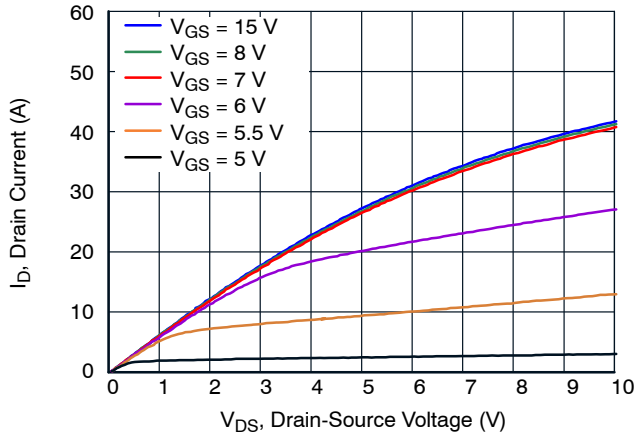


Figure 3. Typical Output Characteristics at $T_J = 175\text{ }^{\circ}\text{C}$, $t_p < 250\text{ }\mu\text{s}$

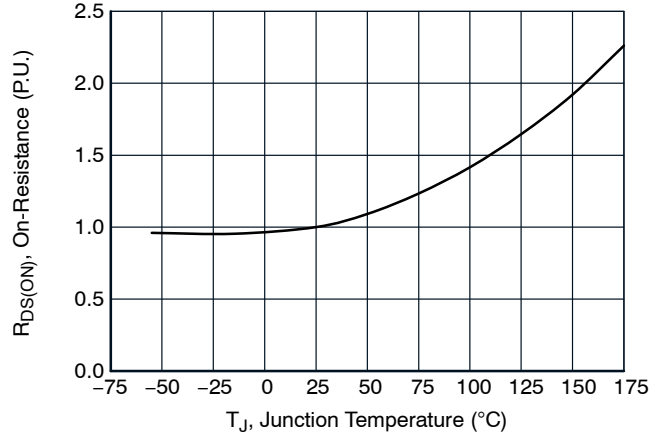


Figure 4. Normalized On-Resistance vs. Temperature at $V_{GS} = 12\text{ V}$ and $I_D = 20\text{ A}$

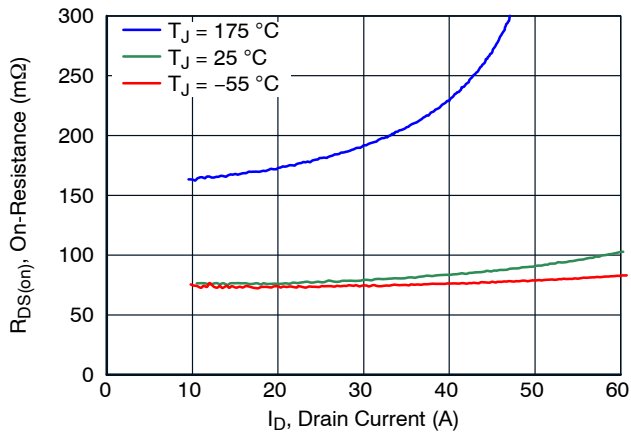


Figure 5. Typical Drain-Source On-Resistances at $V_{GS} = 12\text{ V}$

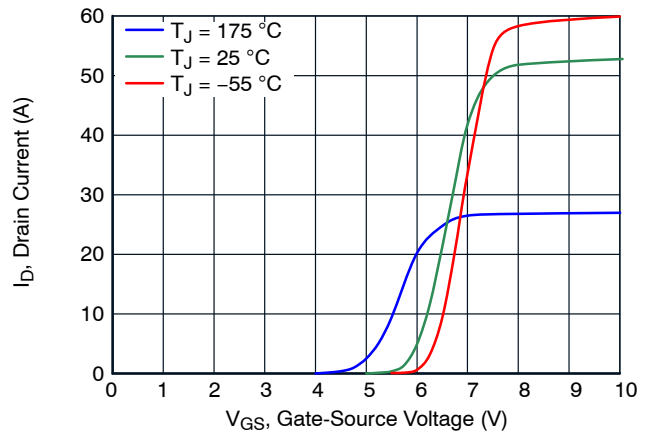


Figure 6. Typical Transfer Characteristics at $V_{DS} = 5\text{ V}$

TYPICAL PERFORMANCE DIAGRAMS (continued)

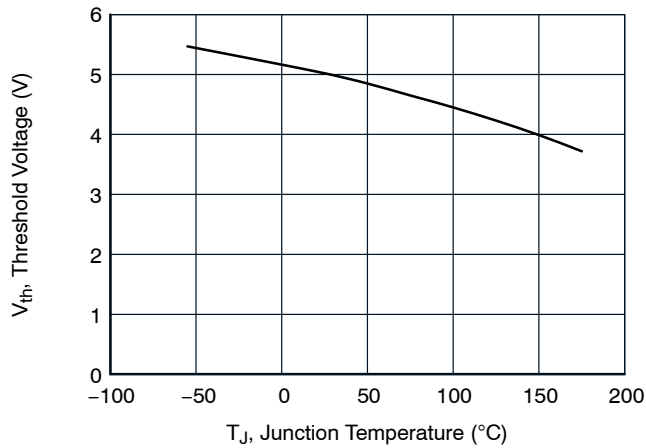


Figure 7. Threshold Voltage vs. Junction Temperature at $V_{DS} = 5\text{ V}$ and $I_D = 10\text{ mA}$

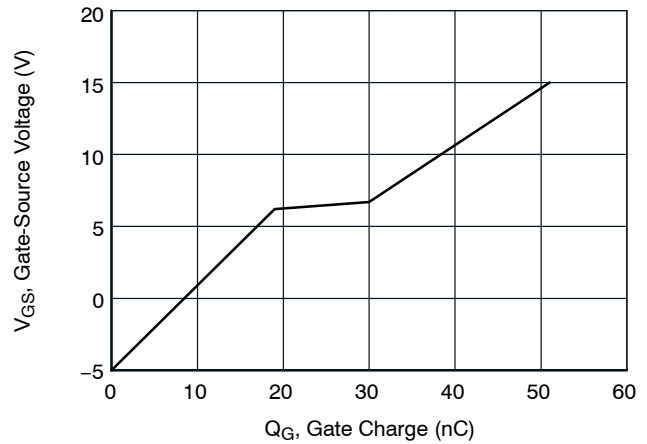


Figure 8. Typical Gate Charge at $V_{DS} = 800\text{ V}$ and $I_D = 20\text{ A}$

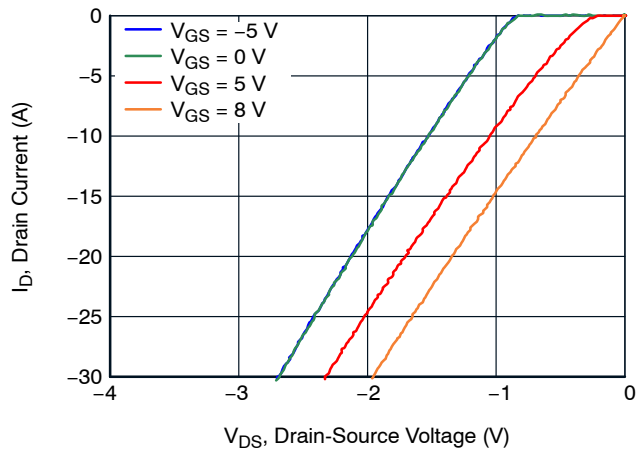


Figure 9. 3rd Quadrant Characteristics at $T_J = -55\text{ °C}$

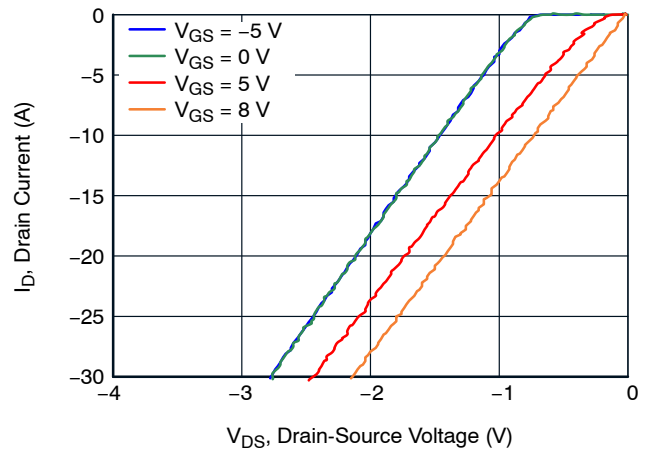


Figure 10. 3rd Quadrant Characteristics at $T_J = 25\text{ °C}$

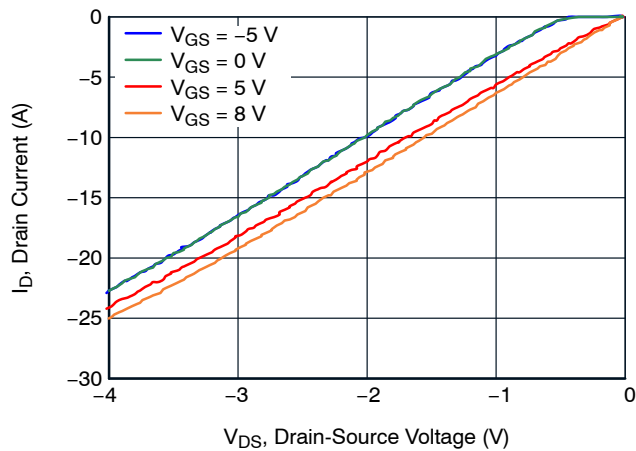


Figure 11. 3rd Quadrant Characteristics at $T_J = 175\text{ °C}$

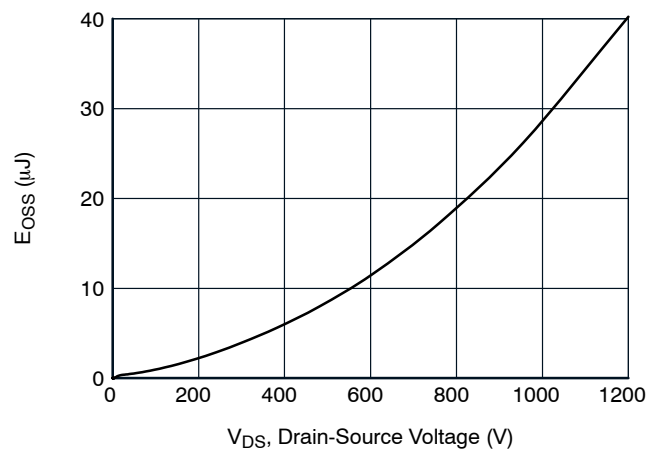


Figure 12. Typical Stored Energy in C_{OSS} at $V_{GS} = 0\text{ V}$

TYPICAL PERFORMANCE DIAGRAMS (continued)

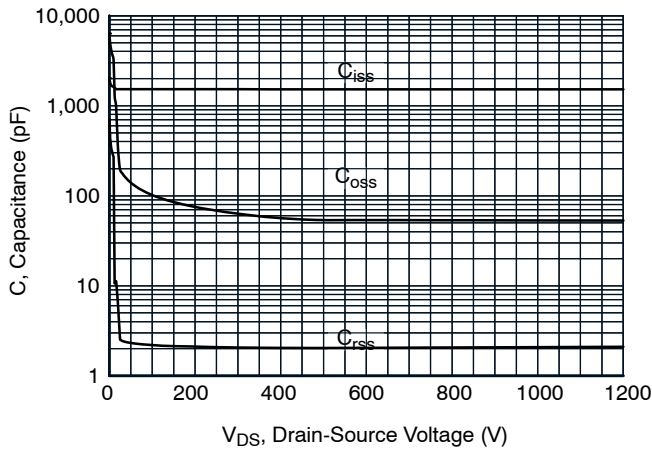


Figure 13. Typical Capacitances at $f = 100 \text{ kHz}$ and $V_{GS} = 0 \text{ V}$

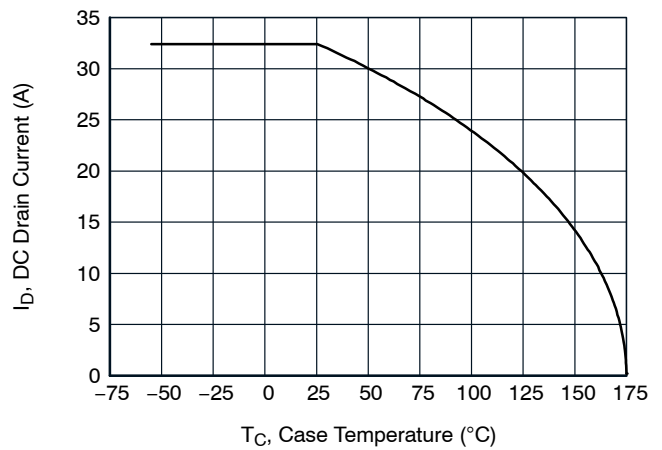


Figure 14. DC Drain Current Derating

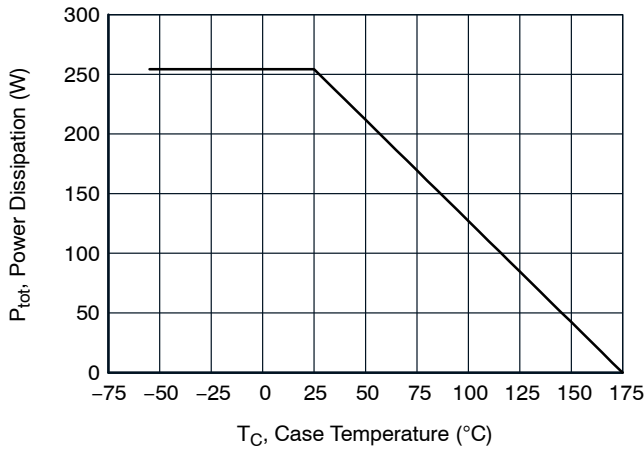


Figure 15. Total Power Dissipation

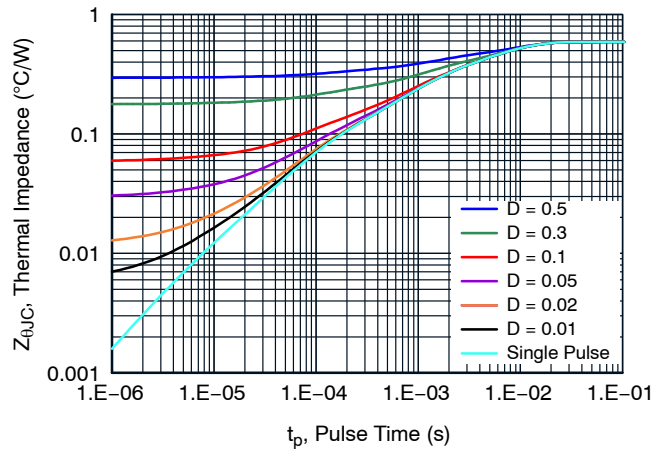


Figure 16. Maximum Transient Thermal Impedance

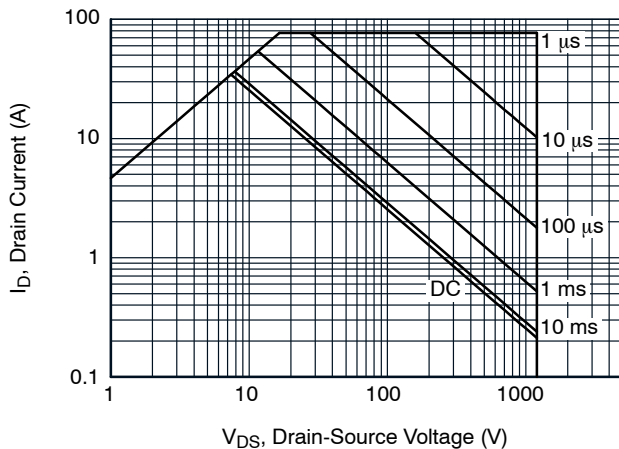


Figure 17. Safe Operation Area at $T_C = 25 \text{ }^\circ\text{C}$, $D = 0$, Parameter t_p

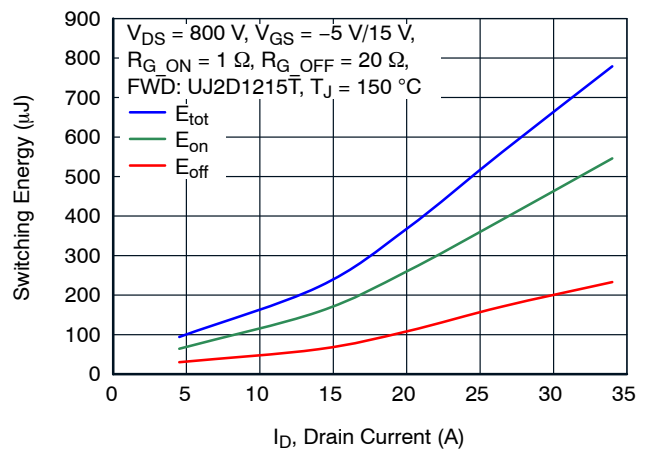


Figure 18. Clamped Inductive Switching Energy vs. Drain Current at $T_J = 150 \text{ }^\circ\text{C}$

TYPICAL PERFORMANCE DIAGRAMS (continued)

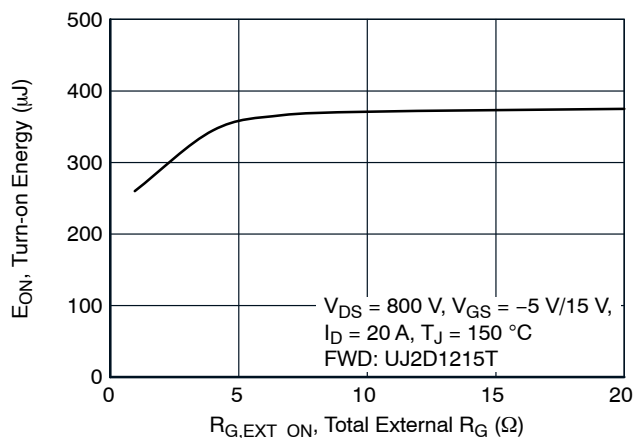


Figure 19. Clamped Inductive Switching
Turn-on Energy vs. R_{G,EXT_ON}

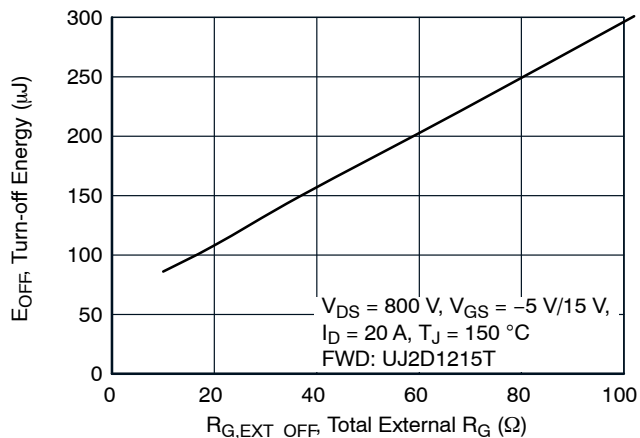


Figure 20. Clamped Inductive Switching
Turn-off Energy vs. R_{G,EXT_OFF}

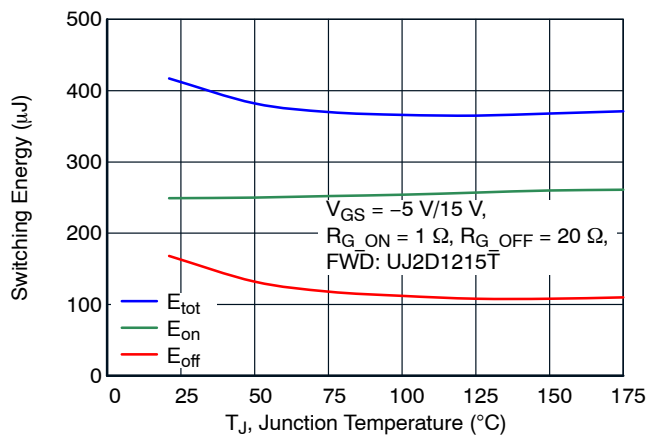


Figure 21. Clamped Inductive Switching
Energy vs. Junction Temperature at
 $V_{DS} = 800\text{ V}$ and $I_D = 20\text{ A}$

APPLICATIONS INFORMATION

SiC FETs are enhancement-mode power switches formed by a high-voltage SiC depletion-mode JFET and a low-voltage silicon MOSFET connected in series. The silicon MOSFET serves as the control unit while the SiC JFET provides high voltage blocking in the off state. This combination of devices in a single package provides compatibility with standard gate drivers and offers superior performance in terms of low on-resistance ($R_{DS(on)}$), output capacitance (C_{oss}), gate charge (Q_G), and reverse recovery charge (Q_{rr}) leading to low conduction and switching losses. The SiC FETs also provide excellent reverse conduction capability eliminating the need for an external anti-parallel diode.

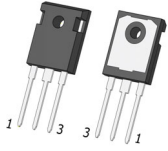
Like other high performance power switches, proper PCB layout design to minimize circuit parasitics is strongly recommended due to the high dv/dt and di/dt rates. An external gate resistor is recommended when the FET is working in the diode mode in order to achieve the optimum

reverse recovery performance. For more information on SiC FET operation, see www.onsemi.com.

A snubber circuit with a small $R_{(G)}$, or gate resistor, provides better EMI suppression with higher efficiency compared to using a high $R_{(G)}$ value. There is no extra gate delay time when using the snubber circuitry, and a small $R_{(G)}$ will better control both the turn-off $V_{(DS)}$ peak spike and ringing duration, while a high $R_{(G)}$ will damp the peak spike but result in a longer delay time. In addition, the total switching loss when using a snubber circuit is less than using high $R_{(G)}$, while greatly reducing $E_{(OFF)}$ from mid-to-full load range with only a small increase in $E_{(ON)}$. Efficiency will therefore improve with higher load current. For more information on how a snubber circuit will improve overall system performance, visit the **onsemi** website at www.onsemi.com.

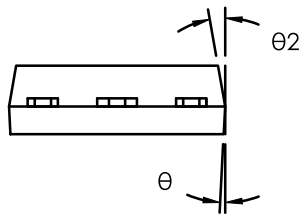
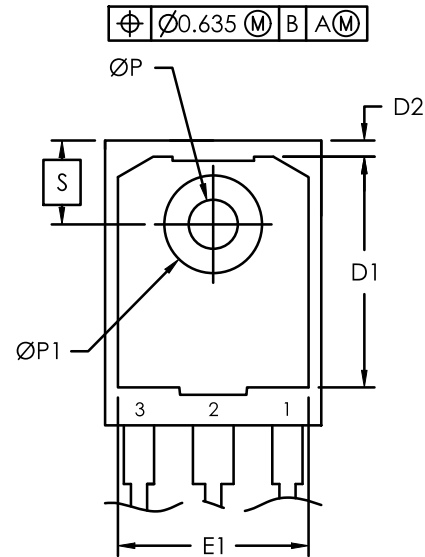
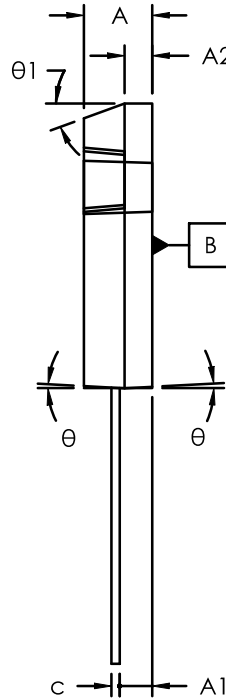
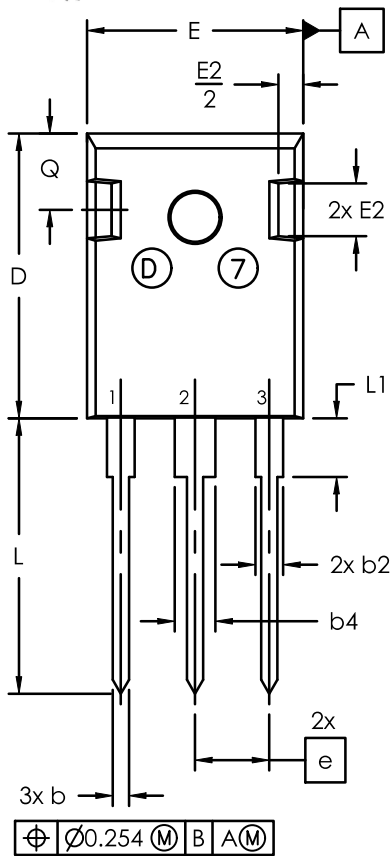
ORDERING INFORMATION

Part Number	Marking	Package	Shipping
UJ3C120080K3S	UJ3C120080K3S	TO247-3 15.90x20.96x5.03, 5.44P (Pb-Free, Halogen Free)	600 / Tube



TO247-3 15.90x20.96x5.03, 5.44P
CASE 340AK
ISSUE B

DATE 14 APR 2025



NOTE:

1. Dimensioning and tolerancing as per ASME Y14.5 - 2018
2. Controlling dimension : millimeters
3. Package Outline in compliance with JEDEC standard var. AD.
4. Dimensions D & E does not include mold flash.
5. ØP to have max draft angle of 1.7° to the top with max. hole diameter of 3.91mm.

SYM	millimeters		
	MIN	NOM	MAX
A	4.70	5.03	5.31
A1	2.21	2.40	2.59
A2	1.50	2.03	2.49
b	0.99	1.20	1.40
b2	1.65	2.03	2.39
b4	2.59	3.00	3.43
c	0.38	0.60	0.89
D	20.70	20.96	21.46
D1	13.08	—	—
D2	0.51	1.19	1.35
E	15.49	15.90	16.26
e	5.44 BSC		
E1	13.00	13.30	13.60
E2	3.43	3.89	5.20
L	19.62	20.27	20.32
L1	—	—	4.50
ØP	3.40	3.60	3.80
ØP1	7.06	7.19	7.39
Q	5.38	5.62	6.20
S	6.15 BSC		
θ	3°		
θ1	20°		
θ2	10°		

DOCUMENT NUMBER: 98AON88794E

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DESCRIPTION: TO247-3 15.90x20.96x5.03, 5.44P

PAGE 1 OF 1

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