

MOSFET - Power, Single N-Channel, D2PAK-7L 650 V, 110 mΩ, 30 A

NVBG110N65S3F

Description

SUPERFET[®] III MOSFET is onsemi's brand-new high voltage super-junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low on-resistance and lower gate charge performance. This advanced technology is tailored to minimize conduction loss, provide superior switching performance, and withstand extreme dv/dt rate.

Consequently, SUPERFET III MOSFET is very suitable for the various power system for miniaturization and higher efficiency. SUPERFET III FRFET[®] MOSFET's optimized reverse recovery performance of body diode can remove additional component and improve system reliability.

In addition, the D2PAK 7 lead package offers Kelvin sense. This allows higher switching speeds and gives designers the ability to reduce the overall application footprint.

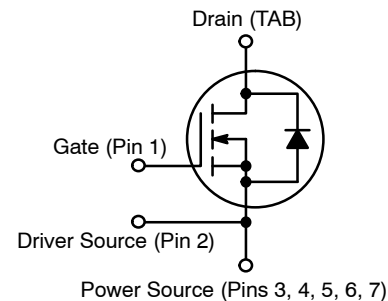
Features

- 700 V @ $T_J = 150^{\circ}\text{C}$
- Typ. $R_{DS(on)} = 93\text{ m}\Omega$
- Ultra Low Gate Charge (Typ. $Q_g = 58\text{ nC}$)
- Low Effective Output Capacitance (Typ. $C_{oss(eff.)} = 553\text{ pF}$)
- 100% Avalanche Tested
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

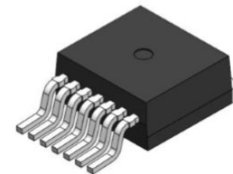
Typical Applications

- Automotive On Board Charger
- Automotive DC/DC Converter for BEV

$V_{(BR)DSS}$	$R_{DS(ON)}\text{ MAX}$	$I_D\text{ MAX}$
650 V	110 mΩ @ 10 V	30 A

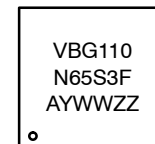


N-CHANNEL MOSFET



**D2PAK-7L
CASE 418BJ**

MARKING DIAGRAM



VBG110N65S3F = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
ZZ = Lot Traceability

ORDERING INFORMATION

See detailed ordering and shipping information on page 6 of this data sheet.

NVBG110N65S3F

Table 1. ABSOLUTE MAXIMUM RATINGS ($T_C = 25^\circ\text{C}$ unless otherwise stated)

Symbol	Parameter		Value	Unit
V_{DSS}	Drain-to-Source Voltage		650	V
V_{GS}	Gate-to-Source Voltage	– DC	± 30	V
		– AC ($f > 1\text{ Hz}$)	± 30	
I_D	Drain Current	– Continuous ($T_C = 25^\circ\text{C}$)	30	A
		– Continuous ($T_C = 100^\circ\text{C}$)	19.5	
I_{DM}	Drain Current	– Pulsed (Note 1)	69	A
E_{AS}	Single Pulse Avalanche Energy (Note 2)		380	mJ
I_{AS}	Avalanche Current		3.5	A
E_{AR}	Repeated Avalanche Energy (Note 1)		2.4	mJ
dv/dt	MOSFET dv/dt		100	V/ns
	Peak Diode Recovery dv/dt (Note 3)		50	
P_D	Power Dissipation	$T_C = 25^\circ\text{C}$	240	W
		– Derate Above 25°C	1.92	W/ $^\circ\text{C}$
T_J, T_{stg}	Operating Junction and Storage Temperature Range		–55 to 150	$^\circ\text{C}$
T_L	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds		300	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Repetitive rating: pulse – width limited by maximum junction temperature.

2. $I_{AS} = 3.5\text{ A}$, $R_G = 25\ \Omega$, starting $T_J = 25^\circ\text{C}$.

3. $I_{SD} \leq 15\text{ A}$, $di/dt \leq 200\text{ A}/\mu\text{s}$, $V_{DD} \leq 400\text{ V}$, starting $T_C = 25^\circ\text{C}$.

Table 2. THERMAL RESISTANCE RATINGS

Symbol	Parameter	Max	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case, Max.	0.52	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient, Max.	40	

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ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

BV _{DSS}	Drain-to-Source Breakdown Voltage	V _{GS} = 0 V, I _D = 1 mA, T _J = 25°C	650	–	–	V
		V _{GS} = 0 V, I _D = 10 mA, T _J = 150°C	700	–	–	V
ΔBV _{DSS} /ΔT _J	Breakdown Voltage Temperature Coefficient	I _D = 20 mA, Referenced to 25°C	–	0.61	–	V/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 650 V, V _{GS} = 0 V	–	–	10	μA
		V _{DS} = 520 V, T _C = 125°C	–	128	–	μA
I _{GSS}	Gate-to-Body Leakage Current	V _{DS} = 0 V, V _{GS} = ±30 V	–	–	±100	nA

ON CHARACTERISTICS

V _{GS(th)}	Gate Threshold Voltage	V _{GS} = V _{DS} , I _D = 0.74 mA	3.0	–	5.0	V
R _{DS(on)}	Static Drain-to-Source On Resistance	V _{GS} = 10 V, I _D = 15 A	–	93	110	mΩ
g _{FS}	Forward Transconductance	V _{GS} = 20 V, I _D = 15 A	–	17	–	S

DYNAMIC CHARACTERISTICS

C _{iss}	Input Capacitance	V _{DS} = 400 V, V _{GS} = 0 V, f = 1 MHz	–	2560	–	pF
C _{oss}	Output Capacitance		–	50	–	pF
C _{oss(eff.)}	Effective Output Capacitance	V _{DS} = 0 to 400 V, V _{GS} = 0 V	–	553	–	pF
C _{oss(er.)}	Energy Related Output Capacitance	V _{DS} = 0 to 400 V, V _{GS} = 0 V	–	83	–	pF
Q _{g(total)}	Total Gate Charge at 10 V	V _{DS} = 400 V, I _D = 15 A, V _{GS} = 10 V (Note 4)	–	58	–	nC
Q _{gs}	Gate-to-Source Gate Charge		–	19	–	nC
Q _{gd}	Gate-to-Drain "Miller" Charge		–	23	–	nC
ESR	Equivalent Series Resistance	F = 1 MHz	–	2	–	Ω

SWITCHING CHARACTERISTICS, V_{GS} = 10 V

t _{d(on)}	Turn-On Delay Time	V _{DD} = 400 V, I _D = 15 A, V _{GS} = 10 V, R _G = 4.7 Ω (Note 4)	–	31	–	ns
t _r	Rise Time		–	23	–	ns
t _{d(off)}	Turn-Off Delay Time		–	67	–	ns
t _f	Fall Time		–	4.6	–	ns

SOURCE-DrAIN DIODE CHARACTERISTICS

I _S	Maximum Continuous Source-to-Drain Diode Forward Current		–	–	30	A
I _{SM}	Maximum Pulsed Source-to-Drain Diode Forward Current		–	–	69	A

TYPICAL CHARACTERISTICS

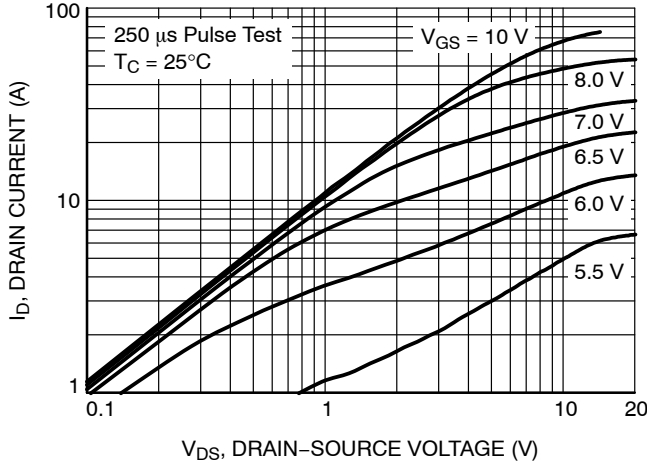


Figure 1. On-Region Characteristics

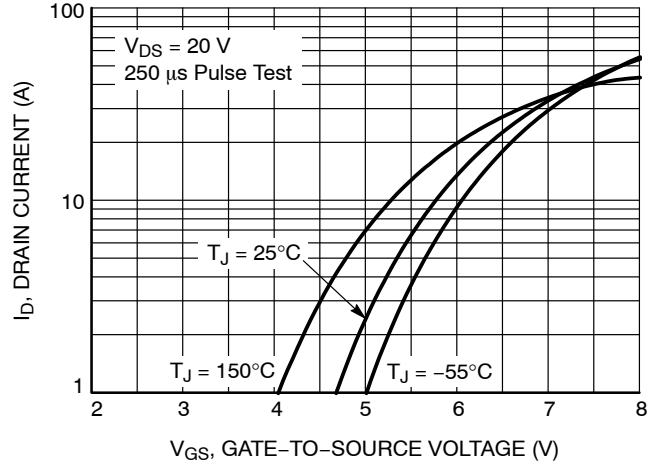


Figure 2. Transfer Characteristics

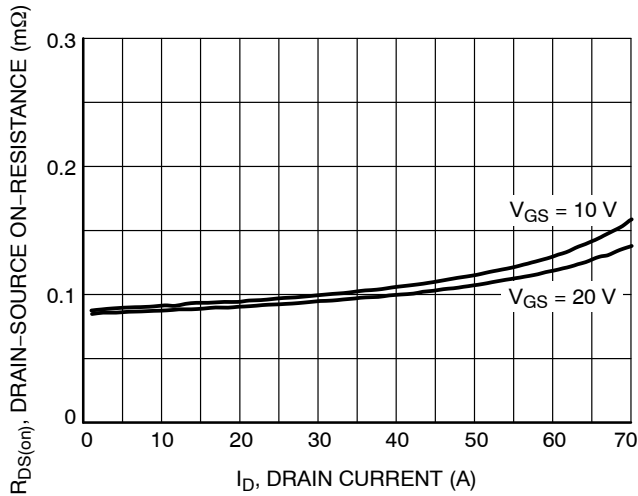


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

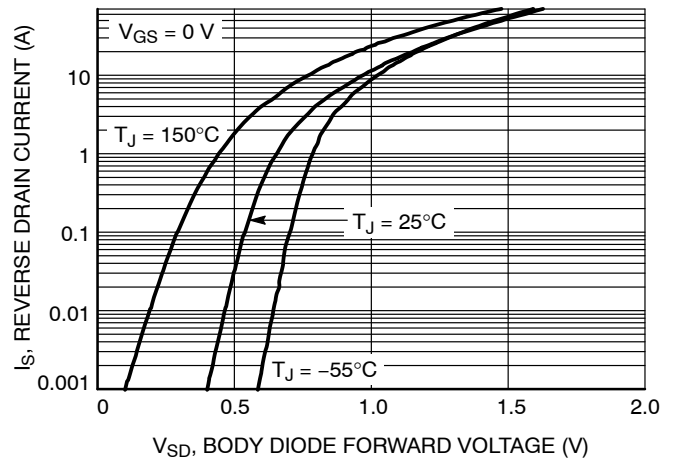


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

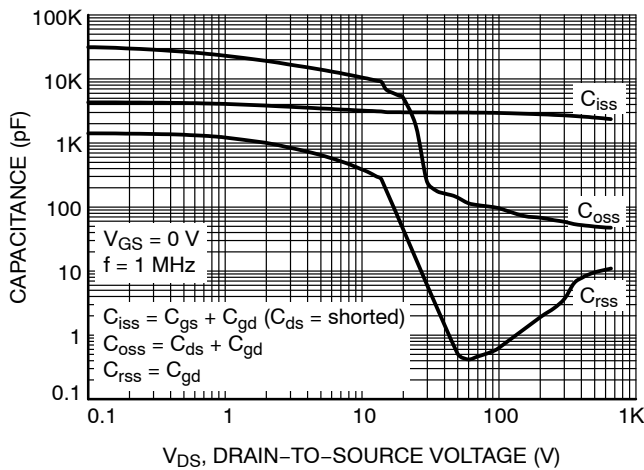


Figure 5. Capacitance Characteristics

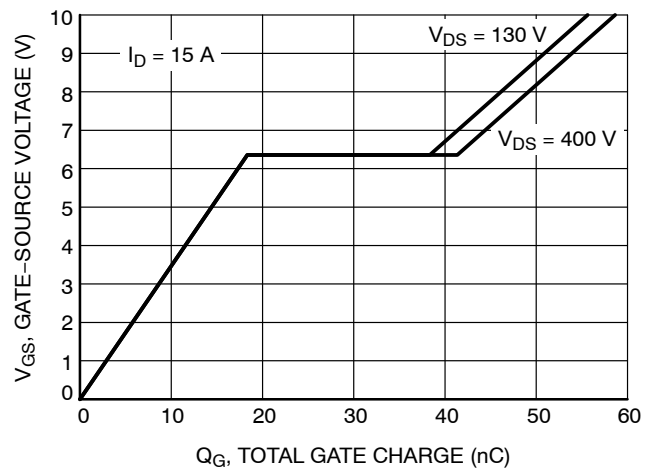


Figure 6. Gate Charge Characteristics

TYPICAL CHARACTERISTICS

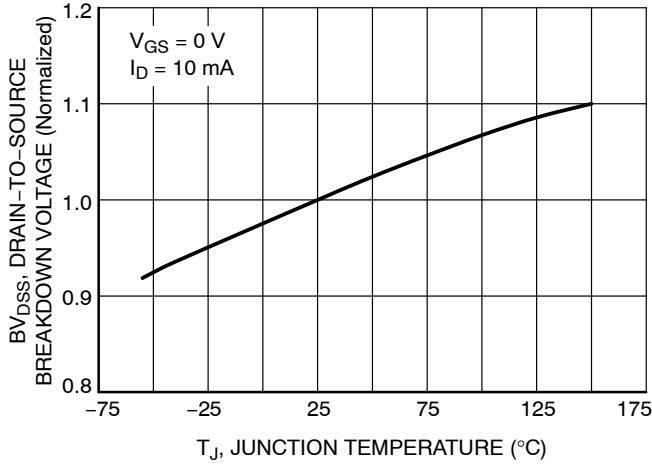


Figure 7. Breakdown Voltage Variation vs. Temperature

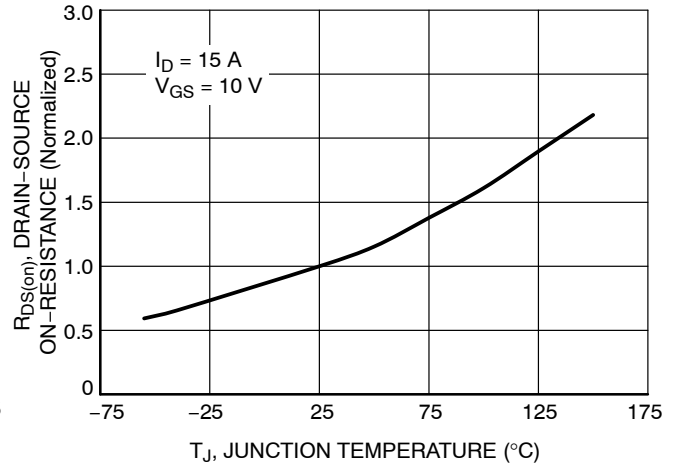


Figure 8. On-Resistance Variation vs. Temperature

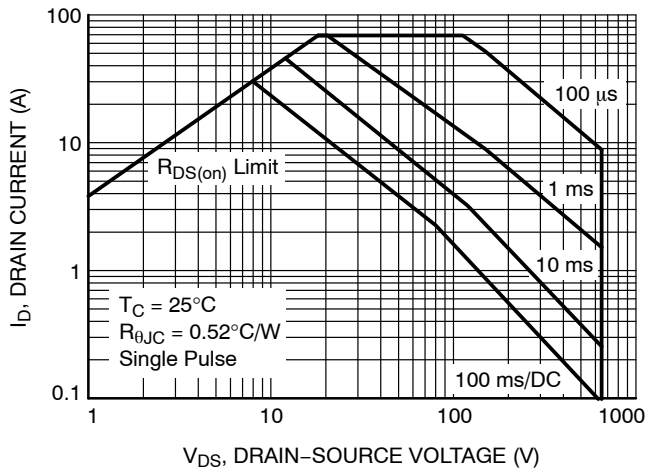


Figure 9. Maximum Safe Operating Area

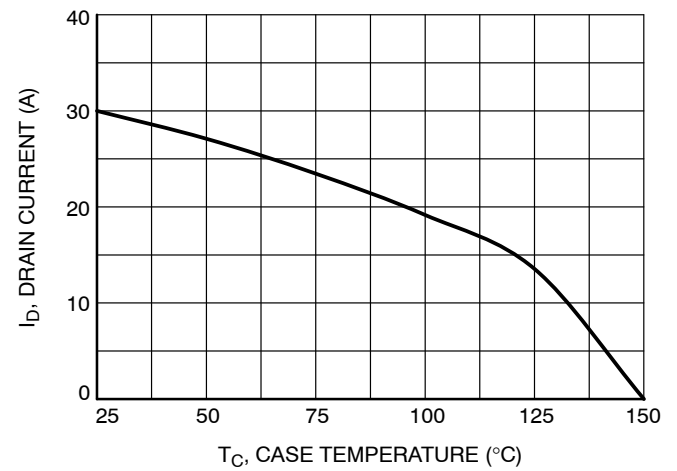


Figure 10. Maximum Drain Current vs. Case Temperature

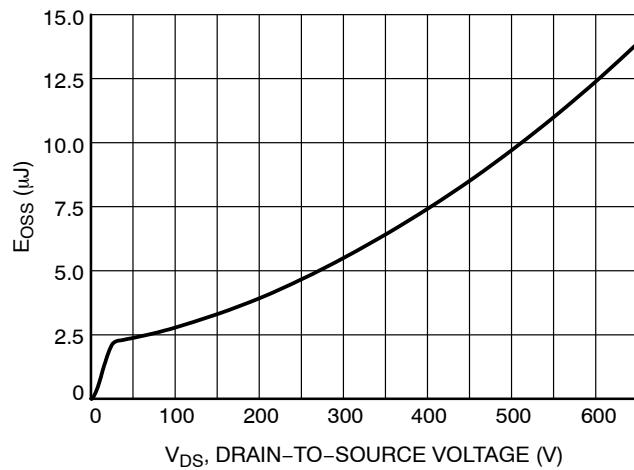


Figure 11. E_{OSS} vs. Drain-to-Source Voltage

NVBG110N65S3F

TYPICAL CHARACTERISTICS

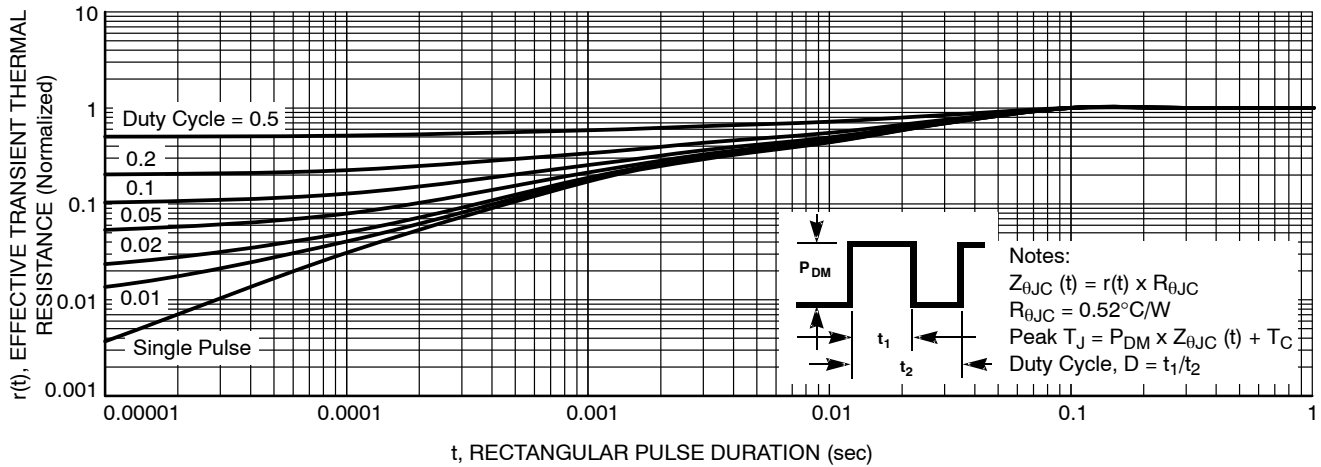


Figure 12. Transient Thermal Response

DEVICE ORDERING INFORMATION

Device	Package	Shipping [†]
NVBG110N65S3F	D2PAK-7L	800 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

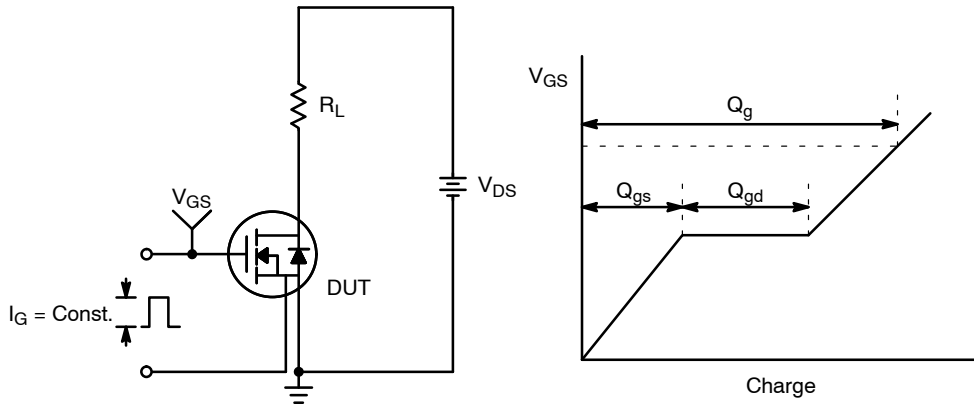


Figure 13. Gate Charge Test Circuit & Waveform

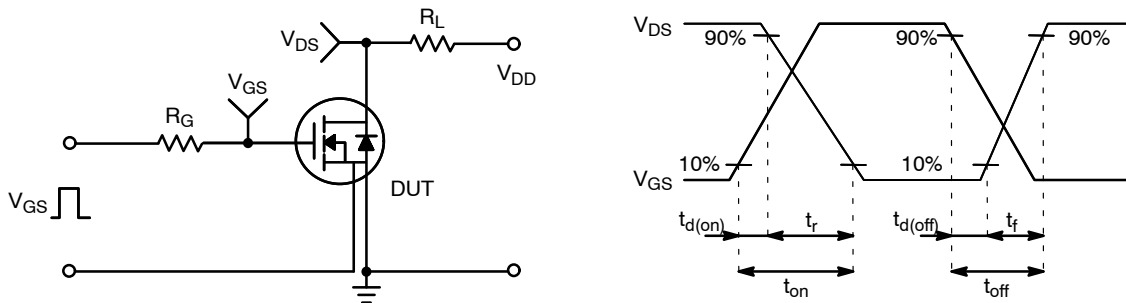


Figure 14. Resistive Switching Test Circuit & Waveforms

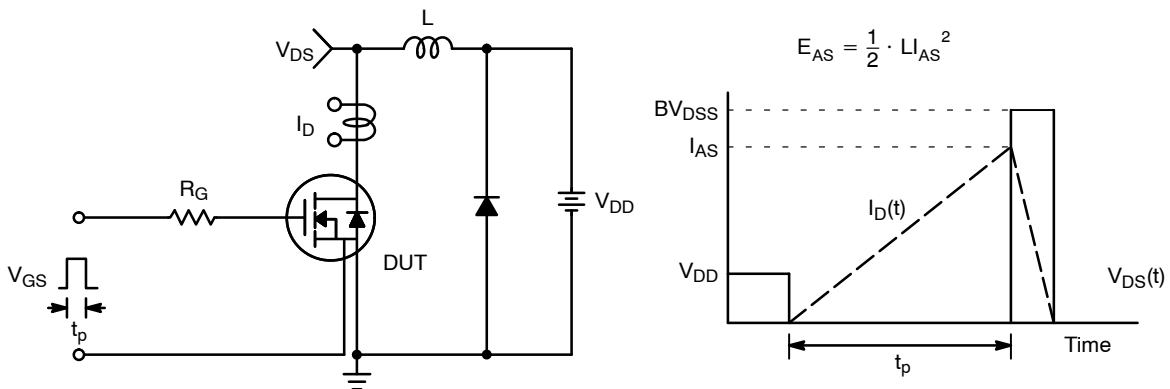


Figure 15. Unclamped Inductive Switching Test Circuit & Waveforms

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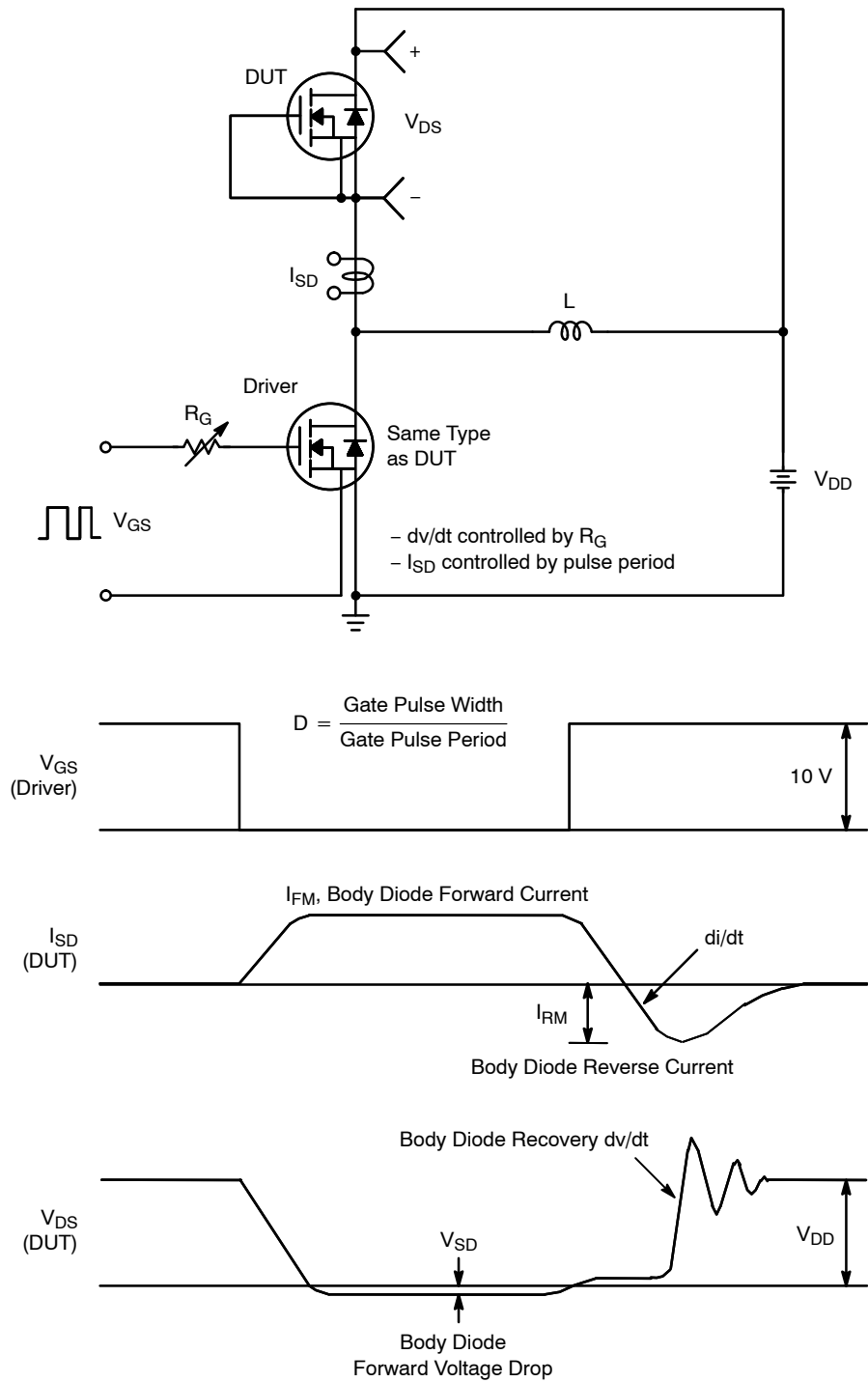
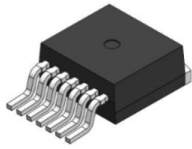
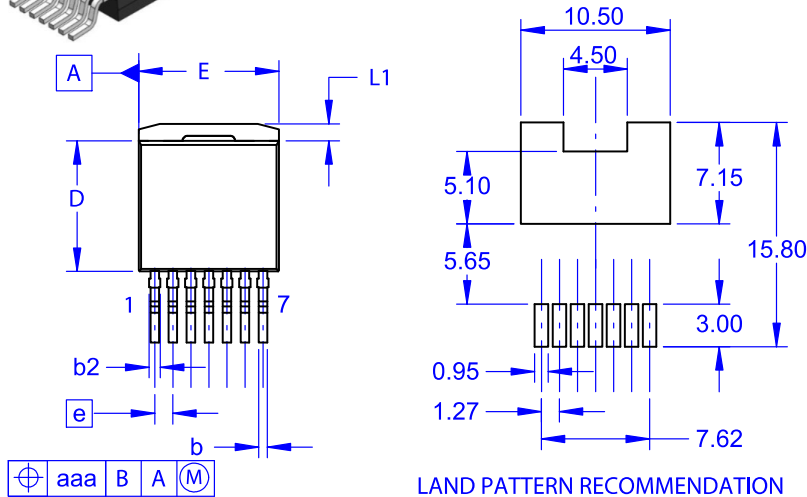


Figure 16. Peak Diode Recovery dv/dt Test Circuit & Waveforms



D²PAK7 (TO-263-7L HV)
CASE 418BJ
ISSUE B

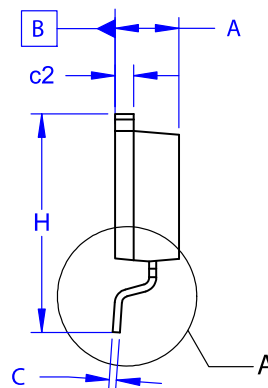
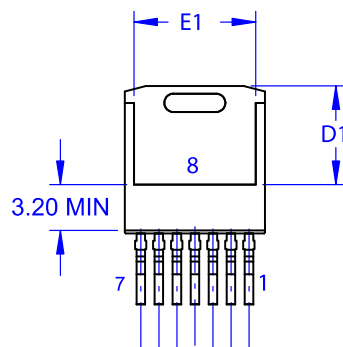
DATE 16 AUG 2019



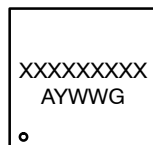
NOTES:

- A. PACKAGE CONFORMS TO JEDEC TO-263 VARIATION CB EXCEPT WHERE NOTED.
- B. ALL DIMENSIONS ARE IN MILLIMETERS.
- C. OUT OF JEDEC STANDARD VALUE.
- D. DIMENSION AND TOLERANCE AS PER ASME Y14.5-2009.
- E. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR PROTRUSIONS.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	4.30	4.50	4.70
A1	0.00	0.10	0.20
b2	0.60	0.70	0.80
b	0.51	0.60	0.70
c	0.40	0.50	0.60
c2	1.20	1.30	1.40
D	9.00	9.20	9.40
D1	6.15	6.80	7.15
E	9.70	9.90	10.20
E1	7.15	7.65	8.15
e	~	1.27	~
H	15.10	15.40	15.70
L	2.44	2.64	2.84
L1	1.00	1.20	1.40
L3	~	0.25	~
aaa	~	~	0.25

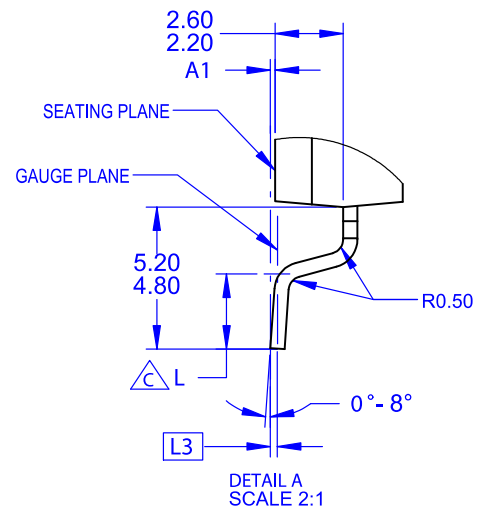


GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.



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