

NTZD3152P

MOSFET – Dual, P-Channel with ESD Protection, Small Signal, SOT-563

-20 V, -430 mA

Features

- Low $R_{DS(on)}$ Improving System Efficiency
- Low Threshold Voltage
- ESD Protected Gate
- Small Footprint 1.6 x 1.6 mm
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

- Load/Power Switches
- Power Supply Converter Circuits
- Battery Management
- Cell Phones, Digital Cameras, PDAs, Pagers, etc.

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted.)

Parameter		Symbol	Value	Unit
Drain-to-Source Voltage		V_{DS}	-20	V
Gate-to-Source Voltage		V_{GS}	± 6.0	V
Continuous Drain Current (Note 1)	Steady State	I_D	$T_A = 25^\circ\text{C}$ -430	mA
			$T_A = 85^\circ\text{C}$ -310	
Power Dissipation (Note 1)	Steady State	P_D	250	mW
Continuous Drain Current (Note 1)	$t \leq 5\text{ s}$	I_D	$T_A = 25^\circ\text{C}$ -455	mA
			$T_A = 85^\circ\text{C}$ -328	
Power Dissipation (Note 1)	$t \leq 5\text{ s}$	P_D	280	mW
Pulsed Drain Current	$t_p = 10\text{ }\mu\text{s}$	I_{DM}	-750	mA
Operating Junction and Storage Temperature		T_J, T_{STG}	-55 to 150	$^\circ\text{C}$
Source Current (Body Diode)		I_S	-350	mA
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)		T_L	260	$^\circ\text{C}$

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Unit
Junction-to-Ambient – Steady State (Note 1)	$R_{\theta JA}$	500	$^\circ\text{C/W}$
Junction-to-Ambient – $t \leq 5\text{ s}$ (Note 1)		447	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

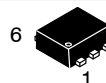
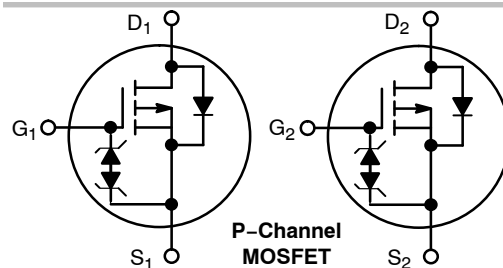
1. Surface mounted on FR4 board using 1 in. sq. pad size
(Cu. area = 1.127 in. sq. [1 oz.] including traces).



ON Semiconductor®

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$V_{(BR)DS}$	$R_{DS(on)}$ Typ	I_D Max
-20 V	0.5 Ω @ -4.5 V	-430 mA
	0.6 Ω @ -2.5 V	
	1.0 Ω @ -1.8 V	

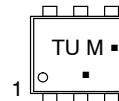


**SOT-563-6
CASE 463A**

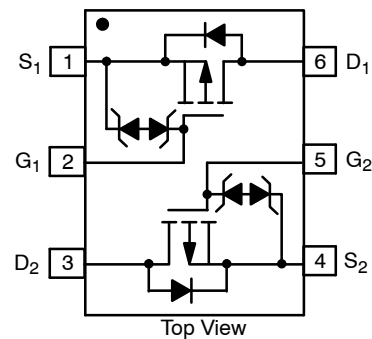
TU = Specific Device Code
M = Date Code
■ = Pb-Free Package

(Note: Microdot may be in either location)

MARKING DIAGRAM



PINOUT: SOT-563



Top View

ORDERING INFORMATION

Device	Package	Shipping†
NTZD3152PT1G	SOT-563	4000 / Tape & Reel
NTZD3152PT1H	(Pb-Free)	
NTZD3152PT5H	SOT-563 (Pb-Free)	8000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NTZD3152P

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted.)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = -250\text{ }\mu\text{A}$	-20			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$			18		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	$V_{GS} = 0\text{ V}, V_{DS} = -16\text{ V}$	$T_J = 25^\circ\text{C}$		-1.0	μA
			$T_J = 125^\circ\text{C}$		-2.0	
Gate-to-Source Leakage Current	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 4.5\text{ V}$			± 2.0	μA

ON CHARACTERISTICS (Note 2)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = -250\text{ }\mu\text{A}$	-0.45		-1.0	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$			-1.9		mV/°C
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = -4.5\text{ V}, I_D = -430\text{ mA}$		0.5	0.9	Ω
		$V_{GS} = -2.5\text{ V}, I_D = -300\text{ mA}$		0.6	1.2	
		$V_{GS} = -1.8\text{ V}, I_D = -150\text{ mA}$		1.0	2.0	
Forward Transconductance	g_{FS}	$V_{DS} = -10\text{ V}, I_D = -430\text{ mA}$		1.0		S

CHARGES AND CAPACITANCES

Input Capacitance	C_{ISS}	$V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}, V_{DS} = -16\text{ V}$		105	175	pF
Output Capacitance	C_{OSS}			15	30	
Reverse Transfer Capacitance	C_{RSS}			10	20	
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = -4.5\text{ V}, V_{DS} = -10\text{ V}, I_D = -215\text{ mA}$		1.7	2.5	nC
Threshold Gate Charge	$Q_{G(TH)}$			0.1		
Gate-to-Source Charge	Q_{GS}			0.3		
Gate-to-Drain Charge	Q_{GD}			0.4		

SWITCHING CHARACTERISTICS (Note 3)

Turn-On Delay Time	$t_{d(on)}$	$V_{GS} = -4.5\text{ V}, V_{DD} = -10\text{ V}, I_D = -215\text{ mA}, R_G = 10\text{ }\Omega$		10		ns
Rise Time	t_r			12		
Turn-Off Delay Time	$t_{d(off)}$			35		
Fall Time	t_f			19		

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V_{SD}	$V_{GS} = 0\text{ V}, I_S = -350\text{ mA}$	$T_J = 25^\circ\text{C}$		-0.8	-1.2	V
Reverse Recovery Time	t_{RR}	$V_{GS} = 0\text{ V}, dI_{SD}/dt = 100\text{ A}/\mu\text{s}, I_S = -350\text{ mA}$			13		ns

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Pulse Test: pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.

3. Switching characteristics are independent of operating junction temperatures.

TYPICAL PERFORMANCE CURVES ($T_J = 25^\circ\text{C}$ unless otherwise noted)

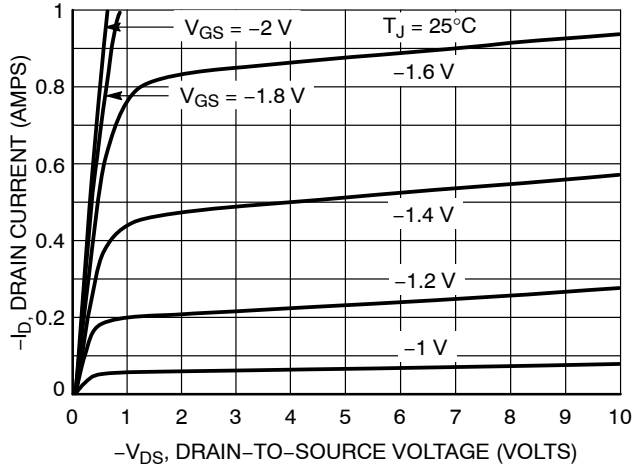


Figure 1. On-Region Characteristics

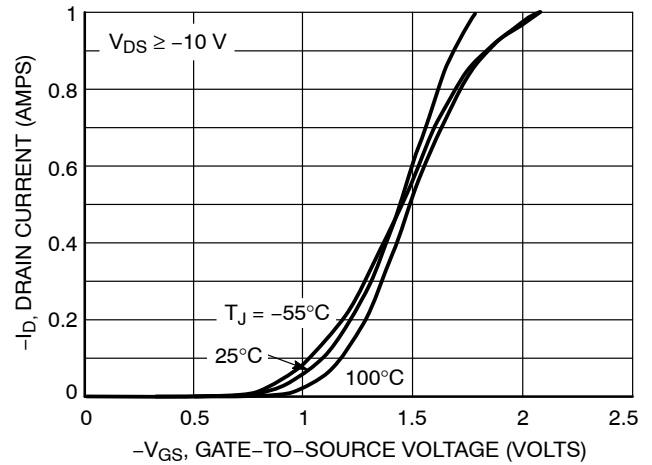


Figure 2. Transfer Characteristics

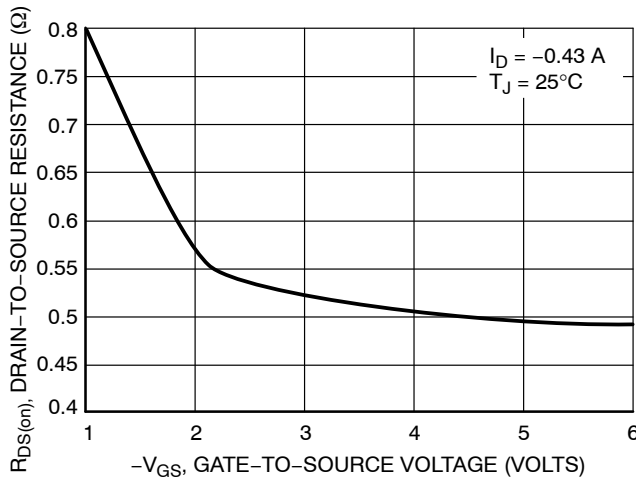


Figure 3. On-Resistance vs. Gate-to-Source Voltage

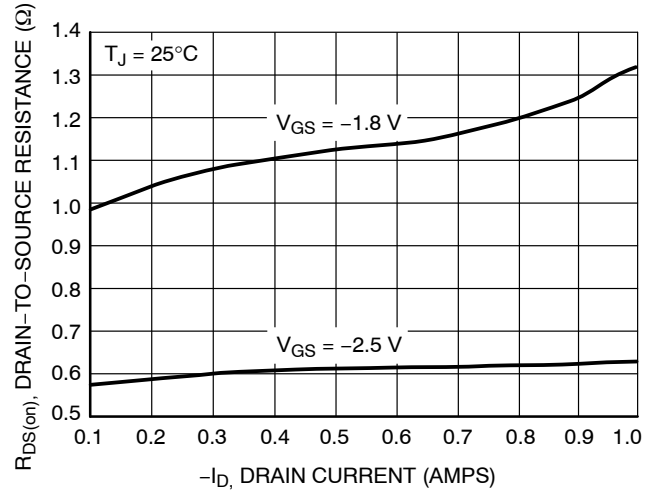


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

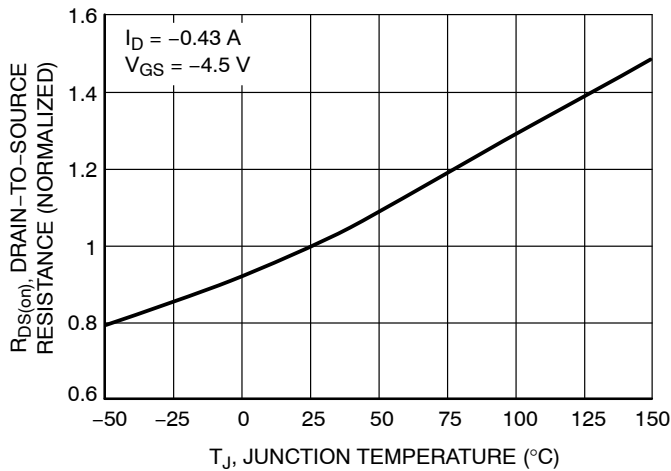


Figure 5. On-Resistance Variation with Temperature

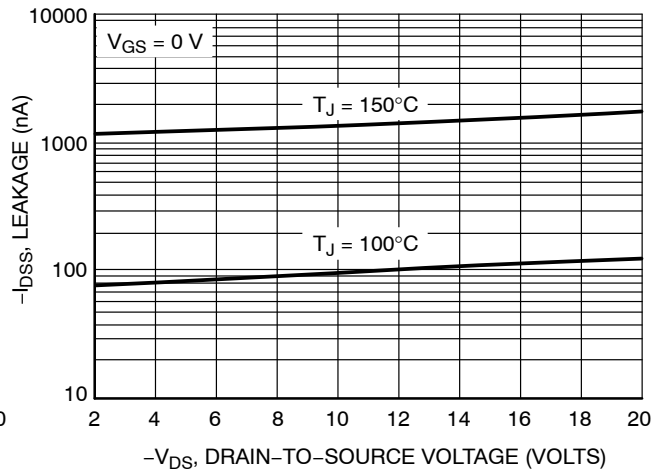


Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL PERFORMANCE CURVES ($T_J = 25^\circ\text{C}$ unless otherwise noted)

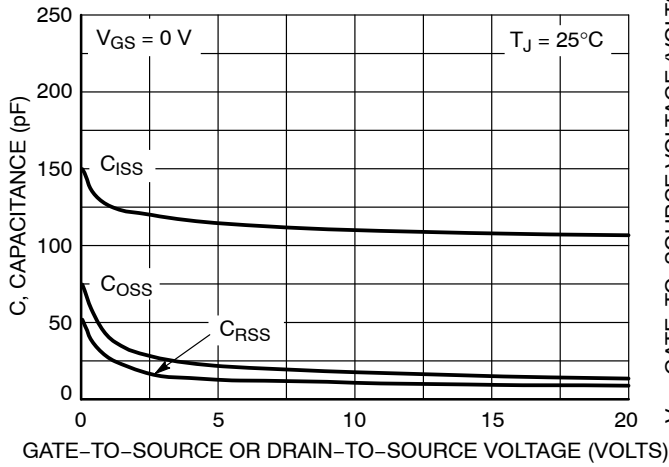


Figure 7. Capacitance Variation

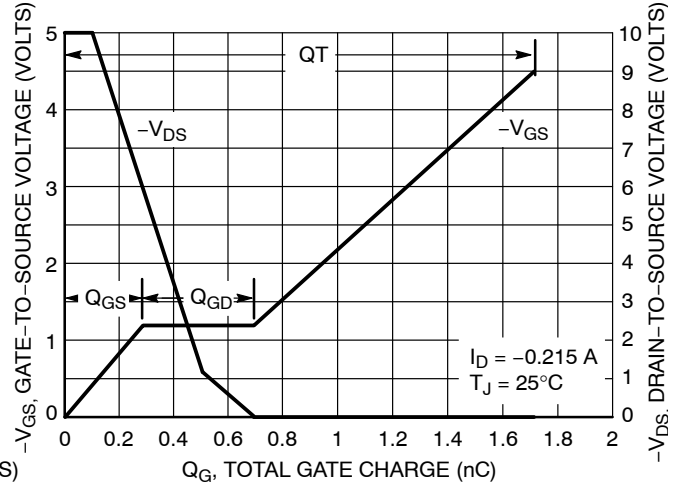


Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

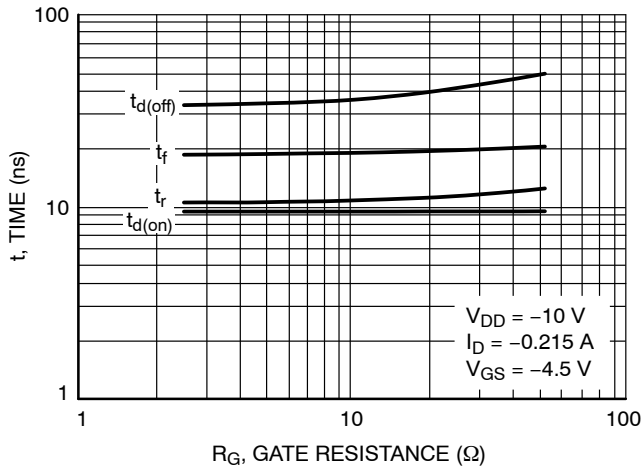


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

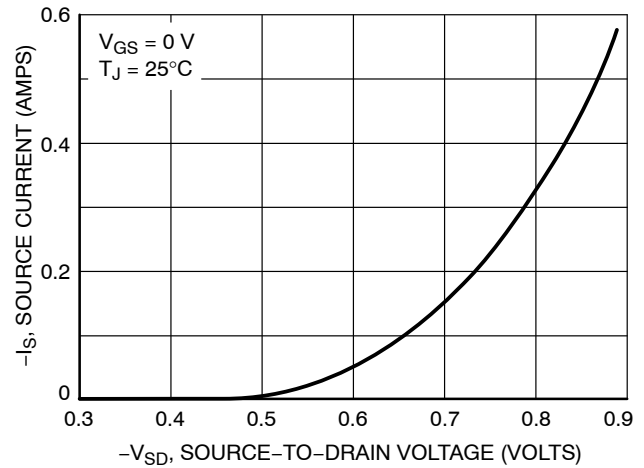


Figure 10. Diode Forward Voltage vs. Current

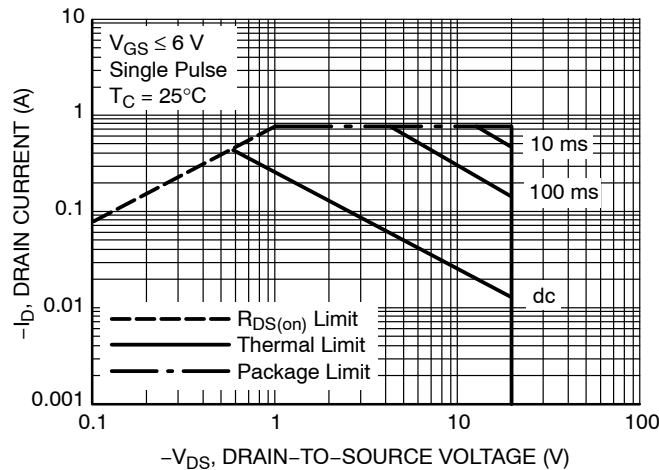
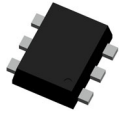


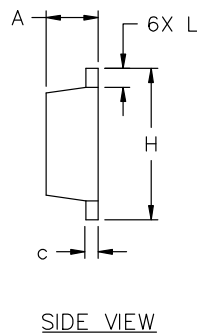
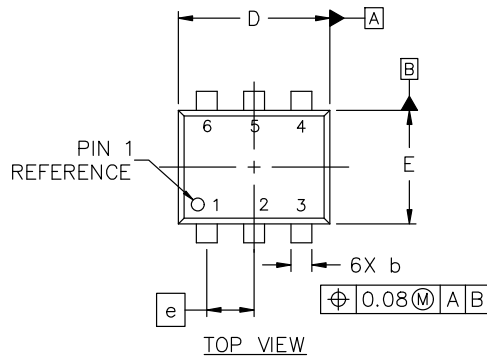
Figure 11. Safe Operating Area


SOT-563-6 1.60x1.20x0.55, 0.50P
CASE 463A
ISSUE J

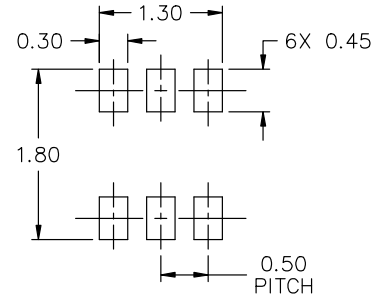
15 FEB 2024

NOTES:

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5-2018.
2. ALL DIMENSION ARE IN MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

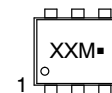


DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.50	0.55	0.60
b	0.17	0.22	0.27
c	0.08	0.13	0.18
D	1.50	1.60	1.70
E	1.10	1.20	1.30
e	0.50 BSC		
H	1.50	1.60	1.70
L	0.10	0.20	0.30



RECOMMENDED MOUNTING FOOTPRINT*

* FOR ADDITIONAL INFORMATION ON OUR Pb-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERM/D.

GENERIC MARKING DIAGRAM*


XX = Specific Device Code

M = Month Code

▪ = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLE 1:
PIN 1. EMITTER 1
2. BASE 1
3. COLLECTOR 2
4. EMITTER 2
5. BASE 2
6. COLLECTOR 1

STYLE 2:
PIN 1. EMITTER 1
2. EMITTER 2
3. BASE 2
4. COLLECTOR 2
5. BASE 1
6. COLLECTOR 1

STYLE 3:
PIN 1. CATHODE 1
2. CATHODE 1
3. ANODE/ANODE 2
4. CATHODE 2
5. CATHODE 2
6. ANODE/ANODE 1

STYLE 4:
PIN 1. COLLECTOR
2. COLLECTOR
3. BASE
4. EMITTER
5. COLLECTOR
6. COLLECTOR

STYLE 5:
PIN 1. CATHODE
2. CATHODE
3. ANODE
4. ANODE
5. CATHODE
6. CATHODE

STYLE 6:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE

STYLE 7:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. CATHODE
5. ANODE
6. CATHODE

STYLE 8:
PIN 1. DRAIN
2. DRAIN
3. GATE
4. SOURCE
5. DRAIN
6. DRAIN

STYLE 9:
PIN 1. SOURCE 1
2. GATE 1
3. DRAIN 2
4. SOURCE 2
5. GATE 2
6. DRAIN 1

STYLE 10:
PIN 1. CATHODE 1
2. N/C
3. CATHODE 2
4. ANODE 2
5. N/C
6. ANODE 1

STYLE 11:
PIN 1. EMITTER 2
2. BASE 2
3. COLLECTOR 1
4. EMITTER 1
5. BASE 1
6. COLLECTOR 2

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