

# MOSFET – Power, Single N-Channel, SO-8FL

30 V, 0.65 mΩ, 409 A

# NTMFS0D7N03CG

#### **Features**

- Wide SOA to Improve Inrush Current Management
- Advanced Package (5x6mm) with Excellent Thermal Conduction
- Ultra Low R<sub>DS(on)</sub> to Improve System Efficiency
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

# **Applications**

- Hot Swap Application
- Power Load Switch
- Battery Management and Protection

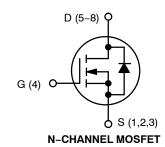
# MAXIMUM RATINGS (T<sub>J</sub> = 25°C unless otherwise stated)

Parameter			Symbol	Value	Unit
Drain-to-Source Voltage			$V_{DSS}$	30	V
Gate-to-Source Volta	ge		V <sub>GS</sub>	±20	V
Continuous Drain		T <sub>C</sub> = 25°C	I <sub>D</sub>	409	Α
Current R <sub>θJC</sub> (Note 2)	Steady State	T <sub>C</sub> =100°C		289	
Power Dissipation R <sub>θJC</sub> (Note 2)	State	T <sub>C</sub> = 25°C	P <sub>D</sub>	187	W
Continuous Drain		T <sub>A</sub> = 25°C	I <sub>D</sub>	59	Α
Current R <sub>θJA</sub> (Notes 1, 2)	Steady	T <sub>A</sub> = 100°C		42	
Power Dissipation R <sub>0JA</sub> (Notes 1, 2)	State	T <sub>A</sub> = 25°C	P <sub>D</sub>	4.0	W
Pulsed Drain Current	T <sub>A</sub> = 25°	'C, t <sub>p</sub> = 10 μs	I <sub>DM</sub>	900	Α
Source Current (Body Diode)			I <sub>S</sub>	155	Α
Single Pulse Drain-to-Source Avalanche Energy (I <sub>L</sub> = 40.8 A <sub>pk</sub> )			E <sub>AS</sub>	1080	mJ
Operating Junction and Storage Temperature Range			T <sub>J</sub> , T <sub>STG</sub>	–55 to +175	°C
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)			T <sub>L</sub>	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

- 1. Surface–mounted on FR4 board using 1 in<sup>2</sup> pad, 2 oz Cu pad.
- The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.

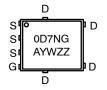
V <sub>(BR)DSS</sub>	R <sub>DS(ON)</sub> MAX	I <sub>D</sub> MAX	
30 V	0.65 m $\Omega$ @ 10 V	409 A	





DFN5 (SO-8FL) CASE 506EZ

# **MARKING DIAGRAMS**



A = Assembly Location

Y = Year
W = Work Week
ZZ = Lot Traceability

# **ORDERING INFORMATION**

See detailed ordering, marking and shipping information in the package dimensions section on page 5 of this data sheet.

# THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Case - Steady State (Note 1)	$R_{ heta JC}$	0.8	°C/W
Junction-to-Ambient - Steady State (Note 1)	$R_{ heta JA}$	38	C/VV
Junction-to-Ambient - Steady State (Note 2)	$R_{\theta JA}$	134	°C/W

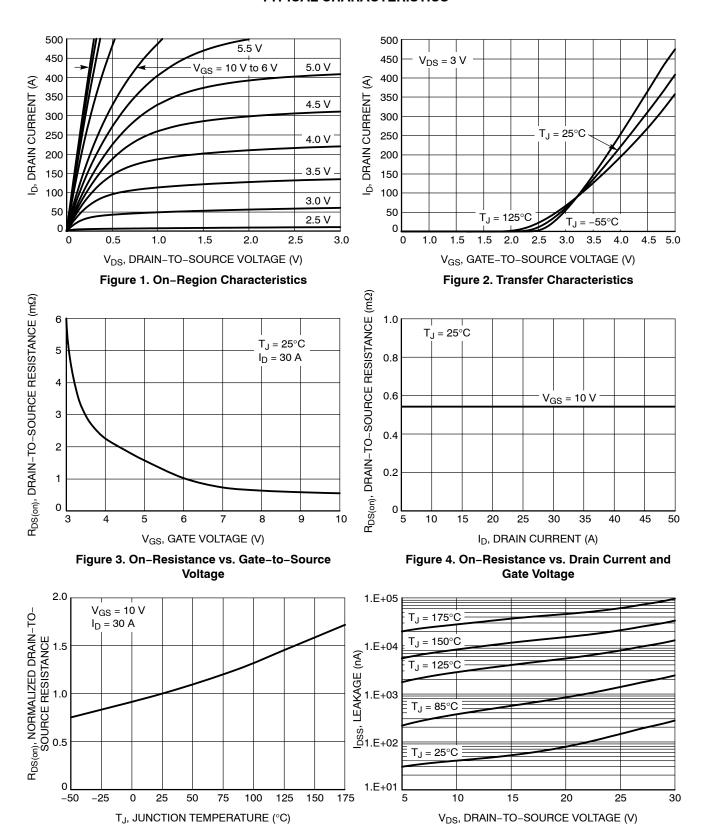
# **ELECTRICAL CHARACTERISTICS** (T<sub>J</sub> = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition		Min	Тур	Max	Unit
OFF CHARACTERISTICS							
Drain-to-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$		30			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V <sub>(BR)DSS</sub> /	I <sub>D</sub> = 250 μA. ref to 25°C			11		mV/°C
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	$V_{GS} = 0 \text{ V}, \qquad T_{J} = 25^{\circ}\text{C}$				1.0	
		V <sub>DS</sub> = 30 V	T <sub>J</sub> = 125°C			100	μΑ
Gate-to-Source Leakage Current	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>G</sub>	<sub>S</sub> = 20 V			100	nA
ON CHARACTERISTICS (Note 3)							
Gate Threshold Voltage	V <sub>GS(TH)</sub>	$V_{GS} = V_{DS}, I_D$	= 280 μΑ	1.3		2.2	V
Threshold Temperature Coefficient	V <sub>GS(TH)</sub> /T <sub>J</sub>	I <sub>D</sub> = 280 μA. re	of to 25°C		-5.1		mV/°C
Drain-to-Source On Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>I</sub>	<sub>O</sub> = 30 A		0.55	0.65	mΩ
Forward Transconductance	9 <sub>FS</sub>	$V_{DS} = 3 \text{ V}, I_{D}$	= 30 A		100		S
Gate Resistance	$R_{G}$	T <sub>A</sub> = 25°C			0.4	3.0	Ω
CHARGES AND CAPACITANCES							
Input Capacitance	C <sub>ISS</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 15 V, f = 1 MHz		8600	12300	16000	pF
Output Capacitance	C <sub>OSS</sub>			4000	5800	7500	
Reverse Transfer Capacitance	C <sub>RSS</sub>			50	88	360	
Total Gate Charge	Q <sub>G(TOT)</sub>	V <sub>GS</sub> = 10 V, V <sub>DS</sub> = 15 V; I <sub>D</sub> = 30 A		103	147	191	nC
Threshold Gate Charge	Q <sub>G(TH)</sub>			13	19	25	
Gate-to-Source Charge	Q <sub>GS</sub>			24	34	44	
Gate-to-Drain Charge	$Q_{GD}$			5.2	8.6	20.5	
SWITCHING CHARACTERISTICS (Note 4	4)						
Turn-On Delay Time	t <sub>d(ON)</sub>				28		
Rise Time	t <sub>r</sub>	$V_{GS}$ = 10 V, $V_{D}$	s = 15 V,		13		
Turn-Off Delay Time	t <sub>d(OFF)</sub>	$I_D = 30 \text{ A}, R_G = 3.0 \Omega$			85		ns
Fall Time	t <sub>f</sub>				16		
DRAIN-SOURCE DIODE CHARACTERIS	TICS						
Forward Diode Voltage	$V_{SD}$	V <sub>GS</sub> = 0 V,	T <sub>J</sub> = 25°C		0.78	1.2	V
			T <sub>J</sub> = 125°C		0.62		V
Reverse Recovery Time	t <sub>RR</sub>	V <sub>GS</sub> = 0 V, dIS/dt = 100 A/μs,			98		ns
Reverse Recovery Charge	Q <sub>RR</sub>	$V_{DS} = 15 \text{ V}, I_S = 30 \text{ A}$			143		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions. 3. Pulse Test: pulse width  $\leq$  300  $\mu$ s, duty cycle  $\leq$  2%.

<sup>4.</sup> Switching characteristics are independent of operating junction temperatures.

### TYPICAL CHARACTERISTICS



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Figure 5. On-Resistance Variation with

**Temperature** 

Figure 6. Drain-to-Source Leakage Current vs. Voltage

# **TYPICAL CHARACTERISTICS**

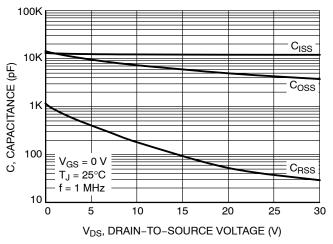


Figure 7. Capacitance Variation

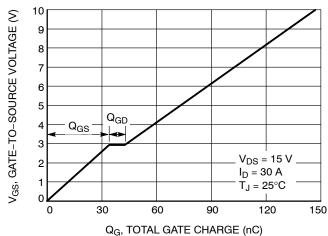


Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

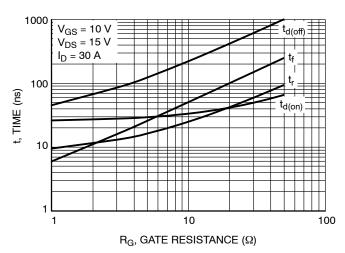


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

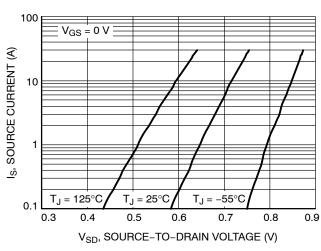


Figure 10. Diode Forward Voltage vs. Current

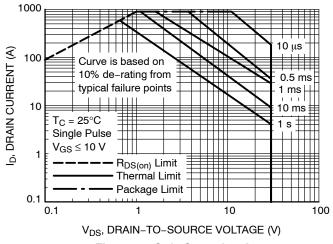


Figure 11. Safe Operating Area

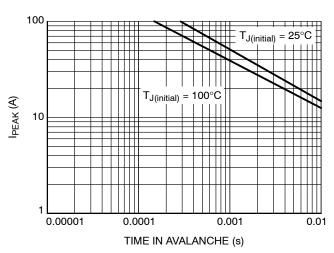


Figure 12. I<sub>PEAK</sub> vs. Time in Avalanche

# **TYPICAL CHARACTERISTICS**

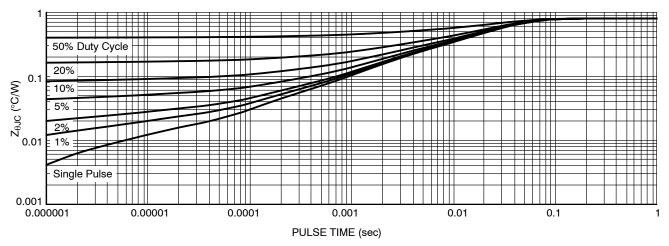


Figure 13. Thermal Impedance

# **DEVICE ORDERING INFORMATION**

Device	Marking	Package	Shipping <sup>†</sup>
NTMFS0D7N03CGT1G	0D7NG	DFN5 (Pb-Free)	1500 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.





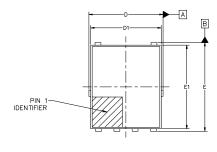
// 0.10 C

△ 0.10 C

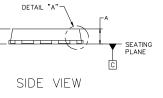
# DFN5, 4.90 x 5.90 x 1.00, 1.27P CASE 506EZ **ISSUE B**

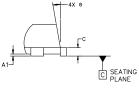
# **DATE 16 SEP 2024**

- DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
- CONTROLLING DIMENSION: MILLIMETERS.
  DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.



TOP VIEW

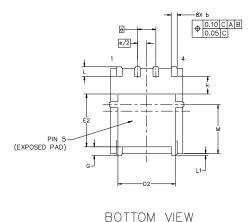




SCALED 2:1

DETAIL "A"

MILLIMETERS						
DIM	MIN	NOM	MAX			
А	0.90	1.00	1.10			
Α1	0.00		0.05			
b	0.33	0.41	0.51			
С	0.23	0.28	0.33			
D	5.00	5.15	5.30			
D1	4.70	4.90	5.10			
D2	3.80	4.00	4.20			
Е	6.00	6.15	6.30			
E1	5.70	5.90	6.10			
E2	3.45	3.80	3.85			
е	1	.27 BSC	)			
G	0.51	0.575	0.71			
k	1.10	1.20	1.40			
L	0.51	0.575	0.71			
L1	0.125 REF					
М	3.00	3.40	3.80			
Θ	0.		12°			



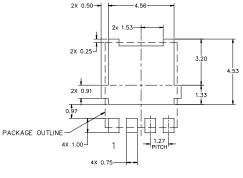
**GENERIC MARKING DIAGRAM\*** 



XXXXXX	= Specific Device Code
Α	= Assembly Location

Υ = Year W = Work Week 77 = Lot Traceability

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot " ■", may or may not be present. Some products may not follow the Generic Marking.



# RECOMMENDED MOUNTING FOOTPRINT

\*For additional information on our Pb-Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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DESCRIPTION:	DFN5, 4.90 x 5.90 x 1.00, 1.27P		PAGE 1 OF 1	

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