

MOSFET – N-Channel, Field Effect Transistor, Enhancement Mode

NDP6060 / NDB6060

General Description

These N-Channel enhancement mode power field effect transistors are produced using onsemi's proprietary, high cell density, DMOS technology. This very high density process has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulses in the avalanche and commutation modes. These devices are particularly suited for low voltage applications such as automotive, DC/DC converters, PWM motor controls, and other battery powered circuits where fast switching, low in-line power loss, and resistance to transients are needed.

Features

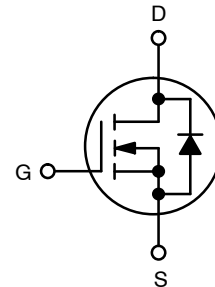
- 48 A, 60 V
 - ♦ $R_{DS(ON)} = 0.025 \text{ m}\Omega @ V_{GS} = 10 \text{ V}$
- Critical DC Electrical Parameters Specified at Elevated Temperature
- Rugged Internal Source-Drain Diode Can Eliminate the Need for an External Zener Diode Transient Suppressor
- 175°C Maximum Junction Temperature Rating
- High Density Cell Design for Extremely Low $R_{DS(ON)}$
- TO-220 Package for Both Through Hole and Surface Mount Applications
- This is a Halide Free Device

MAXIMUM RATINGS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

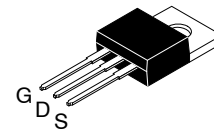
Symbol	Rating	NDP6060	Unit
V_{DSS}	Drain-Source Voltage	60	V
V_{DGR}	Drain-Gate Voltage ($R_{GS} \leq 1 \text{ M}\Omega$)	60	V
V_{GSS}	Drain-Source Voltage – Continuous – Nonrepetitive ($t_p < 50 \mu\text{s}$)	± 20 ± 40	V
I_D	Drain Current – Continuous $T_C = 25^\circ\text{C}$ – Continuous $T_C = 100^\circ\text{C}$ – Pulsed	48 32 144	A
P_D	Total Power Dissipation @ $T_C = 25^\circ\text{C}$ – Derate above 25°C	100 0.67	W W/°C
T_J, T_{STG}	Operating and Storage Temperature Range	–65 to 175	°C
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	275	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

V_{DSS}	$R_{DS(ON)} \text{ MAX}$	$I_D \text{ MAX}$
60 V	0.025 m Ω @ 10 V	48 A

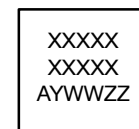


N-CHANNEL MOSFET



TO-220-3LD
CASE 340AT

MARKING DIAGRAM



XXXX = Specific Device Code
 A = Assembly Location
 Y = Year
 WW = Work Week
 ZZ = Assembly Lot Code

ORDERING INFORMATION

Device	Package	Shipping [†]
NDP6060	TO-220-3LD (Halide Free)	800 / Units / Tube

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, [BRD8011/D](#).

NDP6060 / NDB6060

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
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DRAIN-SOURCE AVALANCHE RATINGS (Note 1)

W_{DSS}	Single Pulse Drain-Source Avalanche Energy	$V_{DD} = 25\text{ V}$, $I_D = 48\text{ A}$	–	–	200	mJ
I_{AR}	Maximum Drain-Source Avalanche Current		–	–	48	A

OFF CHARACTERISTICS

BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}$, $I_D = 250\text{ }\mu\text{A}$	60	–	–	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 60\text{ V}$, $V_{GS} = 0\text{ V}$	–	–	250	μA
		$T_J = 125^\circ\text{C}$	–	–	1	mA
I_{GSSF}	Gate-Body Leakage, Forward	$V_{GS} = 20\text{ V}$, $V_{DS} = 0\text{ V}$	–	–	100	nA
I_{GSSR}	Gate-Body Leakage, Reverse	$V_{GS} = -20\text{ V}$, $V_{DS} = 0\text{ V}$	–	–	-100	nA

ON CHARACTERISTICS (Note 1)

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	2	2.9	4	V
		$T_J = 125^\circ\text{C}$	1.4	2.3	3.6	
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}$, $I_D = 24\text{ A}$	–	0.02	0.025	W
		$T_J = 125^\circ\text{C}$	–	0.032	0.04	
$I_{D(on)}$	On-State Drain Current	$V_{GS} = 10\text{ V}$, $V_{DS} = 10\text{ V}$	48	–	–	A
g_{FS}	Forward Transconductance	$V_{DS} = 10\text{ V}$, $I_D = 24\text{ A}$	10	19	–	S

DYNAMIC CHARACTERISTICS

C_{iss}	Input Capacitance	$V_{DS} = 25\text{ V}$, $V_{GS} = 0\text{ V}$, $f = 1.0\text{ MHz}$	–	1190	1800	pF
C_{oss}	Output Capacitance		–	475	800	pF
C_{rss}	Reverse Transfer Capacitance		–	150	400	pF

SWITCHING CHARACTERISTICS (Note 1)

$t_{D(on)}$	Turn – On Delay Time	$V_{DD} = 30\text{ V}$, $I_D = 48\text{ A}$, $V_{GS} = 10\text{ V}$, $R_{GEN} = 7.5\text{ W}$	–	10	20	nS
t_r	Turn – On Rise Time		–	145	300	nS
$t_{D(off)}$	Turn – Off Delay Time		–	28	60	nS
t_f	Turn – Off Fall Time		–	77	150	nS
Q_g	Total Gate Charge	$V_{DS} = 48\text{ V}$, $I_D = 48\text{ A}$, $V_{GS} = 10\text{ V}$	–	39	70	nC
Q_{gs}	Gate-Source Charge		–	7.6	–	nC
Q_{gd}	Gate-Drain Charge		–	22	–	nC

DRAIN-SOURCE DIODE CHARACTERISTICS

I_S	Maximum Continuous Drain-Source Diode Forward Current		–	–	48	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current		–	–	144	A
V_{SD}	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}$, $I_S = 24\text{ A}$ (Note 1)	–	0.9	1.3	V
		$T_J = 125^\circ\text{C}$	–	0.8	1.2	
t_{rr}	Reverse Recovery Time	$V_{GS} = 0\text{ V}$, $I_F = 48\text{ A}$, $dI_F/dt = 100\text{ A}/\mu\text{s}$	35	87	140	ns
I_{rr}	Reverse Recovery Current		2	3.6	8	A

THERMAL CHARACTERISTICS

$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	–	–	1.5	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	–	–	62.5	$^\circ\text{C}/\text{W}$

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. Pulse Test: pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.

TYPICAL CHARACTERISTICS

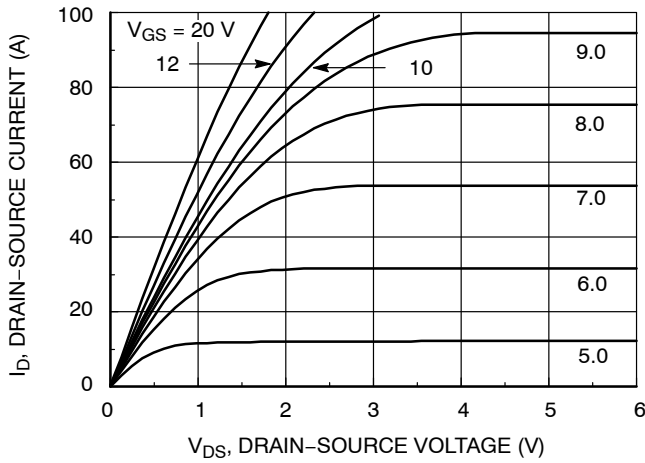


Figure 1. On-Region Characteristics

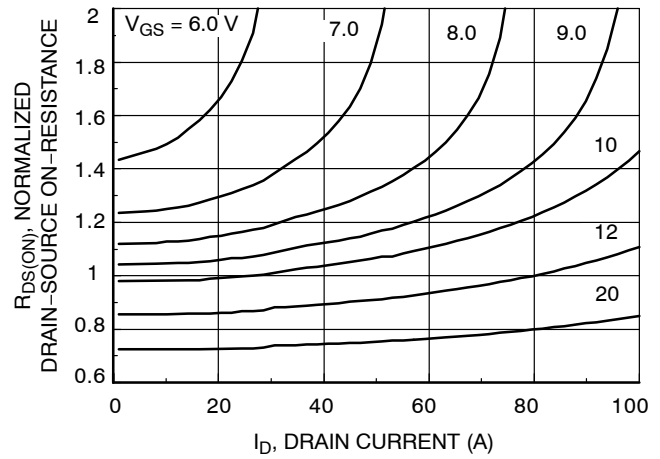


Figure 2. On-Resistance Variation with Gate Voltage and Drain Current

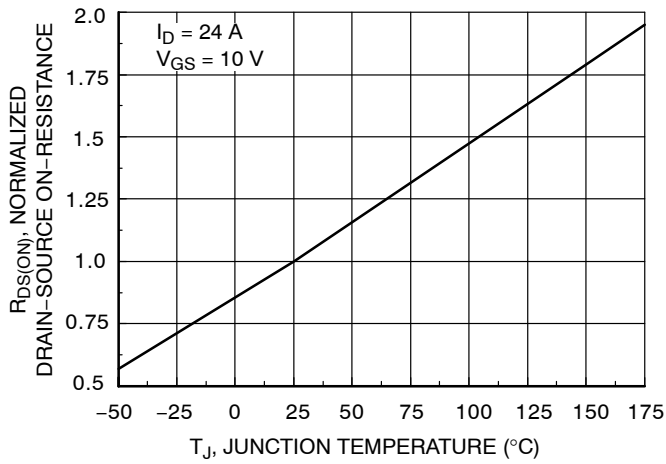


Figure 3. On-Resistance Variation with Temperature

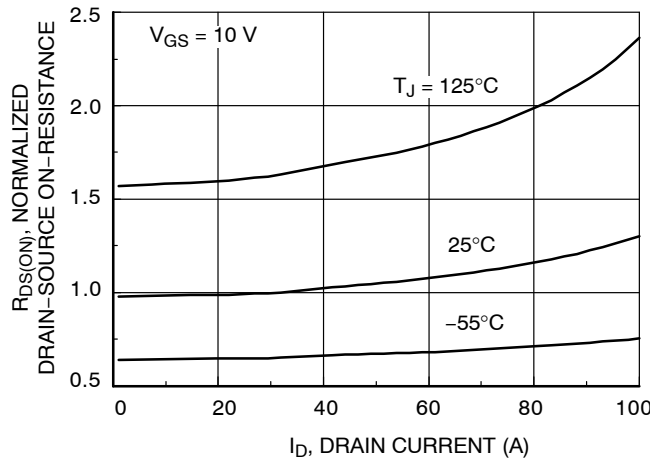


Figure 4. On-Resistance Variation with Drain Current and Temperature

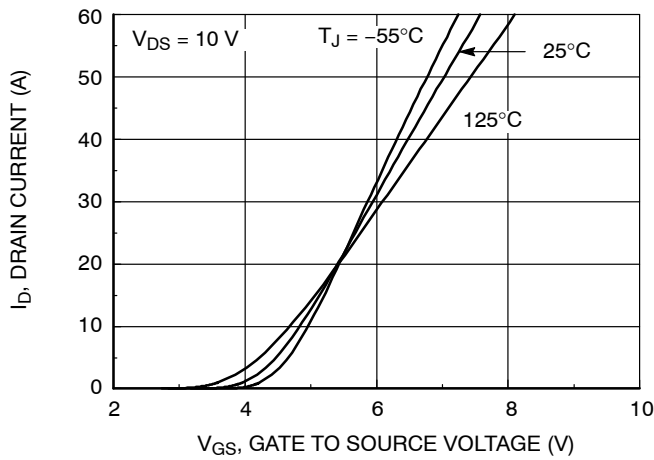


Figure 5. Transfer Characteristics

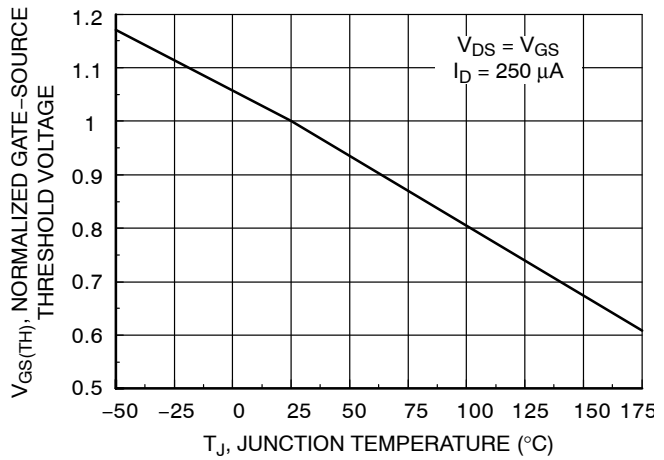


Figure 6. Gate Threshold Variation with Temperature

TYPICAL CHARACTERISTICS (continued)

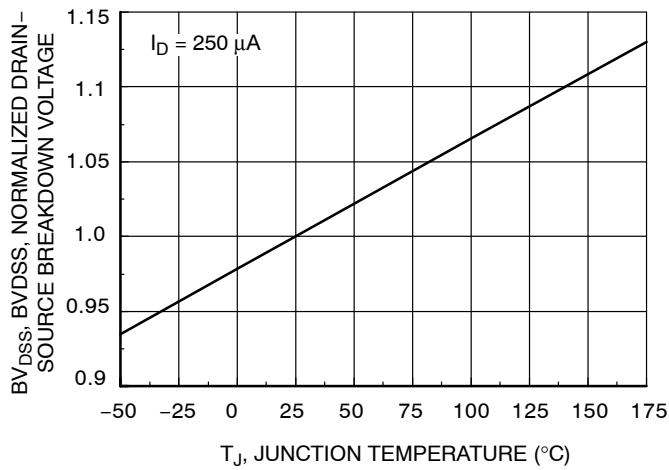


Figure 7. Breakdown Voltage Variation with Temperature

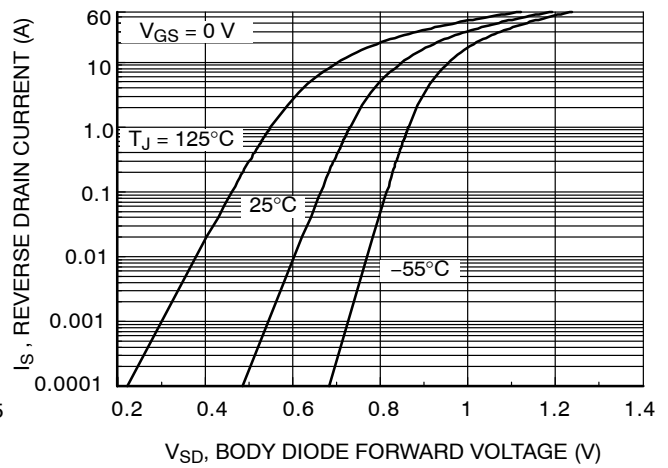


Figure 8. Body Diode Forward Voltage Variation with Current and Temperature

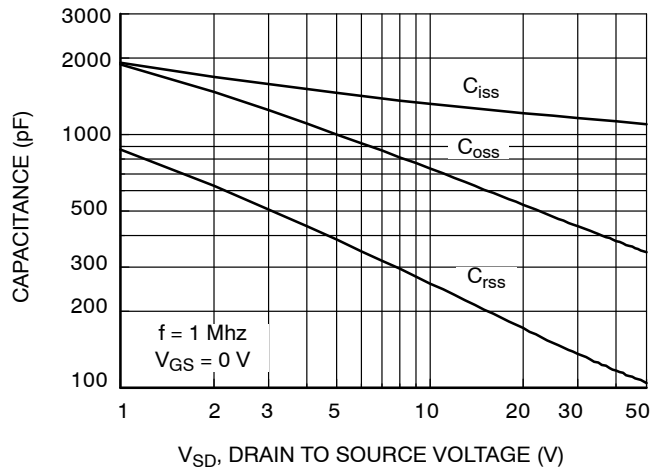


Figure 9. Capacitance Characteristics

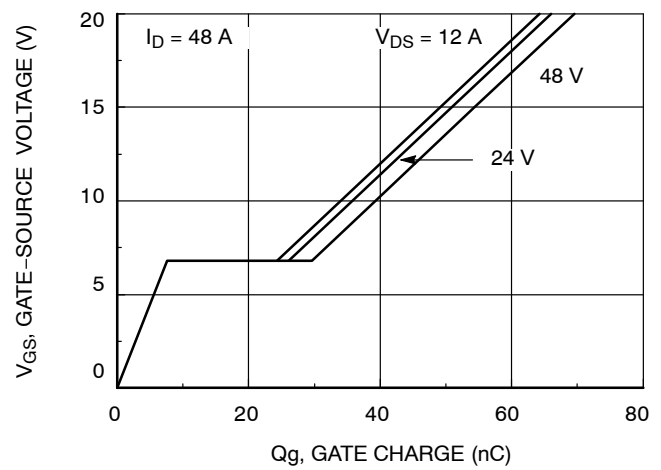


Figure 10. Gate Charge Characteristics

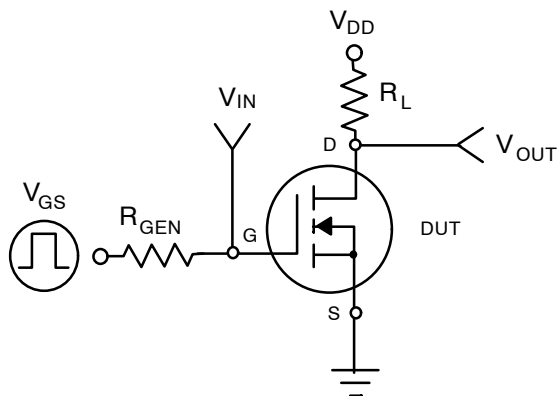


Figure 11. Switching Test Circuit

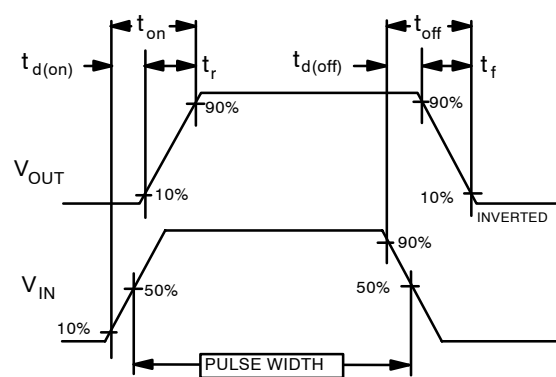


Figure 12. Switching Waveforms

TYPICAL CHARACTERISTICS

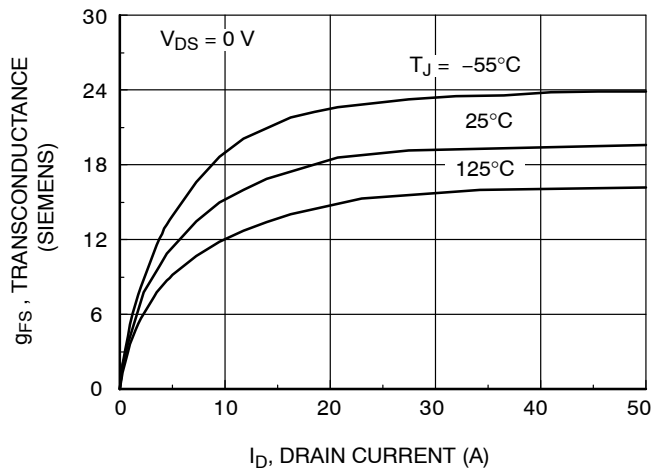


Figure 13. Transconductance Variation with Drain Current and Temperature

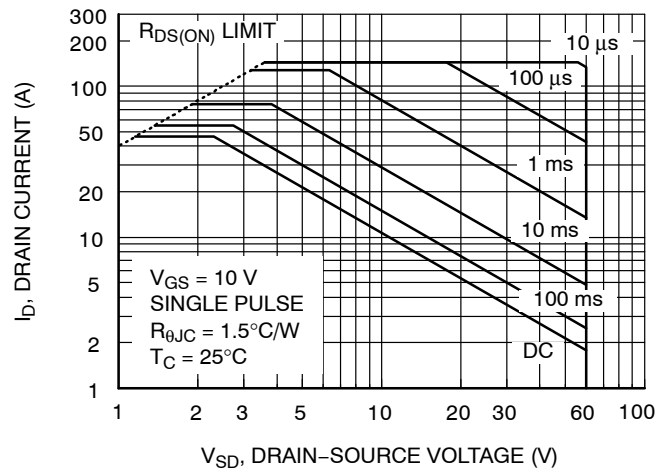


Figure 14. Maximum Safe Operating Area

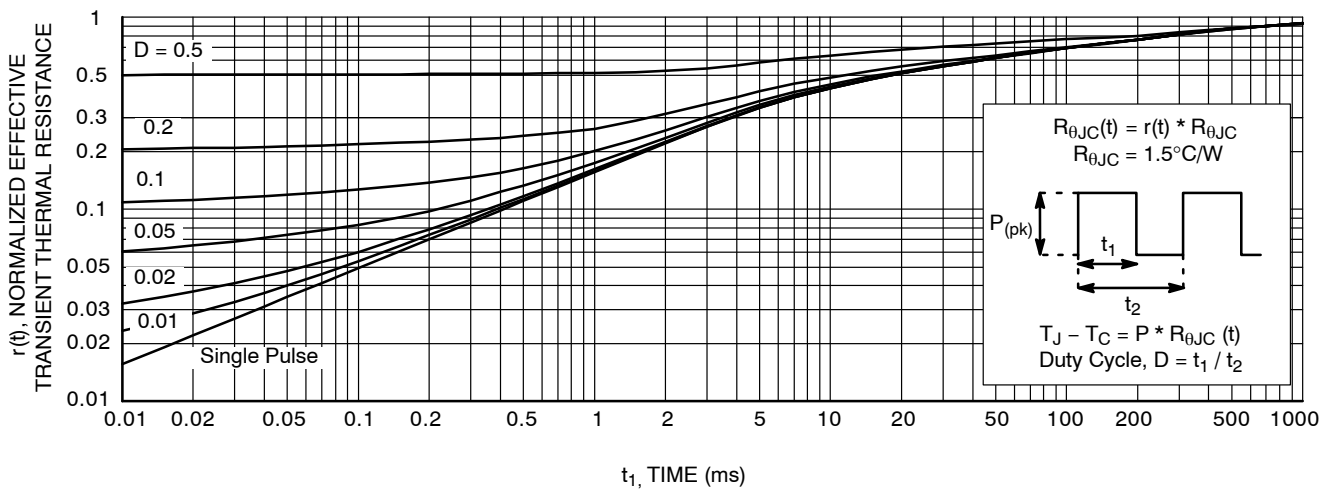
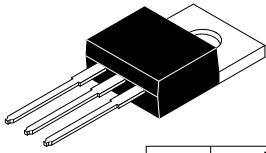


Figure 15. Transient Thermal Response Curve



TO-220-3LD
CASE 340AT
ISSUE B

DATE 08 AUG 2022

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	4.00	--	4.70
A1	SEE NOTE "F"		
A2	2.10	--	2.85
b	0.55	--	1.00
b2	1.10	--	1.62
b4	1.42	--	1.62
c	0.36	--	0.60
D	13.90	--	16.30
D1	8.13	--	9.40
D2	11.50	--	14.30
D3	15.42	--	16.51
E	9.65	--	10.67
E1	7.59	--	8.65
e	2.40	--	2.67
H1	6.06	--	6.69
L	12.70	--	14.04
L1	2.70	--	4.10
P	3.50	--	4.00
Q	2.50	--	3.40
z	2.13 REF		
z1	2.06 REF		
θ	3°	--	5°

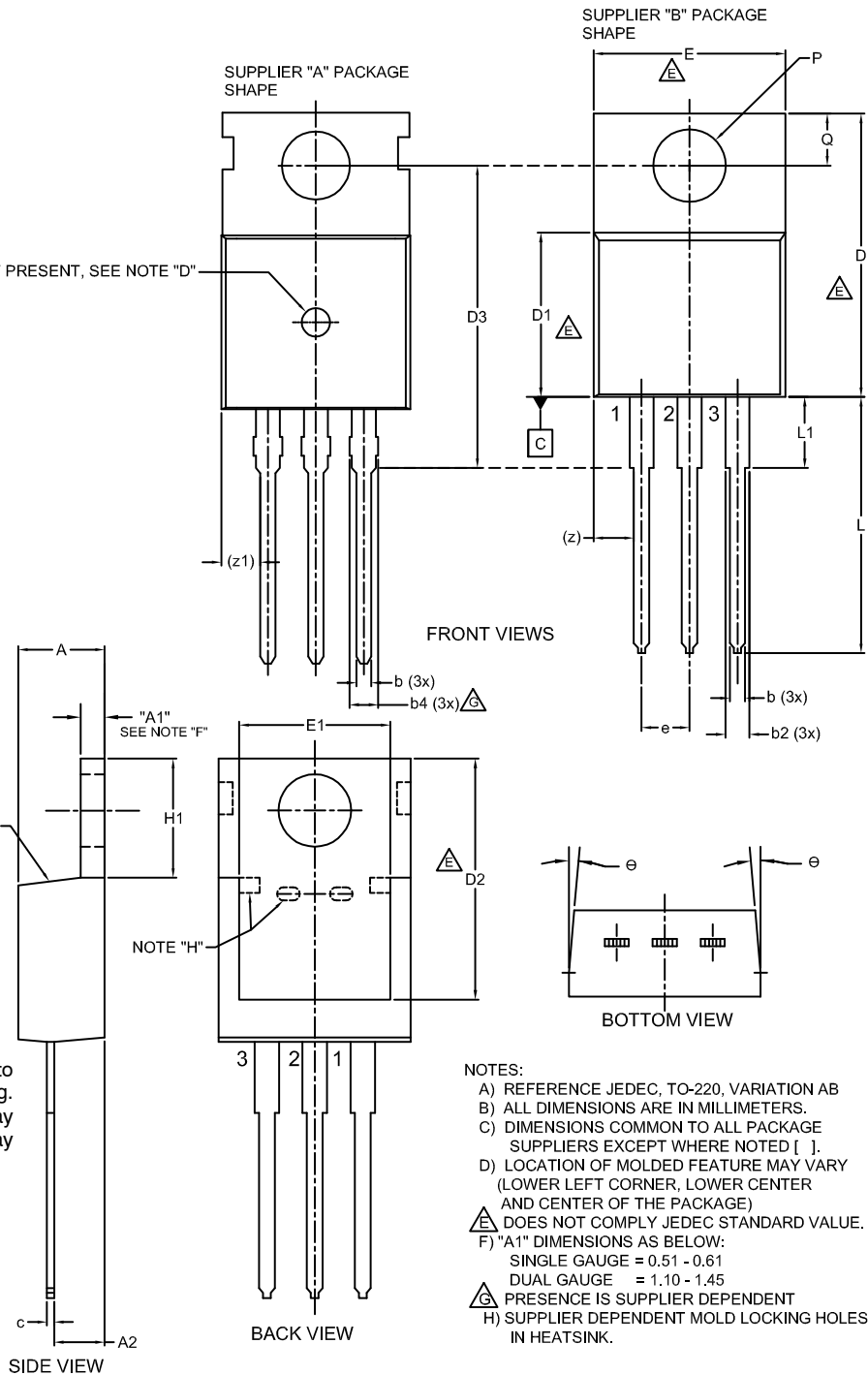
IF PRESENT, SEE NOTE "D"

GENERIC
MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
ZZ = Assembly Lot Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.



NOTES:

- A) REFERENCE JEDEC, TO-220, VARIATION AB
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS COMMON TO ALL PACKAGE SUPPLIERS EXCEPT WHERE NOTED [].
- D) LOCATION OF MOLDED FEATURE MAY VARY (LOWER LEFT CORNER, LOWER CENTER AND CENTER OF THE PACKAGE)
- △ DOES NOT COMPLY JEDEC STANDARD VALUE.
- F) "A1" DIMENSIONS AS BELOW:
SINGLE GAUGE = 0.51 - 0.61
DUAL GAUGE = 1.10 - 1.45
- △ PRESENCE IS SUPPLIER DEPENDENT
- H) SUPPLIER DEPENDENT MOLD LOCKING HOLES IN HEATSINK.

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