

NCN9252

High-Speed USB 2.0 (480 Mbps) DP3T Switch for USB/UART/Data Multiplexing

Brief Description

The NCN9252 is a DP3T switch for combined UART and USB 2.0 high-speed data applications. It allows portable systems to use a single external port to transmit and receive signals to and from three separate locations within the portable system. It is comprised of two switches, each with a single common I/O that alternates between 3 terminals. They are operated together to allow three data sources, such as a USB or UART transceiver, to pass differential data through a shared USB connector port.

The NCN9252 features low R_{ON} —4 Ω (max) at 4.2 V V_{CC} , 5 Ω (typ) at a 3.3 V V_{CC} . It also features low C_{ON} , < 30 pF (max) across the supply voltage range. This performance makes it ideal for both USB full-speed and high-speed applications that require both low R_{ON} and C_{ON} for effective signal transmission.

The NCN9252 is capable of accepting control input signals down to 1.4 V, over a range of V_{CC} supply voltages with minimal leakage current. The NCN9252 is offered in a Pb-Free, 12 pin, 1.7 x 2.0 x 0.5 mm, UQFN package. An Evaluation Board specifically designed for the NCN9252 is available and features USB connectors and test points to allow straightforward testing of the device. Please see part number NCN9252MUGEVB.

Features

- USB 2.0 Signal Routing
- -3 dB Bandwidth: 525 MHz
- R_{ON} : 4 Ω Max @ V_{CC} = 4.2 V
- C_{ON} : < 20 pF @ V_{CC} = 3.3 V
- OVT Protection up to 5.25 V on Common Pins
- V_{CC} Range: 1.65 V to 4.5 V
- 3 kV ESD Protection
- 1.7 x 2.0 x 0.5 mm UQFN12 Package
- This is a Pb-Free Device

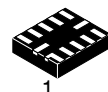
Typical Applications

- USB/UART/Data Multiplexing
- Shared USB Connector
- Mobile Phones
- Portable Devices



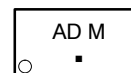
ON Semiconductor®

<http://onsemi.com>



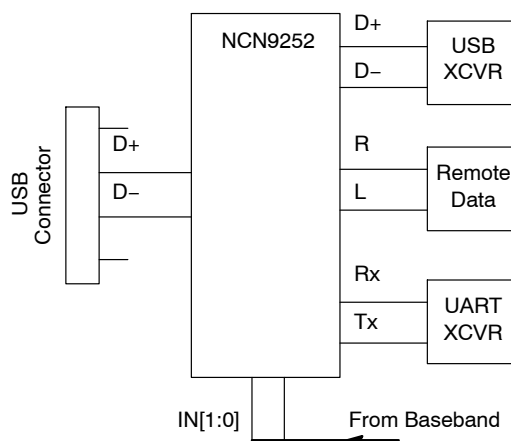
UQFN12
MU SUFFIX
CASE 523AE

MARKING DIAGRAM



AD = Specific Device Code
M = Date Code
■ = Pb-Free Package

APPLICATION DIAGRAM



ORDERING INFORMATION

Device	Package	Shipping†
NCN9252MUTAG	UQFN12 (Pb-Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

FUNCTIONAL BLOCK DIAGRAM AND PINOUT

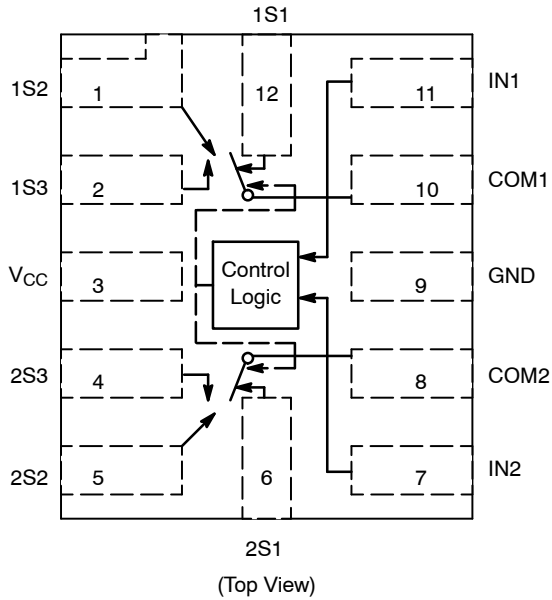


Figure 1. Internal Block Diagram

PIN DESCRIPTIONS

Pin#	Name	Direction	Description
1	1S2	I/O	Switch #1 Position 2 Signal Line
2	1S3	I/O	Switch #1 Position 3 Signal Line
3	V _{CC}	Input	Power Supply
4	2S3	I/O	Switch #2 Position 3 Signal Line
5	2S2	I/O	Switch #2 Position 2 Signal Line
6	2S1	I/O	Switch #2 Position 1 Signal Line
7	IN2	Input	Bit 1 Control Input Select Line
8	COM2	I/O	Switch #2 Common Signal Line
9	GND	Input	Ground
10	COM1	I/O	Switch #1 Common Signal Line
11	IN1	Input	Bit 0 Control Input Select Line
12	1S1	I/O	Switch #1 Position 1 Signal Line

FUNCTION TABLE

IN1 [0]	IN2 [1]	COM1 Closed to:	COM2 Closed to:
0	0	No Connect	No Connect
1	0	1S1	2S1
0	1	1S2	2S2
1	1	1S3	2S3

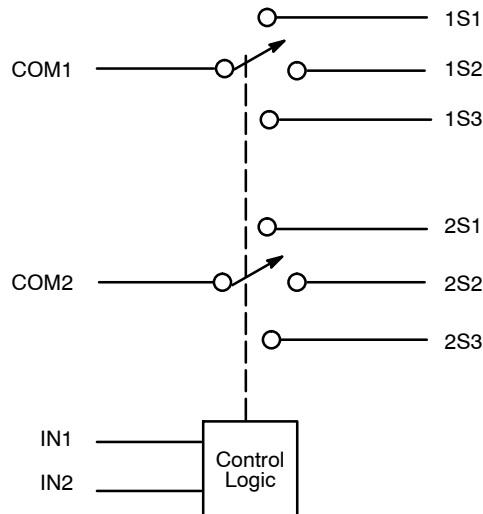


Figure 2. Functional Block Diagram

OPERATING CONDITIONS

MAXIMUM RATINGS

Symbol	Pins	Parameter	Value	Condition	Unit
V_{CC}	V_{CC}	Positive DC Supply Voltage	-0.5 to +5.5		V
V_{IS}	1Sx, 2Sx	Analog Signal Voltage	-0.5 to $V_{CC} + 0.3$		V
	COMx		-0.5 to 5.3		
V_{IN}	IN1, IN2	Control Input Voltage	-0.5 to 4.6		V
I_{CC}	V_{CC}	Positive DC Supply Current	50		mA
I_{IS_CON}	1Sx, 2Sx COMx	Analog Signal Continuous Current	± 300	Closed Switch	mA
I_{IS_PK}	1Sx, 2Sx COMx	Analog Signal Peak Current	± 500	10% Duty Cycle	mA
I_{IN}	IN1, IN2	Control Input Current	± 20		mA
T_{STG}		Storage Temperature Range	-65 to 150		°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Symbol	Pins	Parameter	Value	Condition	Unit
V_{CC}	V_{CC}	Positive DC Supply Voltage	1.65 to 4.5		V
V_{IS}	1Sx, 2Sx	Analog Signal Voltage	GND to V_{CC}		V
	COMx		GND to 4.5		
V_{IN}	IN1, IN2	Control Input Voltage	GND to V_{CC}		V
T_A		Operating Temperature Range	-40 to 85		°C

Minimum and maximum values are guaranteed through test or design across the **Recommended Operating Conditions**, where applicable. Typical values are listed for guidance only and are based on the particular conditions listed for each section, where applicable. These conditions are valid for all values found in the characteristics tables unless otherwise specified in the test conditions.

ESD PROTECTION

Pins	Description	Minimum Voltage
All Pins	Human Body Model	3 kV

DC ELECTRICAL CHARACTERISTICS

CONTROL INPUT (TYPICAL: T = 25°C; V_{CC} = 3.3 V)

Symbol	Pins	Parameter	Test Conditions	V _{CC}	Min	Typ	Max	Unit
V _{IH}	INx	Control Input High	Figure 3	2.7 V 3.3 V 4.2 V	1.25 1.35 1.50			V
V _{IL}	INx	Control Input Low	Figure 3	2.7 V 3.3 V 4.2 V			0.4 0.4 0.5	V
I _{IN}	INx	Control Input Leakage	V _{IS} = GND				± 1.0	μA

SUPPLY CURRENT AND LEAKAGE (TYPICAL: T = 25°C; V_{CC} = 3.3 V, V_{IN} = V_{CC} or GND)

Symbol	Pins	Parameter	Test Conditions	V _{CC}	Min	Typ	Max	Unit
I _{NO/NC} (OFF)	NC, NO	OFF State Leakage	V _{COM} = 3.6 V V _{NC} = 1.0 V				± 1.0	μA
I _{COM} (ON)	COM	ON State Leakage					± 1.0	μA
I _{CC}	V _{CC}	Quiescent Supply	V _{IS} = V _{CC} or GND, I _D = 0;				1.0	μA
I _{OFF}		Power OFF Leakage	V _{IS} = GND				1.0	μA

ON RESISTANCE (TYPICAL: T = 25°C; V_{CC} = 3.3 V)

Symbol	Pins	Parameter	Test Conditions	V _{CC}	Min	Typ	Max	Unit
R _{ON}	1Sx, 2Sx COMx	ON Resistance	I _{ON} = -8 mA, V _{IS} = 0 to V _{CC} ;	2.7 V 3.3 V 4.2 V		5 4 3.5	6 5 4.5	Ω
R _{FLAT}	1Sx, 2Sx COMx	R _{ON} Flatness	I _{ON} = -8 mA, V _{IS} = 0 to V _{CC} ;	2.7 V 3.3 V 4.2 V			1.3 1.4 1.6	Ω
ΔR _{ON}	1Sx, 2Sx COMx	R _{ON} Matching	I _{ON} = -8 mA, V _{IS} = 0 to V _{CC} ;	2.7 V 3.3 V 4.2 V		0.35		Ω

AC ELECTRICAL CHARACTERISTICS

TIMING/FREQUENCY (TYPICAL: T = 25°C; V_{CC} = 3.3 V, R_L = 50 Ω, C_L = 5 pF, f = 1 MHz)

Symbol	Pins	Parameter	Test Conditions	Min	Typ	Max	Unit
BW		–3 dB Bandwidth	Power level = 0 dBm		525		MHz
THD		Total Harmonic Distortion	20 Hz to 20 kHz, 1.0 V _{pp}		0.01		%
t _{ON}	1Sx to 1Sy, 2Sx to 2Sy	Turn On Time			13	30	nS
t _{OFF}	1Sy to 1Sx, 2Sy to 2Sx	Turn Off Time			12	25	nS
t _{BBM}	1Sx to 1Sy, 2Sx to 2Sy	Break Before Make		2.0			nS

CROSSTALK: (TYPICAL: T = 25°C; V_{CC} = 3.3V, R_L = 50 Ω, C_L = 35 pF, f = 1MHz)

Symbol	Pins	Parameter	Test Conditions	Min	Typ	Max	Unit
O _{IRR}	1Sx or 2Sx	Off Isolation	V _{IN} = 0		–60		dB
X _{talk}	COMx to COMy	Non-Adjacent Channel			–60		dB

CAPACITANCE (TYPICAL: T = 25°C; V_{CC} = 3.3V, R_L = 50 Ω, C_L = 5 pF, f = 1 MHz)

Symbol	Pins	Parameter	Test Conditions	Min	Typ	Max	Unit
C _{IN}	INx	Control Input	V _{CC} = 0 V		3		pF
C _{ON}	1Sx or 2Sx to COM	Through Switch	V _{CC} = 3.3 V, V _{IN} = 0 V		16	20	pF
C _{OFF}	1Sx, 2Sx COMx	Unselected Port	V _{CC} = V _{IN} = 3.3 V		8		pF

Control Inputs Select Logic

The NCN9252 is made up of two, triple-throw switches operating off of the same internal enable signal. For each switch, a signal can pass from the common pin to any of three terminals. Whenever COM1 is closed to terminal 1S2, COM2 will respectively be closed to terminal 2S2. The

select logic is controlled by two inputs, IN1 and IN2, connecting the common pins to the terminals according to the function table found on page 2. Since there are four possible control states but only 3 possible terminals, the first combination results in a open connection for all three terminals.

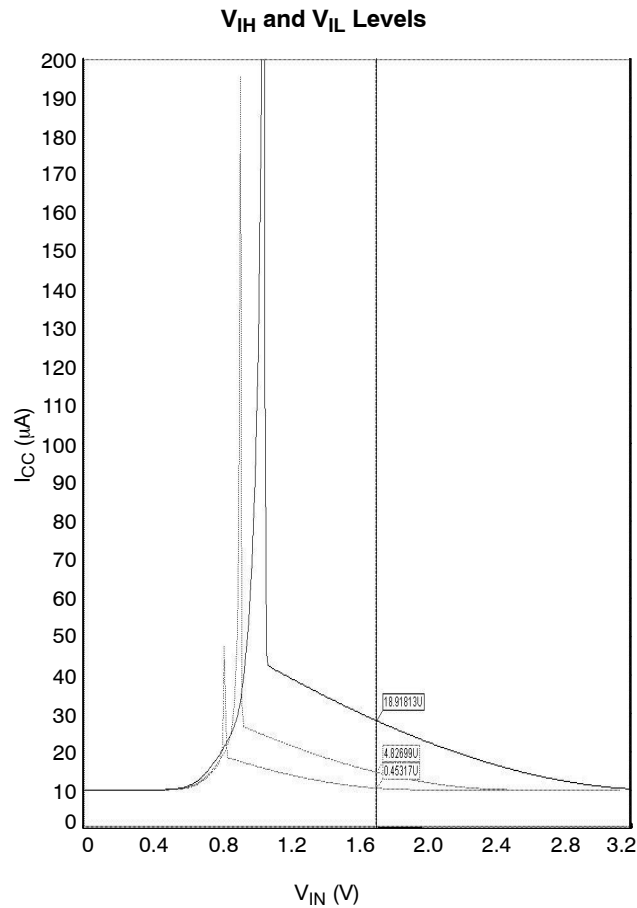
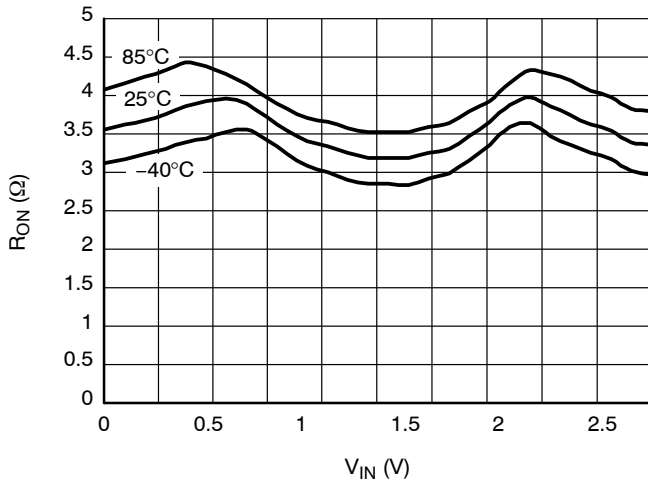
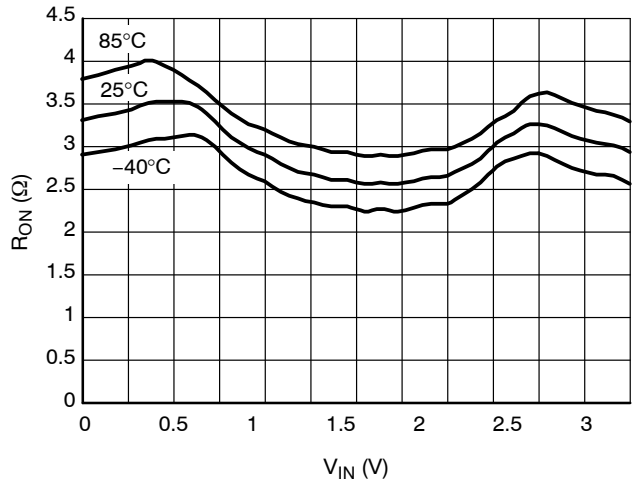


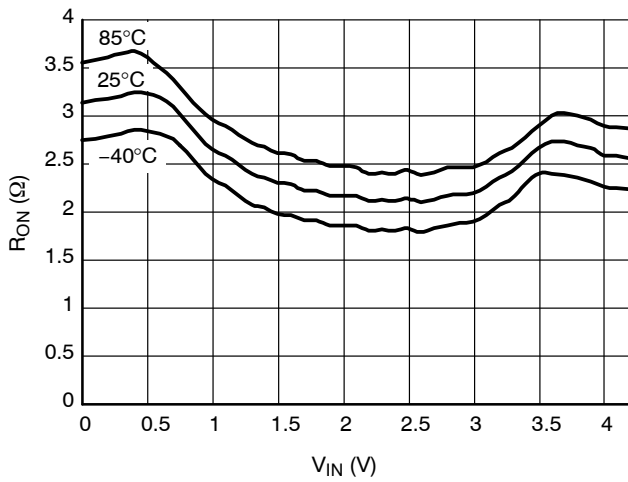
Figure 3. I_{CC} Leakage Current vs. V_{IN}



**Figure 4. On-Resistance vs. Input Voltage
@ $V_{CC} = 2.7\text{ V}$**



**Figure 5. On-Resistance vs. Input Voltage
@ $V_{CC} = 3.3\text{ V}$**



**Figure 6. On-Resistance vs. Input Voltage
@ $V_{CC} = 4.2\text{ V}$**

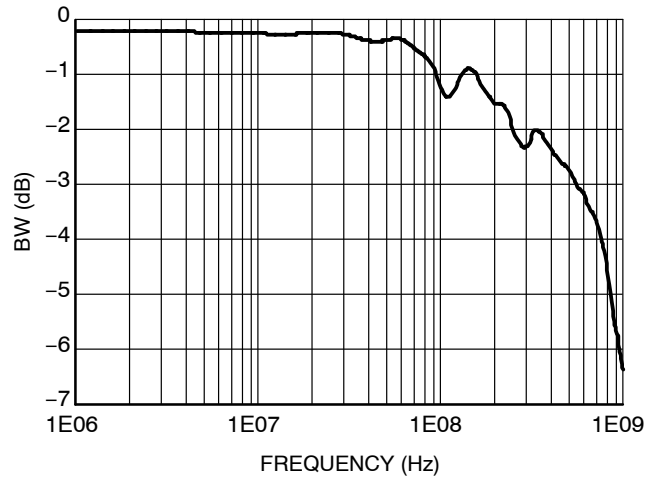
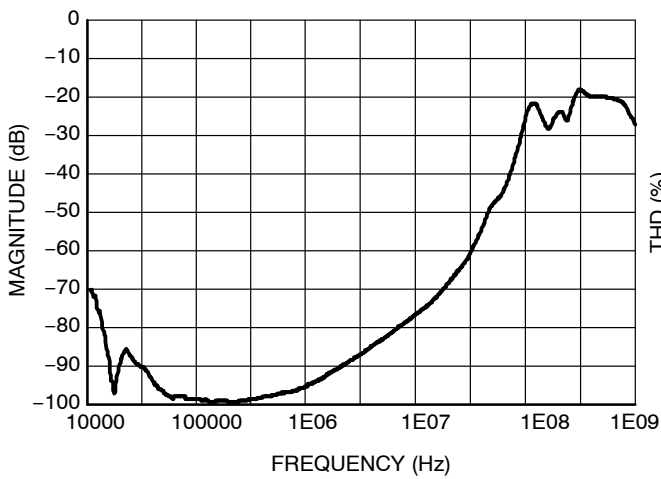
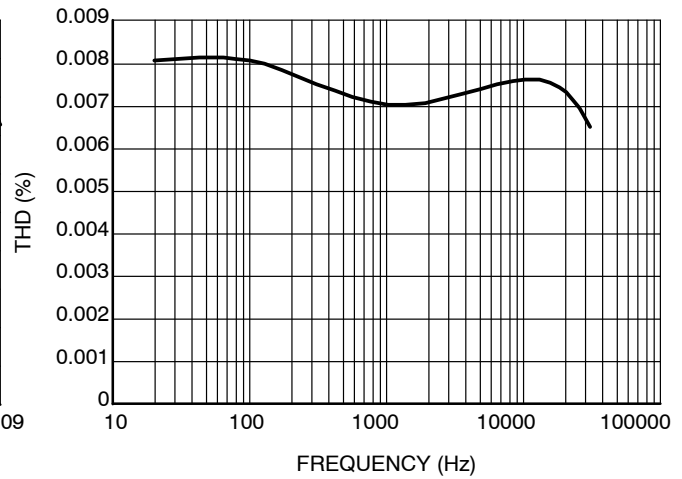


Figure 7. Bandwidth vs. Frequency



**Figure 8. Cross Talk vs. Frequency
@ 25°C**



**Figure 9. Total Harmonic Distortion vs.
Frequency**

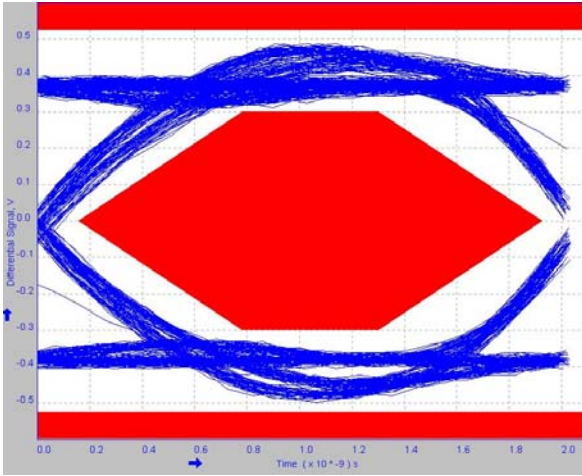


Figure 10. Channel 1S1/2S1 USB2.0 Near End Eye Diagram ($V_{CC} = 3.3$ V, $IN1 = 1$, $IN2 = 0$, Temp = 25°C)

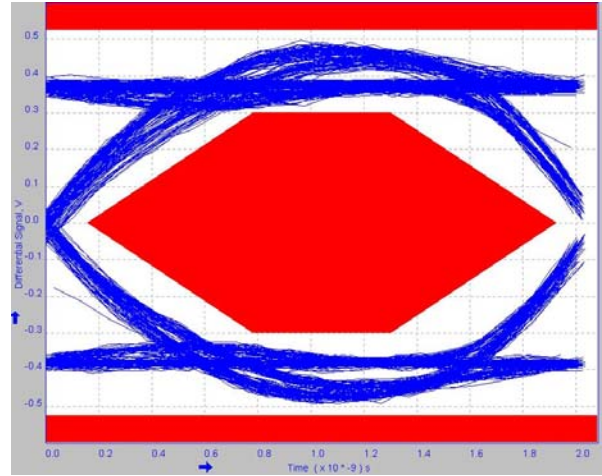


Figure 11. Channel 1S2/2S2 USB2.0 Near End Eye Diagram ($V_{CC} = 3.3$ V, $IN1 = 0$, $IN2 = 1$, Temp = 25°C)

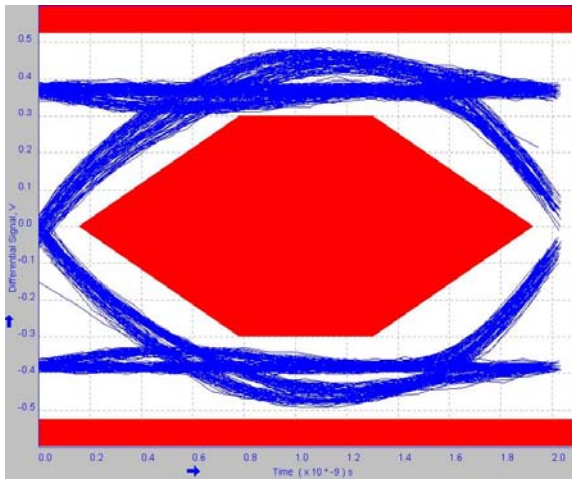


Figure 12. Channel 1S3/2S3 USB2.0 Near End Eye Diagram ($V_{CC} = 3.3$ V, $IN1 = 1$, $IN2 = 1$, Temp = 25°C)

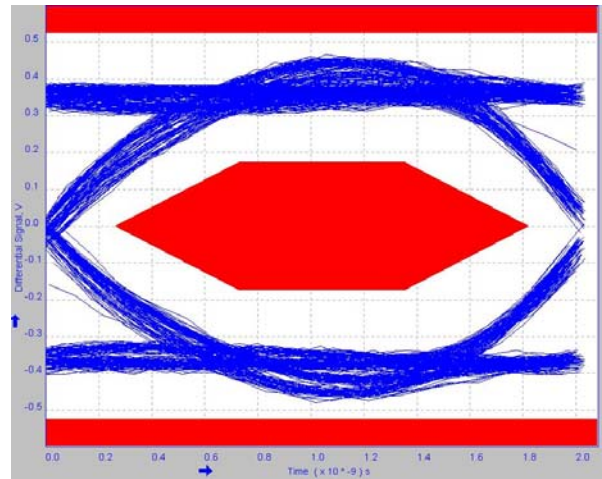


Figure 13. Channel 1S1/2S1 USB2.0 Far End Eye Diagram ($V_{CC} = 3.3$ V, $IN1 = 1$, $IN2 = 0$, Temp = 25°C)

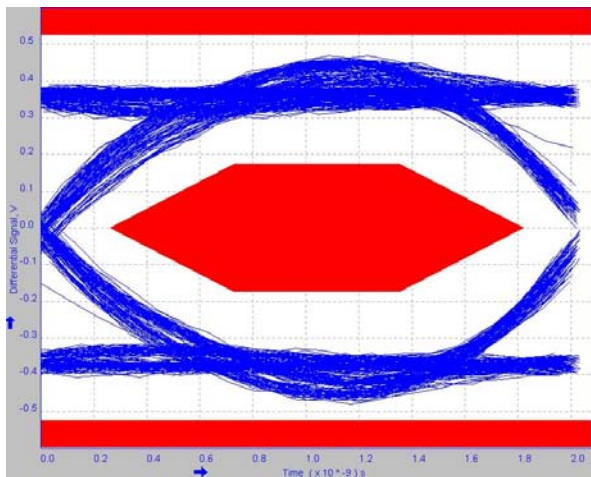


Figure 14. Channel 1S2/2S2 USB2.0 Far End Eye Diagram ($V_{CC} = 3.3$ V, $IN1 = 0$, $IN2 = 1$, Temp = 25°C)

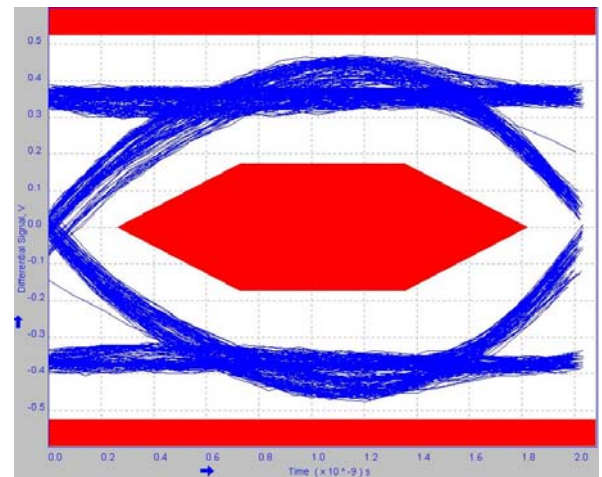
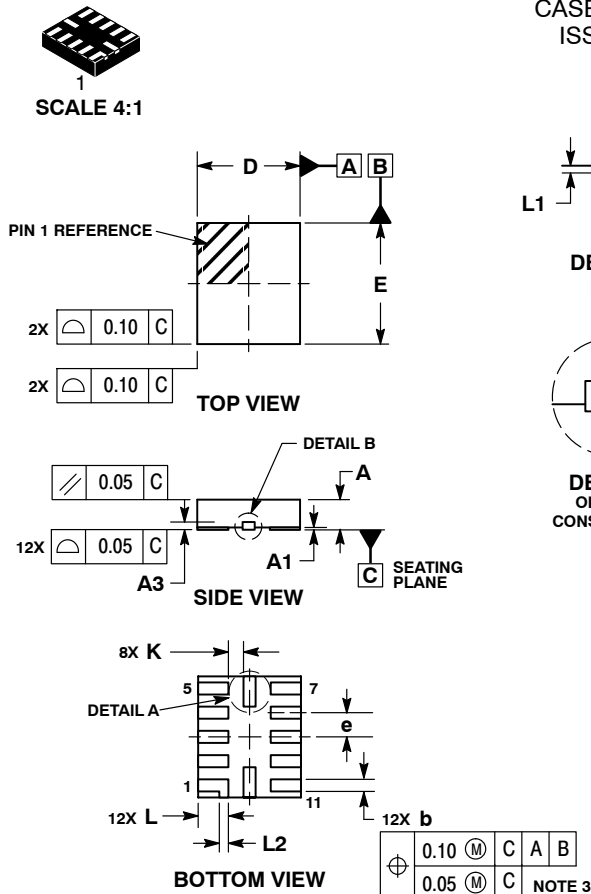


Figure 15. Channel 1S3/2S3 USB2.0 Far End Eye Diagram ($V_{CC} = 3.3$ V, $IN1 = 1$, $IN2 = 1$, Temp = 25°C)

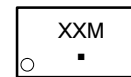
UQFN12 1.7x2.0, 0.4P
CASE 523AE
ISSUE A

DATE 11 JUN 2007


NOTES:

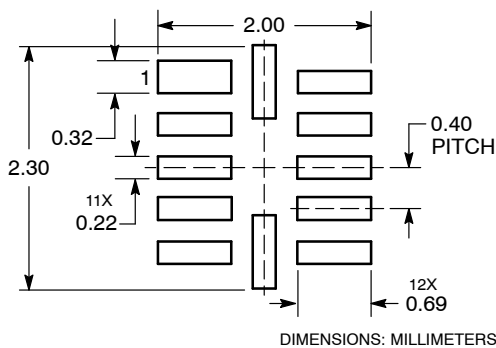
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM TERMINAL TIP.
4. MOLD FLASH ALLOWED ON TERMINALS ALONG EDGE OF PACKAGE. FLASH 0.03 MAX ON BOTTOM SURFACE OF TERMINALS.
5. DETAIL A SHOWS OPTIONAL CONSTRUCTION FOR TERMINALS.

DIM	MILLIMETERS	
	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A3	0.127 REF	
b	0.15	0.25
D	1.70 BSC	
E	2.00 BSC	
e	0.40 BSC	
K	0.20	----
L	0.45	0.55
L1	0.00	0.03
L2	0.15 REF	

GENERIC MARKING DIAGRAM*


XX = Specific Device Code
M = Date Code
■ = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present.

MOUNTING FOOTPRINT
SOLDERMASK DEFINED


DOCUMENT NUMBER:	98AON23418D	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	UQFN12 1.7 X 2.0, 0.4P	PAGE 1 OF 1

onsemi and onsemi are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.

onsemi, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:

Technical Library: www.onsemi.com/design/resources/technical-documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support

For additional information, please contact your local Sales Representative at
www.onsemi.com/support/sales