

Inverting Octal 3-STATE Buffer

MM74HC240

General Description

The MM74HC240 3-STATE buffer utilizes advanced silicon-gate CMOS technology. It possesses high drive current outputs which enable high speed operation even when driving large bus capacitances. These circuits achieve speeds comparable to low power Schottky devices, while retaining the advantage of CMOS circuitry, i.e., high noise immunity and low power consumption. It has a fanout of 15 LS-TTL equivalent inputs.

The MM74HC240 is an inverting buffer and has two active LOW enables ($1\bar{G}$ and $2\bar{G}$). Each enable independently controls 4 buffers.

All inputs are protected from damage due to static discharge by diodes to V_{CC} and ground.

Features

- Typical Propagation Delay: 12 ns
- 3-STATE Outputs for Connection to System Buses
- Wide Power Supply Range: 2–6 V
- Low Quiescent Supply Current: 160 μ A (74 Series)
- Output Current: 6 mA
- These are Pb-Free Devices

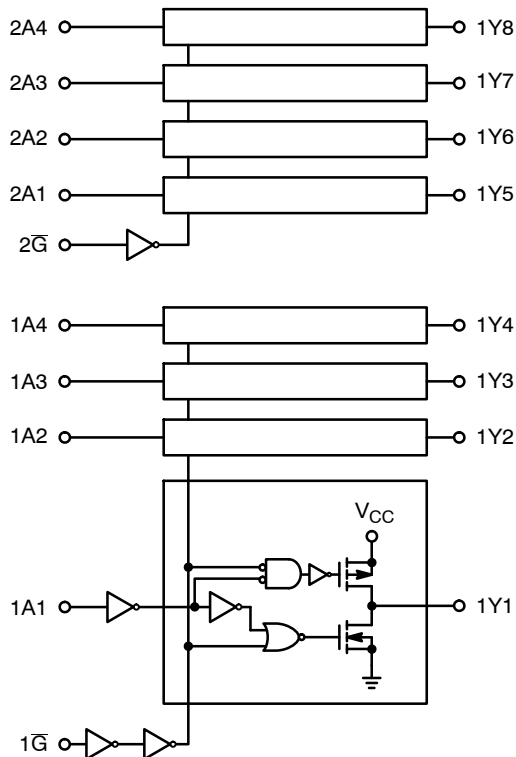
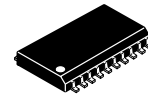


Figure 1. Logic Diagram

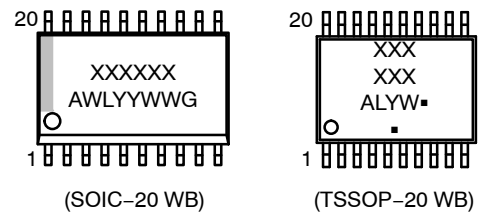


SOIC-20 WB
CASE 751D-05



TSSOP-20 WB
CASE 948E

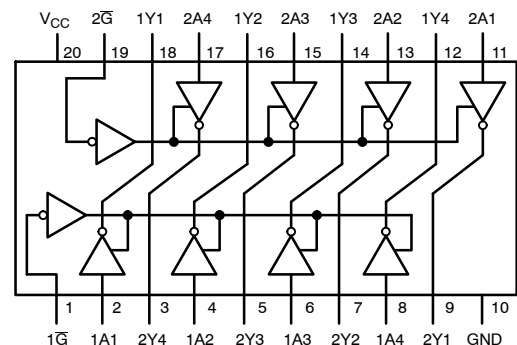
MARKING DIAGRAMS



XXXXXX = Specific Device Code
A = Assembly Location
L/WL = Wafer Lot
Y/YY = Year
W/WW = Work Week
▪ or G = Pb-Free Package

(Note: Microdot may be in either location)

CONNECTION DIAGRAM



(Top View)

TRUTH TABLE

$1\bar{G}$	1A	1Y	$2\bar{G}$	2A	2Y
L	L	H	L	L	H
L	H	H	L	H	H
H	L	Z	H	L	Z
H	H	Z	H	H	Z

H = HIGH Level
L = LOW Level
Z = HIGH Impedance

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 4 of this data sheet.

MM74HC240

MAXIMUM RATINGS (Note 1)

Symbol	Parameter	Value	Unit
V _{CC}	Supply Voltage	–0.5 to +6.5	V
V _{IN}	DC Input Voltage	–0.5 to V _{CC} + 0.5	V
V _{OUT}	DC Output Voltage	–0.5 to V _{CC} + 0.5	V
I _{IK} , I _{OK}	Clamp Diode Current	±20	mA
I _{OUT}	DC Output Current, per Pin	±35	mA
I _{CC}	DC VCC or GND Current, per Pin	±70	mA
T _{STG}	Storage Temperature Range	–65 to +150	°C
P _D	Power Dissipation SOIC TSSOP	1302 833	mW
T _L	Lead Temperature (Soldering 10 seconds)	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Unless otherwise specified all voltages are referenced to ground.

RECOMMENDED OPERATING CONDITIONS (Note 1)

Symbol	Parameter	Min	Max	Unit
V _{CC}	Supply Voltage	2	6	V
V _{IN} , V _{OUT}	DC Input or Output Voltage	0	V _{CC}	V
T _A	Operating Temperature Range	–55	+125	°C
t _r , t _f	Input Rise or Fall Times V _{CC} = 2.0 V V _{CC} = 4.5 V V _{CC} = 6.0 V	– – –	1000 500 400	ns

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

DC ELECTRICAL CHARACTERISTICS (Note 2)

Symbol	Parameter	Conditions	V _{CC} (V)	T _A = 25°C		–40°C ≤ T _A ≤ 85°C	–55°C ≤ T _A ≤ 125°C	Unit
				Typ	Guaranteed Limits			
V _{IH}	Minimum HIGH Level Input Voltage		2.0	–	1.5	1.5	1.5	V
			4.5	–	3.15	3.15	3.15	
			6.0	–	4.2	4.2	4.2	
V _{IL}	Maximum LOW Level Input Voltage		2.0	–	0.5	0.5	0.5	V
			4.5	–	1.35	1.35	1.35	
			6.0	–	1.8	1.8	1.8	
V _{OH}	Minimum HIGH Level Output Voltage	V _{IN} = V _{IH} or V _{IL} I _{OUT} ≤ 20 μA	2.0	2.0	1.9	1.9	1.9	V
			4.5	4.5	4.4	4.4	4.4	
		6.0	6.0	5.9	5.9	5.9	V	
		V _{IN} = V _{IH} or V _{IL} I _{OUT} ≤ 6.0 mA I _{OUT} ≤ 7.8 mA	4.5	4.2	3.98	3.84		3.7
		6.0	5.7	5.48	5.34	5.2		
V _{OL}	Maximum LOW Level Output Voltage	V _{IN} = V _{IH} or V _{IL} I _{OUT} ≤ 20 μA	2.0	0	0.1	0.1	0.1	V
			4.5	0	0.1	0.1	0.1	
		6.0	0	0.1	0.1	0.1	V	
		V _{IN} = V _{IH} or V _{IL} I _{OUT} ≤ 6.0 mA I _{OUT} ≤ 7.8 mA	4.5	0.2	0.26	0.33		0.4
		6.0	0.2	0.26	0.33	0.4		
I _{IN}	Maximum Input Current	V _{IN} = V _{CC} or GND	6.0	–	±0.1	±1.0	±1.0	μA

MM74HC240

DC ELECTRICAL CHARACTERISTICS (Note 2) (continued)

Symbol	Parameter	Conditions	V _{CC} (V)	T _A = 25°C		-40°C ≤ T _A ≤ 85°C		-55°C ≤ T _A ≤ 125°C		Unit
				Typ	Guaranteed Limits					
I _{OZ}	Maximum 3-STATE Output Leakage Current	V _{IN} = V _{IH} or V _{IL} V _{OUT} = V _{CC} or GND G = V _{IH} , G = V _{IL}	6.0	–	±0.5	±5		±10		μA
I _{CC}	Maximum Quiescent Supply Current	V _{IN} = V _{CC} or GND I _{OUT} = 0 μA	6.0	–	8.0	80		160		μA

2. For a power supply of 5 V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5 V. Thus the 4.5 V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5 V and 4.5 V respectively. (The V_{IH} value at 5.5 V is 3.85 V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0 V values should be used.

AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Unit
t _{PHL} , t _{PLH}	Maximum Propagation Delay	C _L = 45 pF	12	18	ns
t _{PZH} , t _{PZL}	Maximum Enable Delay to Active Output	R _L = 1 kΩ, C _L = 45 pF	14	28	ns
t _{PHZ} , t _{PLZ}	Maximum Disable Delay from Active Output	R _L = 1 kΩ, C _L = 5 pF	13	25	ns

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 2.0 V to 6.0 V, C_L = 50 pF, t_r = t_f = 6 ns (unless otherwise specified))

Symbol	Parameter	Conditions	V _{CC} (V)	T _A = 25°C		–40°C ≤ T _A ≤ 85°C		–55°C ≤ T _A ≤ 125°C		Unit
				Typ	Guaranteed Limits					
t _{PHL} , t _{PLH}	Maximum Propagation Delay	C _L = 50 pF	2.0	55	100	126	149	ns		
		C _L = 150 pF	2.0	80	150	190	224			
		C _L = 50 pF C _L = 150 pF	4.5 4.5	12 22	20 30	25 38	30 45	ns		
		C _L = 50 pF C _L = 150 pF	6.0 6.0	11 28	17 26	21 32	25 38	ns		
		Maximum Output Enable Time	R _L = 1 kΩ C _L = 50 pF C _L = 150 pF	2.0 2.0	75 100	150 200	189 252	224 298	ns	
			C _L = 50 pF C _L = 150 pF	4.5 4.5	15 20	30 40	38 50	45 60	ns	
			C _L = 50 pF C _L = 150 pF	6.0 6.0	13 17	26 34	32 43	38 51	ns	
		Maximum Output Disable Time	R _L = 1 kΩ C _L = 50 pF	2.0 4.5 6.0	75 15 13	150 30 26	189 38 32	224 45 38	ns	
t _{TLH} , t _{THL}	Maximum Output Rise and Fall Time			2.0 4.5 6.0	– – –	60 12 10	75 15 13	90 18 15	ns	
		Power Dissipation Capacitance (Note 3)	(per buffer) G̅ = V _{IH} G̅ = V _{IL}	– –	12 50	– –	– –	– –	pF	
C _{IN}	Maximum Input Capacitance			–	5	10	10	10	pF	
C _{OUT}	Maximum Output Capacitance		–	10	20	20	20	pF		

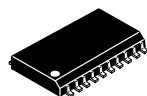
3. C_{PD} determines the no load dynamic power consumption, P_D = C_{PD} · V_{CC}² · f + I_{CC} · V_{CC}, and the no load dynamic current consumption, I_S = C_{PD} · V_{CC} · f + I_{CC}.

MM74HC240

ORDERING INFORMATION

Device	Marking	Package	Shipping [†]
MM74HC240WM	HC240A	SOIC-20 WB (Pb-Free)	38 Units / Tube
MM74HC240WMX	HC240A	SOIC-20 WB (Pb-Free)	1000 Units / Tape & Reel
MM74HC240MTCX	HC 240A	TSSOP-20 WB (Pb-Free)	2500 Units / Tape & Reel

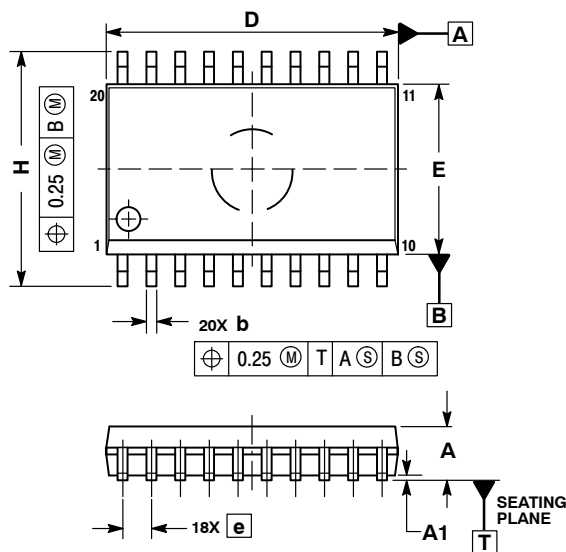
[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



SCALE 1:1

SOIC-20 WB
CASE 751D-05
ISSUE H

DATE 22 APR 2015

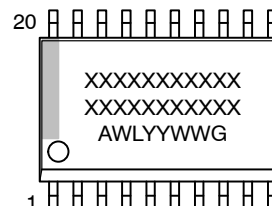


NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS	
	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
b	0.35	0.49
c	0.23	0.32
D	12.65	12.95
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
θ	0°	7°

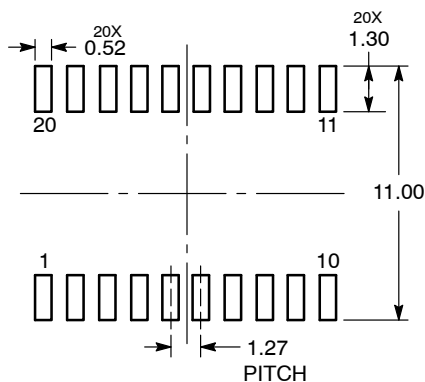
GENERIC
MARKING DIAGRAM*



XXXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

RECOMMENDED
SOLDERING FOOTPRINT*

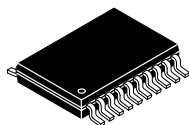


DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

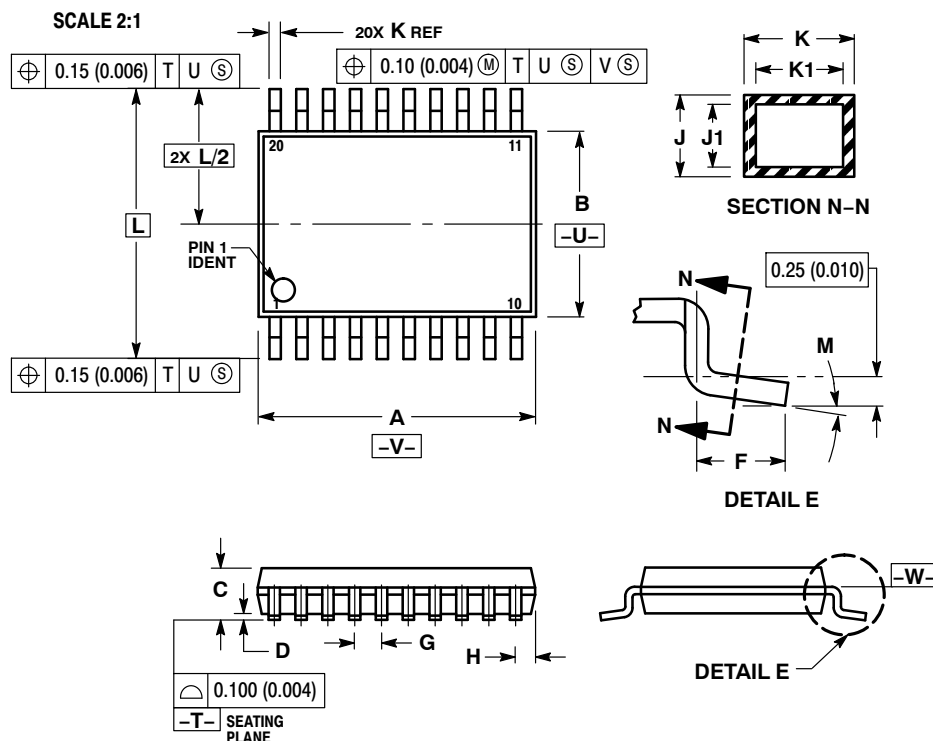
DOCUMENT NUMBER:	98ASB42343B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	SOIC-20 WB	PAGE 1 OF 1

onsemi and onsemi are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.



TSSOP-20 WB
CASE 948E
ISSUE D

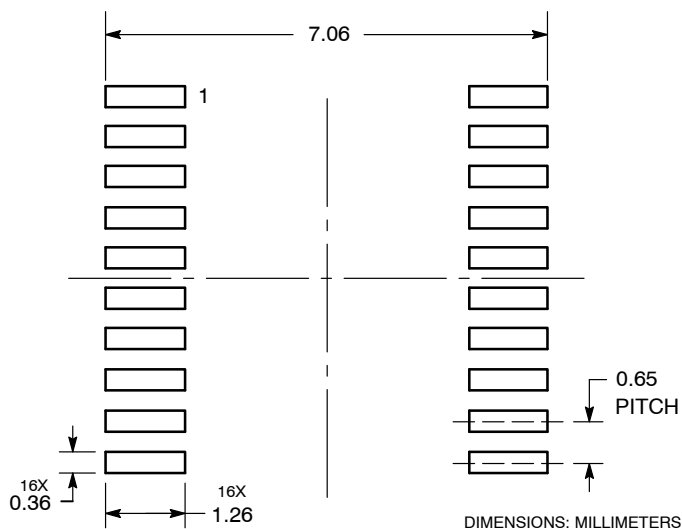
DATE 17 FEB 2016



- NOTES:**
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER
 3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
 4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
 5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
 6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
 7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

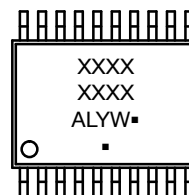
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	6.40	6.60	0.252	0.260
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.27	0.37	0.011	0.015
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

**RECOMMENDED
SOLDERING FOOTPRINT***



*For additional information on our Pb-Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual. SOLDERRM/D.

GENERIC MARKING DIAGRAM*



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	98ASH70169A	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	TSSOP-20 WB	PAGE 1 OF 1

onsemi and **onsemi** are trademarks of Semiconductor Components Industries, LLC dba **onsemi** or its subsidiaries in the United States and/or other countries. **onsemi** reserves the right to make changes without further notice to any products herein. **onsemi** makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. **onsemi** does not convey any license under its patent rights nor the rights of others.

onsemi, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:

Technical Library: www.onsemi.com/design/resources/technical-documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support

For additional information, please contact your local Sales Representative at
www.onsemi.com/support/sales