# High Voltage Power Transistors

## DPAK for Surface Mount Applications

# MJD47, NJVMJD47T4G, MJD50, NJVMJD50T4G

Designed for line operated audio output amplifier, switchmode supply drivers and other switching applications.

### Features

- Lead Formed for Surface Mount Applications in Plastic Sleeves (No Suffix)
- Electrically Similar to Popular TIP47, and TIP50
- Epoxy Meets UL 94 V−0 @ 0.125 in
- NJV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q101 Qualified and PPAP Capable
- These Devices are Pb−Free and are RoHS Compliant

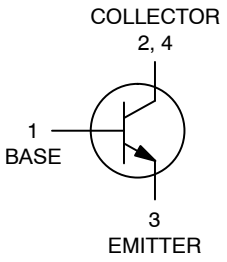
### MAXIMUM RATINGS

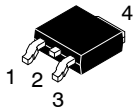
| Rating | Symbol | Max | Unit |
|---|---|---|---|
| Collector−Emitter Voltage<br>MJD47, NJVMJD47T4G<br>MJD50, NJVMJD50T4G | $V_{CEO}$ | <br>250<br>400 | Vdc |
| Collector−Base Voltage<br>MJD47, NJVMJD47T4G<br>MJD50, NJVMJD50T4G | $V_{CB}$ | <br>350<br>500 | Vdc |
| Emitter−Base Voltage | $V_{EB}$ | 5 | Vdc |
| Collector Current − Continuous | $I_C$ | 1 | Adc |
| Collector Current − Peak | $I_{CM}$ | 2 | Adc |
| Base Current | $I_B$ | 0.6 | Adc |
| Total Power Dissipation<br>@ $T_C$ = 25°C<br>Derate above 25°C | $P_D$ | <br>15<br>0.12 | <br>W<br>W/°C |
| Total Power Dissipation (Note 1)<br>@ $T_A$ = 25°C<br>Derate above 25°C | $P_D$ | <br>1.56<br>0.0125 | <br>W<br>W/°C |
| Operating and Storage Junction Temperature Range | $T_J$, $T_{stg}$ | −65 to +150 | °C |
| ESD − Human Body Model | HBM | 3B | V |
| ESD − Machine Model | MM | C | V |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. These ratings are applicable when surface mounted on the minimum pad sizes recommended.

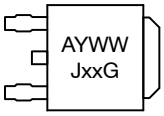
## NPN SILICON POWER TRANSISTORS
## 1 AMPERE
## 250, 400 VOLTS, 15 WATTS




**DPAK**
**CASE 369C**
**STYLE 1**

### MARKING DIAGRAM




A = Assembly Location
Y = Year
WW = Work Week
Jxx = Device Code
xx = 47 or 50
G = Pb−Free Package

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

## THERMAL CHARACTERISTICS

| Characteristic | Symbol | Max | Unit |
|---|---|---|---|
| Thermal Resistance Junction−to−Case | $R_{\theta JC}$ | 8.33 | °C/W |
| Thermal Resistance Junction−to−Ambient (Note 2) | $R_{\theta JA}$ | 80 | °C/W |
| Lead Temperature for Soldering Purpose | $T_L$ | 260 | °C |

2. These ratings are applicable when surface mounted on the minimum pad sizes recommended.

## ELECTRICAL CHARACTERISTICS ($T_C$ = 25°C unless otherwise noted)

| Characteristic | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | |
| Collector−Emitter Sustaining Voltage (Note 3)<br>($I_C$ = 30 mAdc, $I_B$ = 0)<br>MJD47, NJVMJD47T4G<br>MJD50, NJVMJD50T4G | $V_{CEO(sus)}$ | <br><br>250<br>400 | <br><br>–<br>– | Vdc |
| Collector Cutoff Current<br>($V_{CE}$ = 150 Vdc, $I_B$ = 0)<br>MJD47, NJVMJD47T4G<br>($V_{CE}$ = 300 Vdc, $I_B$ = 0)<br>MJD50, NJVMJD50T4G | $I_{CEO}$ | <br><br>–<br><br>– | <br><br>0.2<br><br>0.2 | mAdc |
| Collector Cutoff Current<br>($V_{CE}$ = 350 Vdc, $V_{BE}$ = 0)<br>MJD47, NJVMJD47T4G<br>($V_{CE}$ = 500 Vdc, $V_{BE}$ = 0)<br>MJD50, NJVMJD50T4G | $I_{CES}$ | <br><br>–<br><br>– | <br><br>0.1<br><br>0.1 | mAdc |
| Emitter Cutoff Current<br>($V_{BE}$ = 5 Vdc, $I_C$ = 0) | $I_{EBO}$ | <br>– | <br>1 | mAdc |
| **ON CHARACTERISTICS** (Note 3) | | | | |
| DC Current Gain<br>($I_C$ = 0.3 Adc, $V_{CE}$ = 10 Vdc)<br>($I_C$ = 1 Adc, $V_{CE}$ = 10 Vdc) | $h_{FE}$ | <br>30<br>10 | <br>150<br>– | – |
| Collector−Emitter Saturation Voltage<br>($I_C$ = 1 Adc, $I_B$ = 0.2 Adc) | $V_{CE(sat)}$ | <br>– | <br>1 | Vdc |
| Base−Emitter On Voltage<br>($I_C$ = 1 Adc, $V_{CE}$ = 10 Vdc) | $V_{BE(on)}$ | <br>– | <br>1.5 | Vdc |
| **DYNAMIC CHARACTERISTICS** | | | | |
| Current Gain − Bandwidth Product<br>($I_C$ = 0.2 Adc, $V_{CE}$ = 10 Vdc, f = 2 MHz) | $f_T$ | <br>10 | <br>– | MHz |
| Small−Signal Current Gain<br>($I_C$ = 0.2 Adc, $V_{CE}$ = 10 Vdc, f = 1 kHz) | $h_{fe}$ | <br>25 | <br>– | – |

3. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

## TYPICAL CHARACTERISTICS

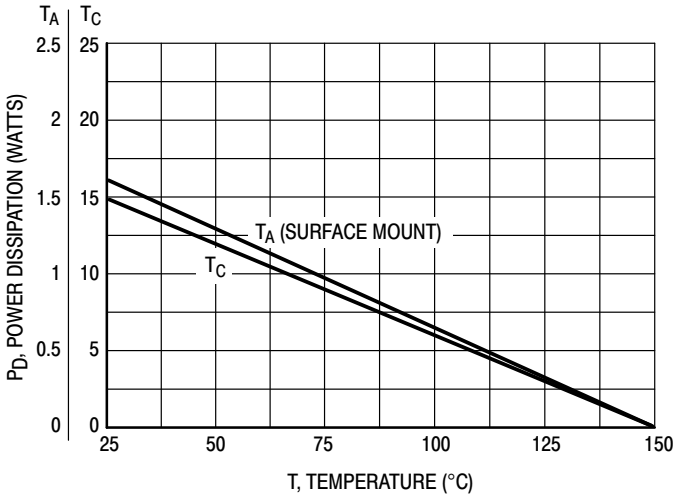



**Figure 1. Power Derating**

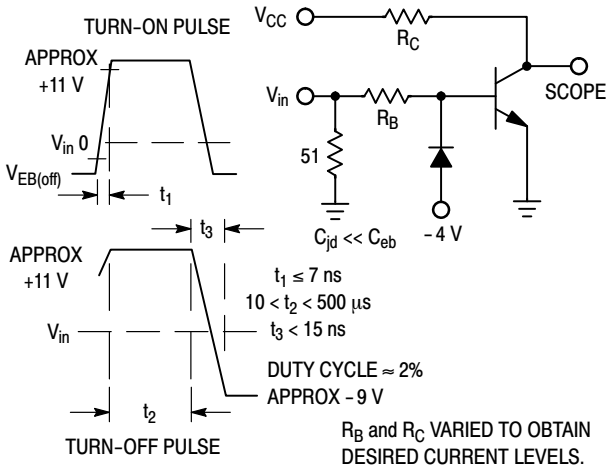



**Figure 2. Switching Time Equivalent Circuit**

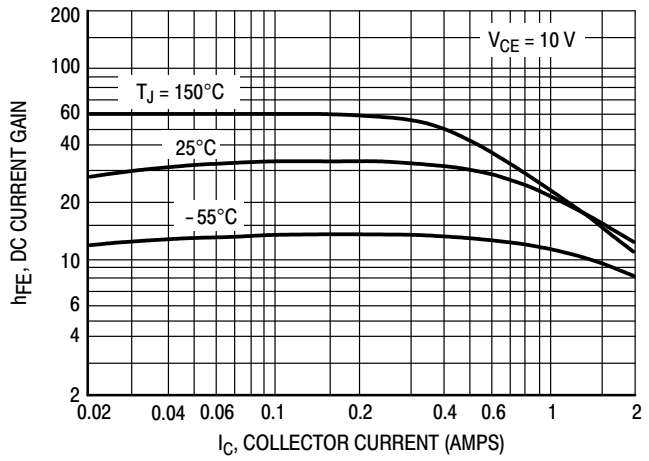



**Figure 3. DC Current Gain**

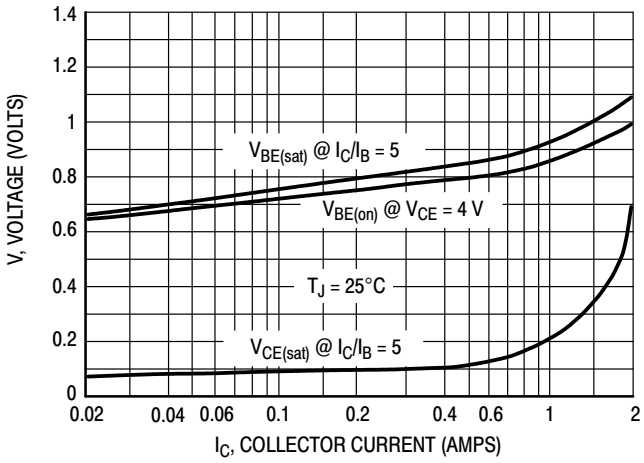



**Figure 4. "On" Voltages**

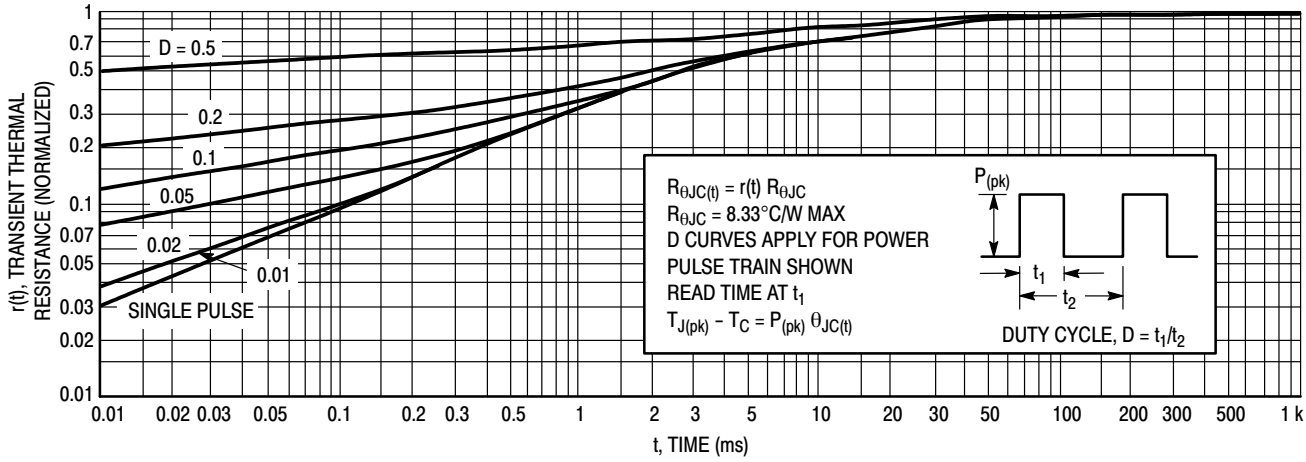



**Figure 5. Thermal Response**

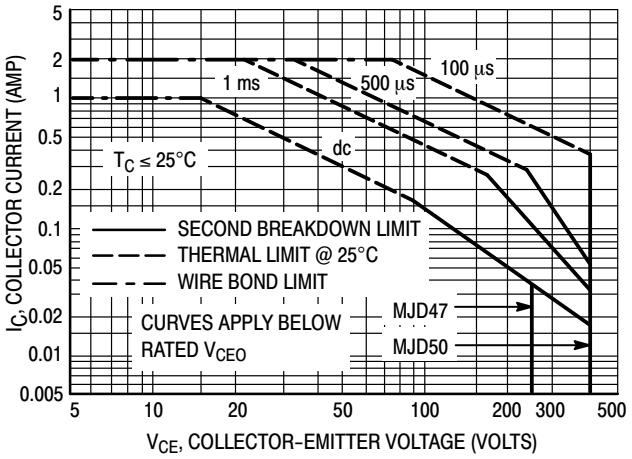



**Figure 6. Active Region Safe Operating Area**

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 6 is based on $T_{J(pk)} = 150°C$; $T_C$ is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \le 150°C$. $T_{J(pk)}$ may be calculated from the data in Figure 5. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

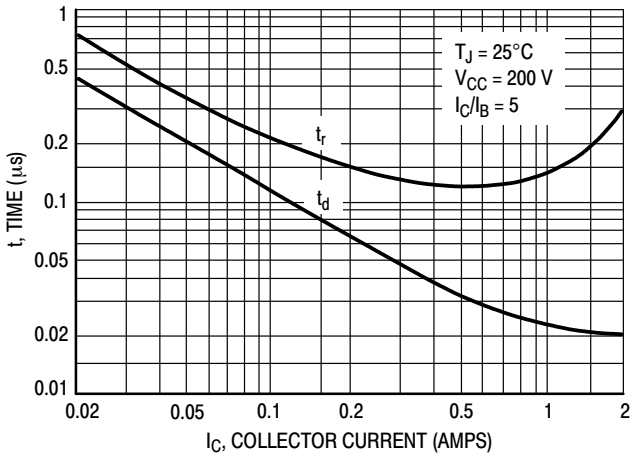



**Figure 7. Turn−On Time**

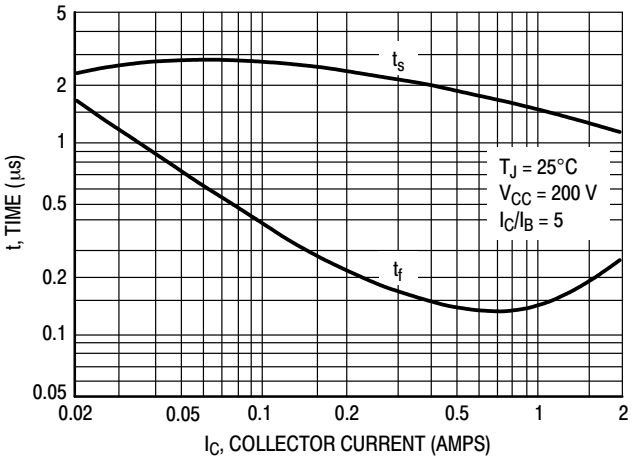


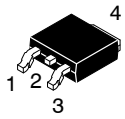

**Figure 8. Turn-Off Time**

## ORDERING INFORMATION

| Device | Package | Shipping† |
|---|---|---|
| MJD47G | 369C<br>(Pb−Free) | 75 Units / Rail |
| MJD47T4G | 369C<br>(Pb−Free) | 2,500 / Tape & Reel |
| NJVMJD47T4G* | 369C<br>(Pb−Free) | 2,500 / Tape & Reel |
| MJD50G | 369C<br>(Pb−Free) | 75 Units / Rail |
| MJD50T4G | 369C<br>(Pb−Free) | 2,500 / Tape & Reel |
| NJVMJD50T4G* | 369C<br>(Pb−Free) | 2,500 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

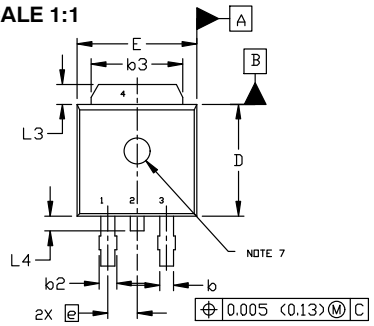
*NJV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q101 Qualified and PPAP Capable.



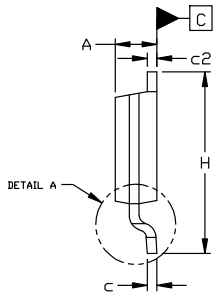

# DPAK (SINGLE GAUGE)
CASE 369C
ISSUE G

DATE 31 MAY 2023

**SCALE 1:1**




TOP VIEW

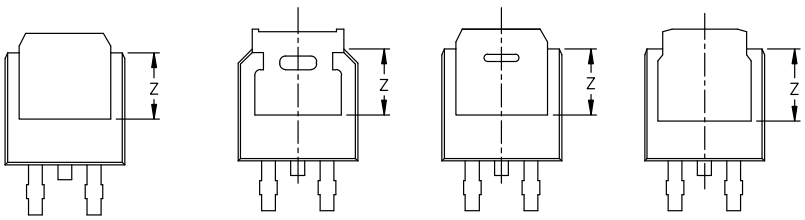



SIDE VIEW

NOTES:

1. DIMENSIONING AND TOLERANCING ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3, AND Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
7. OPTIONAL MOLD FEATURE.

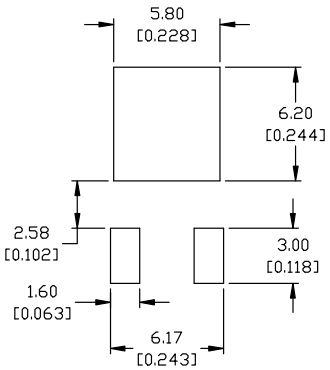
| DIM | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| | MIN. | MAX. | MIN. | MAX. |
| A | 0.086 | 0.094 | 2.18 | 2.38 |
| A1 | 0.000 | 0.005 | 0.00 | 0.13 |
| b | 0.025 | 0.035 | 0.63 | 0.89 |
| b2 | 0.028 | 0.045 | 0.72 | 1.14 |
| b3 | 0.180 | 0.215 | 4.57 | 5.46 |
| c | 0.018 | 0.024 | 0.46 | 0.61 |
| c2 | 0.018 | 0.024 | 0.46 | 0.61 |
| D | 0.235 | 0.245 | 5.97 | 6.22 |
| E | 0.250 | 0.265 | 6.35 | 6.73 |
| e | 0.090 BSC | | 2.29 BSC | |
| H | 0.370 | 0.410 | 9.40 | 10.41 |
| L | 0.055 | 0.070 | 1.40 | 1.78 |
| L1 | 0.114 REF | | 2.90 REF | |
| L2 | 0.020 BSC | | 0.51 BSC | |
| L3 | 0.035 | 0.050 | 0.89 | 1.27 |
| L4 | ---- | 0.040 | --- | 1.01 |
| Z | 0.155 | ---- | 3.93 | --- |




BOTTOM VIEW

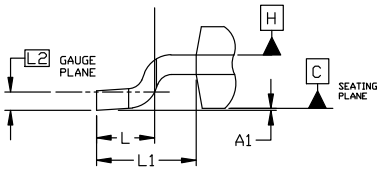
BOTTOM VIEW

ALTERNATE CONSTRUCTIONS



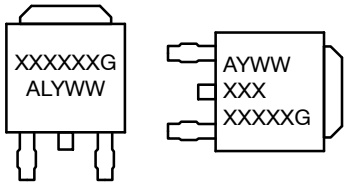

RECOMMENDED MOUNTING FOOTPRINT*

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.




DETAIL A
ROTATED 90° CW

## GENERIC MARKING DIAGRAM*




**IC** **Discrete**

XXXXXX = Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 3:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

STYLE 4:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 5:
PIN 1. GATE
2. ANODE
3. CATHODE
4. ANODE

STYLE 6:
PIN 1. MT1
2. MT2
3. GATE
4. MT2

STYLE 7:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 8:
PIN 1. N/C
2. CATHODE
3. ANODE
4. CATHODE

STYLE 9:
PIN 1. ANODE
2. CATHODE
3. RESISTOR ADJUST
4. CATHODE

STYLE 10:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. ANODE

| | | |
|---|---|---|
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| **DESCRIPTION:** | **DPAK (SINGLE GAUGE)** | **PAGE 1 OF 1** |

## ADDITIONAL INFORMATION

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**onsemi Website:** www.onsemi.com

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**For additional information, please contact your local Sales Representative at** www.onsemi.com/support/sales