

3-to-8 Line Decoder

MC74VHC138, MC74VHCT138A

The MC74VHC138/MC74VHCT138A is an advanced high speed CMOS 3-to-8 decoder fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

When the device is enabled, three Binary Select inputs (A0 – A2) determine which one of the outputs ($\overline{Y0} - \overline{Y7}$) will go Low. When enable input E3 is held Low or either $\overline{E2}$ or $\overline{E1}$ is held High, decoding function is inhibited and all outputs go high. E3, $\overline{E2}$ and $\overline{E1}$ inputs are provided to ease cascade connection and for use as an address decoder for memory systems.

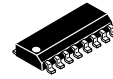
The MC74VHC138 inputs are compatible with standard CMOS levels while the MC74VHCT138A inputs are compatible with TTL levels. The MC74VHCT138A can be used as a level converter for interfacing 3.3 V to 5.0 V, because it has full 5.0 V CMOS level output swings.

The internal circuit is composed of three stages, including a buffer output which provides high noise immunity and stable output. The MC74VHC138 and MC74VHCT138A input structures tolerate voltages up to 5.5 V, allowing the interface of 5 V systems to 3 V systems.

The MC74VHCT138A output structures provide protection when $V_{CC} = 0$ V. These output structures help prevent device destruction caused by supply voltage – input/output voltage mismatch, battery backup, hot insertion, etc.

Features

- High Speed: $t_{PD} = 5.7$ ns (Typ) at $V_{CC} = 5.0$ V
- Low Power Dissipation: $I_{CC} = 4.0$ μ A (Max) at $T_A = 25$ °C
- High Noise Immunity: $V_{NIH} = V_{NIL} = 28\%$ V_{CC}
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Designed for 2.0 V to 5.5 V (VHC)
4.5 V to 5.5 V (VHCT)
- Low Noise: $V_{OLP} = 0.8$ V (Max) (VHC)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 100 mA
- ESD Performance: Human Body Model > 2000 V;
- Chip Complexity: 122 FETs or 30.5 Equivalent Gates
- These Devices are Pb-Free, Halogen Free/BFR Free, Beryllium Free and are RoHS Compliant

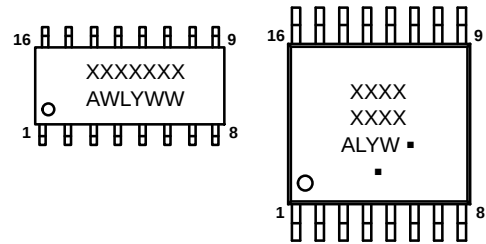


SOIC-16
D SUFFIX
CASE 751B



TSSOP-16
DT SUFFIX
CASE 948F

MARKING DIAGRAM



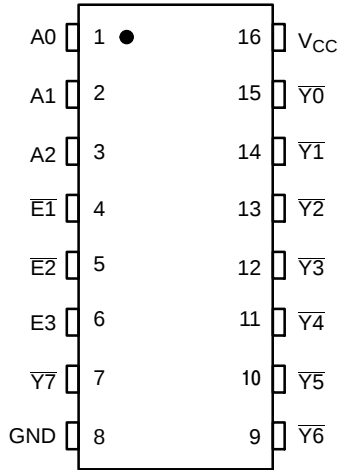
XXXX = Specific Device Code
A = Assembly Location
WL, L = Wafer Lot
Y = Year
WW, W = Work Week
G or ■ = Pb-Free Package

ORDERING INFORMATION

See detailed ordering and shipping information on page 8 of this data sheet.

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PIN ASSIGNMENT

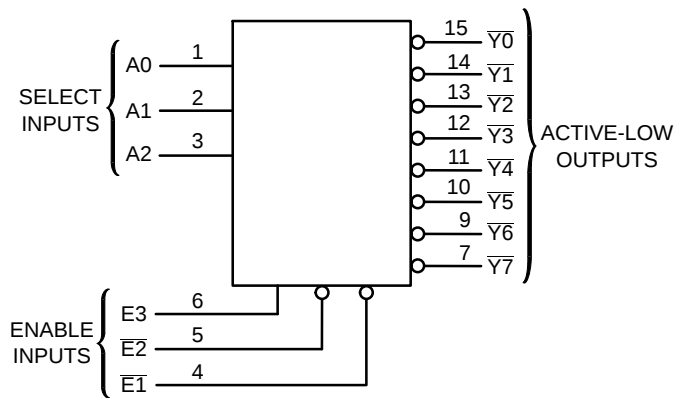


FUNCTION TABLE

Inputs						Outputs							
E3	E2	E1	A2	A1	A0	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	X	H	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	L	H	H	H	H	L	H	H	H	H	H
H	L	L	H	L	H	H	H	H	H	L	H	H	H
H	L	L	H	H	L	H	H	H	H	H	L	H	H
H	L	L	H	H	H	H	H	H	H	H	H	L	H

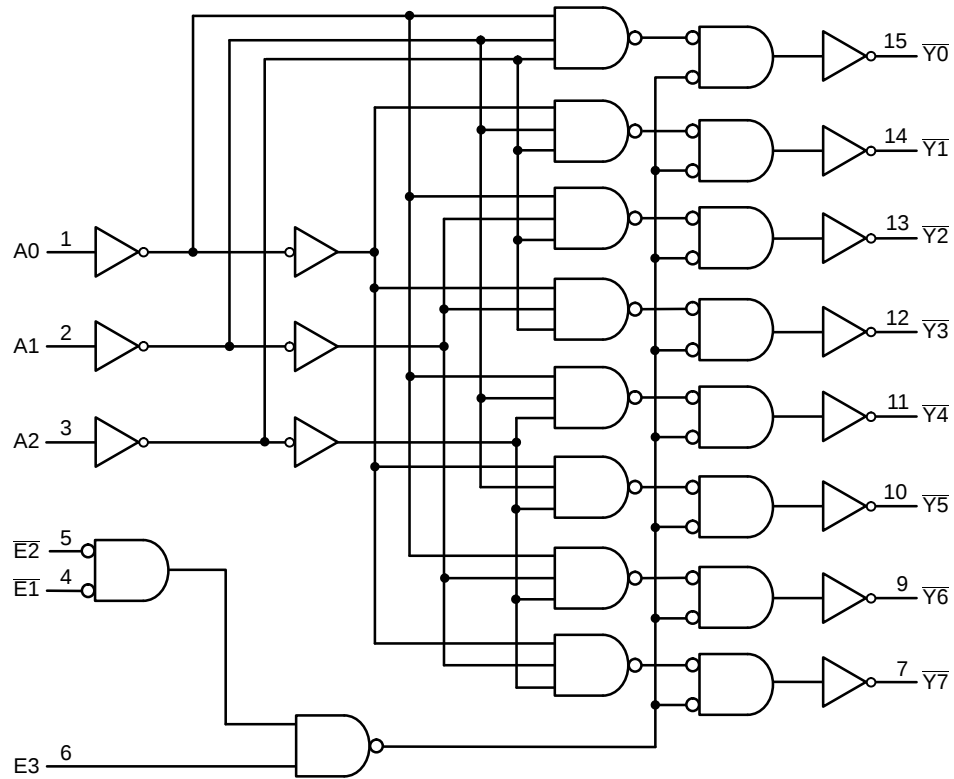
H = high level (steady state); L = low level (steady state);
X = don't care

LOGIC DIAGRAM

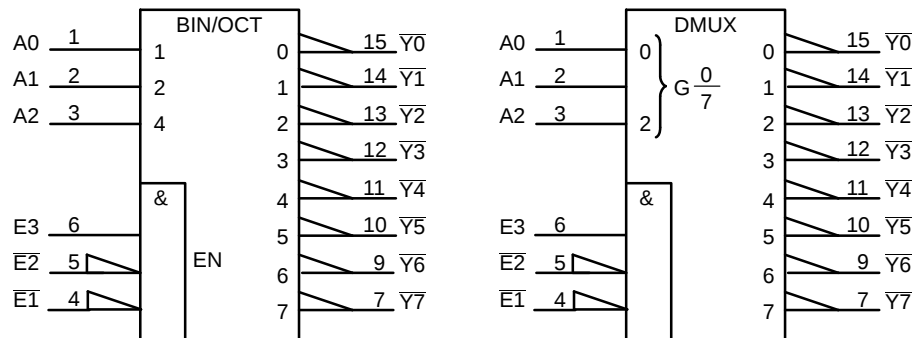


MC74VHC138, MC74VHCT138A

EXPANDED LOGIC DIAGRAM



IEC LOGIC DIAGRAM



MC74VHC138, MC74VHCT138A

MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V _{CC}	DC Supply Voltage		−0.5 to +6.5	V
V _{IN}	DC Input Voltage		−0.5 to +6.5	V
V _{OUT}	DC Output Voltage (MC74VHC)		−0.5 to V _{CC} +0.5	V
	DC Output Voltage (MC74VHCT)	Active Mode (High or Low State) Tristate Mode (Note 1) Power-Off Mode (V _{CC} = 0 V)	−0.5 to V _{CC} +0.5 −0.5 to +6.5 −0.5 to +6.5	
I _{IN}	DC Input Current, per Pin		±20	mA
I _{OUT}	DC Output Current, per Pin		±25	mA
I _{CC}	DC Supply Current, V _{CC} and GND Pins		±75	mA
I _{IK}	Input Clamp Current		−20	mA
I _{OK}	Output Clamp Current	MC74VHC MC74VHCT	±20 −20	mA
T _{STG}	Storage Temperature Range		−65 to +150	°C
T _L	Lead Temperature, 1 mm from Case for 10 Seconds		260	°C
T _J	Junction Temperature Under Bias		+150	°C
θ _{JA}	Thermal Resistance (Note 2)	SOIC-16 TSSOP-16	126 159	°C/W
P _D	Power Dissipation in Still Air at 25 °C	SOIC-16 TSSOP-16	995 787	mW
MSL	Moisture Sensitivity		Level 1	
F _R	Flammability Rating	Oxygen Index: 28 to 34	UL 94 V−0 @ 0.138 in	
V _{ESD}	ESD Withstand Voltage (Note 3)	Human Body Model Charged Device Model	2000 N/A	V
I _{LATCHUP}	Latchup Performance (Note 4)		±100	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Applicable to devices with outputs that may be tri-stated.
2. Measured with minimum pad spacing on an FR4 board, using 76 mm-by-114 mm, 2-ounce copper trace no air flow per JESD51-7.
3. HBM tested to EIA / JESD22-A114-A. CDM tested to JESD22-C101-A. JEDEC recommends that ESD qualification to EIA/JESD22-A115A (Machine Model) be discontinued.
4. Tested to EIA/JESD78 Class II.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
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MC74VHC

V _{CC}	DC Supply Voltage	2.0	5.5	V
V _{IN}	DC Input Voltage (Note 5)	0	5.5	V
V _{OUT}	DC Output Voltage (Note 5)	0	V _{CC}	V
T _A	Operating Temperature	−55	+125	°C
t _r , t _f	Input Rise or Fall Rate	V _{CC} = 3.0 V to 3.6 V V _{CC} = 4.5 V to 5.5 V		0 100 20 ns/V

MC74VHCT

V _{CC}	DC Supply Voltage	2.0	5.5	V
V _{IN}	DC Input Voltage (Note 5)	0	5.5	V
V _{OUT}	DC Output Voltage (Note 5)	Active Mode (High or Low State) Tristate Mode Power-Off Mode (V _{CC} = 0 V)		0 0 0 V _{CC} 5.5 5.5 V
T _A	Operating Temperature	−55	+125	°C
t _r , t _f	Input Rise or Fall Rate	V _{CC} = 4.5 V to 5.5 V		0 20 ns/V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

5. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

MC74VHC138, MC74VHCT138A

DC ELECTRICAL CHARACTERISTICS (MC74VHC138)

Symbol	Parameter	Test Conditions	V _{CC} (V)	T _A = 25 °C			T _A = ≤ 85 °C		T _A = ≤ 125 °C		Unit
				Min	Typ	Max	Min	Max	Min	Max	
V _{IH}	Minimum High-Level Input Voltage		2.0	1.5	–	–	1.5	–	1.5	–	V
			3.0	2.1	–	–	2.1	–	2.1	–	
			4.5	3.15	–	–	3.15	–	3.15	–	
			5.5	3.85	–	–	3.85	–	3.85	–	
V _{IL}	Maximum Low-Level Input Voltage		2.0	–	–	0.5	–	0.5	–	0.5	V
			3.0	–	–	0.9	–	0.9	–	0.9	
			4.5	–	–	1.35	–	1.35	–	1.35	
			5.5	–	–	1.65	–	1.65	–	1.65	
V _{OH}	Minimum High-Level Output Voltage V _{IN} = V _{IH} or V _{IL}	V _{IN} = V _{IH} or V _{IL} I _{OH} = –50 A	2.0	1.9	2.0	–	1.9	–	1.9	–	V
			3.0	2.9	3.0	–	2.9	–	2.9	–	
			4.5	4.4	4.5	–	4.4	–	4.4	–	
		V _{IN} = V _{IH} or V _{IL} I _{OH} = –4 mA I _{OH} = –8 mA	3.0	2.58	–	–	2.48	–	2.34	–	
V _{OL}	Maximum Low-Level Output Voltage V _{IN} = V _{IH} or V _{IL}	V _{IN} = V _{IH} or V _{IL} I _{OL} = 50 A	2.0	–	0.0	0.1	–	0.1	–	0.1	V
			3.0	–	0.0	0.1	–	0.1	–	0.1	
			4.5	–	0.0	0.1	–	0.1	–	0.1	
		V _{IN} = V _{IH} or V _{IL} I _{OL} = 4 mA I _{OL} = 8 mA	3.0	–	–	0.36	–	0.44	–	0.52	
I _{IN}	Maximum Input Leakage Current	V _{IN} = 5.5 V or GND	0 to 5.5	–	–	±0.1	–	±1.0	–	±1.0	μA
I _{CC}	Maximum Quiescent Supply Current	V _{IN} = V _{CC} or GND	5.5	–	–	4.0	–	40.0	–	40.0	μA

AC ELECTRICAL CHARACTERISTICS (MC74VHC138)

Symbol	Parameter	Test Conditions	T _A = 25 °C			T _A = – 40 to 85 °C		T _A = – 55 to 125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, A to Y	V _{CC} = 3.3 ± 0.3 V C _L = 15 pF C _L = 50 pF	–	8.2	11.4	1.0	13.5	1.0	13.5	ns
		V _{CC} = 5.0 ± 0.5 V C _L = 15 pF C _L = 50 pF	–	5.7	8.1	1.0	9.5	1.0	9.5	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, E3 to Y	V _{CC} = 3.3 ± 0.3 V C _L = 15 pF C _L = 50 pF	–	8.1	12.8	1.0	15.0	1.0	15.0	ns
		V _{CC} = 5.0 ± 0.5 V C _L = 15 pF C _L = 50 pF	–	5.6	8.1	1.0	9.5	1.0	9.5	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, E2 or E1 to Y	V _{CC} = 3.3 ± 0.3 V C _L = 15 pF C _L = 50 pF	–	8.2	11.4	1.0	13.5	1.0	13.5	ns
		V _{CC} = 5.0 ± 0.5 V C _L = 15 pF C _L = 50 pF	–	5.8	8.1	1.0	9.5	1.0	9.5	
C _{IN}	Maximum Input Capacitance		–	4	10	–	10	–	10	pF

C _{PD}	Power Dissipation Capacitance (Note 1)	Typical @ 25 °C, V _{CC} = 5.0 V	pF
		34	

1. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I_{CC(OPR)} = C_{PD} • V_{CC} • f_{in} + I_{CC}. C_{PD} is used to determine the no-load dynamic power consumption; P_D = C_{PD} • V_{CC}² • f_{in} + I_{CC} • V_{CC}.

MC74VHC138, MC74VHCT138A

DC ELECTRICAL CHARACTERISTICS (MC74VHCT138A)

Symbol	Parameter	Test Conditions	V _{CC} (V)	T _A = 25 °C			T _A ≤ 85 °C		T _A ≤ 125 °C		Unit
				Min	Typ	Max	Min	Max	Min	Max	
V _{IH}	Minimum High-Level Input Voltage		3.0 4.5 5.5	1.4 2.0 2.0	– – –	– – –	1.4 2.0 2.0	– – –	1.4 2.0 2.0	– – –	V
V _{IL}	Maximum Low-Level Input Voltage		3.0 4.5 5.5	– – –	– – –	0.53 0.8 0.8	– – –	0.53 0.8 0.8	– – –	0.53 0.8 0.8	V
V _{OH}	Minimum High-Level Output Voltage V _{IN} = V _{IH} or V _{IL}	V _{IN} = V _{IH} or V _{IL} I _{OH} = –50 µA	3.0 4.5	2.9 4.4	3.0 4.5	– –	2.9 4.4	– –	2.9 4.4	– –	V
		V _{IN} = V _{IH} or V _{IL} I _{OH} = –4 mA I _{OH} = –8 mA	3.0 4.5	2.58 3.94	– –	– –	2.48 3.80	– –	2.34 3.66	– –	V
V _{OL}	Maximum Low-Level Output Voltage V _{IN} = V _{IH} or V _{IL}	V _{IN} = V _{IH} or V _{IL} I _{OL} = 50 µA	3.0 4.5	– –	0.0 0.0	0.1 0.1	– –	0.1 0.1	– –	0.1 0.1	V
		V _{IN} = V _{IH} or V _{IL} I _{OL} = 4 mA I _{OL} = 8 mA	3.0 4.5	– –	– –	0.36 0.36	– –	0.44 0.44	– –	0.52 0.52	V
I _{IN}	Maximum Input Leakage Current	V _{IN} = 5.5 V or GND	0 to 5.5	–	–	±0.1	–	±1.0	–	±1.0	µA
I _{CC}	Maximum Quiescent Supply Current	V _{IN} = V _{CC} or GND	5.5	–	–	4.0	–	40.0	–	40.0	µA
I _{CC(T)}	Quiescent Supply Current	V _{IN} = 3.4 V	5.5	–	–	1.35	–	1.50	–	1.50	mA
I _{OPD}	Output Leakage Current	V _{OUT} = 5.5 V	0.0	–	–	0.5	–	5.0	–	5.0	µA

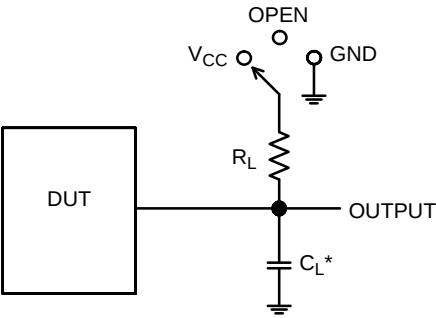
AC ELECTRICAL CHARACTERISTICS (MC74VHCT138A)

Symbol	Parameter	Test Conditions	T _A = 25 °C			T _A ≤ 85 °C		T _A ≤ 125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Input A to Y	V _{CC} = 3.3 ±0.3 V C _L = 15 pF C _L = 50 pF	– –	9.5 10.8	14.5 15.5	1.0 1.0	16.0 17.0	1.0 1.0	16.0 17.0	ns
		V _{CC} = 5.0 ±0.5 V C _L = 15 pF C _L = 50 pF	– –	7.6 8.1	10.4 11.4	1.0 1.0	12.0 13.0	1.0 1.0	12.0 13.0	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Input E3 to Y	V _{CC} = 3.3 ±0.3 V C _L = 15 pF C _L = 50 pF	– –	9.7 9.5	13.0 14.0	1.0 1.0	14.5 15.5	1.0 1.0	14.5 15.5	ns
		V _{CC} = 5.0 ±0.5 V C _L = 15 pF C _L = 50 pF	– –	6.6 7.1	9.1 10.1	1.0 1.0	10.5 11.5	1.0 1.0	10.5 11.5	
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Input E1 or E2 to Y	V _{CC} = 3.3 ±0.3 V C _L = 15 pF C _L = 50 pF	– –	10.1 9.9	14.0 15.0	1.0 1.0	15.5 16.5	1.0 1.0	15.5 16.5	ns
		V _{CC} = 5.0 ±0.5 V C _L = 15 pF C _L = 50 pF	– –	7.0 7.5	9.6 10.6	1.0 1.0	11.0 12.0	1.0 1.0	11.0 12.0	
C _{IN}	Maximum Input Capacitance		–	4	10	–	10	–	10	pF

C _{PD}	Power Dissipation Capacitance (Note 1)	Typical @ 25 °C, V _{CC} = 5.0 V	pF
		49	

1. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I_{CC(OPR)} = C_{PD} • V_{CC} • f_{in} + I_{CC}. C_{PD} is used to determine the no-load dynamic power consumption; P_D = C_{PD} • V_{CC}² • f_{in} + I_{CC} • V_{CC}.

MC74VHC138, MC74VHCT138A



Test	Switch Position	C _L	R _L
t _{PLH} / t _{PHL}	Open	See AC Characteristics Table	1 kΩ
t _{PLZ} / t _{PZL}	V _{CC}		
t _{PHZ} / t _{PZH}	GND		

Figure 1. Test Circuit

Device	V _{IN} , V	V _m , V
MC74VHC138	V _{CC}	50% x V _{CC}
MC74VHCT138A	3 V	1.5 V

SWITCHING WAVEFORMS

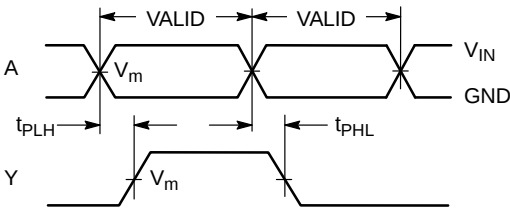


Figure 2.

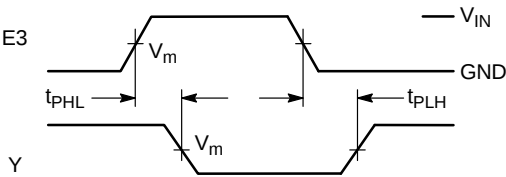


Figure 3.

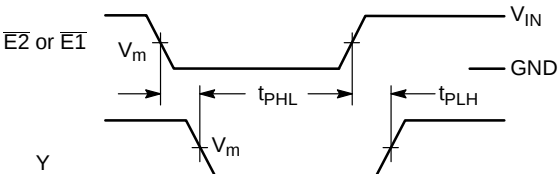


Figure 4.

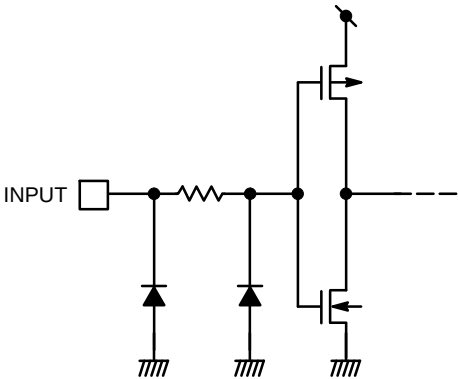


Figure 5. Input Equivalent Circuit

MC74VHC138, MC74VHCT138A

ORDERING INFORMATION

Order Number	Package Number	Package	Shipping [†]
MC74VHC138DR2G	VHC138G	SOIC-16 (Pb-Free)	2500 Units / Tape & Reel
MC74VHC138DTR2G	VHC 138	TSSOP-16 (Pb-Free)	2500 Units / Tape & Reel
MC74VHCT138ADR2G	VHCT138AG	SOIC-16 (Pb-Free)	2500 Units / Tape & Reel
MC74VHCT138ADTR2G	VHCT 138A	TSSOP-16 (Pb-Free)	2500 Units / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.


SOIC-16 9.90x3.90x1.37 1.27P
CASE 751B
ISSUE M

DATE 18 OCT 2024

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. DIMENSION IN MILLIMETERS. ANGLE IN DEGREES.
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15mm PER SIDE.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127mm TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.



MILLIMETERS			
DIM	MIN	NOM	MAX
A	1.35	1.55	1.75
A1	0.10	0.18	0.25
A2	1.25	1.37	1.50
b	0.35	0.42	0.49
c	0.19	0.22	0.25
D	9.90 BSC		
E	6.00 BSC		
E1	3.90 BSC		
e	1.27 BSC		
h	0.25	---	0.50
L	0.40	0.83	1.25
L1	1.05 REF		
θ	0°	---	7°
TOLERANCE OF FORM AND POSITION			
aaa	0.10		
bbb	0.20		
ccc	0.10		
ddd	0.25		
eee	0.10		



*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE onsemi SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERM/D

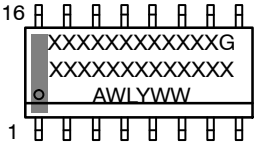
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SOIC-16 9.90x3.90x1.37 1.27P
CASE 751B
ISSUE M

DATE 18 OCT 2024

GENERIC
MARKING DIAGRAM*



XXXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLE 1: PIN 1. COLLECTOR 2. BASE 3. EMITTER 4. NO CONNECTION 5. EMITTER 6. BASE 7. COLLECTOR 8. COLLECTOR 9. BASE 10. EMITTER 11. NO CONNECTION 12. EMITTER 13. BASE 14. COLLECTOR 15. EMITTER 16. COLLECTOR	STYLE 2: PIN 1. CATHODE 2. ANODE 3. NO CONNECTION 4. CATHODE 5. CATHODE 6. NO CONNECTION 7. ANODE 8. CATHODE 9. CATHODE 10. ANODE 11. NO CONNECTION 12. CATHODE 13. CATHODE 14. NO CONNECTION 15. ANODE 16. CATHODE	STYLE 3: PIN 1. COLLECTOR, DYE #1 2. BASE, #1 3. EMITTER, #1 4. COLLECTOR, #1 5. COLLECTOR, #2 6. BASE, #2 7. EMITTER, #2 8. COLLECTOR, #2 9. COLLECTOR, #3 10. BASE, #3 11. EMITTER, #3 12. COLLECTOR, #3 13. COLLECTOR, #4 14. BASE, #4 15. EMITTER, #4 16. COLLECTOR, #4	STYLE 4: PIN 1. COLLECTOR, DYE #1 2. COLLECTOR, #1 3. COLLECTOR, #2 4. COLLECTOR, #2 5. COLLECTOR, #3 6. COLLECTOR, #3 7. COLLECTOR, #4 8. COLLECTOR, #4 9. BASE, #4 10. EMITTER, #4 11. BASE, #3 12. EMITTER, #3 13. BASE, #2 14. EMITTER, #2 15. BASE, #1 16. EMITTER, #1
STYLE 5: PIN 1. DRAIN, DYE #1 2. DRAIN, #1 3. DRAIN, #2 4. DRAIN, #2 5. DRAIN, #3 6. DRAIN, #3 7. DRAIN, #4 8. DRAIN, #4 9. GATE, #4 10. SOURCE, #4 11. GATE, #3 12. SOURCE, #3 13. GATE, #2 14. SOURCE, #2 15. GATE, #1 16. SOURCE, #1	STYLE 6: PIN 1. CATHODE 2. CATHODE 3. CATHODE 4. CATHODE 5. CATHODE 6. CATHODE 7. CATHODE 8. CATHODE 9. ANODE 10. ANODE 11. ANODE 12. ANODE 13. ANODE 14. ANODE 15. ANODE 16. ANODE	STYLE 7: PIN 1. SOURCE N-CH 2. COMMON DRAIN (OUTPUT) 3. COMMON DRAIN (OUTPUT) 4. GATE P-CH 5. COMMON DRAIN (OUTPUT) 6. COMMON DRAIN (OUTPUT) 7. COMMON DRAIN (OUTPUT) 8. SOURCE P-CH 9. SOURCE P-CH 10. COMMON DRAIN (OUTPUT) 11. COMMON DRAIN (OUTPUT) 12. COMMON DRAIN (OUTPUT) 13. GATE N-CH 14. COMMON DRAIN (OUTPUT) 15. COMMON DRAIN (OUTPUT) 16. SOURCE N-CH	

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TSSOP-16 WB
CASE 948F
ISSUE B

DATE 19 OCT 2006

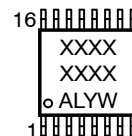

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

**RECOMMENDED
SOLDERING FOOTPRINT***


*For additional information on our Pb-Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

**GENERIC
MARKING DIAGRAM***


XXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
G or ■ = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.

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