Octal Bus Transceiver

With 5 V-Tolerant Inputs

MC74LVX245

The MC74LVX245 is an advanced high speed CMOS octal bus transceiver.

It is intended for two-way asynchronous communication between data buses. The direction of data transmission is determined by the level of the T/$\overline{R}$ input. The output enable pin ($\overline{OE}$) can be used to disable the device, so that the buses are effectively isolated.

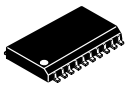
All inputs are equipped with protection circuits against static discharge.

Features

- High Speed: t_{PD} = 4.7 ns (Typ) at V_{CC} = 3.3 V
- Low Power Dissipation: I_{CC} = 4 μA (Max) at T_A = 25 °C
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Low Noise: V_{OLP} = 0.8 V (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 100 mA
- ESD Performance: Human Body Model > 2000 V
- These Devices are Pb-Free and are RoHS Compliant

Application Notes

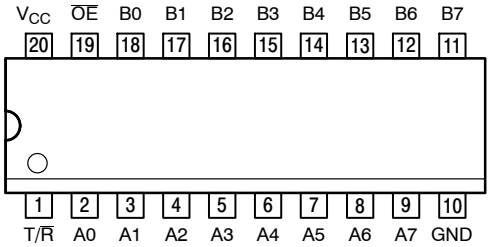
- Do Not Force a Signal on an I/O Pin when it is an Active Output, Damage May Occur
- All Floating (High Impedance) Input or I/O Pins must be Fixed by Means of Pullup or Pulldown Resistors or Bus Terminator ICs
- A Parasitic Diode is Formed between the Bus and V_{CC} Terminals Therefore, the LVX245 cannot be Used to Interface 5.0 V to 3.0 V Systems Directly



SOIC-20
DW SUFFIX
CASE 751D

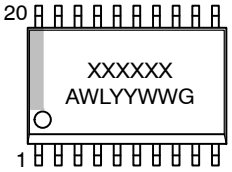
TSSOP-20
DT SUFFIX
CASE 948E

PIN ASSIGNMENT

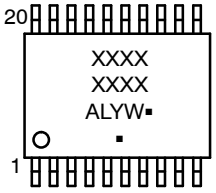


20-Lead (Top View)

MARKING DIAGRAMS



SOIC-20



TSSOP-20

XXXXXXX	= Specific Device Code
A	= Assembly Location
WL, L	= Wafer Lot
Y	= Year
WW, W	= Work Week
G or ▪	= Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information on page 6 of this data sheet.

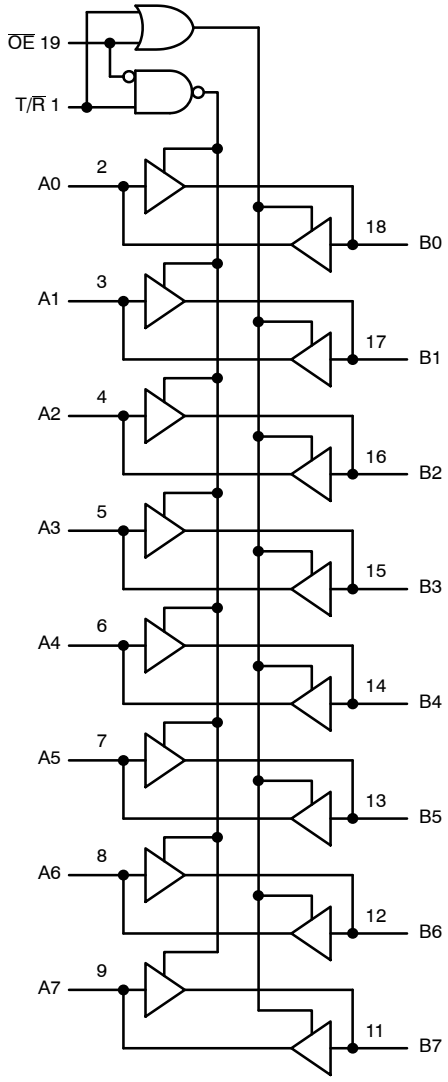


Figure 1. Logic Diagram

Table 1. PIN NAMES

Pins	Function
$\overline{OE}$	Output Enable Input
T/$\overline{R}$	Transmit/Receive Input
A0–A7	Side A 3-State Inputs or 3-State Outputs
Bo–B7	Side B 3-State Inputs or 3-State Outputs

Inputs		Operating Mode Non-Inverting
OE	T/$\overline{R}$	
L	L	B Data to A Bus
L	H	A Data to B Bus
H	X	Z

H = High Voltage Level;
L = Low Voltage Level;
Z = High Impedance State;
X = High or Low Voltage Level and Transitions are Acceptable;
For I_{CC} reasons, Do Not Float Inputs

MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}	DC Supply Voltage		−0.5 to +6.5	V
V_{IN}	DC Input Voltage		−0.5 to +6.5	V
V_{OUT}	DC Output Voltage		−0.5 to V_{CC}+0.5	V
I_{IN}	DC Input Current, per Pin		±20	mA
I_{OUT}	DC Output Current, Per Pin		±25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins		±75	mA
I_{IK}	Input Clamp Current		−20	mA
I_{OK}	Output Clamp Current		±20	mA
T_{STG}	Storage Temperature Range		−65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 secs		260	°C
T_J	Junction Temperature Under Bias		+150	°C
θ_{JA}	Thermal Resistance (Note 2)	SOIC-20W TSSOP-20	96 150	°C/W
P_D	Power Dissipation in Still Air at 25 °C	SOIC-20W TSSOP-20	1302 833	mW
MSL	Moisture Sensitivity	SOIC-20W All Other Packages	Level 3 Level 1	–
F_R	Flammability Rating	Oxygen Index: 28 to 34	UL 94 V-0 @ 0.573 in	–
V_{ESD}	ESD Withstand Voltage (Note 3)	Human Body Model Charged Device Model	2000 N/A	V
$I_{LATCHUP}$	Latchup Performance (Note 4)		±100	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Applicable to devices with outputs that may be tri-stated.
2. Measured with minimum pad spacing on an FR4 board, using 76 mm-by-114 mm, 2-ounce copper trace no air flow per JESD51-7.
3. HBM tested to EIA / JESD22-A114-A. CDM tested to JESD22-C101-A. JEDEC recommends that ESD qualification to EIA/JESD22-A115A (Machine Model) be discontinued.
4. Tested to EIA/JESD78 Class II.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage	2.0	3.6	V
V_{in}	DC Input Voltage ($T/\overline{R}$, $\overline{OE}$)	0	5.5	V
$V_{I/O}$	DC Output Voltage	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	−40	+85	°C
$\Delta t/\Delta V$	Input Rise and Fall Time	0	100	ns/V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} V	T_A = 25 °C			T_A = −40 to 85 °C		Unit
				Min	Typ	Max	Min	Max	
V_{IH}	High-Level Input Voltage		2.0 3.0 3.6	1.5 2.0 2.4			1.5 2.0 2.4		V
V_{IL}	Low-Level Input Voltage		2.0 3.0 3.6			0.5 0.8 0.8		0.5 0.8 0.8	V
V_{OH}	High-Level Output Voltage (V_{in} = V_{IH} or V_{IL})	I_{OH} = −50 μA I_{OH} = −50 μA I_{OH} = −4 mA	2.0 3.0 3.0	1.9 2.9 2.58	2.0 3.0		1.9 2.9 2.48		V
V_{OL}	Low-Level Output Voltage (V_{in} = V_{IH} or V_{IL})	I_{OL} = 50 μA I_{OL} = 50 μA I_{OL} = 4 mA	2.0 3.0 3.0		0.0 0.0	0.1 0.1 0.36		0.1 0.1 0.44	V
I_{in}	Input Leakage Current	V_{in} = 5.5 V or GND ($T/\overline{R}$, $\overline{OE}$)	3.6			±0.1		±1.0	μA
I_{OZ}	Maximum 3-State Leakage Current	V_{in} = V_{IL} or V_{IH} V_{out} = V_{CC} or GND	3.6			±0.2 5		±2.5	μA
I_{CC}	Quiescent Supply Current	V_{in} = V_{CC} or GND	3.6			4.0		40.0	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

AC ELECTRICAL CHARACTERISTICS (Input t_r = t_f = 3.0 ns)

Symbol	Parameter	Test Conditions		T_A = 25 °C			T_A = −40 to 85 °C		Unit
				Min	Typ	Max	Min	Max	
t_{PLH}, t_{PHL}	Propagation Delay Input to Output	V_{CC} = 2.7 V	C_L = 15 pF C_L = 50 pF		6.1 8.6	10.7 14.2	1.0 1.0	13.5 17.0	ns
		V_{CC} = 3.3 ± 0.3 V	C_L = 15 pF C_L = 50 pF		4.7 7.2	6.6 10.1	1.0 1.0	8.0 11.5	
t_{PZL}, t_{PZH}	Output Enable Time to High and Low Level	V_{CC} = 2.7 V R_L = 1 kΩ	C_L = 15 pF C_L = 50 pF		9.0 11.5	16.9 20.4	1.0 1.0	20.5 24.0	ns
		V_{CC} = 3.3 ± 0.3 V R_L = 1 kΩ	C_L = 15 pF C_L = 50 pF		7.1 9.6	11.0 14.5	1.0 1.0	13.0 16.5	
t_{PLZ}, t_{PHZ}	Output Disable Time From High and Low Level	V_{CC} = 2.7 V R_L = 1 kΩ	C_L = 50 pF		11.5	18.0	1.0	21.0	ns
		V_{CC} = 3.3 ± 0.3 V R_L = 1 kΩ	C_L = 50 pF		9.6	12.8	1.0	14.5	
t_{OSHL} t_{OSLH}	Output-to-Output Skew (Note 5)	V_{CC} = 2.7 V V_{CC} = 3.3 ± 0.3 V	C_L = 50 pF C_L = 50 pF			1.5 1.5		1.5 1.5	ns

5. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}); parameter guaranteed by design.

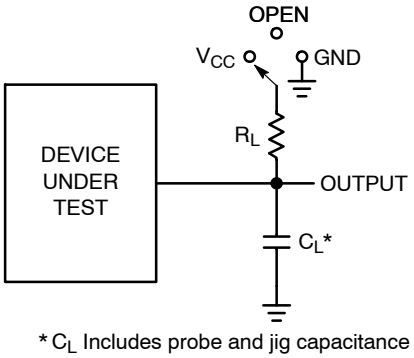
CAPACITIVE CHARACTERISTICS

Symbol	Parameter	T_A = 25 °C			T_A = −40 to 85 °C		Unit
		Min	Typ	Max	Min	Max	
C_{in}	Input Capacitance (T/$\overline{R}$, $\overline{OE}$)		4	10		10	pF
$C_{I/O}$	Maximum 3-State I/O Capacitance		8				pF
C_{PD}	Power Dissipation Capacitance (Note 6)		21				pF

6. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}/8$ (per bit). C_{PD} is used to determine the no-load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

NOISE CHARACTERISTICS (Input $t_r = t_f$ = 3.0 ns, C_L = 50 pF, V_{CC} = 3.3 V, Measured in SOIC Package)

Symbol	Characteristic	T_A = 25 °C		Unit
		Typ	Max	
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	0.5	0.8	V
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	−0.5	−0.8	V
V_{IHD}	Minimum High Level Dynamic Input Voltage		2.0	V
V_{ILD}	Maximum Low Level Dynamic Input Voltage		0.8	V



* C_L Includes probe and jig capacitance

Test	Switch Position	C_L	R_L
t_{PLH} / t_{PHL}	Open	See AC Charact eristics Table	1 kΩ
t_{PLZ} / t_{PZL}	V_{CC}		
t_{PHZ} / t_{PZH}	GND		

Figure 2. Test Circuit

SWITCHING WAVEFORMS

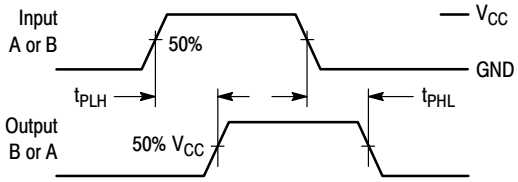


Figure 3.

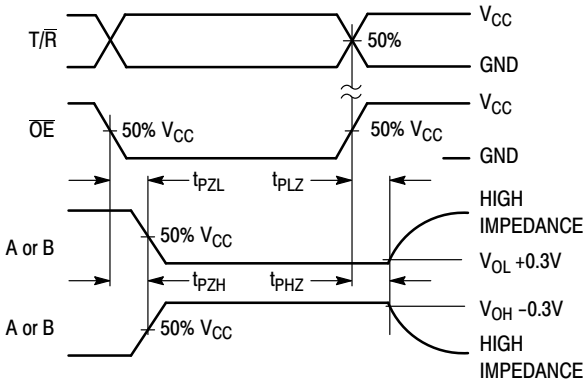


Figure 4.

ORDERING INFORMATION

Device	Marking	Package	Shipping†
MC74LVX245DWR2G	LVX245G	SOIC-20 WB	1000 / Tape & Reel
MC74LVX245DTR2G	LVX 245	TSSOP-20	2500 / Tape & Reel

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

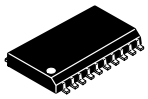
REVISION HISTORY

Revision	Description of Changes	Date
7	Modified voltage ratings from 7.0 V to 6.5 V.	07/09/2025

This document has undergone updates prior to the inclusion of this revision history table. The changes tracked here only reflect updates made on the noted approval dates.

SOIC−20 WB
CASE 751D−05
ISSUE H

DATE 22 APR 2015



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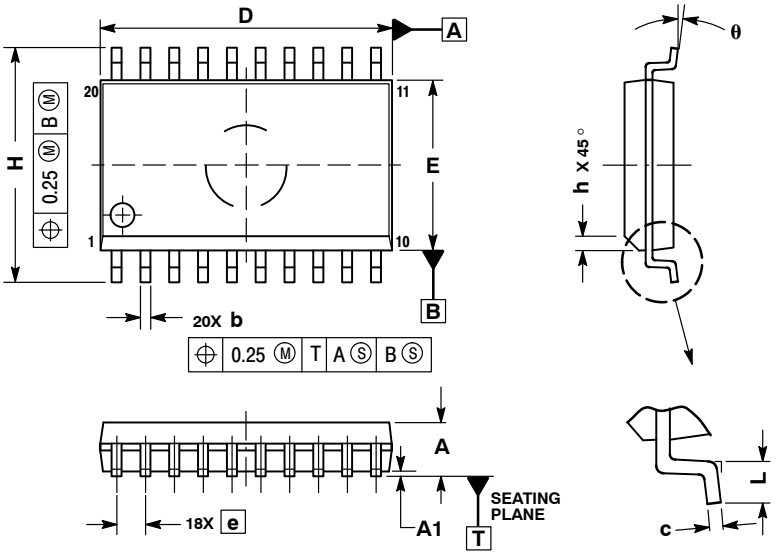
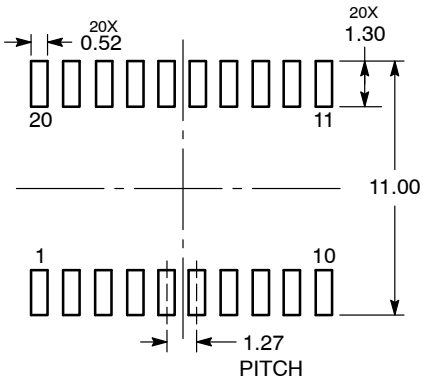


NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS	
DIM	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
b	0.35	0.49
c	0.23	0.32
D	12.65	12.95
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
θ	0°	7°

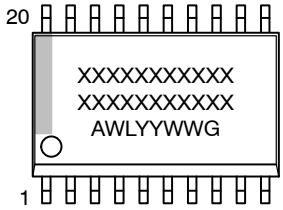
RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



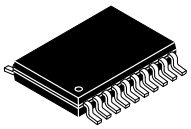
XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	**98ASB42343B**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.	
DESCRIPTION:	**SOIC−20 WB**		**PAGE 1 OF 1**

TSSOP–20 WB
CASE 948E
ISSUE D

DATE 17 FEB 2016



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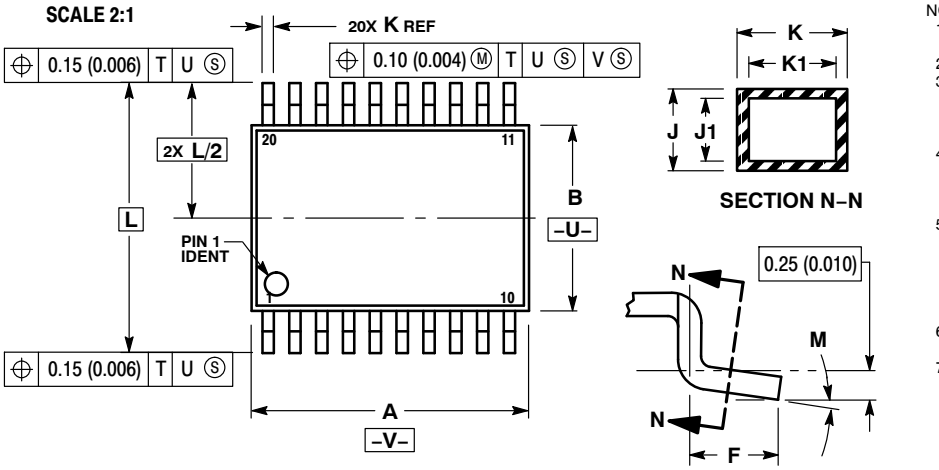
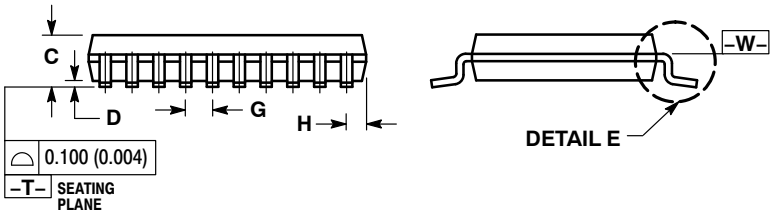


SECTION N–N

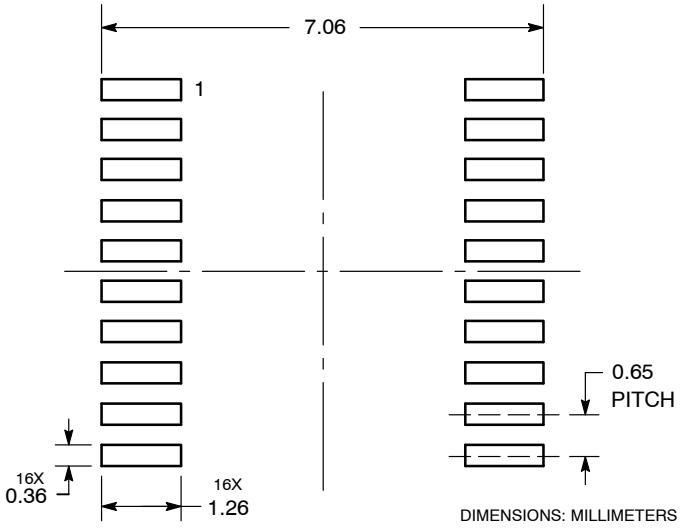
DETAIL E



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE –W–.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	6.40	6.60	0.252	0.260
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.27	0.37	0.011	0.015
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

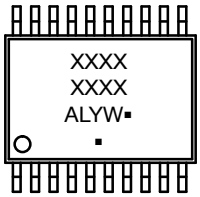
RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb–Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



A = Assembly Location
L = Wafer Lot
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▪ = Pb–Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb–Free indicator, “G” or microdot “ ▪”, may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	**TSSOP–20 WB**		**PAGE 1 OF 1**

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