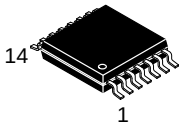
4-Channel LVTTL to GTL Transceiver

FXGL2014



TSSOP-14 WB
CASE 948G

Description

The FXGL2014 is a 4-channel translator to interface between 3.3-V LVTTL chip set I/O and Xeon processor GTL−/GTL/GTL+ I/O.

The FXGL2014 integrates ESD protection cells on all terminals and is available in a TSSOP package (5.0 mm x 4.4 mm). The device is characterized over free air temperature range of −40 °C to 85 °C.

Features

- Operates as a 4-bit GTL−/GTL/GTL+ Sampling Receiver or as a LVTTL to GTL−/GTL/GTL+ Driver
- 3.0 V to 3.6 V Operation with 5 V Tolerant LVTTL Input
- GTL Input and Output 3.6 V Tolerant
- Vref Adjustable from 0.5 V to VCC / 2
- Partial Power-down Permitted
- Under-Voltage Lockout (UVLO)
- ESD Protection Exceeds 2000 V HBM per JESD22-A114 and 1000 V CDM per JESD22-CC101
- Latch-up Protection Exceeds 500 mA per JESD78
- Package Offered: TSSOP14
- −40 °C to 85 °C Operating Temperature Range

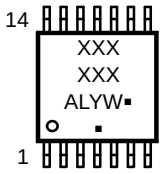
Applications

- Server
- Base Station
- Wire-line Communication

FUNCTIONAL DESCRIPTION

INPUT	INPUT/OUTPUT	
DIR	**A (LVTTL)**	**B (GTL)**
High Voltage	Input	Bn = An
Low Voltage	An = Bn	Input

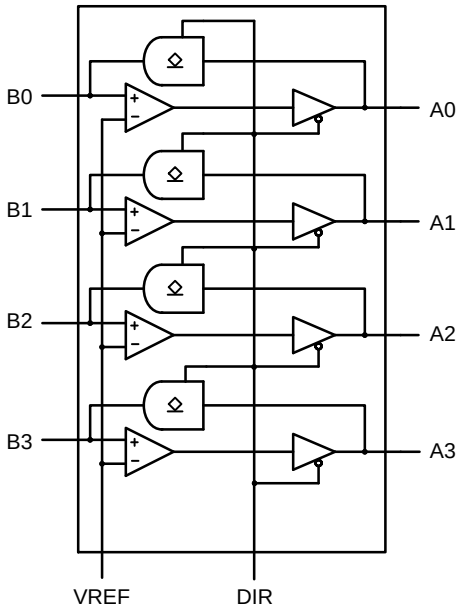
MARKING DIAGRAM



XXX	= Specific Device Code
A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
▪	= Pb-Free Package

(Note: Microdot may be in either location)

ANALOG SYMBOLS



ORDERING INFORMATION

See detailed ordering and shipping information on page 9 of this data sheet.

PIN CONFIGURATION

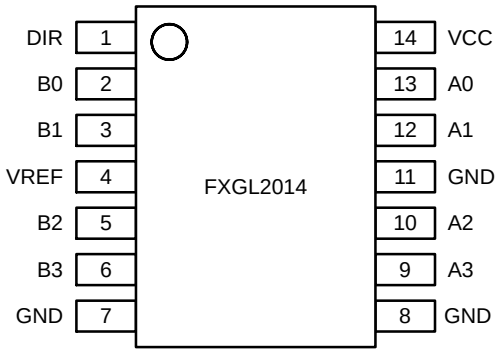


Figure 1. Pin Assignment (Top Through View)

PIN DESCRIPTION

Pin Name	Pin #	Description
A0	13	LVTTL Data Input / Output
A1	12	
A2	10	
A3	9	
B0	2	GTL Data Input / Output
B1	3	
B2	5	
B3	6	
DIR	1	Direction Control Input (LVTTL)
GND	7	Ground
	8	
	11	
VCC	14	Supply Voltage
VREF	4	GTL Reference Voltage

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Min	Max	Unit
V_{CC}	Supply Voltage		−0.5	4.6	V
I_{IK}	Input Clamping Current, V_I < 0 V		−	−50	mA
V_{DIR}	Input Control Voltages DIR		−0.5	6	V
V_I	Input Voltage	A Port	−0.5	6.5	V
		B Port	−0.5	4.6	
I_{CK}	Control Input Clamp Current, V_O < 0 V		−	−50	mA
V_O	Output Voltage in Off-State	A Port	−0.5	6.5	V
		B Port	−0.5	4.6	
I_{OL}	Current into Any Output in the Low State	A Port	−	40	mA
		B Port	−	80	
I_{OH}	Current into Any Output in the High State		−	−40	mA
T_{stg}	Storage Temperature Range		−55	150	°C
V_{ESD}	Human Body Model (HBM), JEDEC: JESD22-A114	All Pins	2	−	kV
	Charged Device Model, JEDEC: JESD22-C101	All Pins	1	−	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage		3.0	3.3	3.6	V
V_{TT}	Termination Voltage	GTL−	0.85	0.90	0.95	V
		GTL	1.14	1.20	1.26	
		GTL+	1.35	1.50	1.65	
V_{REF}	Reference Voltage	Overall	0.5	2/3 V_{TT}	V_{CC}/2	V
		GTL−	0.50	0.60	0.63	
		GTL	0.76	0.80	0.84	
		GTL+	0.87	1.00	1.10	
V_I	Input Voltage	A Port	0	3.3	5.5 (Note 3)	V
		B Port	0	VTT	3.6	
V_{IH}	High−level Input Voltage	A Port and DIR	2	−	−	V
		B Port	V_{REF} + 50 mV	−	−	
V_{IL}	Low-level Input Voltage	A Port and DIR	−	−	0.8	V
		B Port	−	−	V_{REF} − 50 mV	
I_{OL}	Low-level Output Current	A Port	−	−	20	mA
		B Port	−	−	50	
I_{OH}	High-level Output Current	A Port	−	−	−20	mA

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

1. Over operating free-air temperature range (unless otherwise noted).
2. All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation.
3. The V_I (max) of LVTTL port is 3.6 V if configured as output (DIR=L).

THERMAL INFORMATION

Thermal Metric		Value	Unit
$R_{\theta JA}$	Junction-to-Ambient Thermal Resistance	116	°C/W
$R_{\theta JC(top)}$	Junction-to-Case (Top) Thermal Resistance	17	

DC ELECTRICAL CHARACTERISTICS (Specified at T_A = −40 °C to 85 °C (unless otherwise noted))

Symbol	Parameter	Conditions	−40 °C to 85 °C			Unit
			Min	Typ	Max	
V_{OH}	A Port	V_{CC} = 3 to 3.6 V, I_{OH} = −100 μA	V_{CC} − 0.2	−	−	V
		V_{CC} = 3 V, I_{OH} = −16 mA	2.0	−	−	
V_{OL}	A Port	V_{CC} = 3 V, I_{OL} = 8 mA	−	0.28	0.40	V
	A Port	V_{CC} = 3 V, I_{OL} = 12 mA	−	0.42	0.60	
	A Port	V_{CC} = 3 V, I_{OL} = 16 mA	−	0.55	0.80	
	B Port	V_{CC} = 3 V, I_{OL} = 40 mA	−	0.23	0.40	
I_I	A Port	V_{CC} = 3.6 V, V_I = V_{CC}	−	−	±1	μA
		V_{CC} = 3.6 V, V_I = 0 V	−	−	±1	
		V_{CC} = 3.6 V, V_I = 5.5 V	−	−	5	
	B Port	V_{CC} = 3.6 V, V_I = V_{TT} or GND	−	−	±1	μA
	Control Pin	V_{CC} = 3.6 V, V_I = V_{CC} or 0 V	−	−	±1	μA
I_{off}	OFF-State Output Current on A Port	V_{CC} = 0 V, V_{IO} = 0 to 3.6 V	−	−	±10	μA
	OFF-State Output Current on A Port	V_{CC} = 0 V, V_{IO} = 3.6 to 5.5 V	−	−	±100	
	OFF-State Output Current on B Port	V_{CC} = 0 V, V_{IO} = 0 to 3.6 V	−	−	±10	
I_{CC}	A Port	V_{CC} = 3.6 V, V_I = V_{CC} or GND, I_O = 0	−	3	10	mA
	B Port	V_{CC} = 3.6 V, V_I = V_{TT} or GND, I_O = 0	−	3	10	mA
ΔI_{CC}	A Port or Control Input	V_{CC} = 3.6 V, V_I = V_{CC} − 0.6 V	−	−	500	μA
V_{UVLO} (Note 4)	Under-Voltage Lockout Threshold	V_{CC} = 0 to 3 V	1.5	−	−	V
C_I (Note 4)	Input Capacitance of Control Pin	V_{CC} = 3 to 3.6 V, V_I = 3.0 V or 0 V	−	2.0	−	pF
C_{IO} (Note 4)	A Port	V_{CC} = 3 to 3.6 V, V_O = 3.0 V or 0 V	−	4.0	−	pF
	B Port	V_{CC} = 3 to 3.6 V, V_O = V_{TT} or 0 V	−	5.46	−	

4. Guaranteed by characterization and / or design. Not production tested.

AC ELECTRICAL CHARACTERISTICS (Over-operating range, T_A = −40 °C to 85 °C, V_{CC} = 3.0 to 3.6 V, GND = 0 V for GTL)

Symbol	Parameter		GTL−			GTL			GTL+			Unit
			V_{CC} = 3.3 V ±0.3 V			V_{CC} = 3.3 V ±0.3 V			V_{CC} = 3.3 V ±0.3 V			
			V_{REF} = 0.6 V			V_{REF} = 0.8 V			V_{REF} = 1 V			
			V_{TT} = 0.9 V			V_{TT} = 1.2 V			V_{TT} = 1.5 V			
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
t_{PLH}	Low to High Propagation Delay (Note 5)	An to Bn	−	2.8	5.0	−	2.8	5.0	−	2.8	5.0	ns
t_{PHL}	High to Low Propagation Delay (Note 5)		−	3.3	7.0	−	3.4	7.0	−	3.4	7.0	
t_{PLH}	Low to High Propagation Delay (Note 5)	Bn to An	−	5.3	8.0	−	5.2	8.0	−	5.1	8.0	ns
t_{PHL}	High to Low Propagation Delay (Note 5)		−	5.2	8.0	−	4.9	7.0	−	4.7	7.0	

5. Guaranteed by characterization and / or design. Not production tested.

TYPICAL CHARACTERISTICS

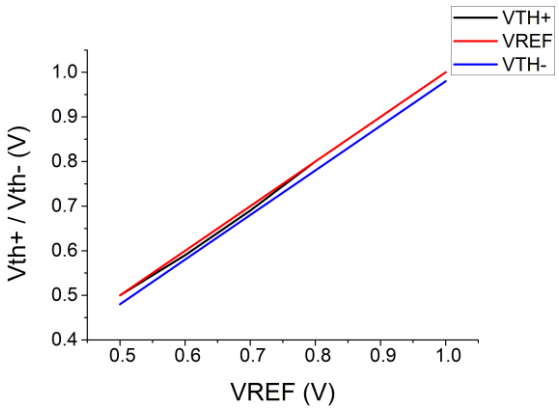


Figure 2. GTL Vth+ and Vth− vs. VREF (−40 °C)

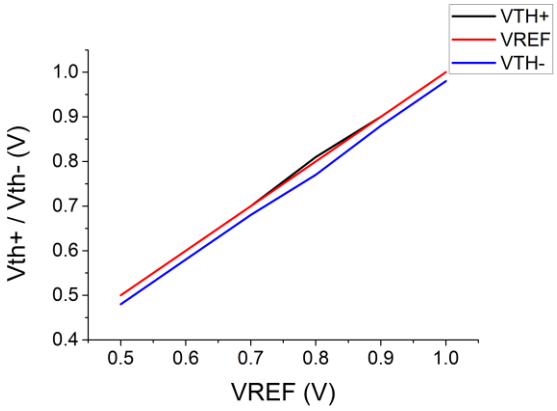


Figure 3. GTL Vth+ and Vth− vs. VREF (25 °C)

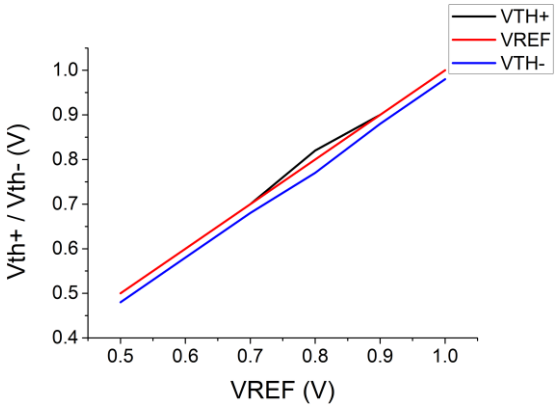


Figure 4. GTL Vth+ and Vth− vs. VREF (85 °C)

TEST INFORMATION

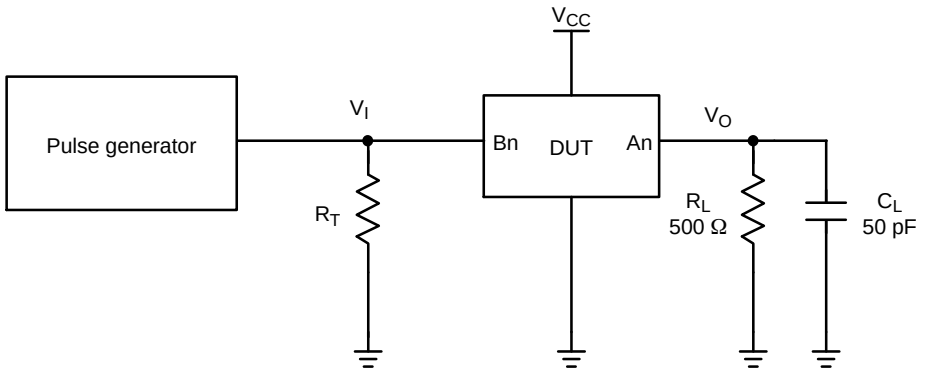


Figure 5. Load Circuit for A Port

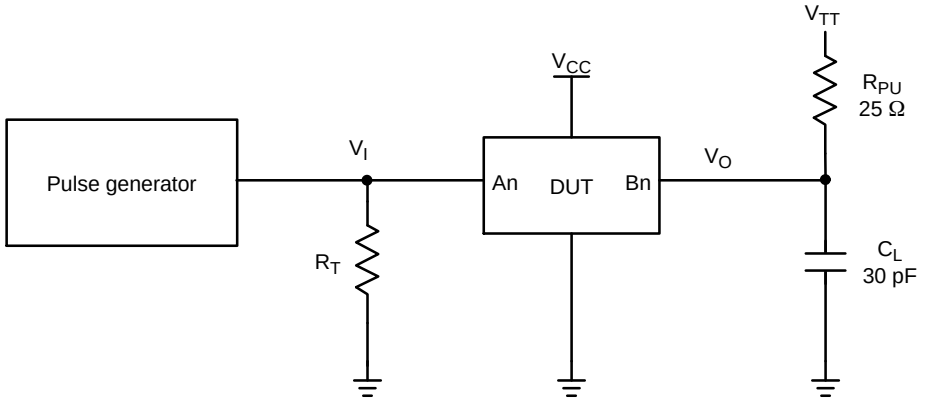
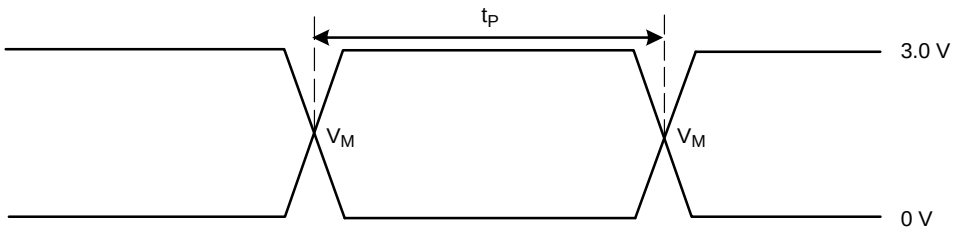


Figure 6. Load Circuit for A Port

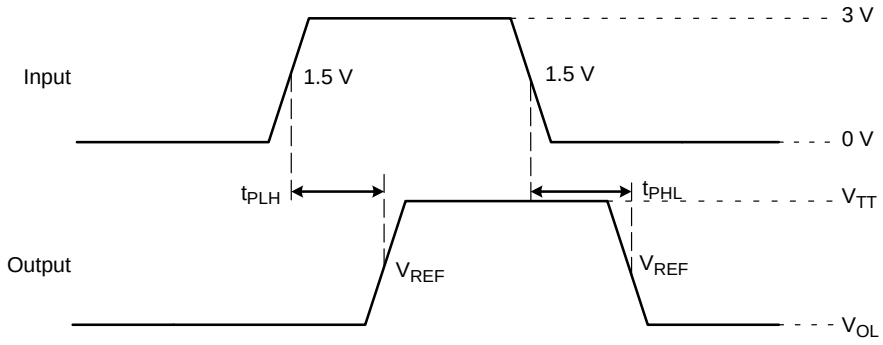
R_T − Termination resistance; should be equal to output impedance of pulse generators.
R_L − Load resistor.
C_L − Load capacitance; includes jig and probe capacitance.

WAVEFORMS

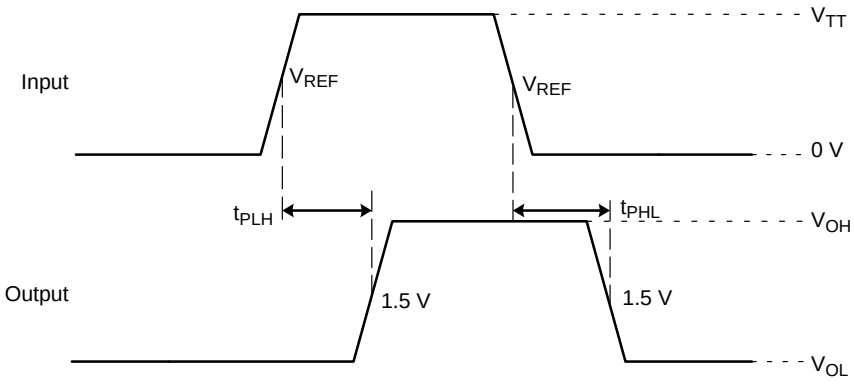
V_M = 1.5 V at V_{CC} ≥ 3.0 V; V_M = V_{CC} at V_{CC} ≥ 2.7 V for A ports and control pins.
V_M = V_{REF} for B ports.



V_M = 1.5 V for A port and V_{REF} for B port
Pulse duration



A port to B port
Propagation delay times



B port to A port
Propagation delay times

Figure 7. Voltage Waveforms

A. All control inputs are LVTTL levels.
B. C_L includes probe and jig capacitance.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time, with one transition per measurement.

APPLICATION INFORMATION

Application Overview

The FXGL2014 is a 4-channel translating transceiver designed for 3.3-V LVTTL system interface with a GTL−/GTL/GTL+ bus, where GTL−/GTL/GTL+ refers to the reference voltage of the GTL bus and the input/output voltage thresholds associated with it.

The direction pin allows the part to function as either a GTL-to-LVTTL sampling receiver or as a LVTTL-to-GTL interface.

The FXGL2014 performs translation in two directions. One direction is GTL−/GTL/GTL+ to LVTTL when DIR is tied to GND. With appropriate V_{REF} set up, the GTL input can be compliant with GTL−/GTL/GTL+. Another direction is LVTTL to GTL−/GTL/GTL+ when DIR is tied to VCC. 3.6 V tolerance on the GTL output allows the GTL outputs to pull up to any voltage level under 3.6 V.

Feature Description

5 V Tolerance on LVTTL Input

The FXGL2014 LVTTL inputs (only) are tolerant up to 5.5 V and allow direct access to TTL or 5 V CMOS inputs. The LVTTL outputs are not 5.5 V tolerant.

3.6 V Tolerance on GTL Input / Output

The FXGL2014 GTL inputs and outputs operate up to 3.6 V, allowing the device to be used in higher voltage open-drain output applications.

Ultra-Low V_{REF} and High Bandwidth

FXGL2014's V_{REF} tracks down to 0.5 V for low voltage CPUs with excellent propagation delay performance. This feature allows the FXGL2014 to support high data rates with the GTL− bus.

Under-Voltage Lockout (UVLO)

Under-voltage lockout circuit is integrated internal. This feature makes sure the data transferred effectively when power unstable.

Typical Application

GTL−/GTL/GTL+ to LVTTL

Select appropriate V_{TT}/V_{REF} based upon GTL−/GTL/GTL+. The parameters in Recommended Operating Conditions are compliant to the GTL specification.

The FXGL2014 requires industrial standard LVTTL and GTL inputs. The design example in the Application Information shows standard voltage level and typical resistor values.

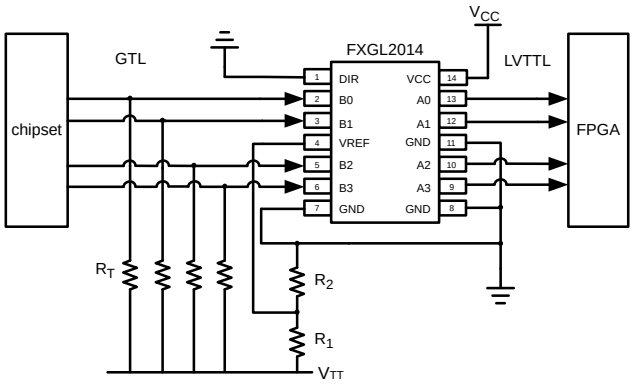


Figure 8. Application Diagram for GTL to LVTTL

Table 1. APPLICATION TABLE FOR GTL TO LVTTL

	Port B to Port A
	GTL to LVTTL
V_{CC}	3.3 V
V_{REF}	2 x VTT/3
V_{TT}	1.0 V
DIR	GND
R_T	75 Ω
R_1	49.9 Ω
R_2	100 Ω

LVTTL to GTL−/GTL/GTL+

Because GTL is an open-drain interface, the selection of the pull-up resistor depends on the application requirement (for example, data rate) and PCB trace capacitance.

The FXGL2014 requires industrial standard LVTTL and GTL inputs. The design example in the Application Information section show standard voltage level and typical resistor values.

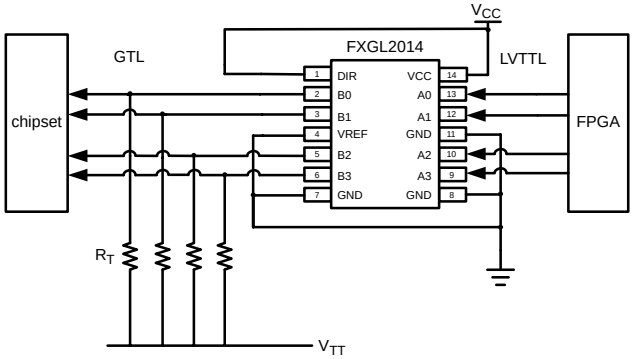


Figure 9. Application Diagram for LVTTL to GTL

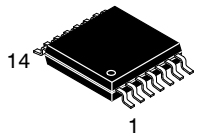
Table 2. APPLICATION TABLE FOR LVTTL TO GTL

	Port A to Port B
	LVTTL to GTL
V_{CC}	3.3 V
V_{REF}	GND
V_{TT}	1.0 V
DIR	GND
R_T	75 Ω
R_1	Not Available
R_2	Not Available

ORDERING INFORMATION

Part Number	Operating Temperature Range	Package	Shipping†
FXGL2014MTCX	−40 °C to 85 °C	5.0 mm x 4.4 mm, 0.65 mm Pitch, 14 Lead TSSOP Package (Pb-Free)	2500 / Tape & Reel

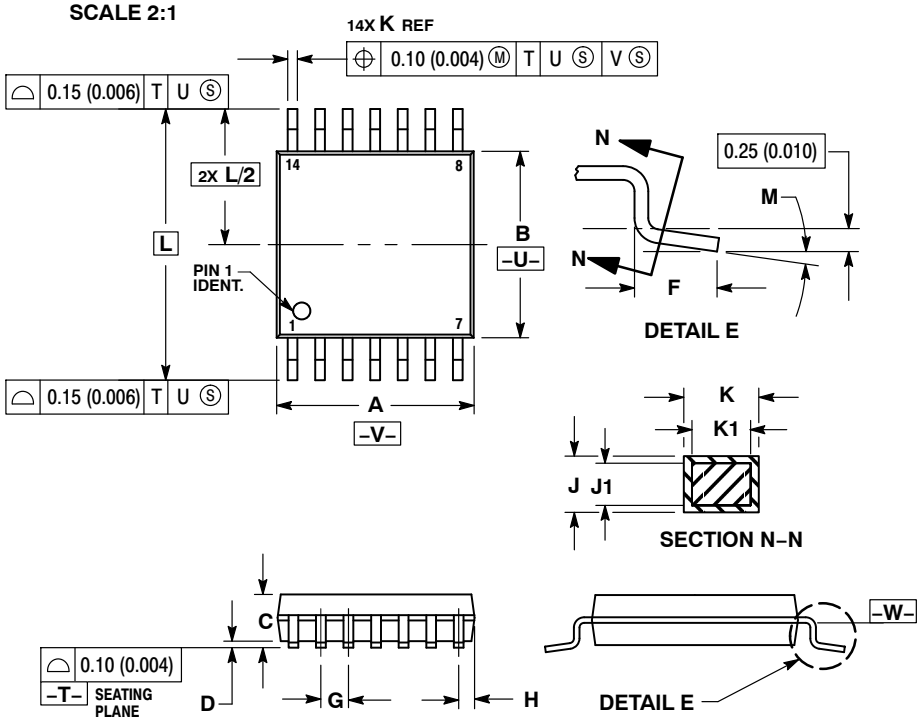
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



SCALE 2:1

TSSOP−14 WB
CASE 948G
ISSUE C

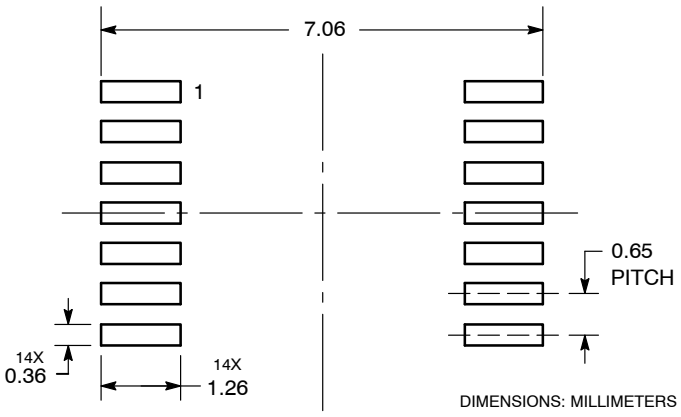
DATE 17 FEB 2016



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

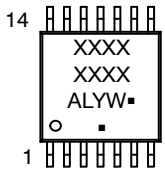
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	−−−	1.20	−−−	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0 °	8 °	0 °	8 °

RECOMMENDED SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
▪	= Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	**TSSOP−14 WB**	**PAGE 1 OF 1**

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
onsemi Website: www.onsemi.com

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