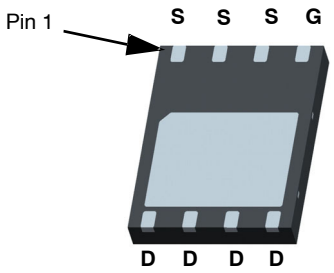
MOSFET – N-Channel, UltraFET Trench

150 V, 27 A, 47 mΩ

FDMS2572



Power 56 (Bottom View)

WDFN8 5x6, 1.27P
CASE 506DP

General Description

UltraFET™ devices combine characteristics that enable benchmark efficiency in power conversion applications. Optimized for $r_{DS(on)}$, low ESR, low total and Miller gate charge, these devices are ideal for high frequency DC to DC converters.

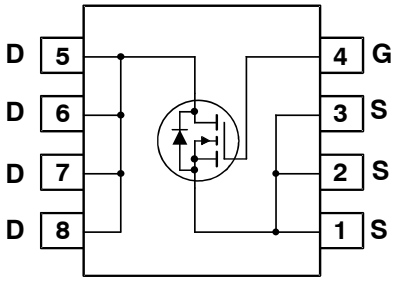
Features

- Max $r_{DS(on)}$ = 47 mΩ at V_{GS} = 10 V, I_D = 4.5 A
- Max $r_{DS(on)}$ = 53 mΩ at V_{GS} = 6 V, I_D = 4.5 A
- Low Miller Charge
- Optimized Efficiency at High Frequencies
- UIS Capability (Single Pulse and Repetitive Pulse)
- This Device is Pb−Free and is RoHS Compliant

Applications

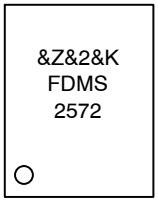
- Distributed Power Architectures and VRMs
- Primary Switch for 24 V and 48 V Systems
- High Voltage Synchronous Rectifier

ELECTRICAL CONNECTION



N-Channel MOSFET

MARKING DIAGRAM



&Z	= Assembly Plant Code
&2	= Numeric Date Code
&K	= Lot Code
FDMS2572	= Specific Device Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 3 of this data sheet.

MOSFET MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Ratings	Unit
V_{DS}	Drain to Source Voltage	150	V
V_{GS}	Gate to Source Voltage	±20	V
I_D	Drain Current: – Continuous (Package limited) T_C = 25°C – Continuous (Silicon limited) T_C = 25°C – Continuous, T_A = 25°C (Note 1a) – Pulsed	 27 27 4.5 30	A
E_{AS}	Single Pulse Avalanche Energy (Note 3)	150	mJ
P_D	Power Dissipation: T_C = 25°C T_A = 25°C (Note 1a)	 78 2.5	W
T_J, T_{STG}	Operating and Storage Junction Temperature Range	−55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

Symbol	Parameter	Ratings	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case	1.6	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	50	

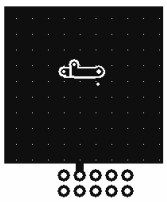
ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250 μA, V_{GS} = 0 V	150			V
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25°C		180		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 120 V, V_{GS} = 0 V			1	μA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±20 V, V_{DS} = 0 V			±100	nA
ON CHARACTERISTICS (Note 2)						
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 μA	2	3	4	V
$\Delta V_{GS(th)}/\Delta T_J$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25 °C		−9.8		mV/°C
$r_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10 V, I_D = 4.5 A		36	47	mΩ
		V_{GS} = 6 V, I_D = 4.5 A		39	53	
		V_{GS} = 10 V, I_D = 4.5 A, T_J = 125 °C		69	103	
g_{FS}	Forward Transconductance	V_{DS} = 10 V, I_D = 4.5 A		14		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 75 V, V_{GS} = 0 V, f = 1 MHz		1960	2610	pF
C_{oss}	Output Capacitance			130	175	pF
C_{rss}	Reverse Transfer Capacitance			30	45	pF
R_g	Gate Resistance	f = 1 MHz	0.1	1.3	2.6	Ω
SWITCHING CHARACTERISTICS						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 75 V, I_D = 1.0 A, V_{GS} = 10 V, R_{GEN} = 6 Ω		11	20	ns
t_r	Rise Time			8	16	ns
$t_{d(off)}$	Turn-Off Delay Time			38	61	ns
t_f	Fall Time			31	50	ns
$Q_{g(TOT)}$	Total Gate Charge at 10 V	V_{GS} = 0 V to 10 V, V_{DD} = 75 V, I_D = 4.5 A		31	43	nC
Q_{gs}	Gate to Source Gate Charge	V_{DD} = 75 V, I_D = 4.5 A		9		nC
Q_{gd}	Gate to Drain “Miller” Charge			7		nC
DRAIN−SOURCE DIODE CHARACTERISTICS						
V_{SD}	Source to Drain Diode Forward Voltage	.V_{GS} = 0 V, I_S = 2.2 A (Note 2)		0.7	1.0	V
t_{rr}	Reverse Recovery Time	I_F = 4.5 A, di/dt = 100 A/μs		67	101	ns
Q_{rr}	Reverse Recovery Charge			130	195	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTES:

1. $R_{\theta JA}$ is determined with the device mounted on a 1 in^2 pad 2 oz copper pad on a 1.5 × 1.5 in. board of FR−4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user’s board design.



a) 50°C/W when mounted on a 1 in^2 pad of 2 oz copper.

b) 125°C/W when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.
3. E_{AS} of 150 mJ is based on starting T_J = 25°C, L = 3 mH, I_{AS} = 10 A, V_{DD} = 150 V. V_{GS} = 10 V.

ORDERING INFORMATION AND PACKAGE MARKING

Device	Device Marking	Package	Shipping†
FDMS2572	FDMS2572	WDFN8 5x6, 1.27P (Pb−Free)	3000 Units / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

TYPICAL CHARACTERISTICS

(T_J = 25°C unless otherwise noted)

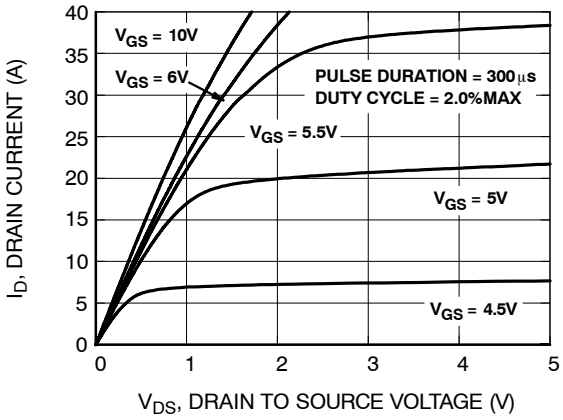


Figure 1. On−Region Characteristics

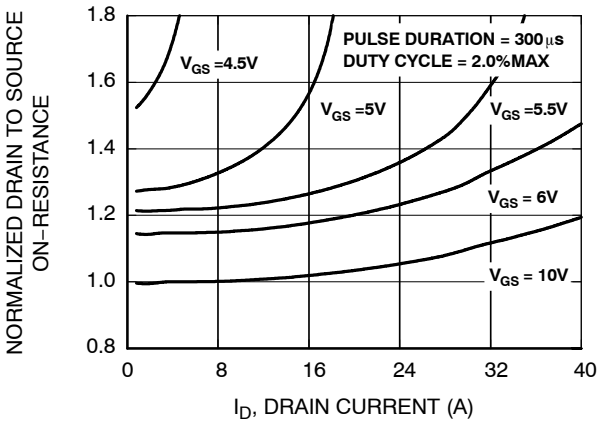


Figure 2. Normalized On−Resistance vs. Drain Current and Gate Voltage

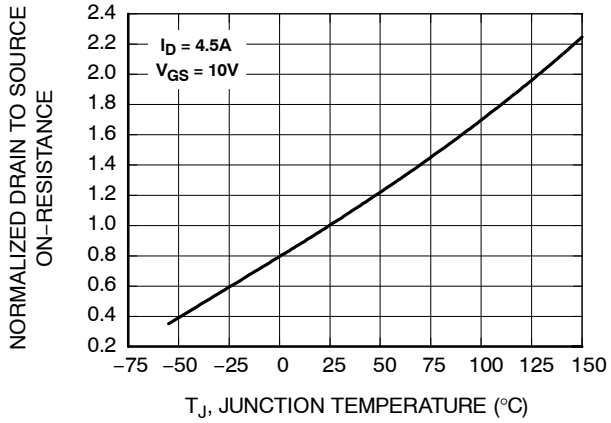


Figure 3. Normalized On−Resistance vs. Junction Temperature

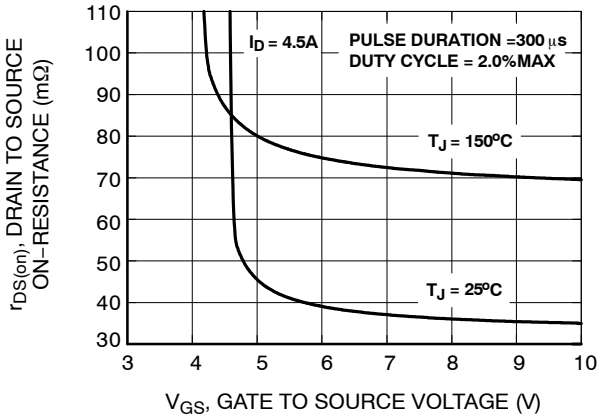


Figure 4. On−Resistance vs. Gate to Source Voltage

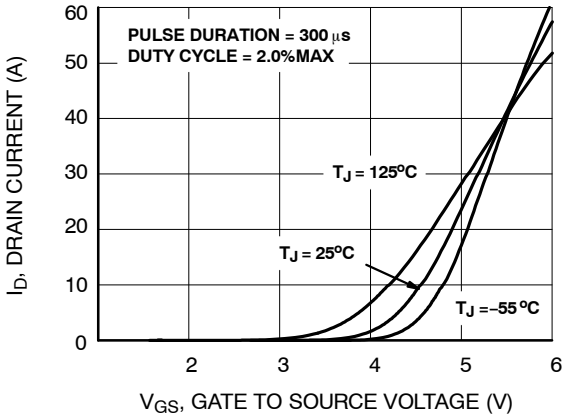


Figure 5. Transfer Characteristics

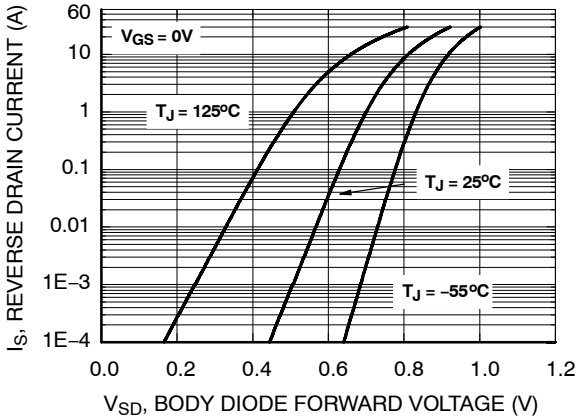


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

TYPICAL CHARACTERISTICS (continued)

(T_J = 25°C unless otherwise noted)

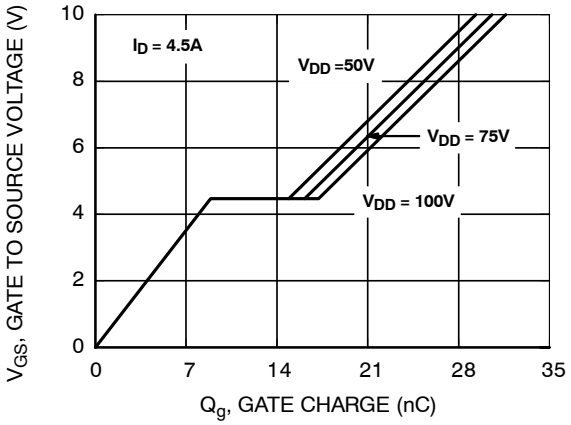


Figure 7. Gate Charge Characteristics

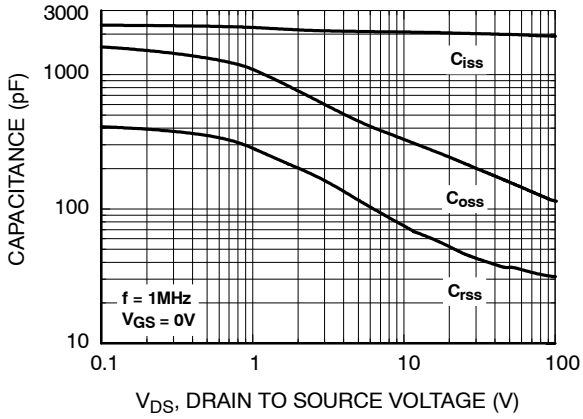


Figure 8. Capacitance vs. Drain to Source Voltage

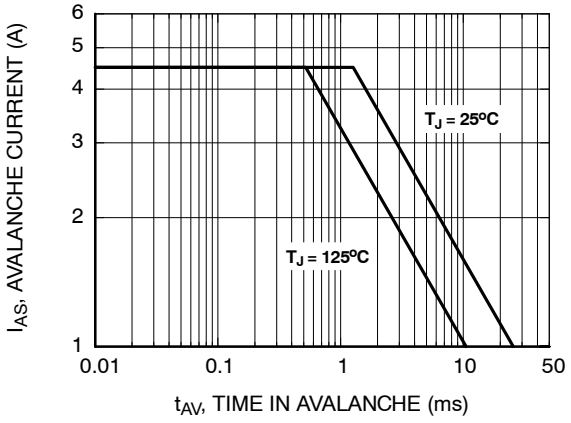


Figure 9. Unclamped Inductive Switching Capability

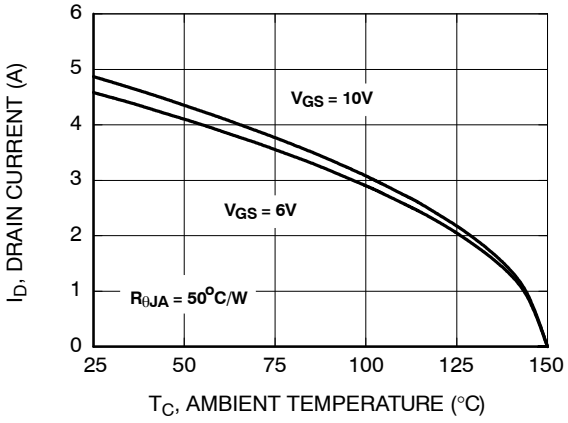


Figure 10. Maximum Continuous Drain Current vs. Ambient Temperature

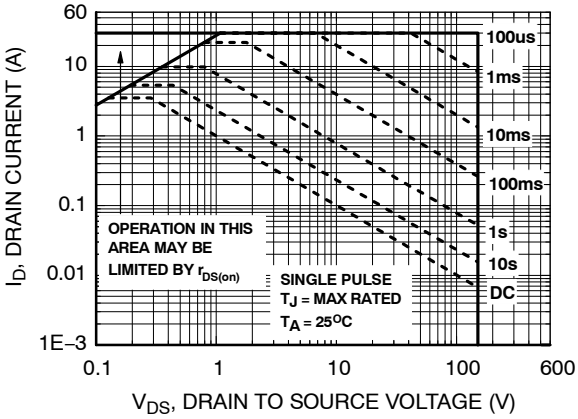


Figure 11. Forward Bias Safe Operating Area

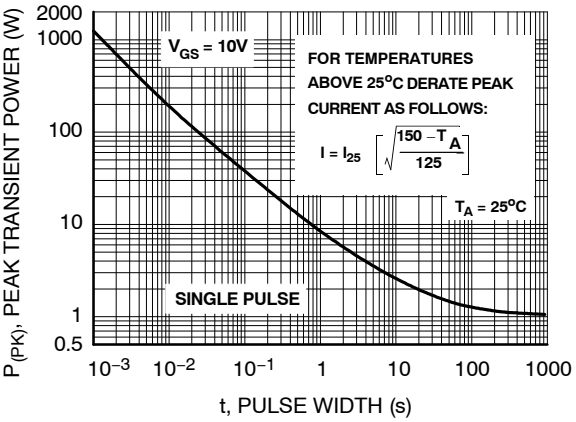


Figure 12. Single Pulse Maximum Power Dissipation

TYPICAL CHARACTERISTICS (continued)

(T_J = 25°C unless otherwise noted)

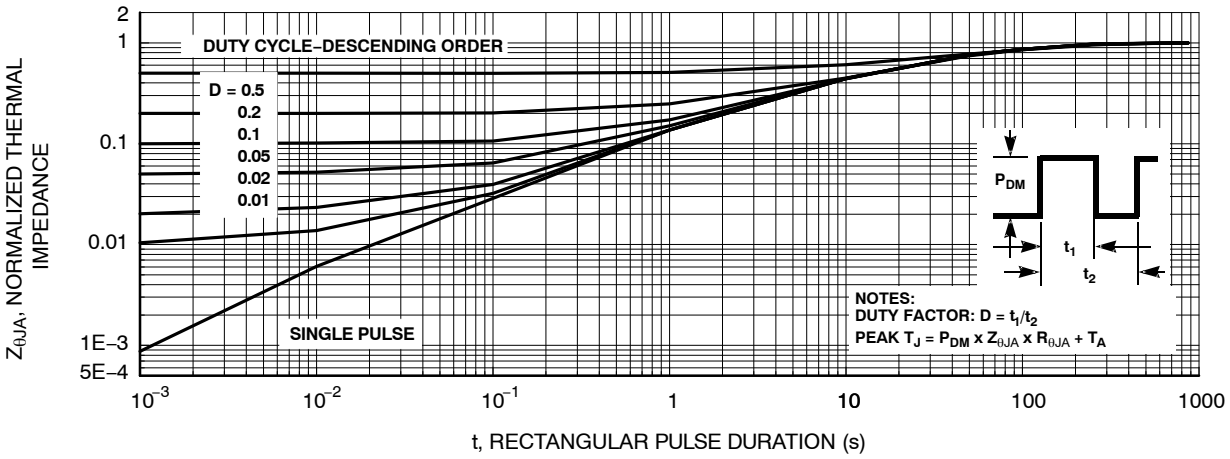
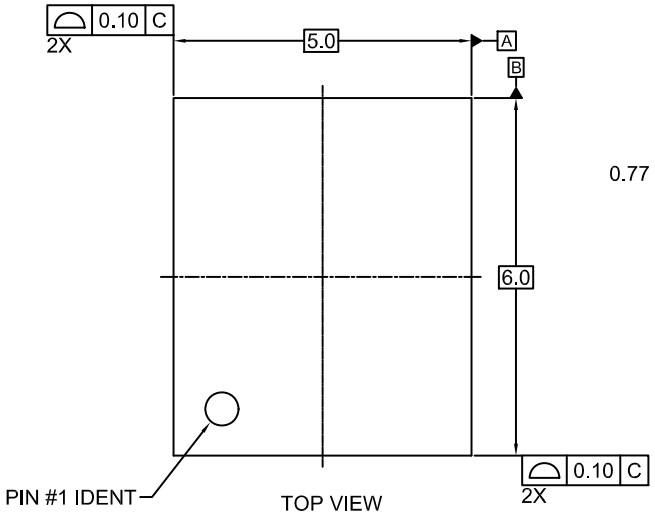
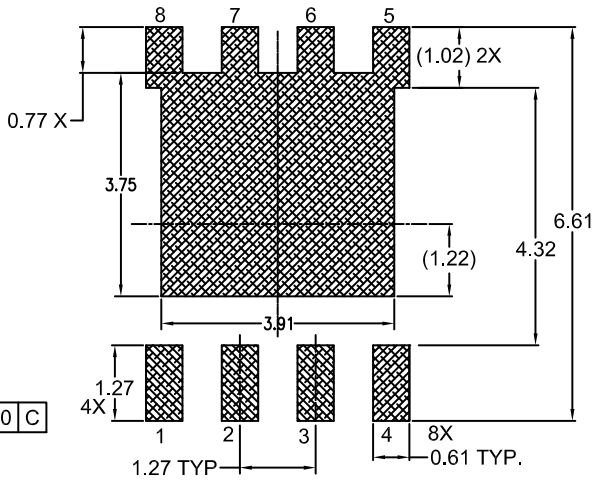


Figure 13. Transient Thermal Response Curve

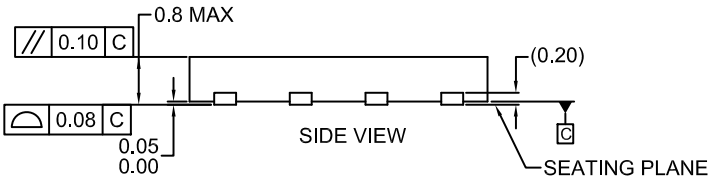
WDFN8 5x6, 1.27P
CASE 506DP
ISSUE O

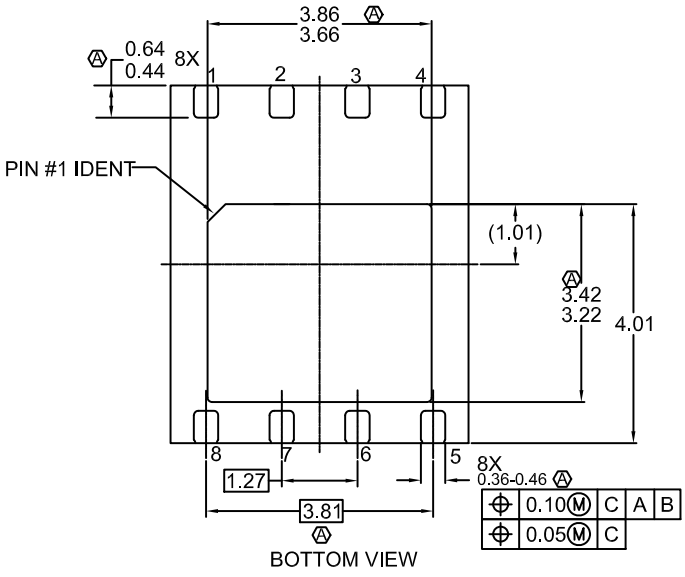
DATE 31 AUG 2016





RECOMMENDED LAND PATTERN





NOTES:

A. DOES NOT FULLY CONFORM TO JEDEC REGISTRATION, MO-229.
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994
D. TERMINALS 5,6,7 AND 8 ARE TIED TO THE EXPOSED PADDLE

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