

MOSFET – N-Channel, POWERTRENCH[®], SyncFET[™]

30 V, 22 A, 5.0 mΩ

FDMS0312AS

General Description

The FDMS0312AS has been designed to minimize losses in power conversion application. Advancements in both silicon and package technologies have been combined to offer the lowest $R_{DS(on)}$ while maintaining excellent switching performance. This device has the added benefit of an efficient monolithic Schottky body diode.

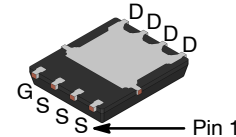
Features

- Max $R_{DS(on)}$ = 5.0 mΩ at V_{GS} = 10 V, I_D = 18 A
- Max $R_{DS(on)}$ = 6.2 mΩ at V_{GS} = 4.5 V, I_D = 16 A
- Advanced Package and Silicon Combination for Low $R_{DS(on)}$ and High Efficiency
- SyncFET Schottky Body Diode
- MSL1 Robust Package Design
- 100% UIL Tested
- This Device is Pb-Free, Halide Free and is RoHS Compliant

Applications

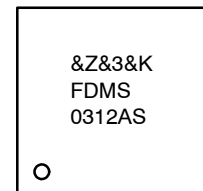
- Synchronous Rectifier for DC–DC Converters
- Notebook Vcore/GPU Low Side Switch
- Networking Point of Load Low Side Switch
- Telecom Secondary Side Rectification

V_{DS}	$R_{DS(on)}$ MAX	I_D MAX
30 V	5.0 mΩ @ 10 V	22 A
	6.2 mΩ @ 4.5 V	



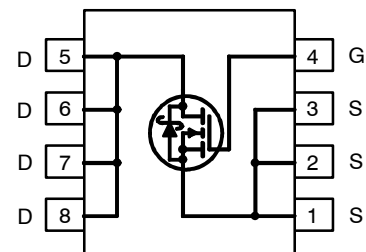
PQFN8 5 × 6, 1.27P
(Power 56)
CASE 483AE

MARKING DIAGRAM



&Z = Assembly Plant Code
&3 = 3-Digit Date Code
&K = 2-Digit Lot Run Traceability Code
FDMS0312AS = Specific Device Code

PIN CONNECTIONS



ORDERING INFORMATION

Device	Package	Shipping [†]
FDMS0312AS	PQFN8 (Pb-Free, Halide Free)	3000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, [BRD8011/D](#).

FDMS0312AS

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Symbol	Parameter			Value	Unit
V _{DS}	Drain to Source Voltage			30	V
V _{GS}	Gate to Source Voltage (Note 4)			±20	V
I _D	Drain Current	Continuous (Package limited)	T _C = 25°C	22	A
		Continuous (Silicon limited)	T _C = 25°C	70	
		Continuous (Note 1a)	T _A = 25°C	18	
		Pulsed		100	
E _{AS}	Single Pulse Avalanche Energy (Note 3)			33	mJ
P _D	Power Dissipation		T _C = 25°C	36	W
			T _A = 25°C (Note 1a)	2.5	
T _J , T _{STG}	Operating and Storage Junction Temperature Range			–55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
R _{θJC}	Thermal Resistance, Junction to Case	3.4	°C/W
R _{θJA}	Thermal Resistance, Junction to Ambient (Note 1a)	50	

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 1\text{ mA}$, $V_{GS} = 0\text{ V}$	30	–	–	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 10\text{ mA}$, referenced to 25°C	–	18	–	$\text{mV}/^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 24\text{ V}$, $V_{GS} = 0\text{ V}$	–	–	500	μA
I_{GSS}	Gate to Source Leakage Current, Forward	$V_{GS} = 20\text{ V}$, $V_{DS} = 0\text{ V}$	–	–	100	nA

ON CHARACTERISTICS

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 1\text{ mA}$	1.2	1.5	3.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 10\text{ mA}$, referenced to 25°C	–	–4	–	$\text{mV}/^\circ\text{C}$
$R_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{ V}$, $I_D = 18\text{ A}$	–	4.2	5.0	$\text{m}\Omega$
		$V_{GS} = 4.5\text{ V}$, $I_D = 16\text{ A}$	–	5.4	6.2	
		$V_{GS} = 10\text{ V}$, $I_D = 18\text{ A}$, $T_J = 125^\circ\text{C}$	–	5.3	6.8	
g_{FS}	Forward Transconductance	$V_{DS} = 5\text{ V}$, $I_D = 18\text{ A}$	–	92	–	S

DYNAMIC CHARACTERISTICS

C_{iss}	Input Capacitance	$V_{DS} = 15\text{ V}$, $V_{GS} = 0\text{ V}$, $f = 1\text{ MHz}$	–	1365	1815	pF
C_{oss}	Output Capacitance		–	550	730	pF
C_{rss}	Reverse Transfer Capacitance		–	70	105	pF
R_g	Gate Resistance		–	0.5	2.5	Ω

SWITCHING CHARACTERISTICS

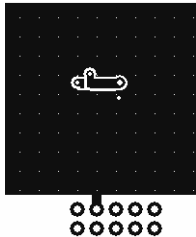
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 15\text{ V}$, $I_D = 18\text{ A}$, $V_{GS} = 10\text{ V}$, $R_{GEN} = 6\text{ }\Omega$	–	10	19	ns
t_r	Rise Time		–	2.3	10	ns
$t_{d(off)}$	Turn-Off Delay Time		–	25	40	ns
t_f	Fall Time		–	6	12	ns
Q_g	Total Gate Charge	$V_{GS} = 0\text{ V}$ to 10 V , $V_{DD} = 15\text{ V}$, $I_D = 18\text{ A}$	–	23	31	nC
		$V_{GS} = 0\text{ V}$ to 4.5 V , $V_{DD} = 15\text{ V}$, $I_D = 18\text{ A}$	–	11	16	nC
Q_{gs}	Gate to Source Charge	$V_{DD} = 15\text{ V}$, $I_D = 18\text{ A}$	–	3.3	–	nC
Q_{gd}	Gate to Drain “Miller” Charge	$V_{DD} = 15\text{ V}$, $I_D = 18\text{ A}$	–	3.7	–	nC

DRAIN-SOURCE DIODE CHARACTERISTICS

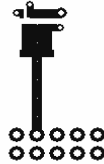
V_{SD}	Source–Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}$, $I_S = 2\text{ A}$ (Note 2)	–	0.63	0.8	V
		$V_{GS} = 0\text{ V}$, $I_S = 18\text{ A}$ (Note 2)	–	0.8	1.2	
t_{rr}	Reverse Recovery Time	$I_F = 18\text{ A}$, $di/dt = 300\text{ A}/\mu\text{s}$	–	23	36	ns
Q_{rr}	Reverse Recovery Charge		–	20	32	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

- $R_{\theta JA}$ is determined with the device mounted on a 1 in^2 pad 2 oz copper pad on a $1.5 \times 1.5\text{ in.}$ board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



- a) $50^\circ\text{C}/\text{W}$ when mounted on a 1 in^2 pad of 2 oz copper.



- b) $125^\circ\text{C}/\text{W}$ when mounted on a minimum pad of 2 oz copper.

- Pulse Test: Pulse Width $< 300\text{ }\mu\text{s}$, Duty cycle $< 2.0\%$.
- E_{AS} of 33 mJ is based on starting $T_J = 25^\circ\text{C}$, $L = 0.3\text{ mH}$, $I_{AS} = 15\text{ A}$, $V_{DD} = 27\text{ V}$, $V_{GS} = 10\text{ V}$.
- As an N–ch device, the negative V_{GS} rating is for low duty cycle pulse occurrence only. No continuous rating is implied.

TYPICAL CHARACTERISTICS

($T_J = 25^\circ\text{C}$ unless otherwise noted)

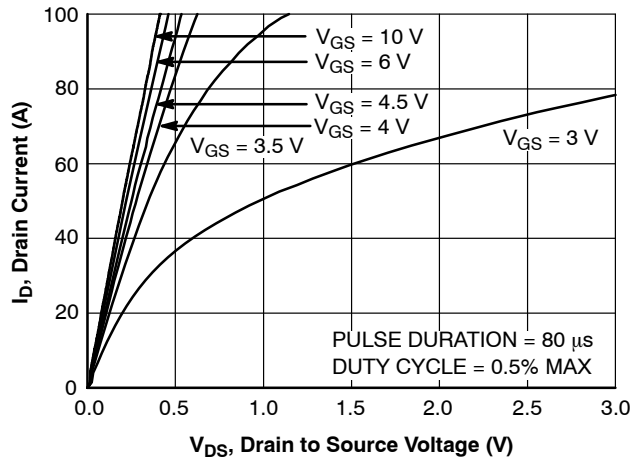


Figure 1. On Region Characteristics

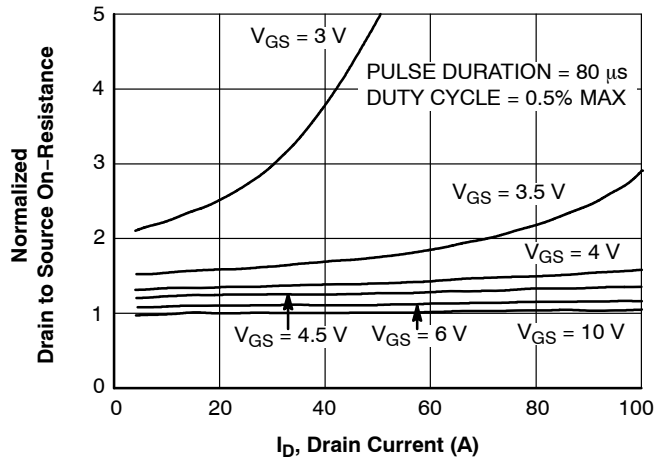


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

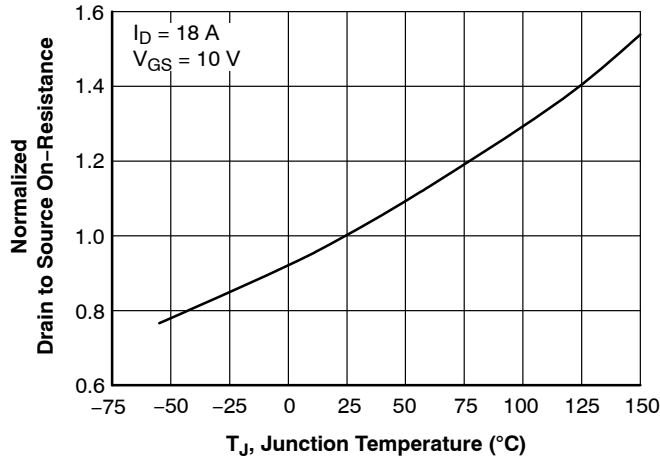


Figure 3. Normalized On Resistance vs. Junction Temperature

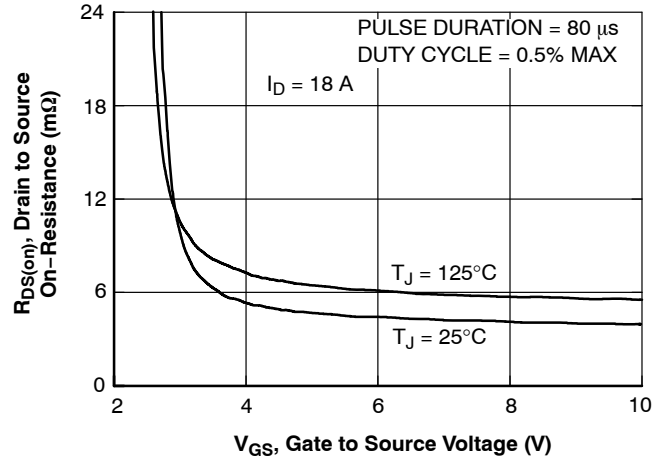


Figure 4. On-Resistance vs. Gate to Source Voltage

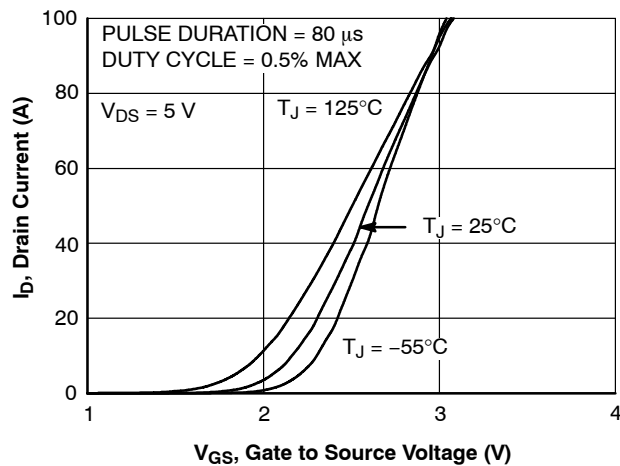


Figure 5. Transfer Characteristics

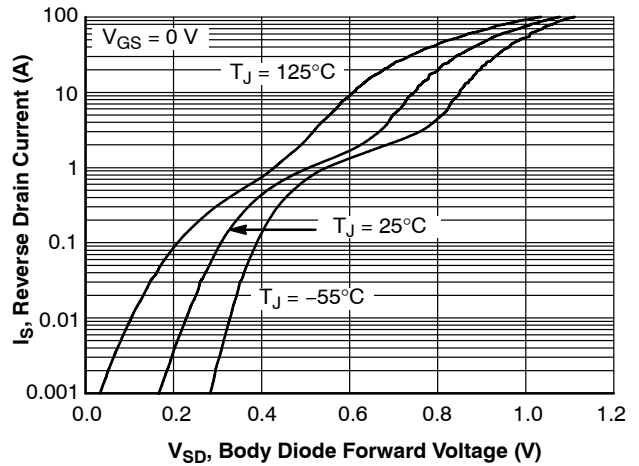


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

TYPICAL CHARACTERISTICS (continued)

($T_J = 25^\circ\text{C}$ unless otherwise noted)

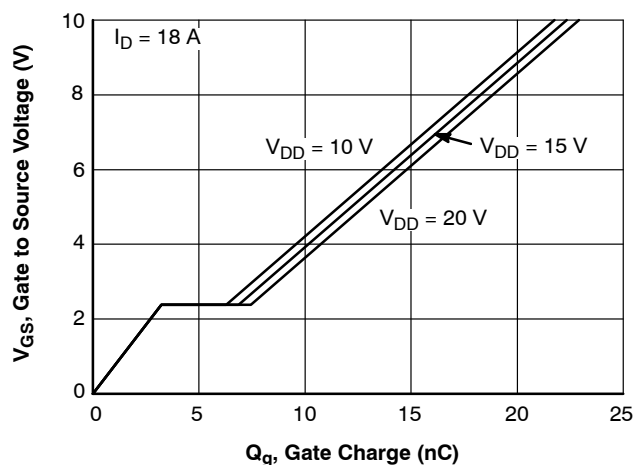


Figure 7. Gate Charge Characteristics

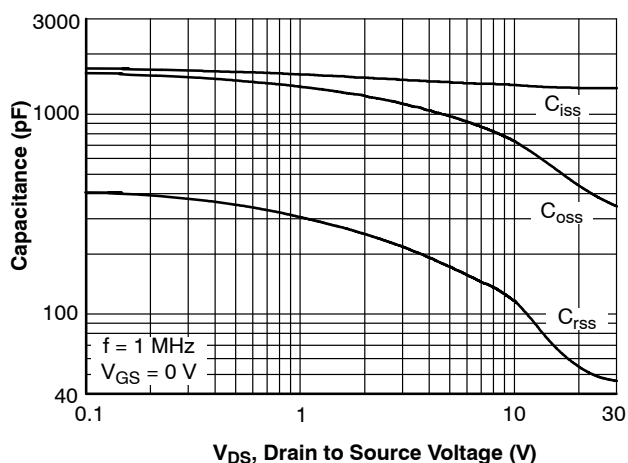


Figure 8. Capacitance vs. Drain to Source Voltage

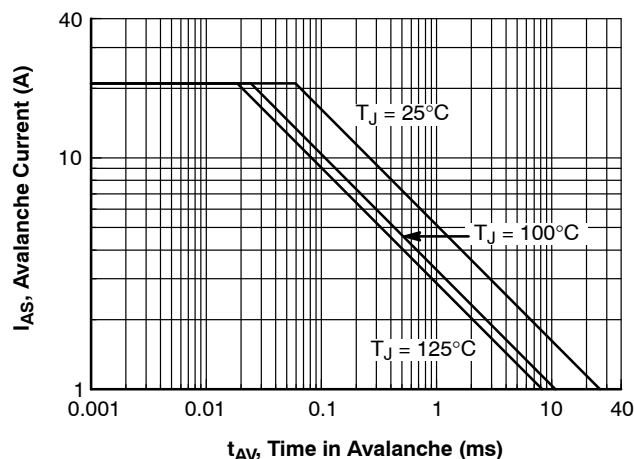


Figure 9. Unclamped Inductive Switching Capability

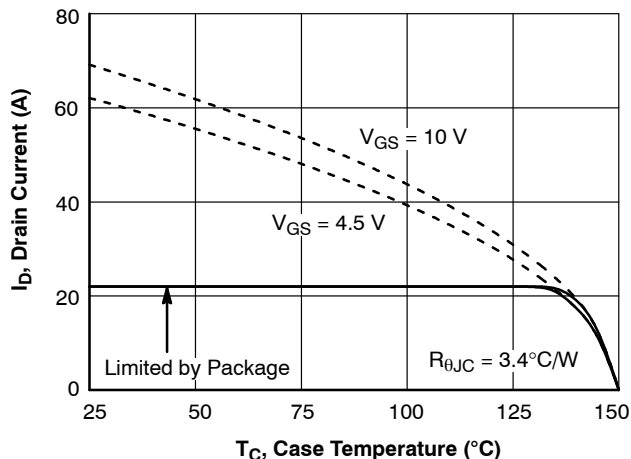


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

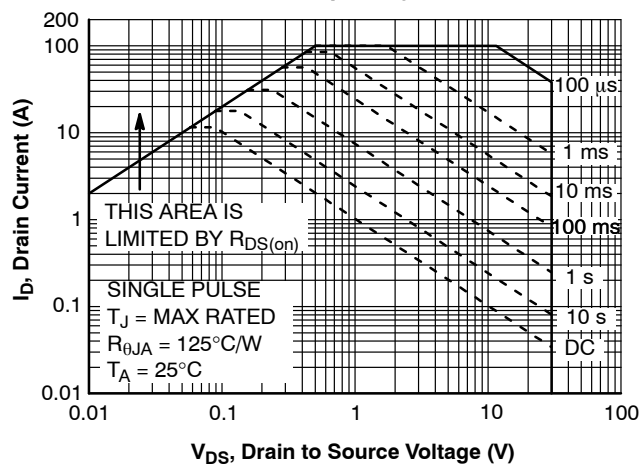


Figure 11. Forward Bias Safe Operating Area

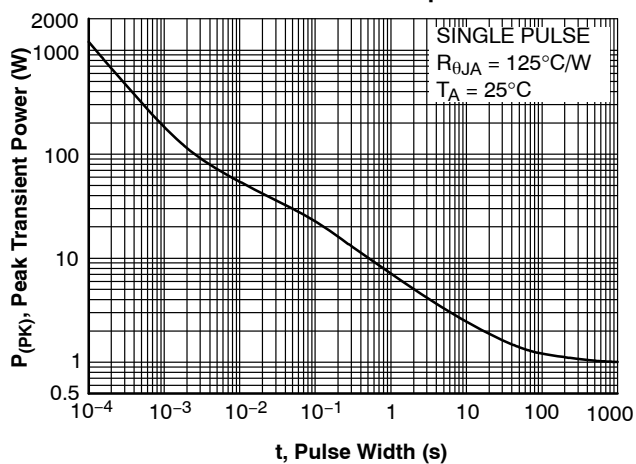


Figure 12. Single Pulse Maximum Power Dissipation

TYPICAL CHARACTERISTICS (continued)

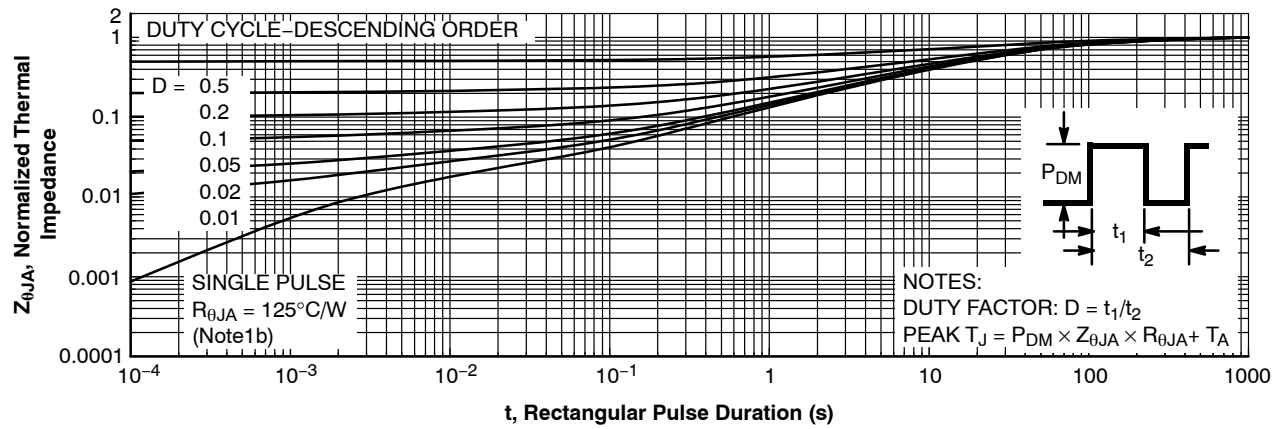
(T_J = 25°C unless otherwise noted)

Figure 13. Junction-to-Ambient Transient Thermal Response Curve

TYPICAL CHARACTERISTICS (continued)

SyncFET Schottky Body Diode Characteristics

onsemi's SyncFET process embeds a Schottky diode in parallel with POWERTRENCH MOSFET. This diode exhibits similar characteristics to a discrete external Schottky diode in parallel with a MOSFET. Figure 14 shows the reverse recovery characteristic of the FDMS0312AS.

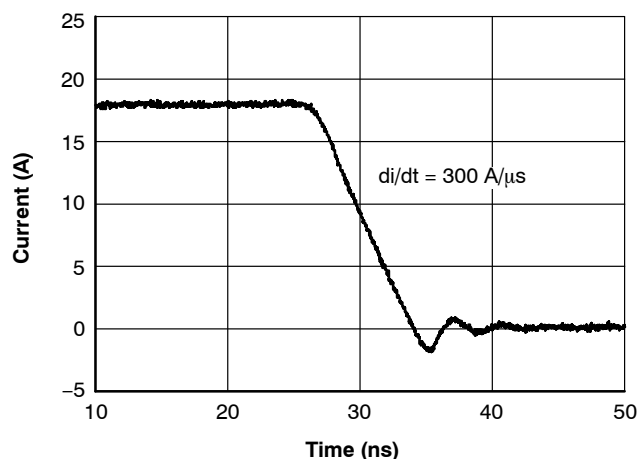


Figure 14. FDMS0312AS SyncFET Body Diode Reverse Recovery Characteristic

Schottky barrier diodes exhibit significant leakage at high temperature and high reverse voltage. This will increase the power in the device.

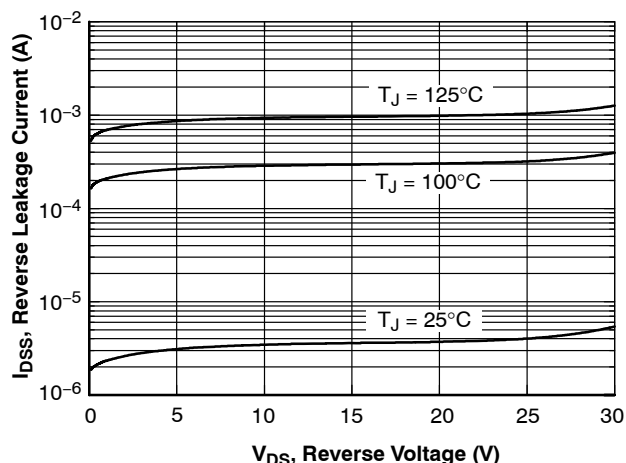
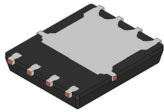


Figure 15. SyncFET Body Diode Reverse Leakage vs. Drain-Source Voltage

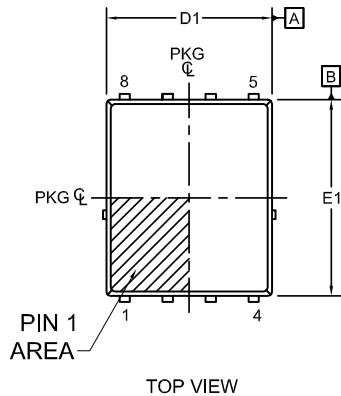
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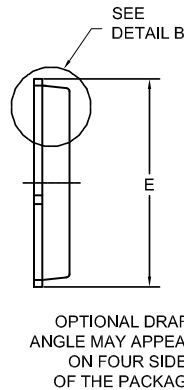


PQFN8 5X6, 1.27P
CASE 483AE
ISSUE C

DATE 21 JAN 2022

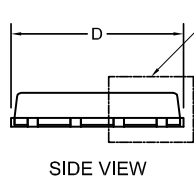


TOP VIEW

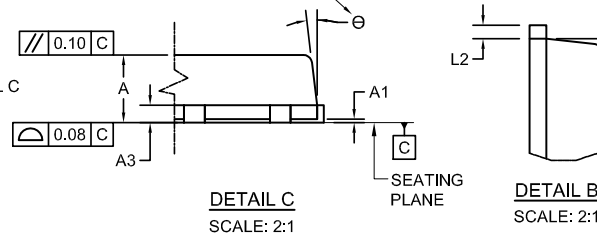


NOTES:

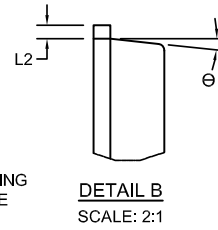
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
5. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
6. IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.



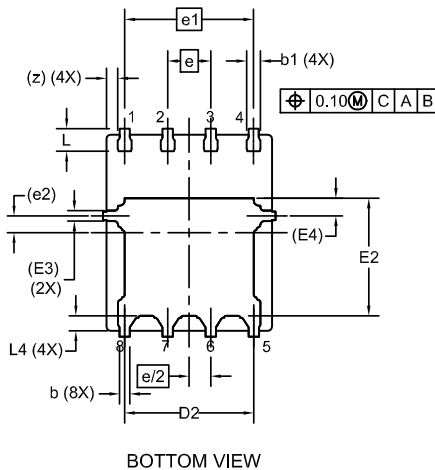
SIDE VIEW



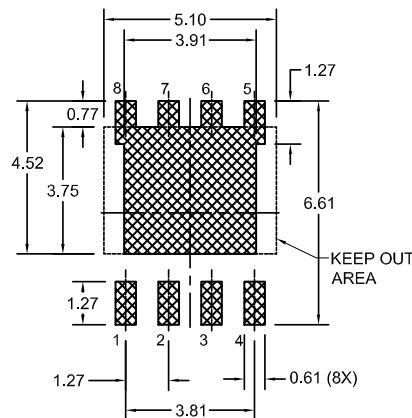
DETAIL C
SCALE: 2:1



DETAIL B
SCALE: 2:1



BOTTOM VIEW



LAND PATTERN
RECOMMENDATION

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERM/D.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
A1	0.00	-	0.05
b	0.21	0.31	0.41
b1	0.31	0.41	0.51
A3	0.15	0.25	0.35
D	4.90	5.00	5.20
D1	4.80	4.90	5.00
D2	3.61	3.82	3.96
E	5.90	6.15	6.25
E1	5.70	5.80	5.90
E2	3.38	3.48	3.78
E3	0.30 REF		
E4	0.52 REF		
e	1.27 BSC		
e/2	0.635 BSC		
e1	3.81 BSC		
e2	0.50 REF		
L	0.51	0.66	0.76
L2	0.05	0.18	0.30
L4	0.34	0.44	0.54
z	0.34 REF		
Θ	0°	-	12°

DOCUMENT NUMBER: 98AON13655G

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DESCRIPTION: PQFN8 5X6, 1.27P

PAGE 1 OF 1

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