

MOSFET – Power, N-Channel, SUPERFET® III, Easy-Drive

650 V, 24 A, 125 mΩ

FCMT125N65S3

General Description

SUPERFET III MOSFET is onsemi's brand-new high voltage super-junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low on-resistance and lower gate charge performance. This advanced technology is tailored to minimize conduction loss, provide superior switching performance, and withstand extreme dv/dt rate.

Consequently, SUPERFET III MOSFET Easy-drive series helps manage EMI issues and allows for easier design implementation.

The Power88 package is an ultra-slim surface-mount package (1 mm high) with a low profile and small footprint (8 × 8 mm²). SUPERFET III MOSFET in a Power88 package offers excellent switching performance due to lower parasitic source inductance and separated power and drive sources. Power88 offers Moisture Sensitivity Level 1 (MSL 1).

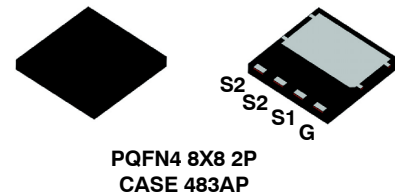
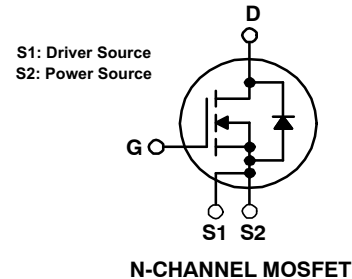
Features

- 700 V @ T_J = 150°C
- Typ R_{DS(on)} = 100 mΩ
- Ultra Low Gate Charge (Typ. Q_g = 49 nC)
- Low Effective Output Capacitance (Typ. C_{oss(eff.)} = 406 pF)
- 100% Avalanche Tested
- These Devices are Pb-Free and are RoHS Compliant

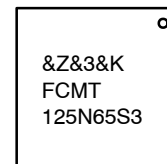
Applications

- Telecom / Server Power Supplies
- Industrial Power Supplies
- UPS / Solar

V _{DSS}	R _{DS(ON)} MAX	I _D MAX
650 V	125 mΩ @ 10 V	24 A



MARKING DIAGRAM



&Z	= Assembly Plant Code
&3	= Data Code (Year & Week)
&K	= Lot
FCMT125N65S3	= Specific Device Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

FCMT125N65S3

ABSOLUTE MAXIMUM RATINGS ($T_C = 25^\circ\text{C}$, Unless otherwise noted)

Symbol	Parameter		Value	Unit
V_{DSS}	Drain to Source Voltage		650	V
V_{GSS}	Gate to Source Voltage	DC	± 30	V
		AC ($f > 1\text{ Hz}$)	± 30	V
I_D	Drain Current	Continuous ($T_C = 25^\circ\text{C}$)	24	A
		Continuous ($T_C = 100^\circ\text{C}$)	15	
I_{DM}	Drain Current	Pulsed (Note 1)	60	A
E_{AS}	Single Pulsed Avalanche Energy (Note 2)		115	mJ
I_{AS}	Avalanche Current (Note 2)		3.7	A
E_{AR}	Repetitive Avalanche Energy (Note 1)		1.81	mJ
dv/dt	MOSFET dv/dt		100	V/ns
	Peak Diode Recovery dv/dt (Note 3)		20	
P_D	Power Dissipation	($T_C = 25^\circ\text{C}$)	181	W
		Derate Above 25°C	1.45	W/ $^\circ\text{C}$
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +150	$^\circ\text{C}$
T_L	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 s		300	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Repetitive rating: pulse-width limited by maximum junction temperature.

2. $I_{AS} = 3.7\text{ A}$, $R_G = 25\ \Omega$ starting $T_J = 25^\circ\text{C}$

3. $I_{SD} \leq 12\text{ A}$, $di/dt \leq 200\text{ A}/\mu\text{s}$, $V_{DD} \leq 400\text{ V}$, starting $T_J = 25^\circ\text{C}$

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	0.69	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max. (Note 4)	45	

4. Device on 1 in² pad 2 oz copper pad on 1.5 × 1.5 in. board of FR-4 material.

ORDERING INFORMATION

Device	Marking	Package	Reel Size	Tape Width	Quantity [†]
FCMT125N65S3	FCMT125N65S3	PQFN8	13"	13.3 mm	3000 Units

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

FCMT125N65S3

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

BV _{DSS}	Drain to Source Breakdown Voltage	V _{GS} = 0 V, I _D = 1 mA, T _J = 25°C	650			V
		V _{GS} = 0 V, I _D = 1 mA, T _J = 150°C	700			V
ΔBV _{DSS} /ΔT _J	Breakdown Voltage Temperature Coefficient	I _D = 1 mA, Referenced to 25°C		0.68		V/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 650 V, V _{GS} = 0 V			10	μA
		V _{DS} = 520 V, T _C = 125°C		1.35		
I _{GSS}	Gate to Body Leakage Current	V _{GS} = ±30 V, V _{DS} = 0 V			±100	nA

ON CHARACTERISTICS

V _{GS(th)}	Gate Threshold Voltage	V _{GS} = V _{DS} , I _D = 0.59 mA	2.5		4.5	V
R _{DS(on)}	Static Drain to Source On Resistance	V _{GS} = 10 V, I _D = 12 A		100	125	mΩ
g _{FS}	Forward Transconductance	V _{DS} = 20 V, I _D = 12 A		16		S

DYNAMIC CHARACTERISTICS

C _{iss}	Input Capacitance	V _{DS} = 400 V, V _{GS} = 0 V, f = 1 MHz		1920		pF
C _{oss}	Output Capacitance			44		pF
C _{oss(eff.)}	Effective Output Capacitance	V _{DS} = 0 V to 400 V, V _{GS} = 0 V		406		pF
C _{oss(er.)}	Energy Related Output Capacitance	V _{DS} = 0 V to 400 V, V _{GS} = 0 V		63		pF
Q _{g(tot)}	Total Gate Charge at 10V	V _{DS} = 400 V, I _D = 12 A, V _{GS} = 10 V (Note 5)		49		nC
Q _{gs}	Gate to Source Gate Charge			12		nC
Q _{gd}	Gate to Drain "Miller" Charge			22		nC
ESR	Equivalent Series Resistance	f = 1 MHz		0.5		Ω

SWITCHING CHARACTERISTICS

t _{d(on)}	Turn-On Delay Time	V _{DD} = 400 V, I _D = 12 A, V _{GS} = 10 V, R _g = 4.7 Ω (Note 5)		22		ns
t _r	Turn-On Rise Time			22		ns
t _{d(off)}	Turn-Off Delay Time			60		ns
t _f	Turn-Off Fall Time			5.8		ns

SOURCE-DRAIN DIODE CHARACTERISTICS

I _S	Maximum Continuous Source to Drain Diode Forward Current			24	A
I _{SM}	Maximum Pulsed Source to Drain Diode Forward Current			60	A
V _{SD}	Source to Drain Diode Forward Voltage	V _{GS} = 0 V, I _{SD} = 12 A		1.2	V
t _{rr}	Reverse Recovery Time	V _{DD} = 400 V, I _{SD} = 12 A, dI _F /dt = 100 A/μs		345	ns
Q _{rr}	Reverse Recovery Charge			5.7	μC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. Essentially independent of operating temperature typical characteristics.

TYPICAL PERFORMANCE CHARACTERISTICS

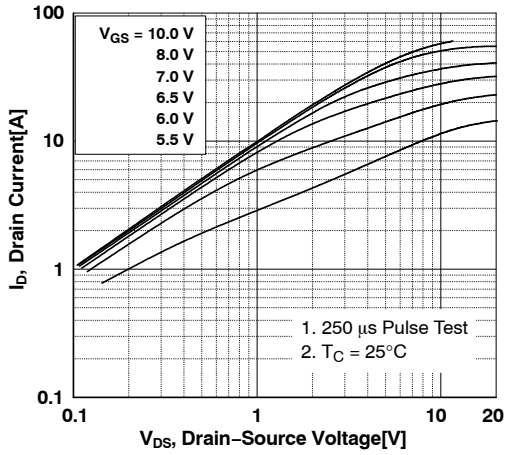


Figure 1. On-Region Characteristics

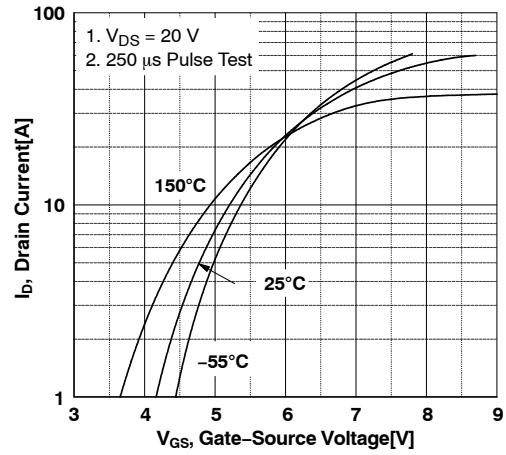


Figure 2. Transfer Characteristics

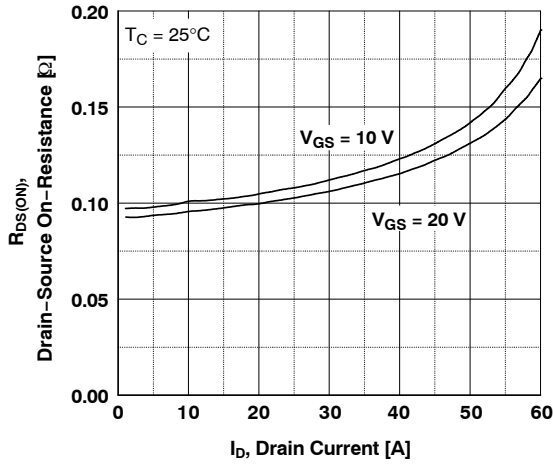


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

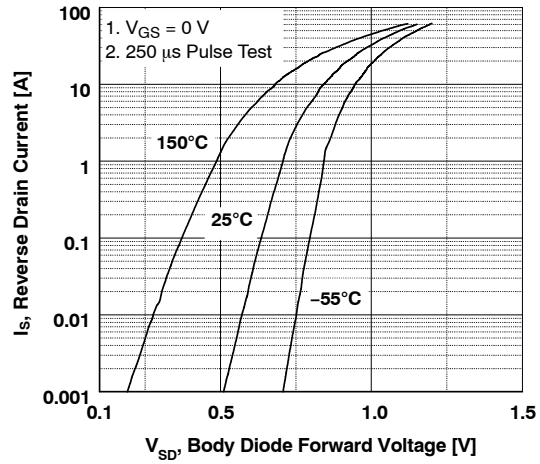


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

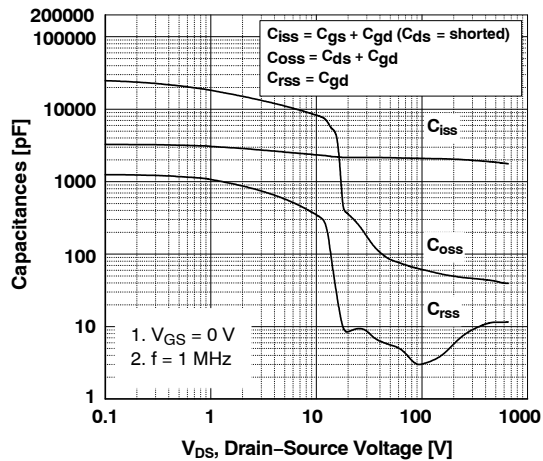


Figure 5. Capacitance Characteristics

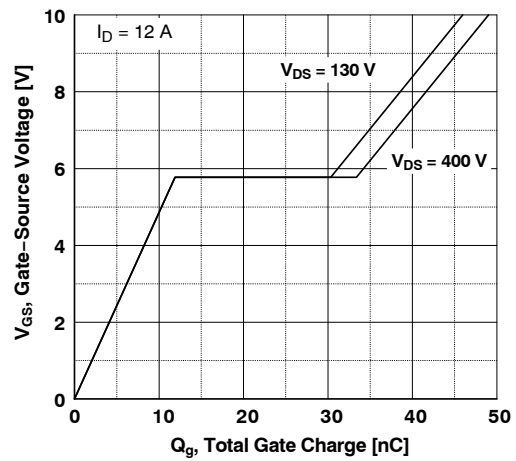


Figure 6. Gate Charge Characteristics

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

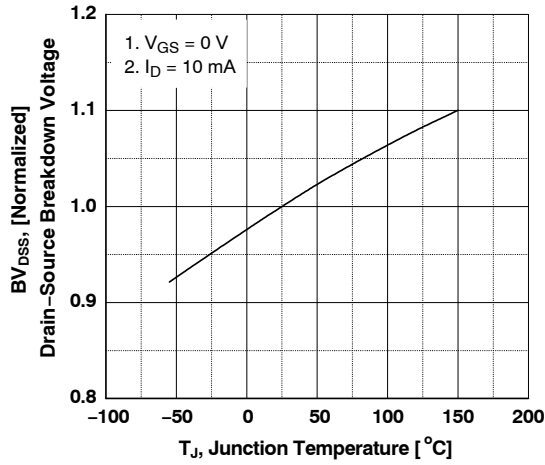


Figure 7. Breakdown Voltage Variation vs. Temperature

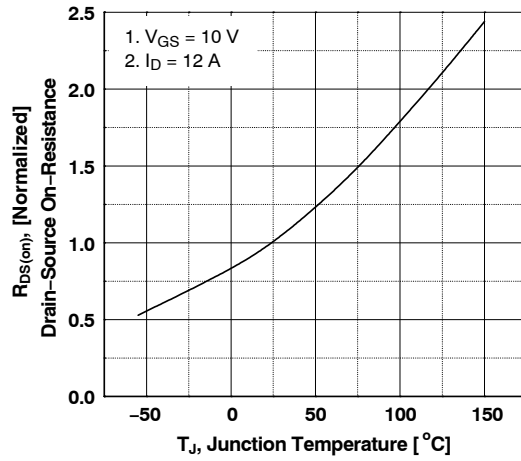


Figure 8. On-Resistance Variant vs. Temperature

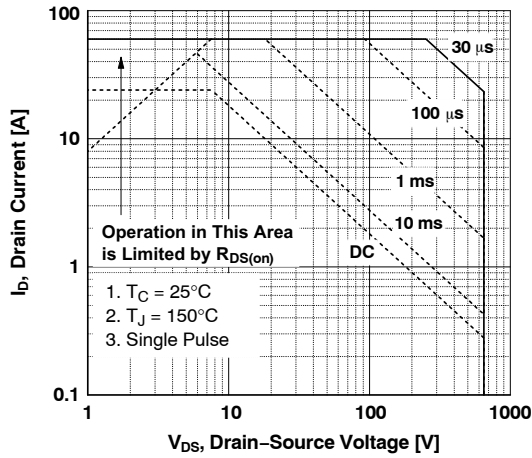


Figure 9. Maximum Safe Operation Area

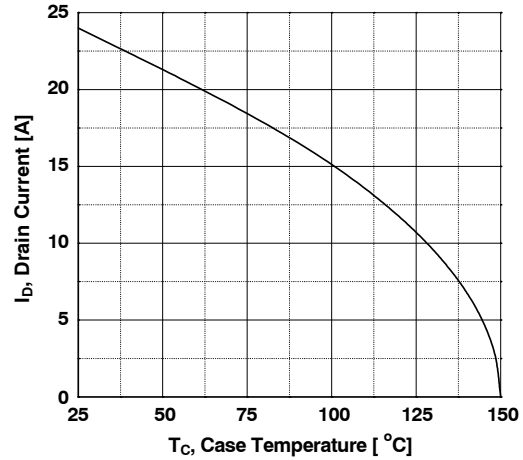


Figure 10. Maximum Drain Current vs. Case Temperature

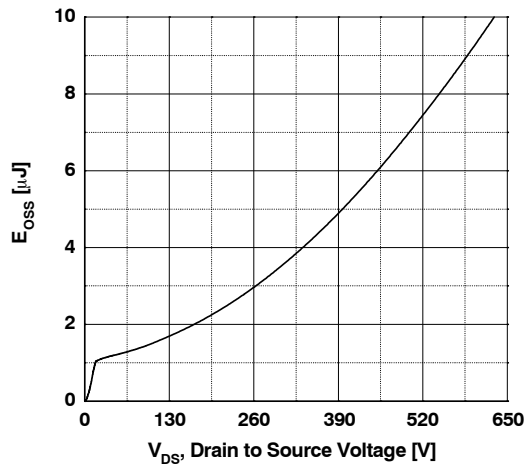


Figure 11. E_{OSS} vs. Drain to Source Voltage

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

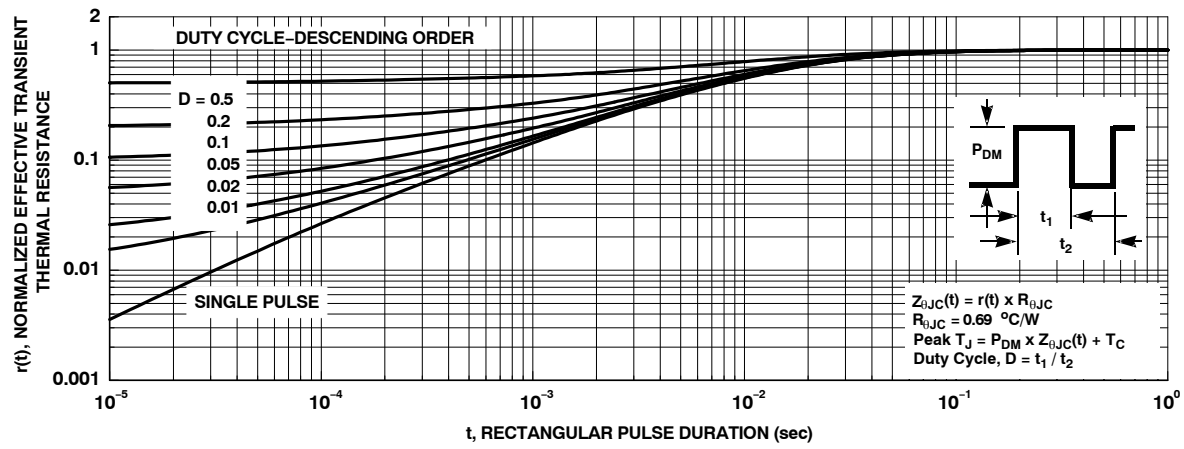


Figure 12. Transient Thermal Response Curve

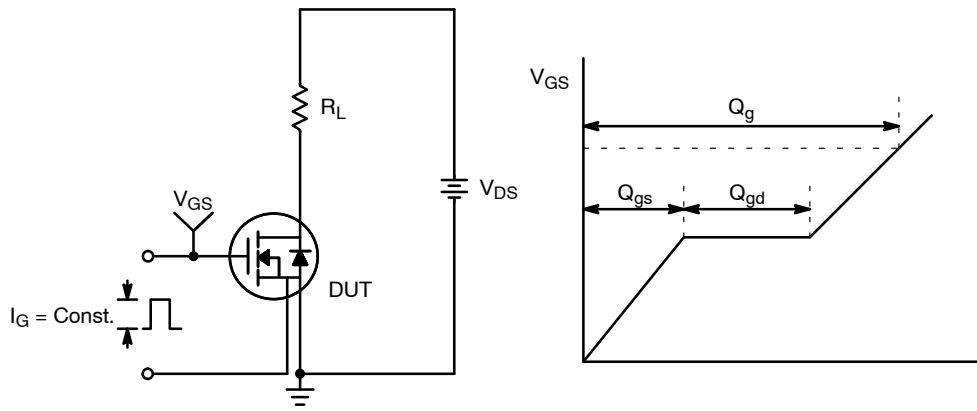


Figure 13. Gate Charge Test Circuit & Waveform

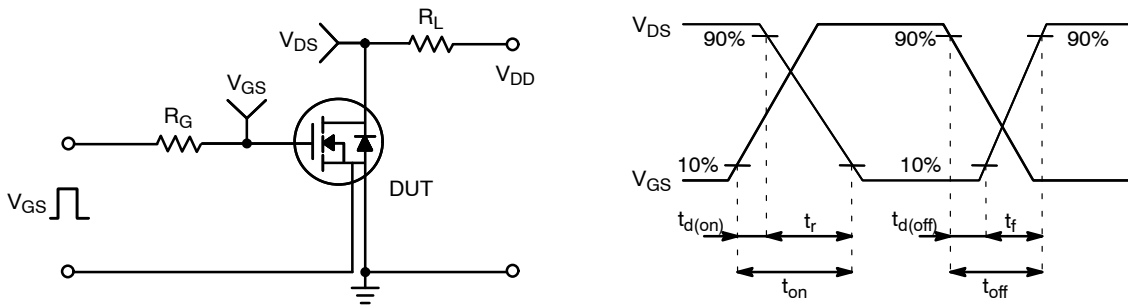


Figure 14. Resistive Switching Test Circuit & Waveforms

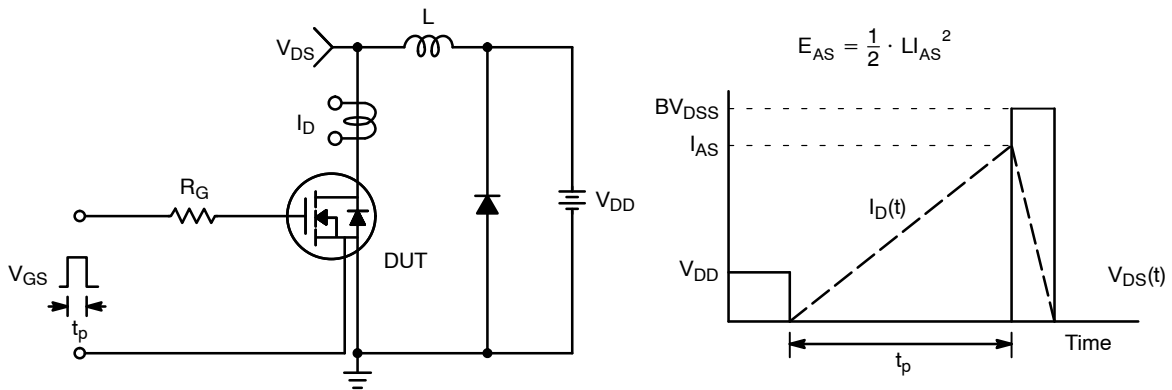


Figure 15. Unclamped Inductive Switching Test Circuit & Waveforms

FCMT125N65S3

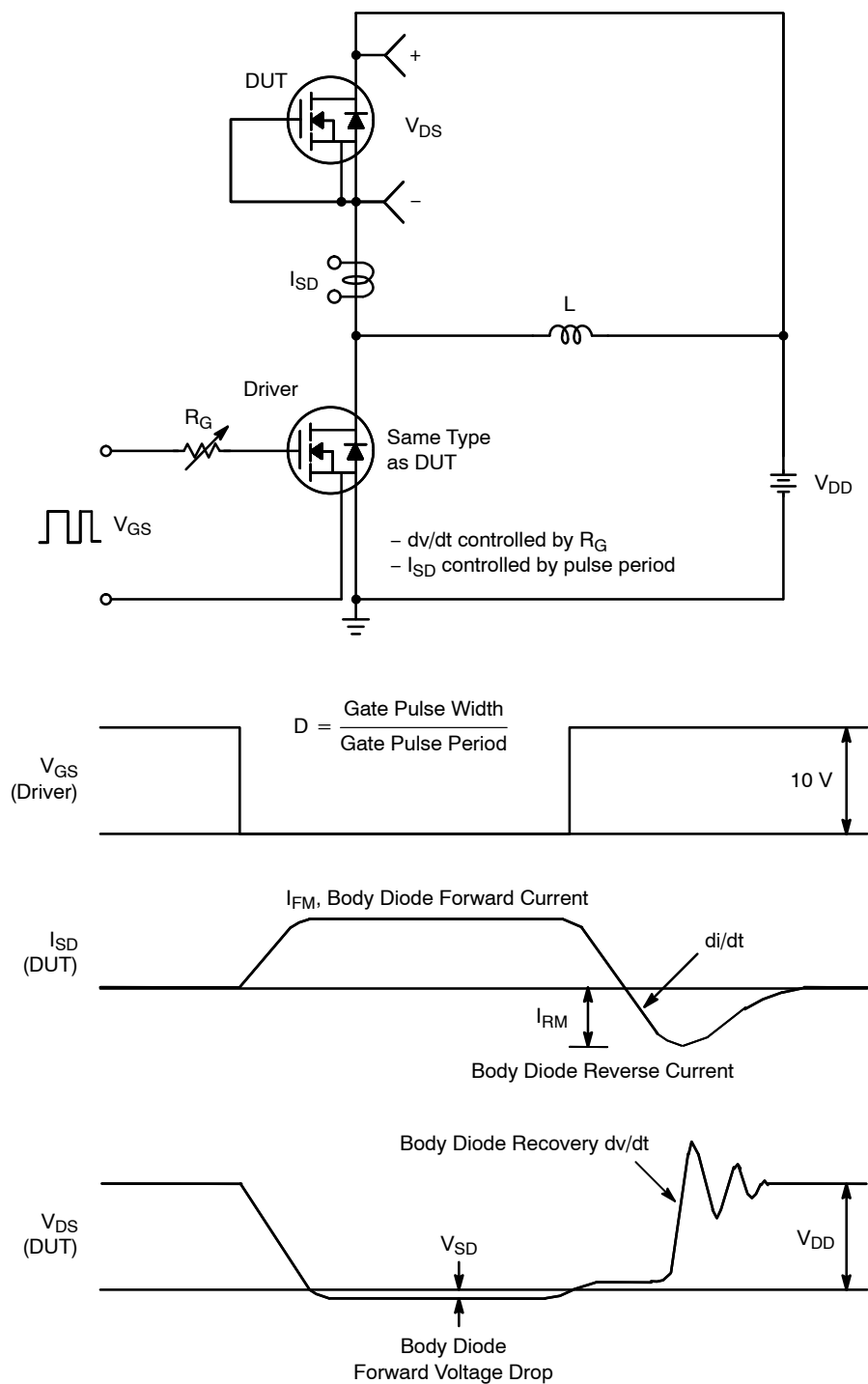
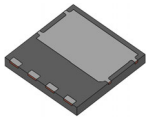
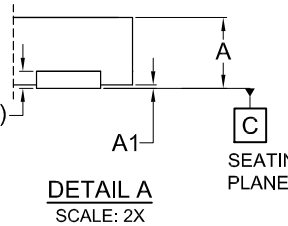
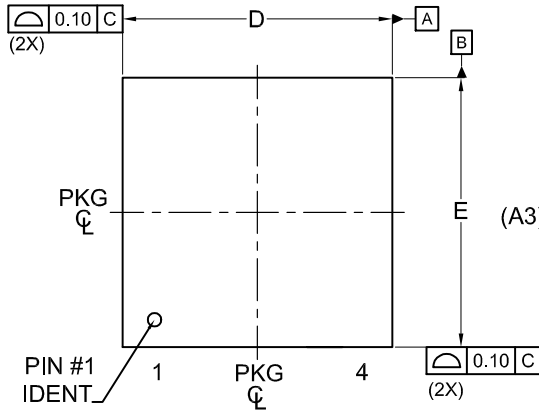


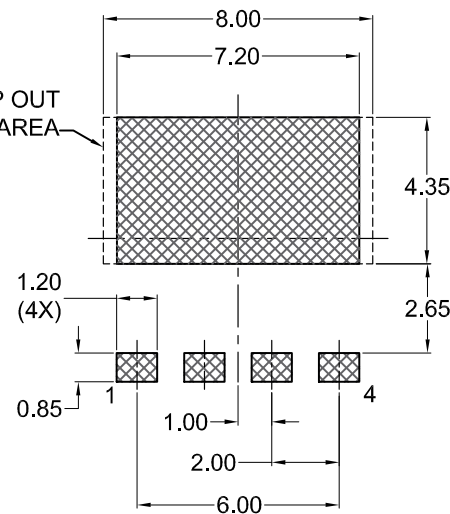
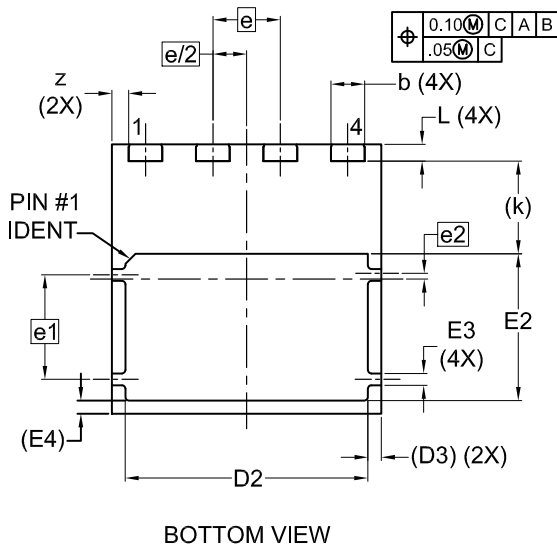
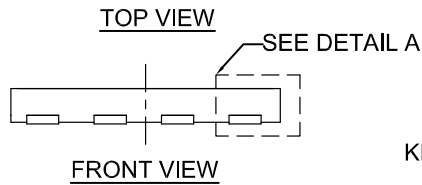
Figure 16. Peak Diode Recovery dv/dt Test Circuit & Waveforms


PQFN4 8X8, 2P
CASE 483AP
ISSUE A

DATE 06 JUL 2021


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
5. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
6. IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.



DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
A1	0.00	-	0.05
A3	0.20 REF		
b	0.90	1.00	1.10
D	7.90	8.00	8.10
D2	7.10	7.20	7.30
D3	0.40 REF		
E	7.90	8.00	8.10
E2	4.25	4.35	4.45
E3	0.25	0.35	0.45
E4	0.40 REF		
e	2.00 BSC		
e/2	1.00 BSC		
e1	3.10 BSC		
e2	0.17 BSC		
k	2.75 REF		
L	0.40	0.50	0.60

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERM/D.

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