

MOSFET – N-Channel, SUPERFET[®], FRFET[®]

600 V, 47 A, 73 mΩ

FCH47N60F

Description

SUPERFET MOSFET is onsemi's first generation of high voltage super-junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low on-resistance and lower gate charge performance. This technology is tailored to minimize conduction loss, provide superior switching performance, dv/dt rate and higher avalanche energy. Consequently, SUPERFET MOSFET is very suitable for the switching power applications such as PFC, server / telecom power, FPD TV power, ATX power and industrial power applications. SUPERFET FRFET MOSFET's optimized body diode reverse recovery performance can remove additional component and improve system reliability.

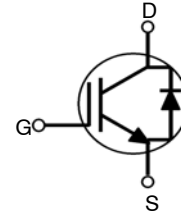
Features

- 650 V @ $T_J = 150^{\circ}\text{C}$
- Typ. $R_{DS(on)} = 58\text{ m}\Omega$
- Ultra Low Gate Charge (Typ. $Q_g = 210\text{ nC}$)
- Low Effective Output Capacitance (Typ. $C_{oss\text{eff.}} = 420\text{ pF}$)
- 100% Avalanche Tested
- These Devices are Pb-Free and are RoHS Compliant

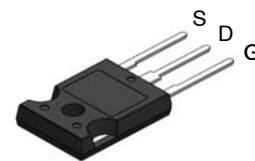
Applications

- Solar Inverter
- AC-DC Power Supply

V_{DS}	$R_{DS(on)}\text{ MAX}$	$I_D\text{ MAX}$
600 V	73 mΩ @ 10 V	47 A

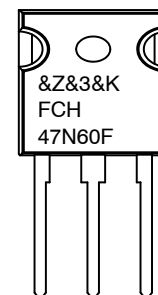


N-CHANNEL MOSFET



**TO-247-3LD
CASE 340CK**

MARKING DIAGRAM



&Z	= Assembly Plant Code
&3	= Numeric Date Code
&K	= Lot Code
FCH47N60F	= Specific Device Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

FCH47N60F

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Symbol	Parameter	FCH47N60F-F133	Unit
V _{DSS}	Drain to Source Voltage	600	V
I _D	Drain Current – –Continuous (T _C = 25°C) –Continuous (T _C = 100°C)	47 29.7	A A
I _{DM}	Drain Current –Pulsed (Note 1)	141	A
V _{GSS}	Gate–Source Voltage	±30	V
E _{AS}	Single Pulsed Avalanche Energy (Note 2)	1800	mJ
I _{AR}	Avalanche Current (Note 1)	47	A
E _{AR}	Repetitive Avalanche Energy (Note 1)	41.7	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	50	V/ns
P _D	Power Dissipation (T _C = 25°C) –Derate Above 25°C	417 3.33	W W/°C
T _J , T _{STG}	Operating and Storage Temperature Range	–55 to + 150	°C
T _L	Maximum Lead Temperature for Soldering Purpose, ¼ from Case for 5 second	300	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Repetitive Rating: Pulse width limited by maximum junction temperature.

2. I_{AS} = 18 A, V_{DD} = 50 V, R_G = 25 Ω, Starting T_J = 25 °C

3. I_{SD} ≤ 47 A, di/dt ≤ 1200 A/μs, V_{DD} ≤ BV_{DSS}, Starting T_J = 25 °C.

PACKAGE MARKING AND ORDERING INFORMATION

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FCH47N60F	FCH47N60F-F133	TO-247-3	–	–	30 Units

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
R _{θJC}	Thermal Resistance, Junction to Case, Max.	0.3	°C/W
R _{θJA}	Thermal Resistance, Junction to Ambient, Max. (Note 4)	41.7	



FCH47N60F

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
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OFF CHARACTERISTICS

BV _{DSS}	Drain to Source Breakdown Voltage	I _D = 250 μA, V _{GS} = 0 V, T _J = 25°C	600	–	–	V
		I _D = 250 μA, V _{GS} = 0 V, T _J = 150°C	–	650	–	V
ΔBV _{DSS} / ΔT _J	Breakdown Voltage Temperature Coefficient	I _D = 250 μA, Referenced to 25°C	–	0.6	–	V/°C
BV _{DS}	Drain–Source Avalanche Breakdown Voltage	I _D = 47 A, V _{GS} = 0 V	–	700	–	V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 600 V, V _{GS} = 0 V	–	–	10	μA
		V _{DS} = 480 V, T _C = 125°C	–	–	100	μA
I _{GSSF}	Gate–Body Leakage Current, Forward	V _{GS} = 30 V, V _{DS} = 0 V	–	–	100	nA
I _{GSSR}	Gate–Body Leakage Current, Reverse	V _{GS} = –30 V, V _{DS} = 0 V	–	–	–100	nA

ON CHARACTERISTICS

V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 250 μA	3	–	5	V
R _{DS(on)}	Static Drain–Source On–Resistance	V _{GS} = 10 V, I _D = 23.5 A	–	0.062	0.073	Ω
g _{FS}	Forward Transconductance	V _{DS} = 40 V, I _D = 23.5 A	–	40	–	S

DYNAMIC CHARACTERISTICS

C _{iss}	Input Capacitance	V _{DS} = 25 V, V _{GS} = 0 V, f = 1 MHz	–	5900	8000	pF
C _{oss}	Output Capacitance		–	3200	4200	pF
C _{rss}	Reverse Transfer Capacitance		–	250	–	pF
C _{oss}	Output Capacitance	V _{DS} = 480 V, V _{GS} = 0 V, f = 1 MHz	–	160	–	pF
C _{oss} eff.	Effective Output Capacitance	V _{DS} = 0 V to 400 V, V _{GS} = 0 V	–	420	–	pF

SWITCHING CHARACTERISTICS

t _{d(on)}	Turn-On Delay Time	V _{DD} = 300 V, I _D = 47 A, R _G = 25 Ω (Note 4)	–	185	430	ns
t _r	Turn–On Rise Time		–	210	450	ns
t _{d(off)}	Turn–Off Delay Time		–	520	1100	ns
t _f	Turn–Off Fall Time		–	75	160	ns
Q _g	Total Gate Charge	V _{DS} = 480 V, I _D = 47 A, V _{GS} = 10 V (Note 4)	–	210	270	nC
Q _{gs}	Gate–Source Charge		–	38	–	nC
Q _{gd}	Gate–Drain Charge		–	110	–	nC

DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS

I _S	Maximum Continuous Drain–Source Diode Forward Current		–	–	47	A
I _{SM}	Maximum Pulsed Drain–Source Diode Forward Current		–	–	141	A
V _{SD}	Source to Drain Diode Voltage	V _{GS} = 0 V, I _S = 47 A	–	–	1.4	V
t _{rr}	Reverse Recovery Time	V _{GS} = 0 V, I _S = 47 A, dI _F /dt = 100 A/μs	–	240	–	ns
Q _{rr}	Reverse Recovery Charge		–	2.04	–	μC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Essentially Independent of Operating Temperature Typical Characteristics.

TYPICAL CHARACTERISTICS

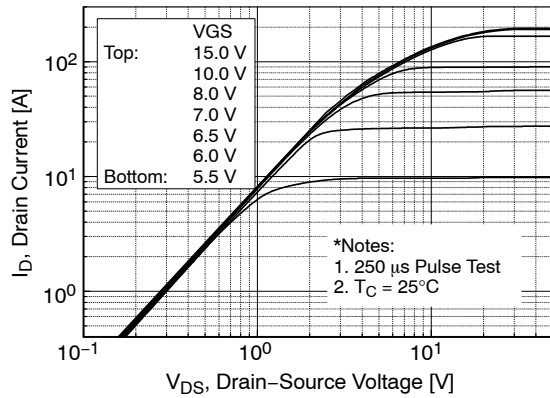


Figure 1. On-Region Characteristics

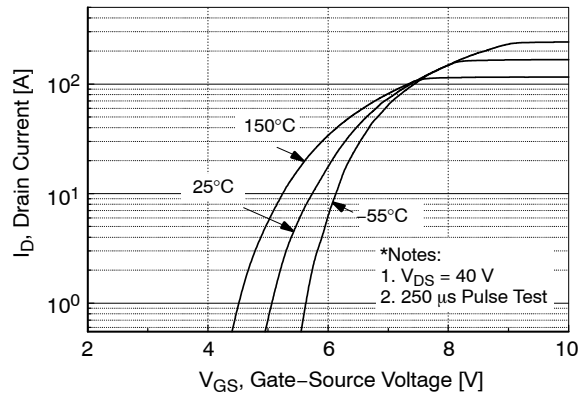


Figure 2. Transfer Characteristics

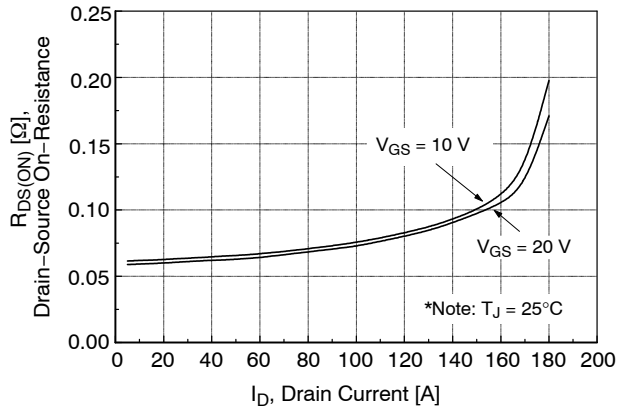


Figure 3. On-Resistance Variation vs. Drain Current and Gate voltage

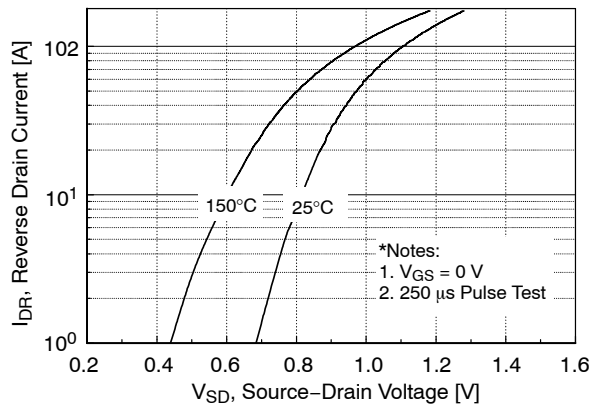


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

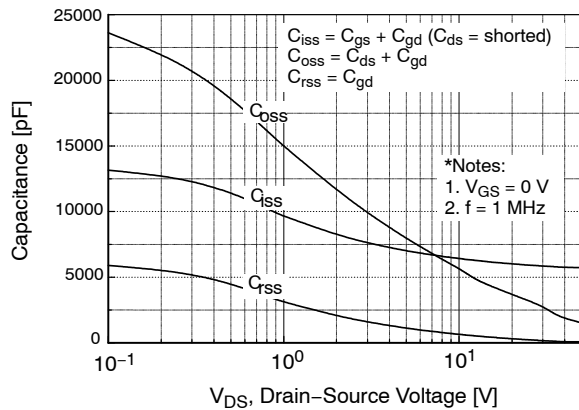


Figure 5. Capacitance Characteristics

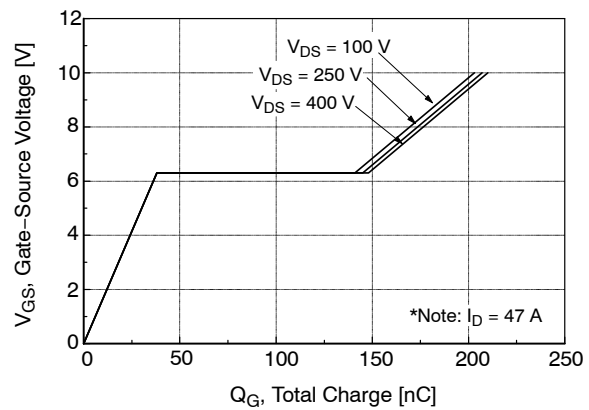


Figure 6. Gate Charge Characteristics

TYPICAL CHARACTERISTICS

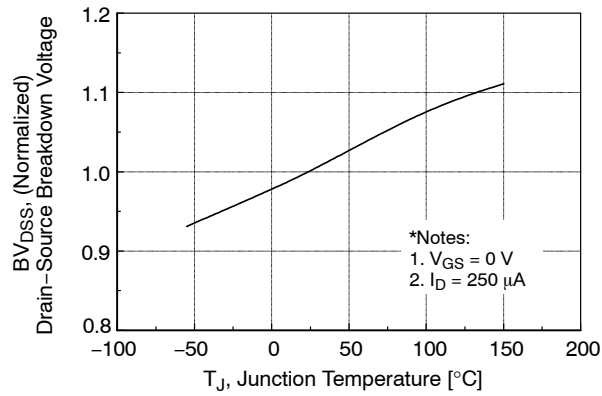


Figure 7. Breakdown Voltage Variation vs. Temperature

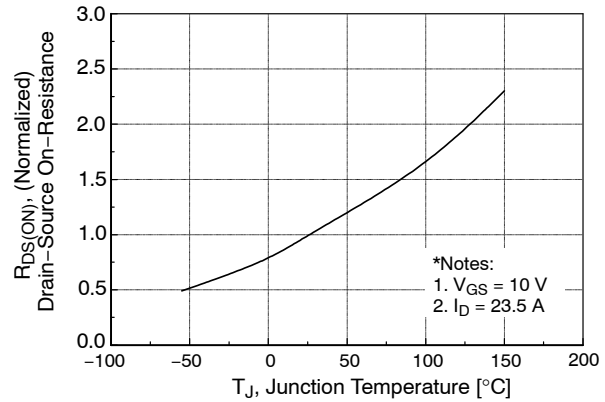


Figure 8. On-Resistance Variation vs. Temperature

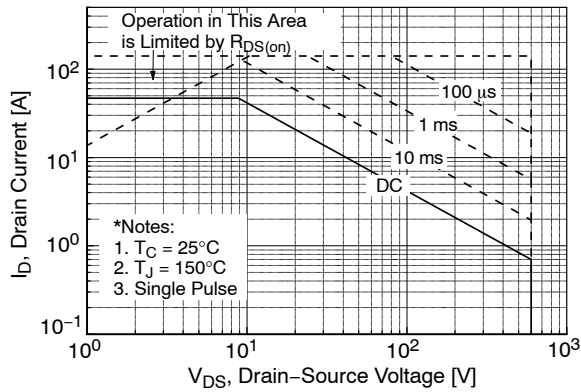


Figure 9. Safe Operating Area

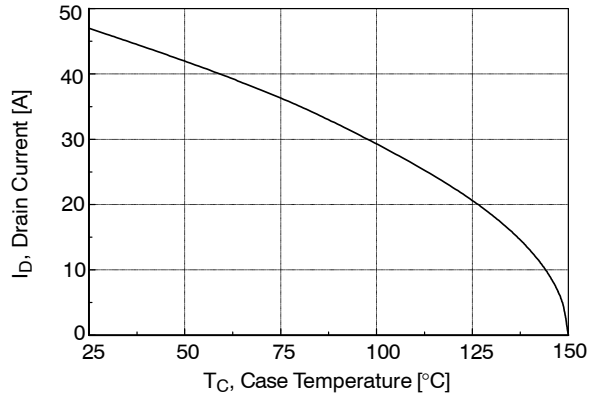


Figure 10. Maximum Drain Current vs. Case Temperature

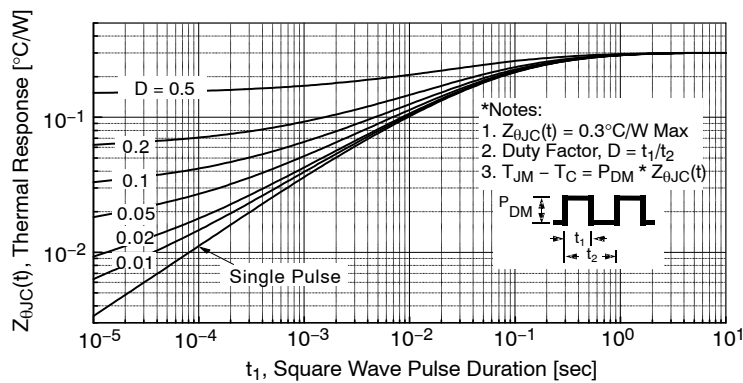


Figure 11. Transient Thermal Response Curve

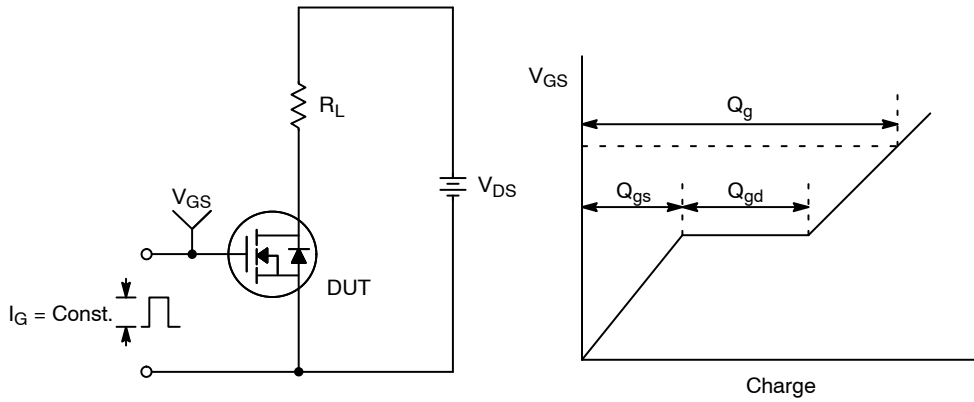


Figure 12. Gate Charge Test Circuit & Waveform

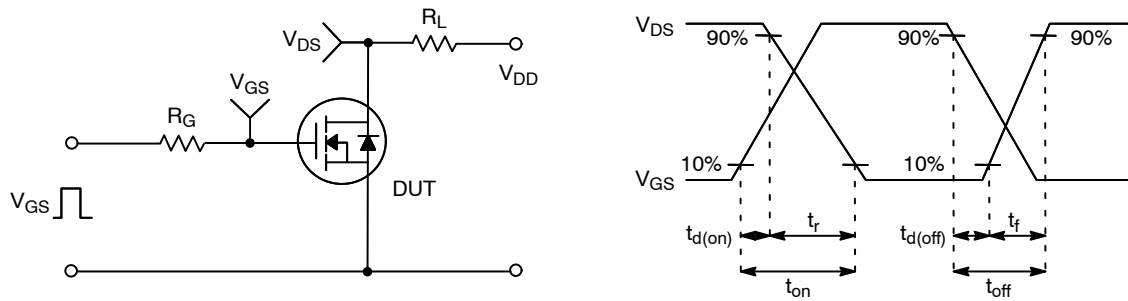


Figure 13. Resistive Switching Test Circuit & Waveforms

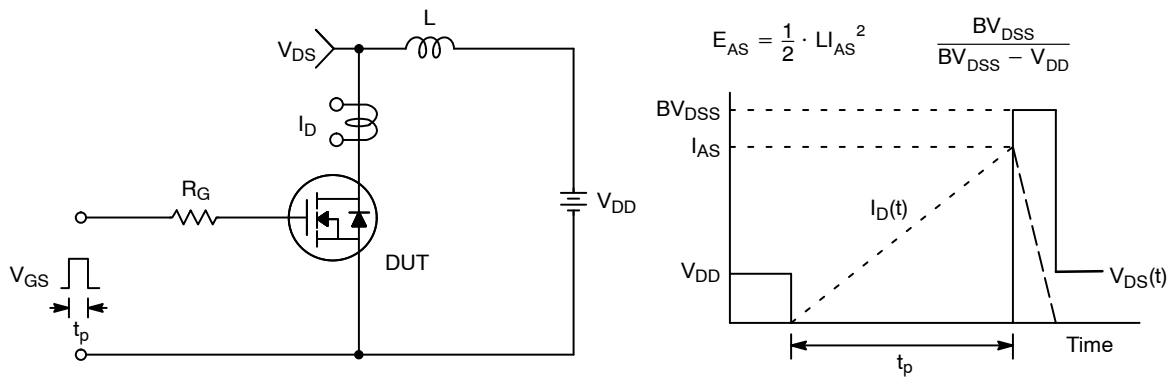


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

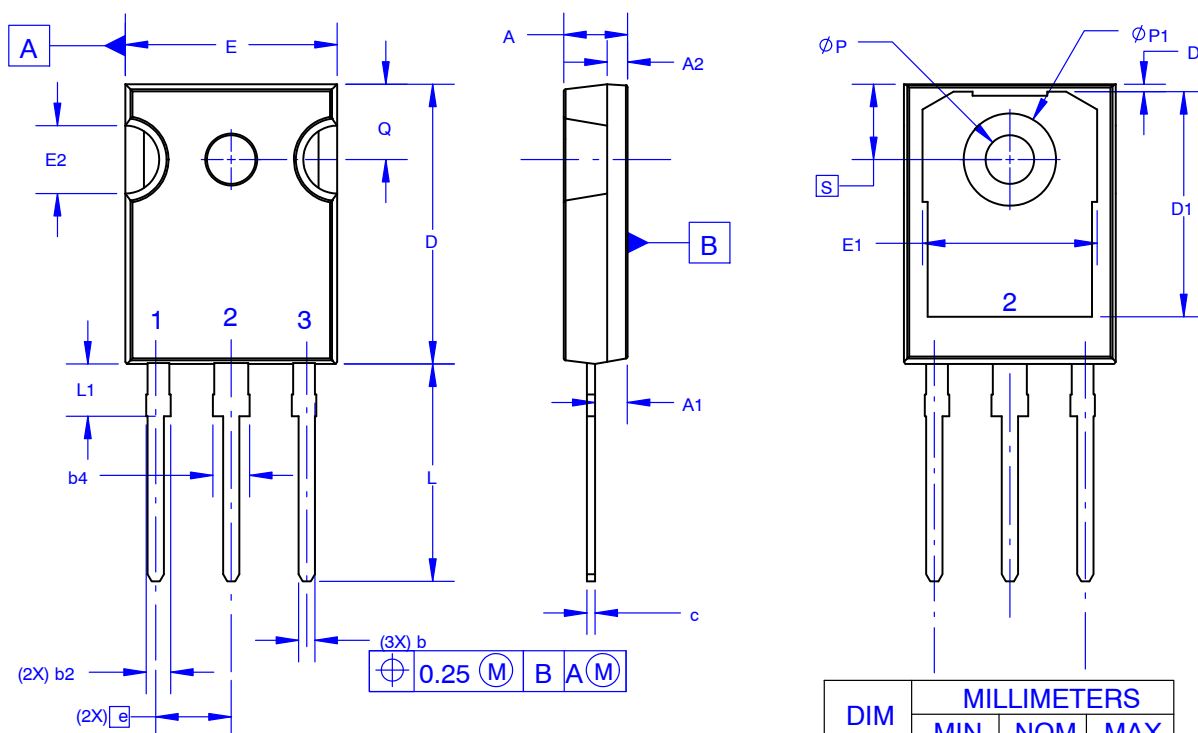
The diagram shows a switching circuit. A MOSFET labeled "Driver" (Same Type as DUT) has its gate connected to a square-wave voltage source V_{GS} through a resistor R_G . The driver's drain is connected to the source of the DUT. The DUT's gate is connected to its drain. The DUT's source is connected to ground through an inductor L . The DUT's drain is connected to a positive supply V_{DD} through a switch. The voltage across the DUT is V_{SD} and the current through the inductor is I_{SD} . The circuit is used to study the switching behavior of the DUT, with dV/dt controlled by R_G and I_{SD} controlled by the pulse period.



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Your Opinion Matters

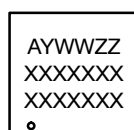
TO-247-3LD SHORT LEAD
CASE 340CK
ISSUE A

DATE 31 JAN 2019



NOTES: UNLESS OTHERWISE SPECIFIED.

- A. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
B. ALL DIMENSIONS ARE IN MILLIMETERS.
C. DRAWING CONFORMS TO ASME Y14.5 - 2009.
D. DIMENSION A1 TO BE MEASURED IN THE REGION DEFINED BY L1.
E. LEAD FINISH IS UNCONTROLLED IN THE REGION DEFINED BY L1.

GENERIC
MARKING DIAGRAM*


XXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
ZZ = Assembly Lot Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	4.58	4.70	4.82
A1	2.20	2.40	2.60
A2	1.40	1.50	1.60
b	1.17	1.26	1.35
b2	1.53	1.65	1.77
b4	2.42	2.54	2.66
c	0.51	0.61	0.71
D	20.32	20.57	20.82
D1	13.08	~	~
D2	0.51	0.93	1.35
E	15.37	15.62	15.87
E1	12.81	~	~
E2	4.96	5.08	5.20
e	~	5.56	~
L	15.75	16.00	16.25
L1	3.69	3.81	3.93
ϕP	3.51	3.58	3.65
$\phi P1$	6.60	6.80	7.00
Q	5.34	5.46	5.58
S	5.34	5.46	5.58

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