

MOSFET – N-Channel, SUPERFET®

600 V, 47 A, 70 mΩ

FCA47N60, FCA47N60-F109

Description

SUPERFET MOSFET is onsemi's first generation of high voltage super-junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low on-resistance and lower gate charge performance. This technology is tailored to minimize conduction loss, provide superior switching performance, dv/dt rate and higher avalanche energy. Consequently, SUPERFET MOSFET is very suitable for the switching power applications such as PFC, server/telecom power, FPD TV power, ATX power and industrial power applications.

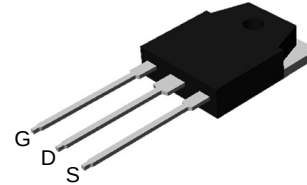
Features

- 650 V @ $T_J = 150^{\circ}\text{C}$
- Typ. $R_{DS(on)} = 58\text{ m}\Omega$
- Ultra Low Gate Charge (Typ. $Q_g = 210\text{ nC}$)
- Low Effective Output Capacitance (Typ. $C_{oss(eff.)} = 420\text{ pF}$)
- 100% Avalanche Tested

Applications

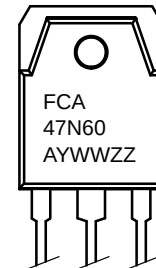
- Solar Inverter
- AC-DC Power Supply

V_{DSS}	$R_{DS(on)}\text{ MAX}$	$I_D\text{ MAX}$
600 V	70 mΩ @ 10 V	47 A



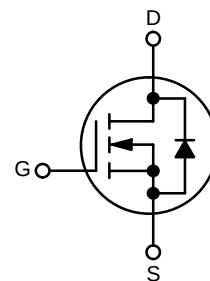
TO-3P-3LD / EIAJ SC-65, ISOLATED
CASE 340BZ

MARKING DIAGRAM



FCA47N60 = Specific Device Code
A = Assembly Location
YWW = Date Code (Year & Week)
ZZ = Assembly Lot

N-CHANNEL MOSFET



ORDERING INFORMATION

Part Number	Package	Shipping
FCA47N60	TO-3P-3LD (Pb-Free)	450 Units / Tube
FCA47N60-F109		450 Units / Tube

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ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		FCA47N60	FCA47N60-F109	Unit
V_{DS}	Drain-Source Voltage			600	V
I_D	Drain Current	- Continuous ($T_C = 25^\circ\text{C}$)		47	A
		- Continuous ($T_C = 100^\circ\text{C}$)		29.7	
I_{DM}	Drain Current	- Pulsed (Note 1)		141	A
V_{GSS}	Gate-Source Voltage			± 30	V
E_{AS}	Single Pulsed Avalanche Energy (Note 2)			1800	mJ
I_{AR}	Avalanche Current (Note 1)			47	A
E_{AR}	Repetitive Avalanche Energy (Note 1)			41.7	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)			4.5	V/ns
P_D	Power Dissipation	($T_C = 25^\circ\text{C}$)		417	W
		- Derate above 25°C		3.33	W/ $^\circ\text{C}$
T_J, T_{STG}	Operating and Storage Temperature Range			-55 to +150	$^\circ\text{C}$
T_L	Maximum Lead Temperature for Soldering Purpose, 1/8" from Case for 5 Seconds			300	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Repetitive Rating: Pulse-width limited by maximum junction temperature.
2. $I_{AS} = 18\text{ A}$, $R_G = 25\ \Omega$, starting $T_J = 25^\circ\text{C}$.
3. $I_{SD} \leq 47\text{ A}$, $di/dt \leq 200\text{ A}/\mu\text{s}$, $V_{DD} = 380\text{ V}$, starting $T_J = 25^\circ\text{C}$.

THERMAL CHARACTERISTICS

Symbol	Parameter	Typ	Max	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case, Max.	-	0.3	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient, Max.	-	41.7	$^\circ\text{C}/\text{W}$

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ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} = 0 V, I _D = 250 μA, T _J = 25°C	600	–	–	V
		V _{GS} = 0 V, I _D = 250 μA, T _J = 150°C	–	650	–	
ΔBV _{DSS} / ΔT _J	Breakdown Voltage Temperature Coefficient	I _D = 250 μA, Referenced to 25°C	–	0.6	–	V/°C
BV _{DS}	Drain-Source Avalanche Breakdown Voltage	V _{GS} = 0 V, I _D = 47 A	–	700	–	V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 600 V, V _{GS} = 0 V	–	–	10	μA
		V _{DS} = 480 V, T _C = 125°C	–	–	100	
I _{GSSF}	Gate-Body Leakage Current, Forward	V _{GS} = 30 V, V _{DS} = 0 V	–	–	100	nA
I _{GSSR}	Gate-Body Leakage Current, Reverse	V _{GS} = –30 V, V _{DS} = 0 V	–	–	–100	nA

ON CHARACTERISTICS

V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 250 μA	3.0	–	5.0	V
R _{DS(on)}	Static Drain-Source On-Resistance	V _{GS} = 10 V, I _D = 23.5 A	–	0.058	0.07	Ω
g _{FS}	Forward Transconductance	V _{DS} = 20 V, I _D = 23.5 A	–	40	–	S

DYNAMIC CHARACTERISTICS

C _{iss}	Input Capacitance	V _{DS} = 25 V, V _{GS} = 0 V, f = 1.0 MHz	–	5900	8000	pF
C _{oss}	Output Capacitance		–	3200	4200	pF
C _{rss}	Reverse Transfer Capacitance		–	250	–	pF
C _{oss}	Output Capacitance	V _{DS} = 480 V, V _{GS} = 0 V, f = 1.0 MHz	–	160	–	pF
C _{oss eff.}	Effective Output Capacitance	V _{DS} = 0 to 400 V, V _{GS} = 0 V	–	420	–	pF

SWITCHING CHARACTERISTICS

t _{d(on)}	Turn-On Delay Time	V _{DD} = 300 V, I _D = 47 A, R _G = 25 Ω (Note 4)	–	185	430	ns
t _r	Turn-On Rise Time		–	210	450	ns
t _{d(off)}	Turn-Off Delay Time		–	520	1100	ns
t _f	Turn-Off Fall Time		–	75	160	ns
Q _g	Total Gate Charge	V _{DS} = 480 V, I _D = 47 A, V _{GS} = 10 V (Note 4)	–	210	270	nC
Q _{gs}	Gate-Source Charge		–	38	–	nC
Q _{gd}	Gate-Drain Charge		–	110	–	nC

DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS

I _S	Maximum Continuous Drain–Source Diode Forward Current		–	–	47	A
I _{SM}	Maximum Pulsed Drain–Source Diode Forward Current		–	–	141	A
V _{SD}	Drain–Source Diode Forward Voltage	V _{GS} = 0 V, I _S = 47 A	–	–	1.4	V
t _{rr}	Reverse Recovery Time	V _{GS} = 0 V, I _S = 47 A, dI _F /dt = 100 A/μs (Note 4)	–	590	–	ns
Q _{rr}	Reverse Recovery Charge		–	25	–	μC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Essentially independent of operating temperature typical characteristics.

TYPICAL CHARACTERISTICS

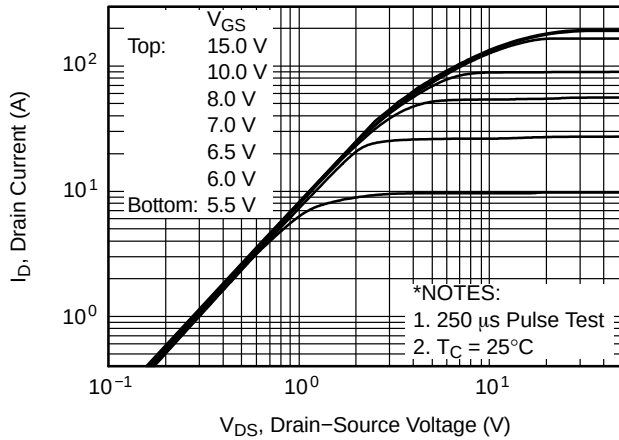


Figure 1. On-Region Characteristics

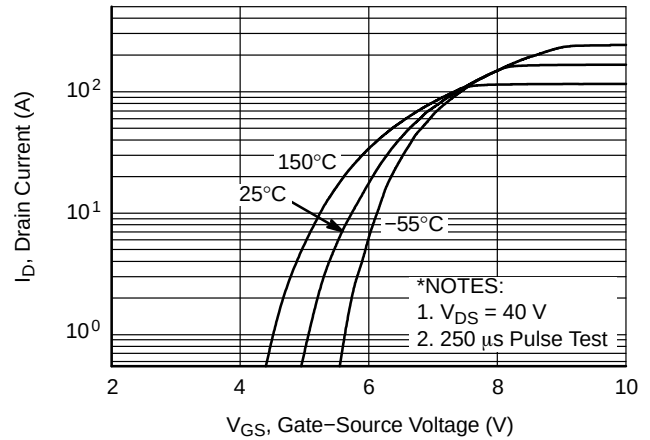


Figure 2. Transfer Characteristics

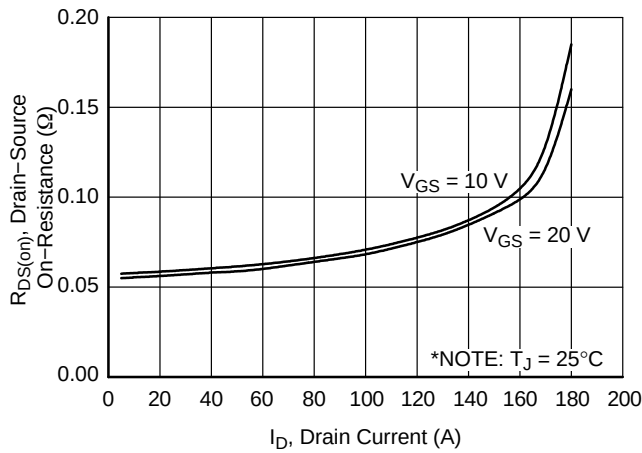


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

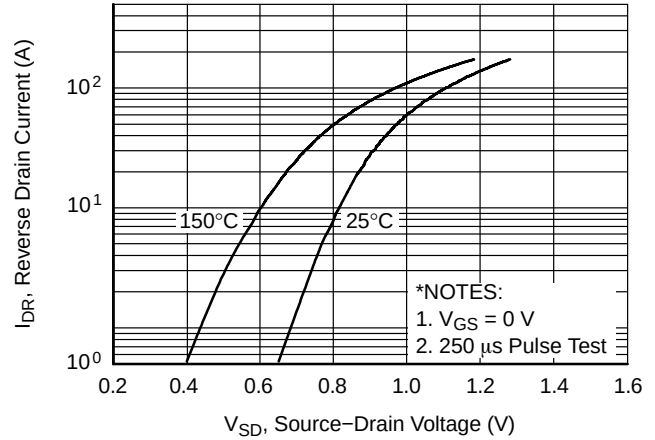


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

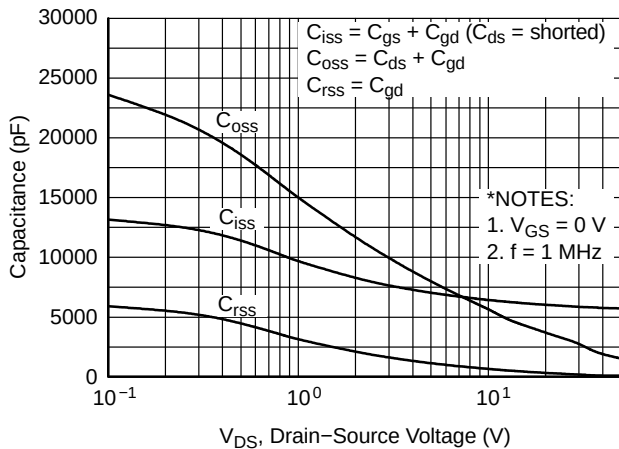


Figure 5. Capacitance Characteristics

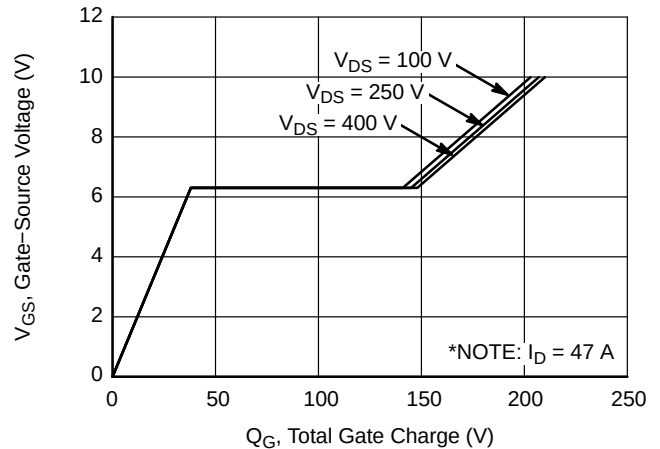
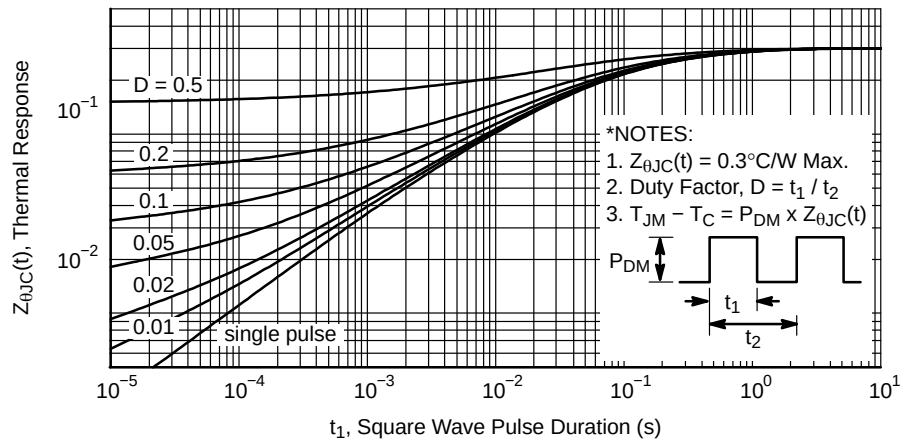
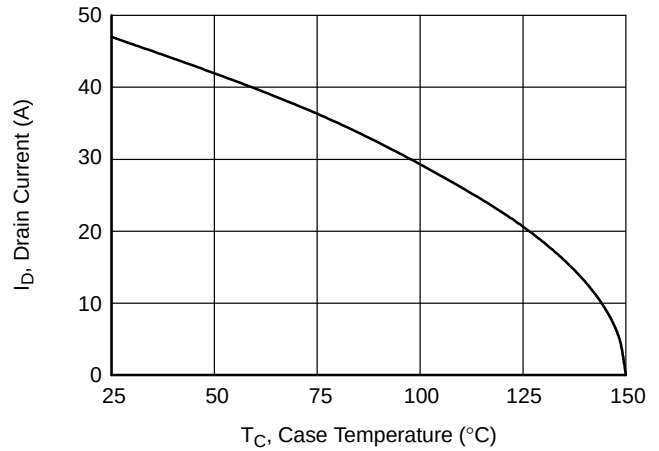
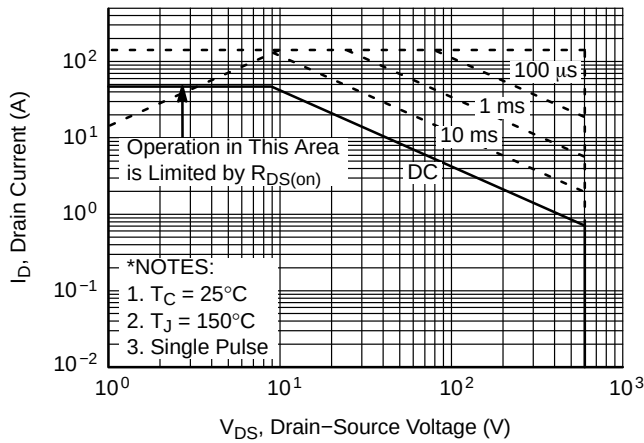
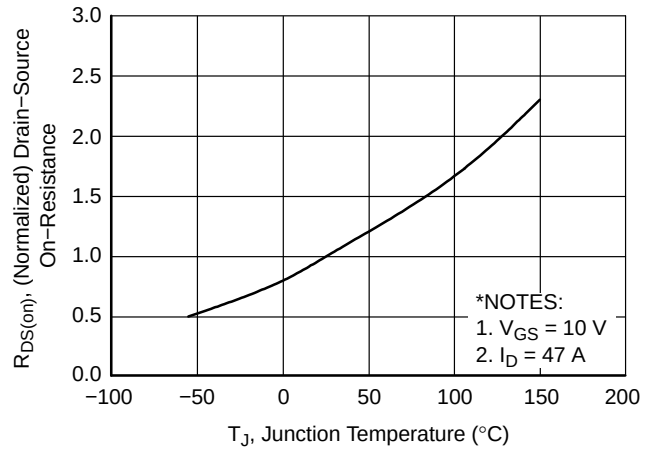
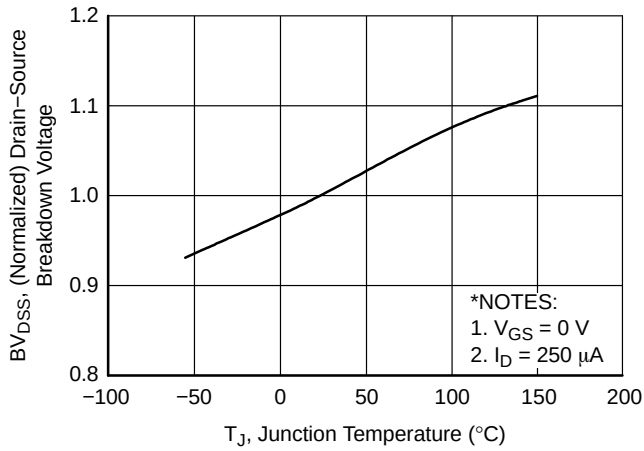


Figure 6. Gate Charge Characteristics

TYPICAL CHARACTERISTICS (CONTINUED)



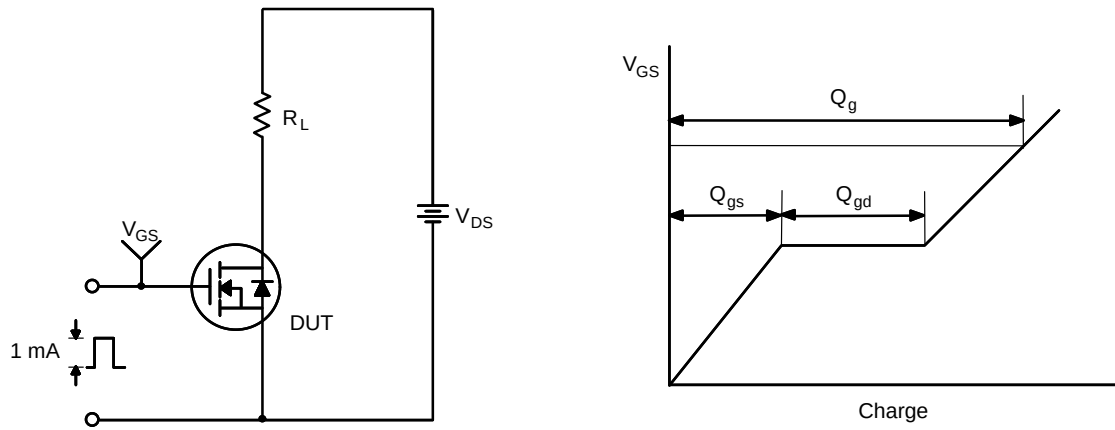


Figure 12. Gate Charge Test Circuit & Waveform

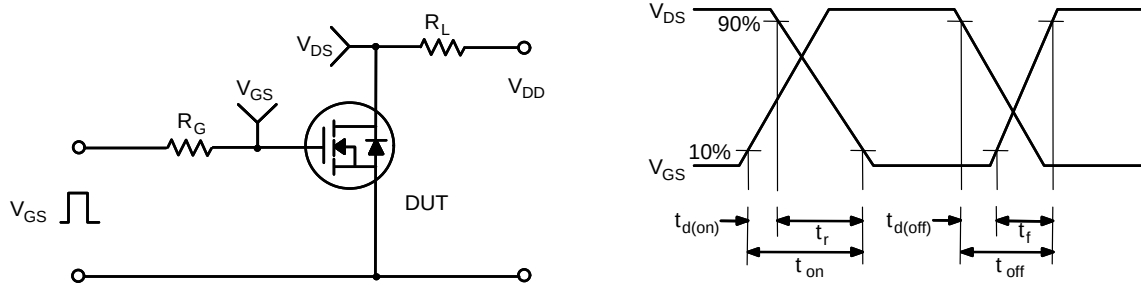


Figure 13. Resistive Switching Test Circuit & Waveforms

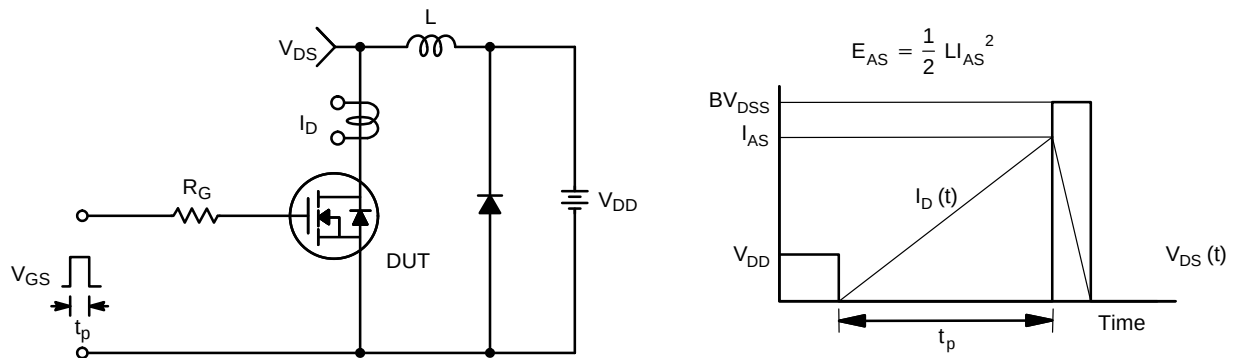


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

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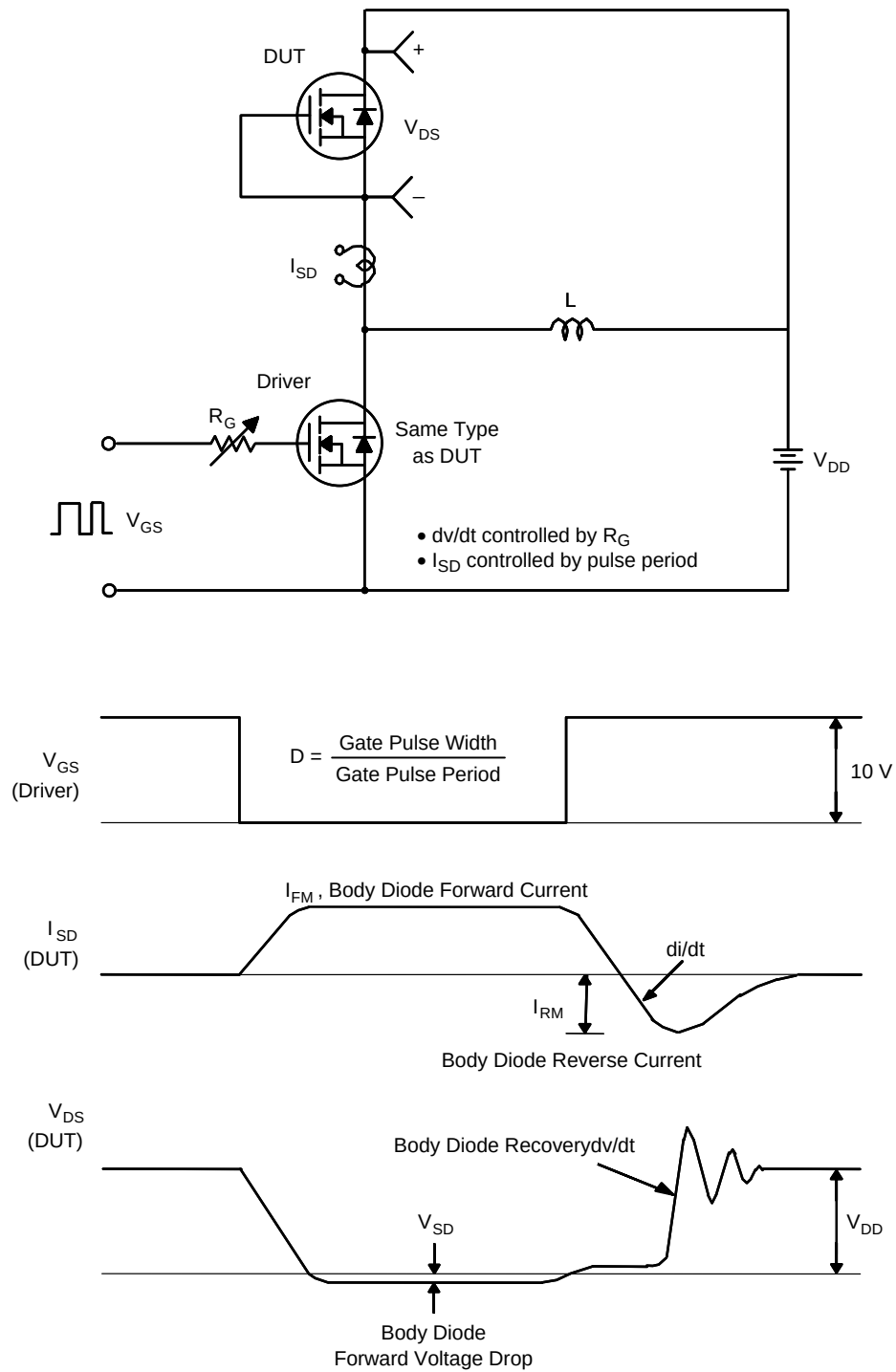
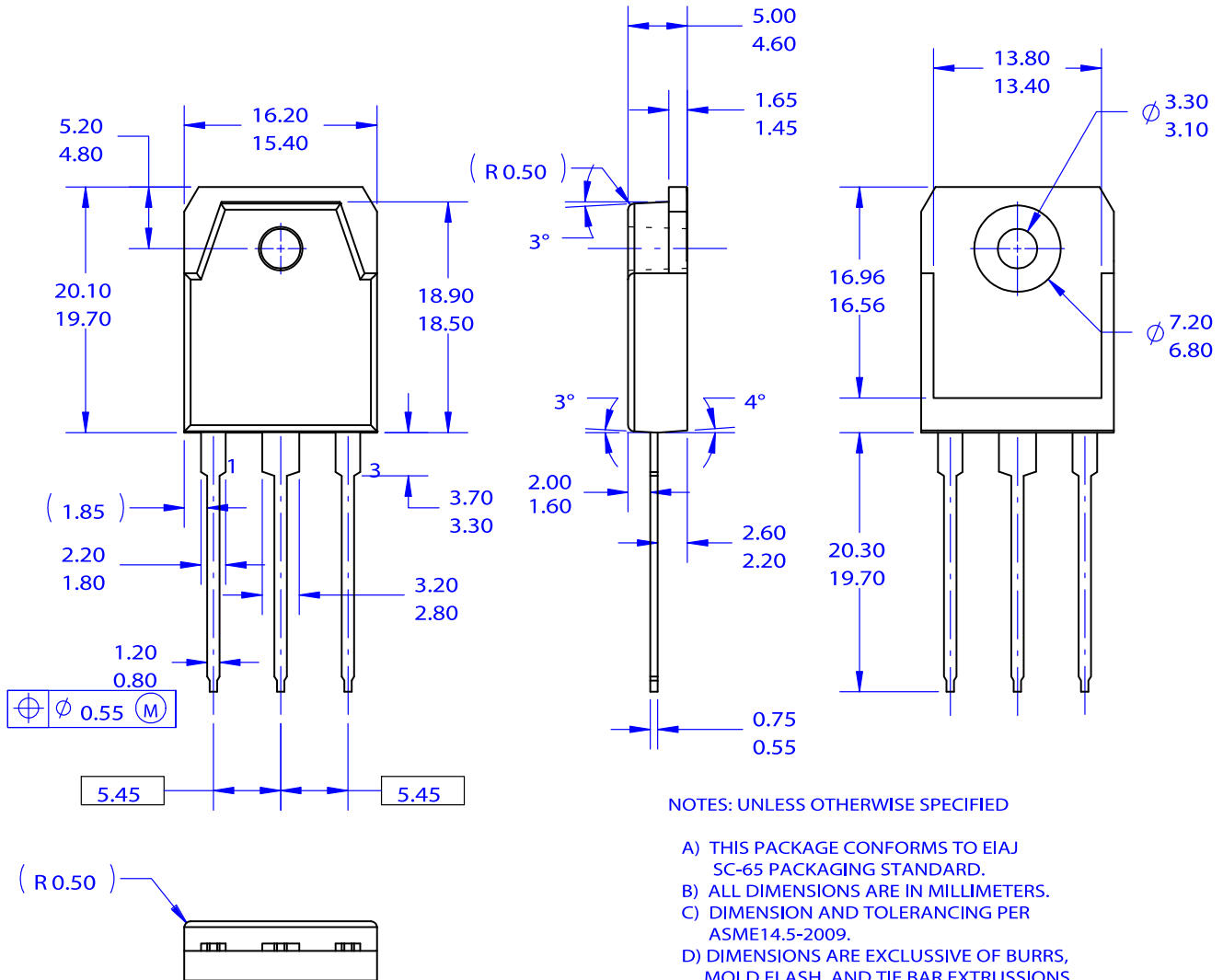


Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms

TO-3P-3LD / EIAJ SC-65, ISOLATED
CASE 340BZ
ISSUE O

DATE 31 OCT 2016



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