

## Evaluation Board User's Manual for High Frequency LQFP32



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### EVAL BOARD USER'S MANUAL

#### INTRODUCTION

ON Semiconductor has developed an evaluation board for the devices in 32-lead LQFP package. These evaluation boards are offered as a convenience for the customers interested in performing their own engineering assessment on the general performance of the 32-lead LQFP device samples. The board provides a high bandwidth 50  $\Omega$  controlled impedance environment. Figures 1 and 2 show the top and bottom view of the evaluation board, which can be configured in several different ways, depending on device under test (see Table 1. Configuration List).

This evaluation board manual contains:

- Information on 32-lead LQFP Evaluation Board
- Assembly Instructions
- Appropriate Lab Setup
- Bill of Materials

This manual should be used in conjunction with the device data sheet, which contains full technical details on the device specifications and operation.

#### Board Lay-Up

The 32-lead LQFP evaluation board is implemented in four layers with split (dual) power supplies (see Figure 3. Evaluation Board Lay-Up). For standard ECL lab setup and test, a split (dual) power supply is essential to enable the 50  $\Omega$  internal impedance in the oscilloscope as a termination for ECL devices. The first layer or primary trace layer is 0.008" thick Rogers RO4003 material, which is designed to have equal electrical length on all signal traces from the device under the test (DUT) to the sense output. The second layer is the 1.0 oz copper ground. The FR4 dielectric material is placed between second and third layer and between third and fourth layer. The third layer is the power plane ( $V_{CC}$  and  $V_{EE}$ ) and a portion of this layer is a ground plane. The fourth layer is the secondary trace layer.

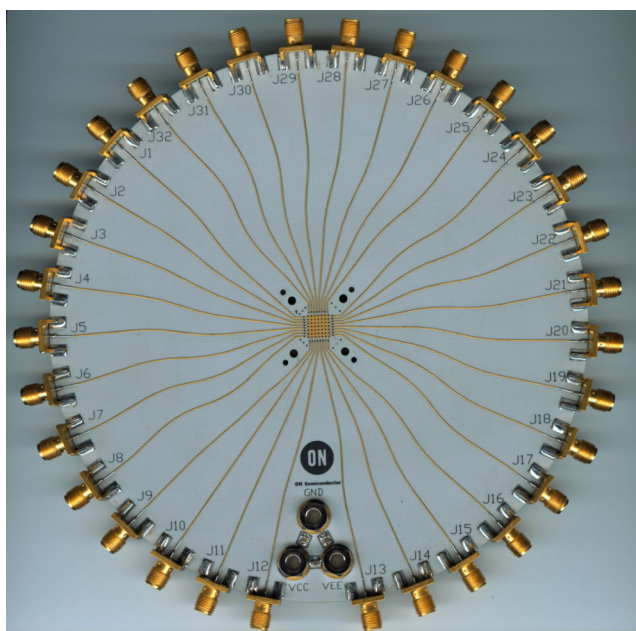
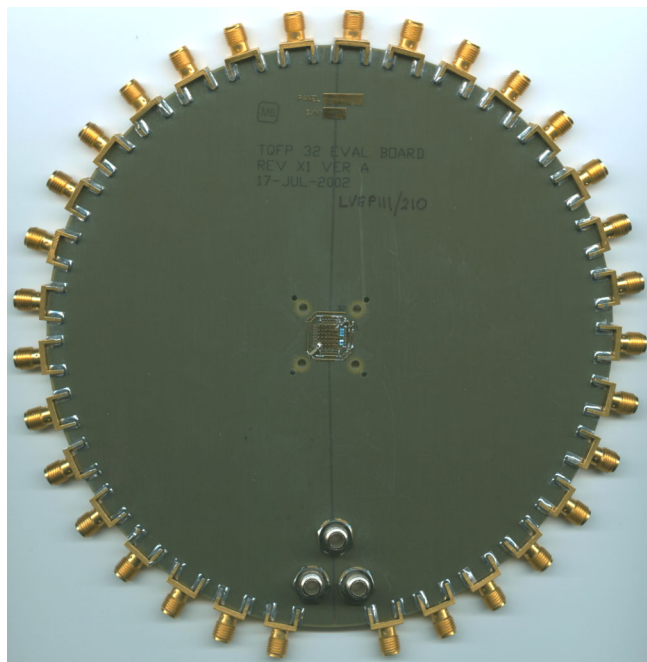
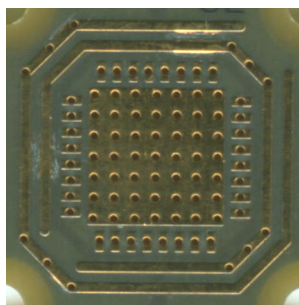


Figure 1. Top View of the 32-lead LQFP Evaluation Board

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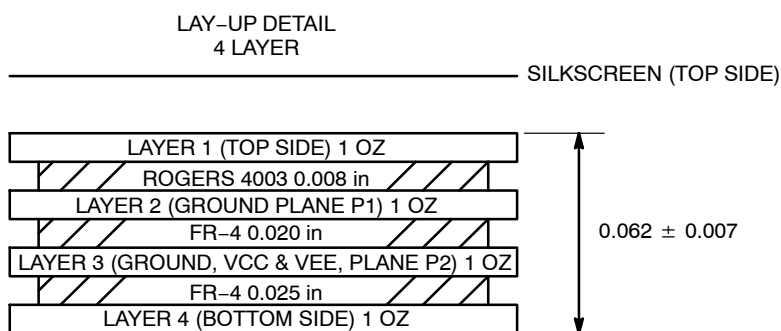


Bottom View



Enlarged Bottom View

**Figure 2. Bottom View of the 32-lead LQFP Evaluation Board**



**Figure 3. Evaluation Board Lay-up**

### Board Layout

The 32-lead LQFP evaluation board was designed to be versatile and accommodate several different configurations. The input, output, and power pin layout of the evaluation board is shown in Figures 4 and 5. The evaluation board has at least thirteen possible configurable options. Table 1, list the devices and the relevant configuration that utilizes this

PCB board. Lists of components and simple schematics are located in Figures 6 through 18. Place SMA connectors on J1 through J32, 50  $\Omega$  chip resistors between ground pad and Pin 1 pad through Pin 32 pad, and chip capacitors C1 through C5 according to configuration figures. (C4 and C5 are 0.01  $\mu$ F and C1, C2, and C3 are 0.1  $\mu$ F); (See Figure 5).

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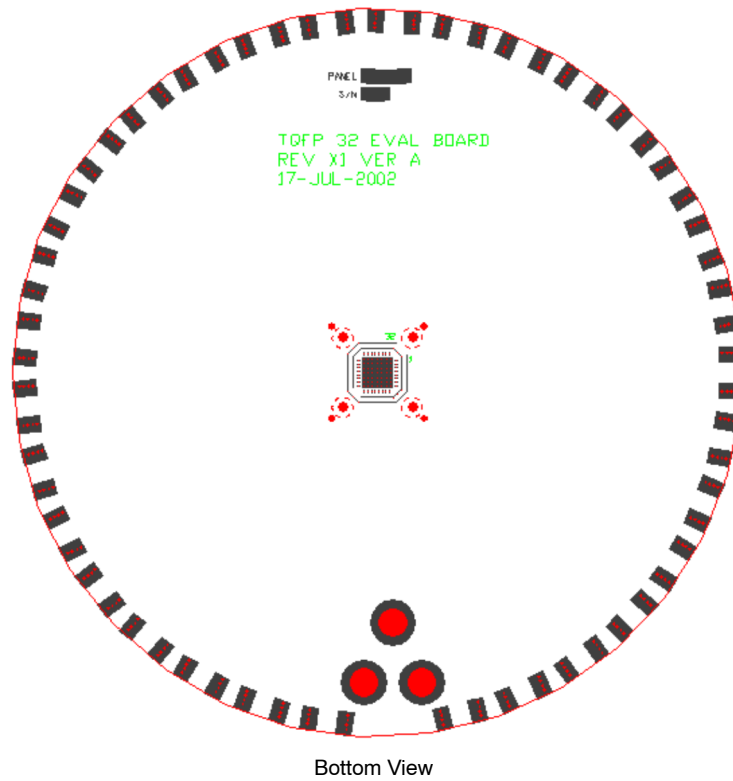
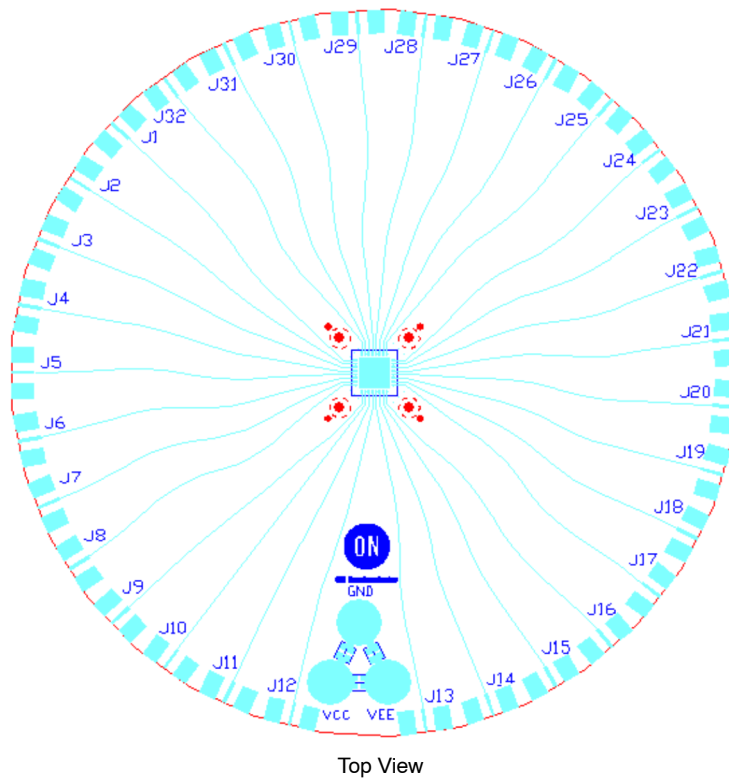
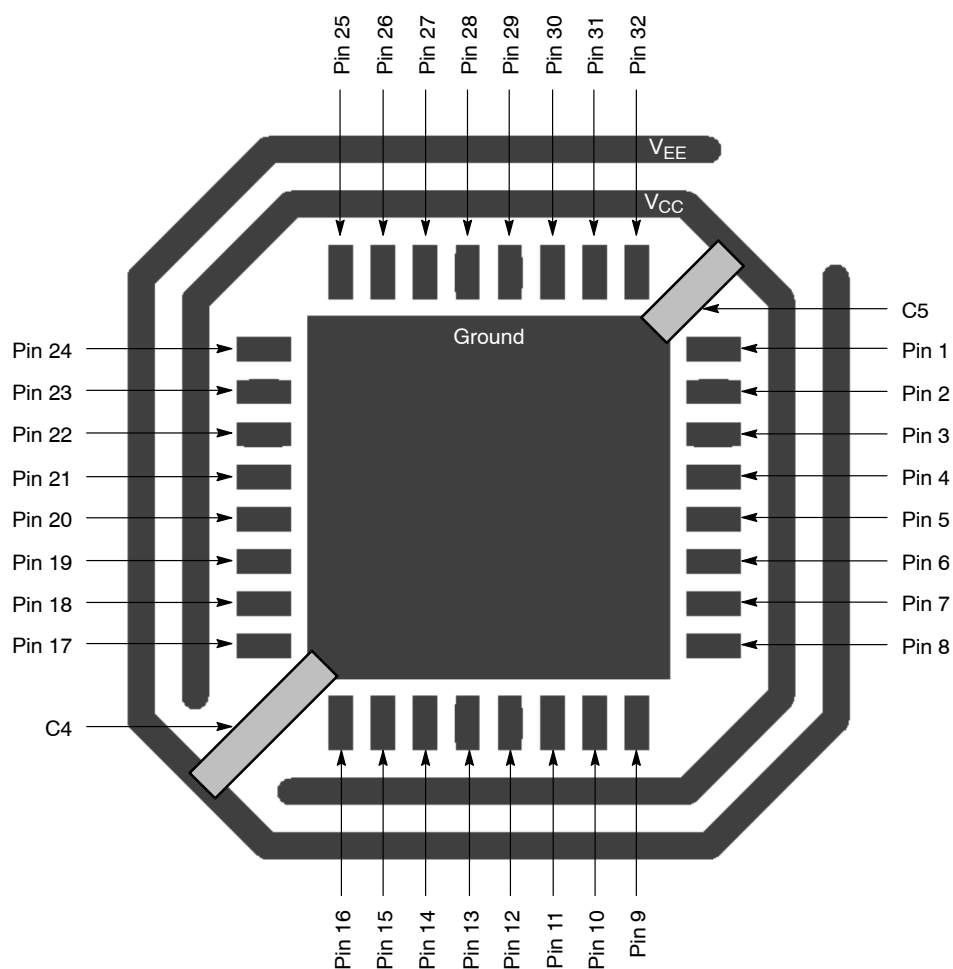


Figure 4. Evaluation Board Layout

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**Figure 5. Enlarged Bottom View of the Evaluation Board**

**Table 1. Configuration List**

| Configuration | Comments      | Device            |
|---------------|---------------|-------------------|
| 1             | See Figure 6  | LVE164            |
| 2             | See Figure 7  | EP016 / EP016A    |
| 3             | See Figure 8  | EP101 / EP105     |
| 4             | See Figure 9  | EP116             |
| 5             | See Figure 10 | EP131             |
| 6             | See Figure 11 | EP142             |
| 7             | See Figure 12 | EP195 / EP196     |
| 8             | See Figure 13 | EP445             |
| 9             | See Figure 14 | EP446             |
| 10            | See Figure 15 | EP451             |
| 11            | See Figure 16 | EP809             |
| 12            | See Figure 17 | LVEP111 / LVEP210 |
| 13            | See Figure 18 | LVEP210S          |

## Evaluation Board Assembly Instructions

The 32-lead LQFP evaluation board is designed for characterizing devices in a 50  $\Omega$  laboratory environment using high bandwidth equipment. Each signal trace on the board has a via, which has an option of placing a termination resistor depending on the input/output configuration (see Table 1, Configuration List). Table 17 contains the Bill of Materials for this evaluation board.

### Solder the Device on the Evaluation Board

The soldering can be accomplished by hand soldering or soldering re-flow techniques. Make sure pin 1 of the device is located next to the white dotted mark and all the pins are aligned to the footprint pads. Solder the 32-lead LQFP device to the evaluation board.

### Connecting Power and Ground Planes

For standard ECL lab setup and test, a split (dual) power supply is required enabling the 50  $\Omega$  internal impedance in the oscilloscope to be used as a termination of the ECL signals ( $V_{TT} = V_{CC} - 2.0$  V, in split power supply setup,  $V_{TT}$  is the system ground,  $V_{CC}$  is 2.0 V, and  $V_{EE}$  is  $-3.0$  V or  $-1.3$  V; see Table 2, Power Supply Levels).

**Table 2. Power Supply Levels**

| Power Supply | $V_{CC}$ | $V_{EE}$ | GND   |
|--------------|----------|----------|-------|
| 5.0 V        | 2.0 V    | $-3.0$ V | 0.0 V |
| 3.3 V        | 2.0 V    | $-1.3$ V | 0.0 V |
| 2.5 V        | 2.0 V    | $-0.5$ V | 0.0 V |

Connect three banana jack sockets to  $V_{CC}$ ,  $V_{EE}$ , and GND labeled holes. Wire bond the appropriate device pin pad on the bottom side of the board to  $V_{CC}$  and  $V_{EE}$  power stripes. (Device specific, please see configuration for each desired device. See Figure 5)

It is recommended to solder 0.01  $\mu$ F capacitors to C4 and C5 to reduce the unwanted noise from the power supplies. C1, C2, and C3 pads are provided for 0.1  $\mu$ F capacitor to further diminish the noise from the power supplies. Adding capacitors can improve edge rates, reduce overshoot and undershoot.

### Termination

All ECL outputs need to be terminated to  $V_{TT}$  ( $V_{TT} = V_{CC} - 2.0$  V = GND) via a 50  $\Omega$  resistor. 0402 chip resistor pads are provided on the bottom side of the evaluation board to terminate the ECL driver (More information on termination is provided in AN8020). Solder the chip resistors to the bottom side of the board between the appropriate input of the device pin pads and the ground pads. For ease of assembly, it is advised to place and solder termination resistors on its vertical (side) position, instead of its original or flat position.

### Installing the SMA Connectors

Each configuration indicates the number of SMA connectors needed to populate an evaluation board for a given configuration. Each input and output requires one SMA connector. Attach all the required SMA connectors onto the board and solder the connectors to the board on J1 through J32. Please note that alignment of the signal connector pin of the SMA can influence the lab results. The reflection and launch of the signals are largely influenced by imperfect alignment and soldering of the SMA connector.

### Validating the Assembled Board

After assembling the evaluation board, it is recommended to perform continuity checks on all soldered areas before commencing with the evaluation process. Time Domain Reflectometry (TDR) is another highly recommended validation test.

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## CONFIGURATIONS

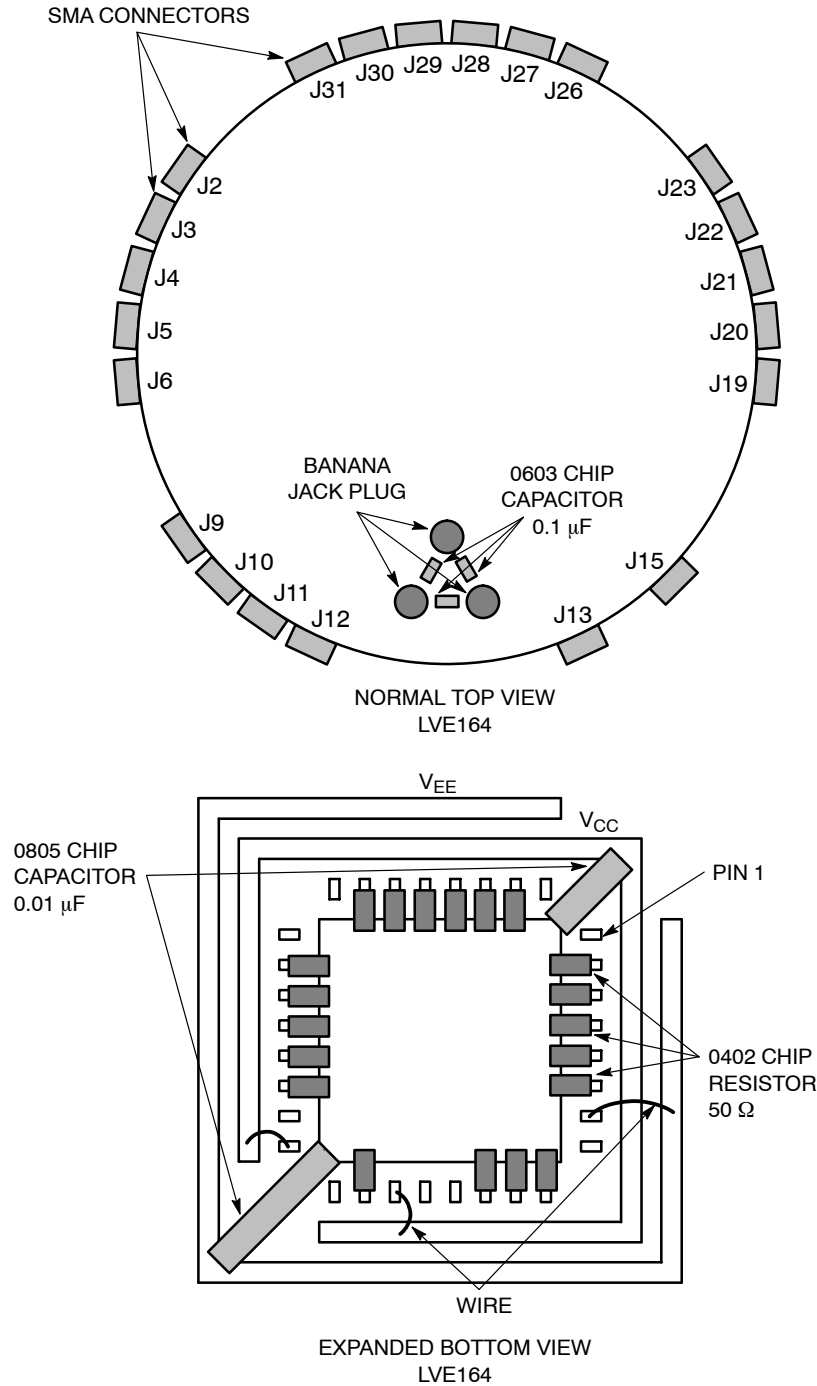
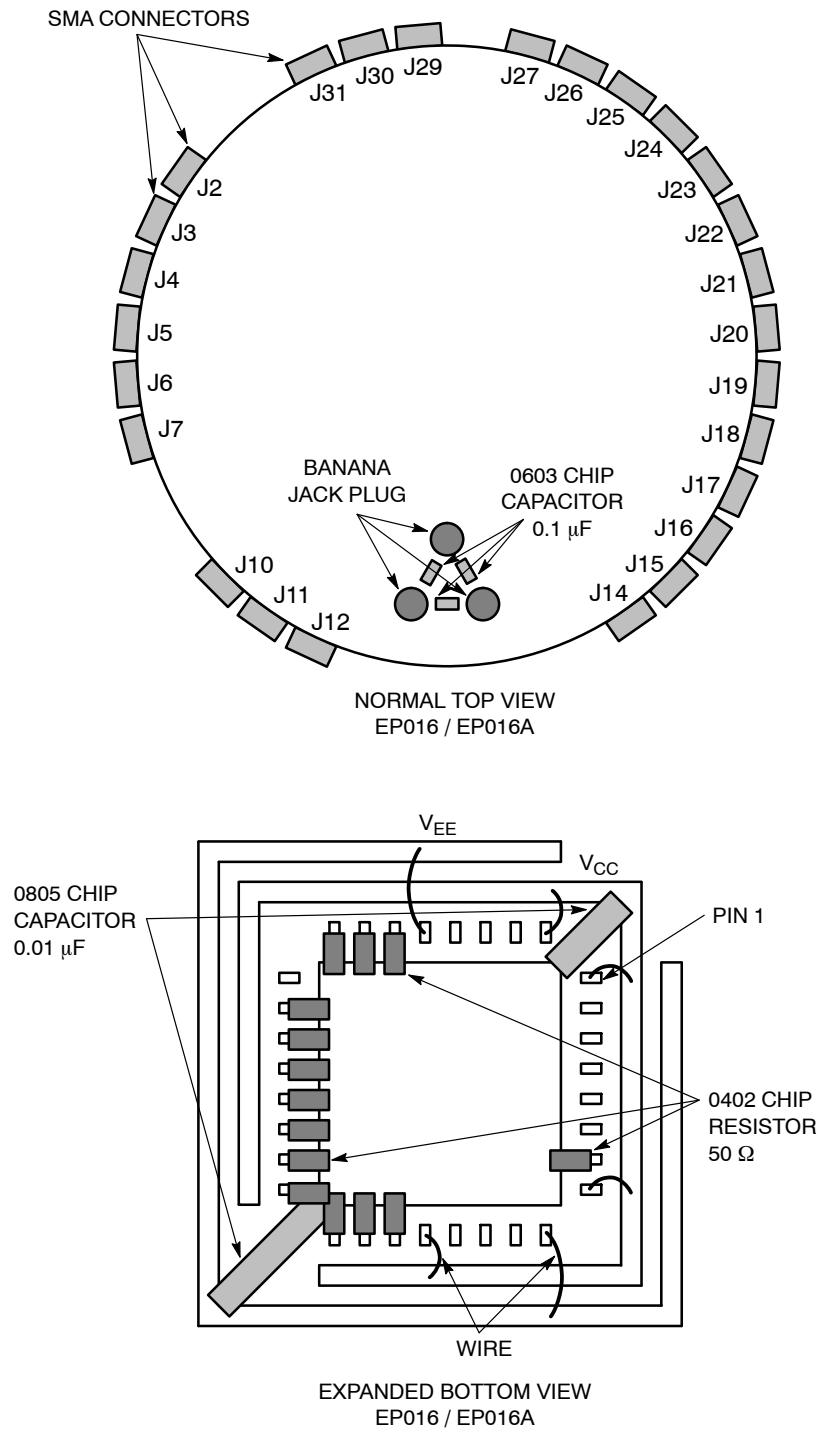


Figure 6. Configuration 1

Table 3. Configuration 1 (Device LVE164)

| Device    | J1 | J2 | J3 | J4 | J5 | J6 | J7 | J8 | J9 | J10 | J11 | J12 | J13 | J14 | J15 | J16 | J17 | J18 | J19 | J20 | J21 | J22 | J23 | J24 | J25 | J26 | J27 | J28 | J29 | J30 | J31 | J32 |
|-----------|----|----|----|----|----|----|----|----|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| Pin #     | 1  | 2  | 3  | 4  | 5  | 6  | 7  | 8  | 9  | 10  | 11  | 12  | 13  | 14  | 15  | 16  | 17  | 18  | 19  | 20  | 21  | 22  | 23  | 24  | 25  | 26  | 27  | 28  | 29  | 30  | 31  | 32  |
| Connector | N  | Y  | Y  | Y  | Y  | Y  | N  | N  | Y  | Y   | Y   | Y   | Y   | N   | Y   | N   | N   | N   | Y   | Y   | Y   | Y   | Y   | N   | N   | Y   | Y   | Y   | Y   | Y   | Y   | N   |
| Resistor  | N  | Y  | Y  | Y  | Y  | Y  | N  | N  | Y  | Y   | Y   | N   | N   | N   | Y   | N   | N   | N   | Y   | Y   | Y   | Y   | Y   | N   | N   | Y   | Y   | Y   | Y   | Y   | Y   | N   |
| Power     | N  | N  | N  | N  | N  | N  | Y  | N  | N  | N   | N   | N   | N   | Y   | N   | N   | N   | Y   | N   | N   | N   | N   | N   | N   | N   | N   | N   | N   | N   | N   | N   | N   |

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**Figure 7. Configuration 2**

**Table 4. Configuration 2 (Device EP016 and EP016A)**

| Device    | J1 | J2 | J3 | J4 | J5 | J6 | J7 | J8 | J9 | J10 | J11 | J12 | J13 | J14 | J15 | J16 | J17 | J18 | J19 | J20 | J21 | J22 | J23 | J24 | J25 | J26 | J27 | J28 | J29 | J30 | J31 | J32 |
|-----------|----|----|----|----|----|----|----|----|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| Pin #     | 1  | 2  | 3  | 4  | 5  | 6  | 7  | 8  | 9  | 10  | 11  | 12  | 13  | 14  | 15  | 16  | 17  | 18  | 19  | 20  | 21  | 22  | 23  | 24  | 25  | 26  | 27  | 28  | 29  | 30  | 31  | 32  |
| Connector | N  | Y  | Y  | Y  | Y  | Y  | Y  | N  | N  | Y   | Y   | Y   | N   | Y   | Y   | Y   | Y   | Y   | Y   | Y   | Y   | Y   | Y   | Y   | Y   | Y   | Y   | N   | Y   | Y   | Y   | N   |
| Resistor  | N  | N  | N  | N  | N  | N  | Y  | N  | N  | N   | N   | N   | N   | Y   | Y   | Y   | Y   | Y   | Y   | Y   | Y   | Y   | Y   | N   | Y   | Y   | Y   | N   | N   | N   | N   | N   |
| Power     | Y  | N  | N  | N  | N  | N  | N  | Y  | Y  | N   | N   | N   | Y   | N   | N   | N   | N   | N   | N   | N   | N   | N   | N   | N   | N   | N   | N   | Y   | N   | N   | N   | Y   |

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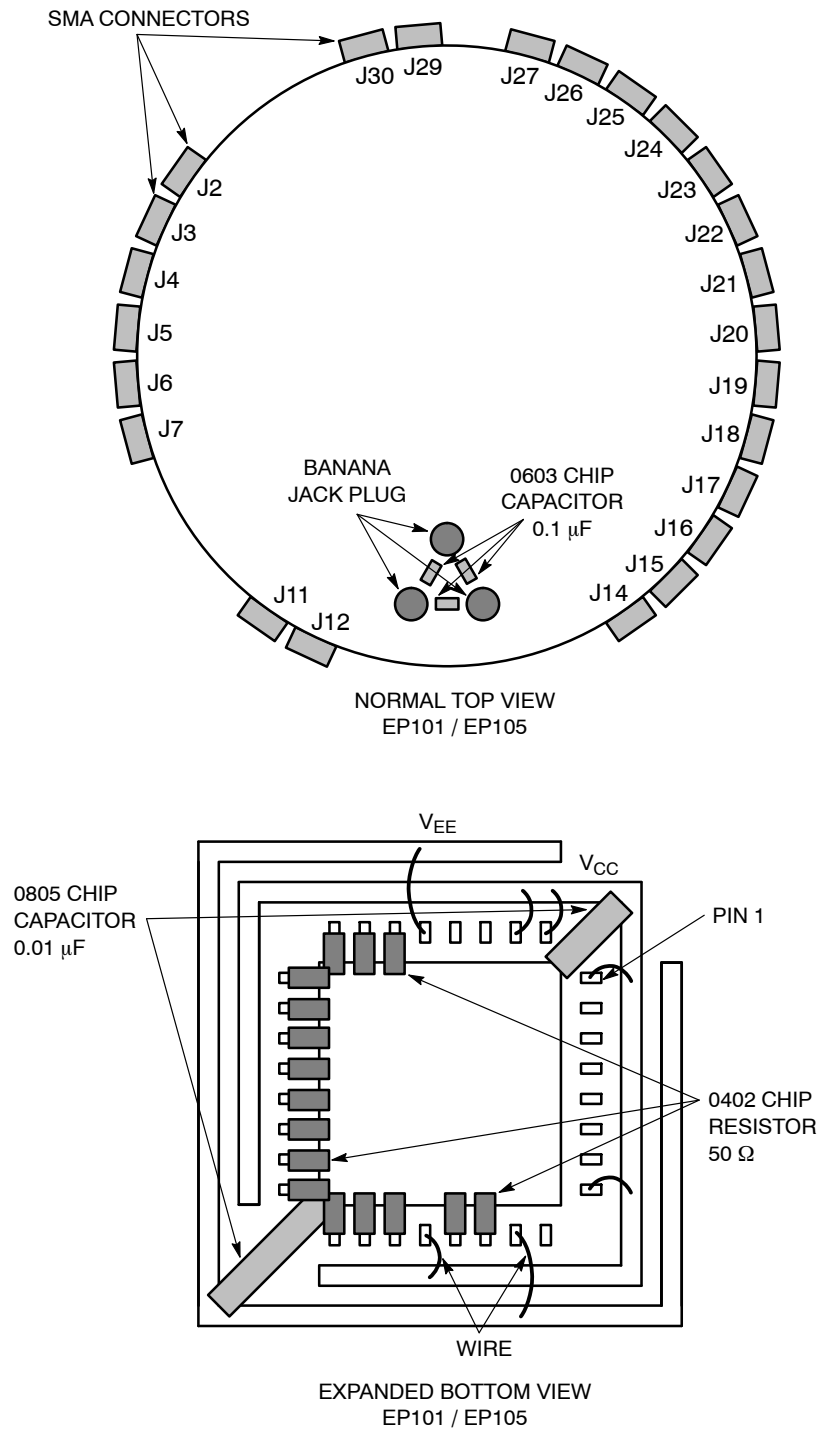


Figure 8. Configuration 3

Table 5. Configuration 3 (Device EP101 and EP105)

| Device    | J1 | J2 | J3 | J4 | J5 | J6 | J7 | J8 | J9 | J10 | J11 | J12 | J13 | J14 | J15 | J16 | J17 | J18 | J19 | J20 | J21 | J22 | J23 | J24 | J25 | J26 | J27 | J28 | J29 | J30 | J31 | J32 |
|-----------|----|----|----|----|----|----|----|----|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| Pin #     | 1  | 2  | 3  | 4  | 5  | 6  | 7  | 8  | 9  | 10  | 11  | 12  | 13  | 14  | 15  | 16  | 17  | 18  | 19  | 20  | 21  | 22  | 23  | 24  | 25  | 26  | 27  | 28  | 29  | 30  | 31  | 32  |
| Connector | N  | Y  | Y  | Y  | Y  | Y  | Y  | N  | N  | N   | Y   | Y   | N   | Y   | Y   | Y   | Y   | Y   | Y   | Y   | Y   | Y   | Y   | Y   | Y   | Y   | Y   | N   | Y   | Y   | N   | N   |
| Resistor  | N  | N  | N  | N  | N  | N  | N  | N  | N  | N   | Y   | Y   | N   | Y   | Y   | Y   | Y   | Y   | Y   | Y   | Y   | Y   | Y   | Y   | Y   | Y   | Y   | N   | N   | N   | N   | N   |
| Power     | Y  | N  | N  | N  | N  | N  | N  | Y  | N  | Y   | N   | N   | Y   | N   | N   | N   | N   | N   | N   | N   | N   | N   | N   | N   | N   | N   | N   | Y   | N   | N   | Y   | Y   |

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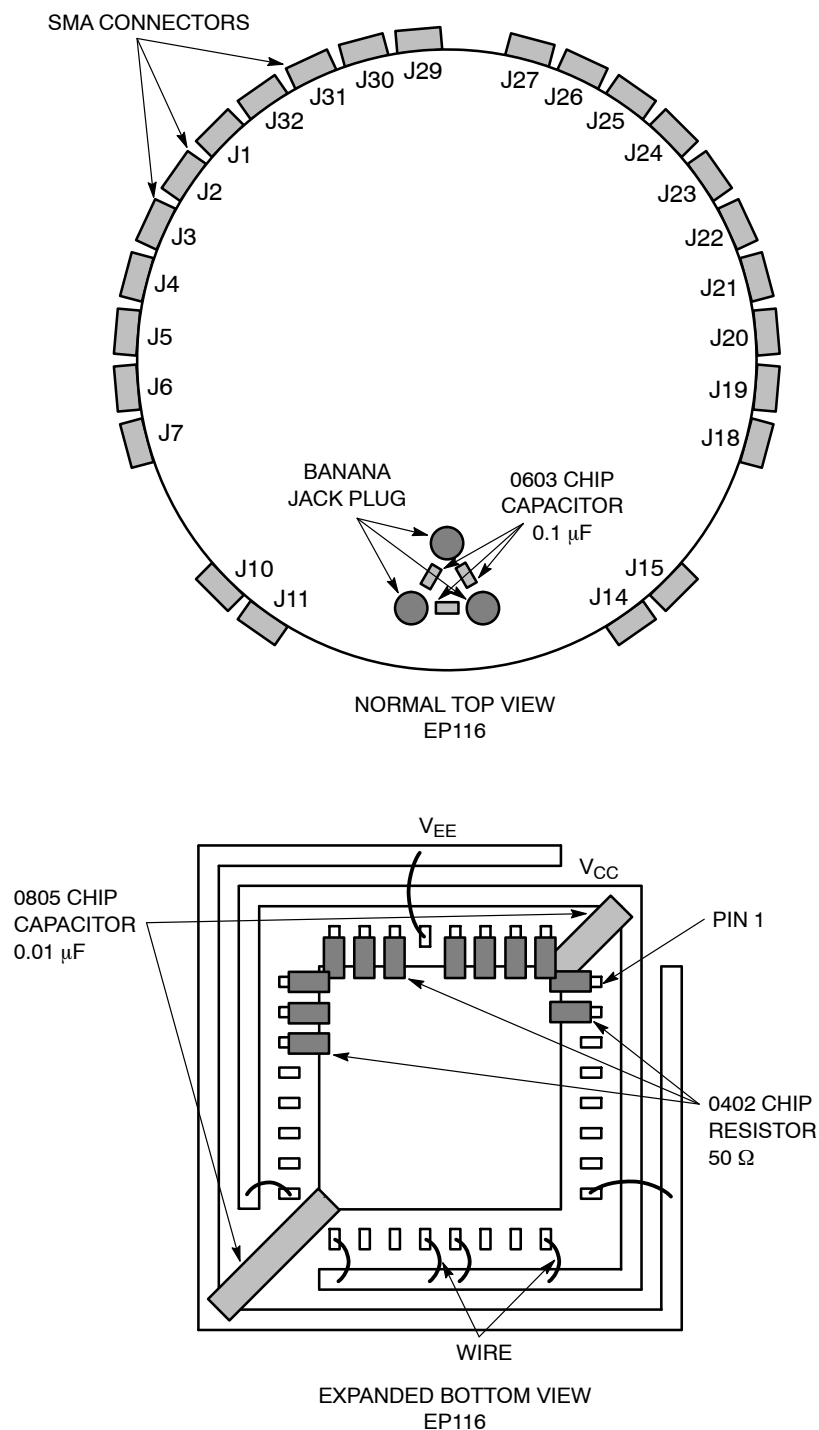


Figure 9. Configuration 4

Table 6. Configuration 4 (Device EP116)

| Device    | J1 | J2 | J3 | J4 | J5 | J6 | J7 | J8 | J9 | J10 | J11 | J12 | J13 | J14 | J15 | J16 | J17 | J18 | J19 | J20 | J21 | J22 | J23 | J24 | J25 | J26 | J27 | J28 | J29 | J30 | J31 | J32 |
|-----------|----|----|----|----|----|----|----|----|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| Pin #     | 1  | 2  | 3  | 4  | 5  | 6  | 7  | 8  | 9  | 10  | 11  | 12  | 13  | 14  | 15  | 16  | 17  | 18  | 19  | 20  | 21  | 22  | 23  | 24  | 25  | 26  | 27  | 28  | 29  | 30  | 31  | 32  |
| Connector | Y  | Y  | Y  | Y  | Y  | Y  | Y  | N  | N  | Y   | Y   | N   | N   | Y   | Y   | N   | N   | Y   | Y   | Y   | Y   | Y   | Y   | Y   | Y   | Y   | Y   | N   | Y   | Y   | Y   | Y   |
| Resistor  | Y  | Y  | N  | N  | N  | N  | N  | N  | N  | N   | N   | N   | N   | N   | N   | N   | N   | N   | N   | N   | N   | Y   | Y   | Y   | Y   | Y   | Y   | N   | Y   | Y   | Y   | Y   |
| Power     | N  | N  | N  | N  | N  | N  | N  | Y  | Y  | N   | N   | Y   | Y   | N   | N   | Y   | Y   | N   | N   | N   | N   | N   | N   | N   | N   | N   | N   | Y   | N   | N   | N   | N   |

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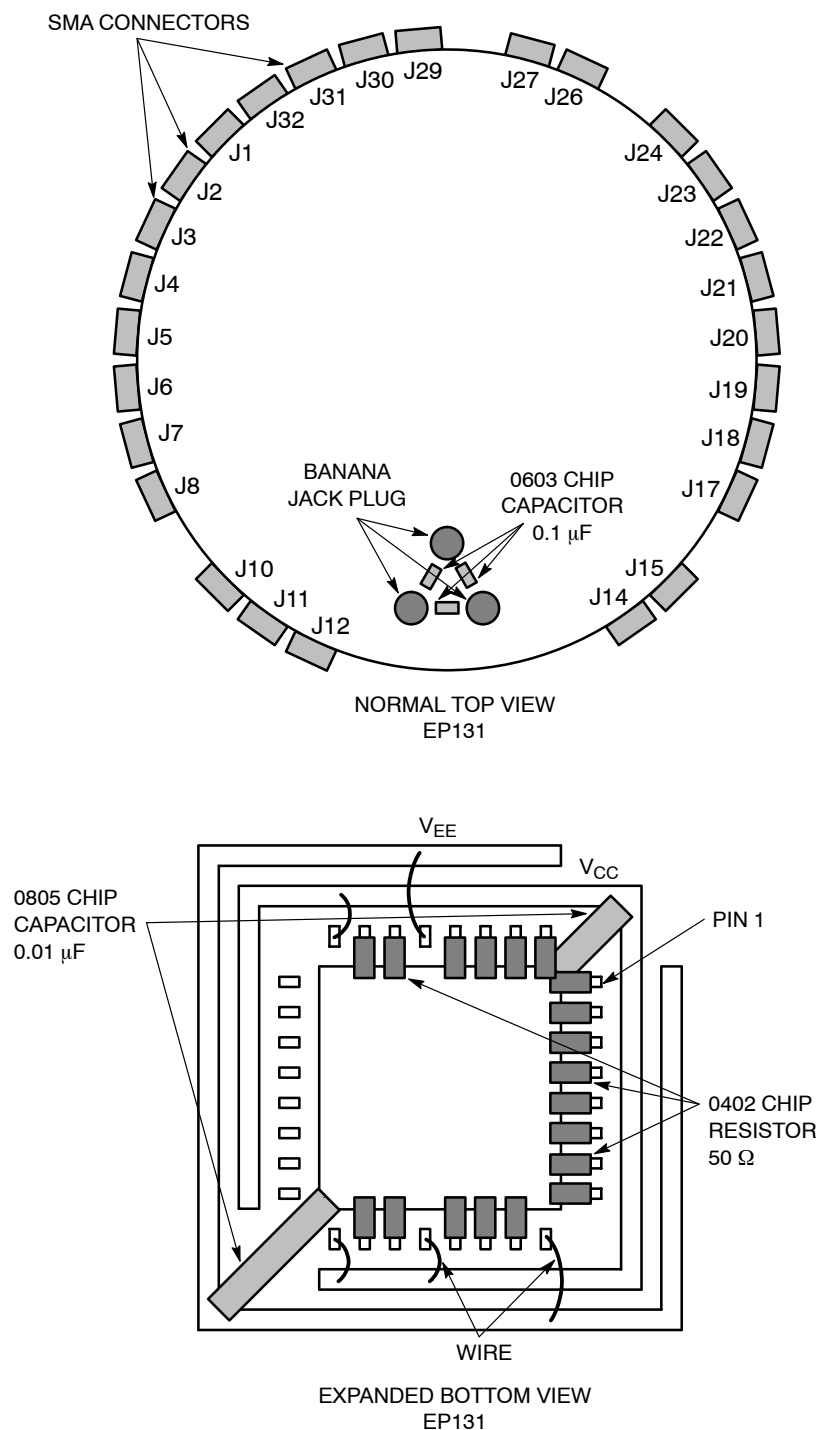


Figure 10. Configuration 5

Table 7. Configuration 5 (Device EP131)

| Device    | J1 | J2 | J3 | J4 | J5 | J6 | J7 | J8 | J9 | J10 | J11 | J12 | J13 | J14 | J15 | J16 | J17 | J18 | J19 | J20 | J21 | J22 | J23 | J24 | J25 | J26 | J27 | J28 | J29 | J30 | J31 | J32 |   |
|-----------|----|----|----|----|----|----|----|----|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|---|
| Pin #     | 1  | 2  | 3  | 4  | 5  | 6  | 7  | 8  | 9  | 10  | 11  | 12  | 13  | 14  | 15  | 16  | 17  | 18  | 19  | 20  | 21  | 22  | 23  | 24  | 25  | 26  | 27  | 28  | 29  | 30  | 31  | 32  |   |
| Connector | Y  | Y  | Y  | Y  | Y  | Y  | Y  | Y  | N  | Y   | Y   | Y   | N   | Y   | Y   | N   | Y   | Y   | Y   | Y   | Y   | Y   | Y   | Y   | N   | Y   | Y   | N   | Y   | Y   | Y   | Y   |   |
| Resistor  | Y  | Y  | Y  | Y  | Y  | Y  | Y  | Y  | N  | Y   | Y   | Y   | N   | Y   | Y   | N   | N   | N   | N   | N   | N   | N   | N   | N   | N   | N   | Y   | Y   | N   | Y   | Y   | Y   | Y |
| Power     | N  | N  | N  | N  | N  | N  | N  | N  | Y  | N   | N   | N   | Y   | N   | N   | Y   | N   | N   | N   | N   | N   | N   | N   | N   | N   | Y   | N   | N   | Y   | N   | N   | N   | N |

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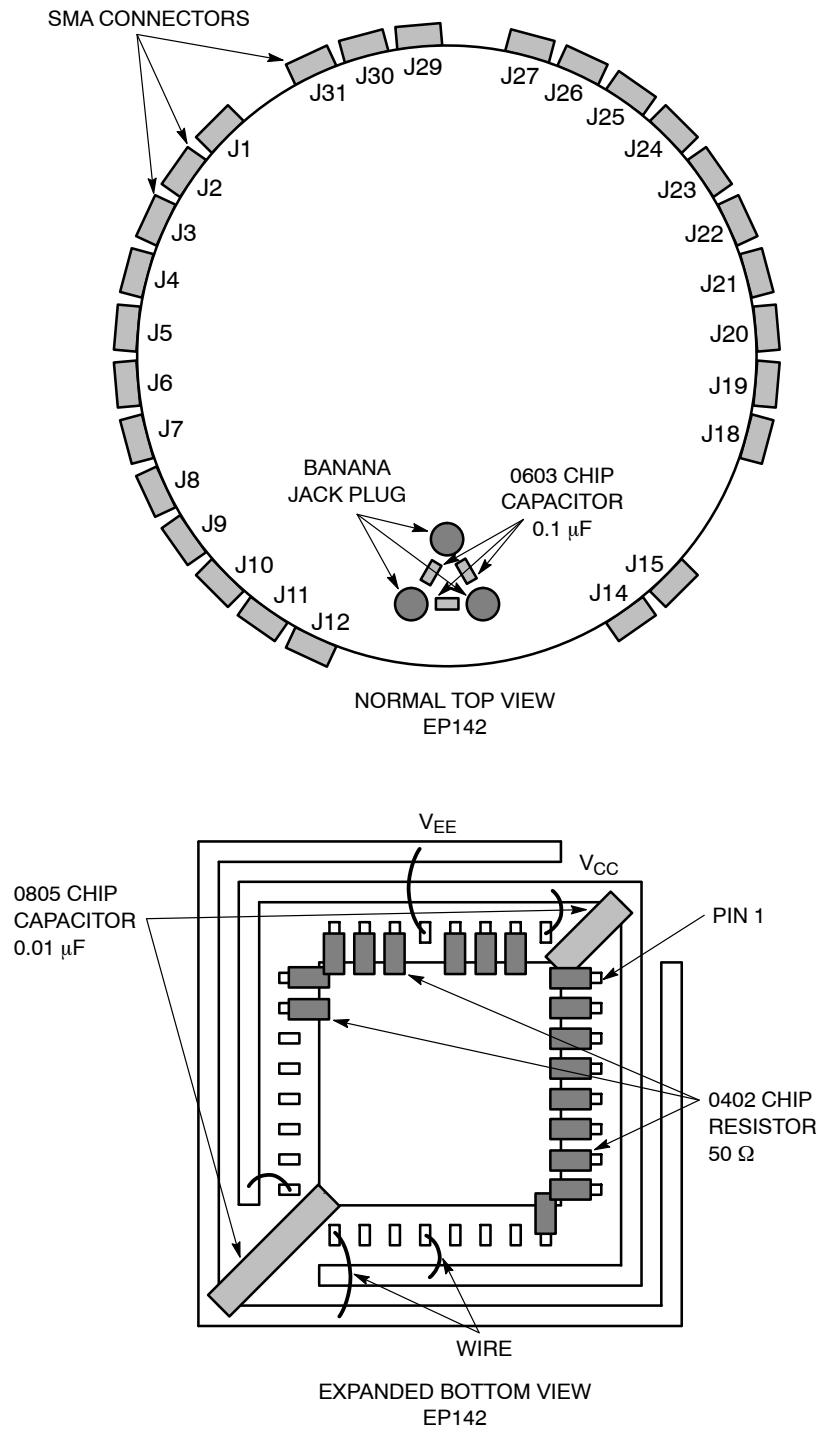


Figure 11. Configuration 6

Table 8. Configuration 6 (Device EP142)

| Device    | J1 | J2 | J3 | J4 | J5 | J6 | J7 | J8 | J9 | J10 | J11 | J12 | J13 | J14 | J15 | J16 | J17 | J18 | J19 | J20 | J21 | J22 | J23 | J24 | J25 | J26 | J27 | J28 | J29 | J30 | J31 | J32 |
|-----------|----|----|----|----|----|----|----|----|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| Pin #     | 1  | 2  | 3  | 4  | 5  | 6  | 7  | 8  | 9  | 10  | 11  | 12  | 13  | 14  | 15  | 16  | 17  | 18  | 19  | 20  | 21  | 22  | 23  | 24  | 25  | 26  | 27  | 28  | 29  | 30  | 31  | 32  |
| Connector | Y  | Y  | Y  | Y  | Y  | Y  | Y  | Y  | Y  | Y   | Y   | Y   | N   | N   | N   | N   | N   | Y   | Y   | Y   | Y   | Y   | Y   | Y   | Y   | Y   | Y   | N   | Y   | Y   | Y   | N   |
| Resistor  | Y  | Y  | Y  | Y  | Y  | Y  | Y  | Y  | Y  | N   | N   | N   | N   | N   | N   | N   | N   | N   | N   | N   | N   | N   | Y   | Y   | Y   | Y   | Y   | N   | Y   | Y   | Y   | N   |
| Power     | N  | N  | N  | N  | N  | N  | N  | N  | N  | N   | N   | N   | Y   | Y   | Y   | Y   | Y   | N   | N   | N   | N   | N   | N   | N   | N   | N   | N   | Y   | N   | N   | N   | Y   |

## ECLLQFP32EVB

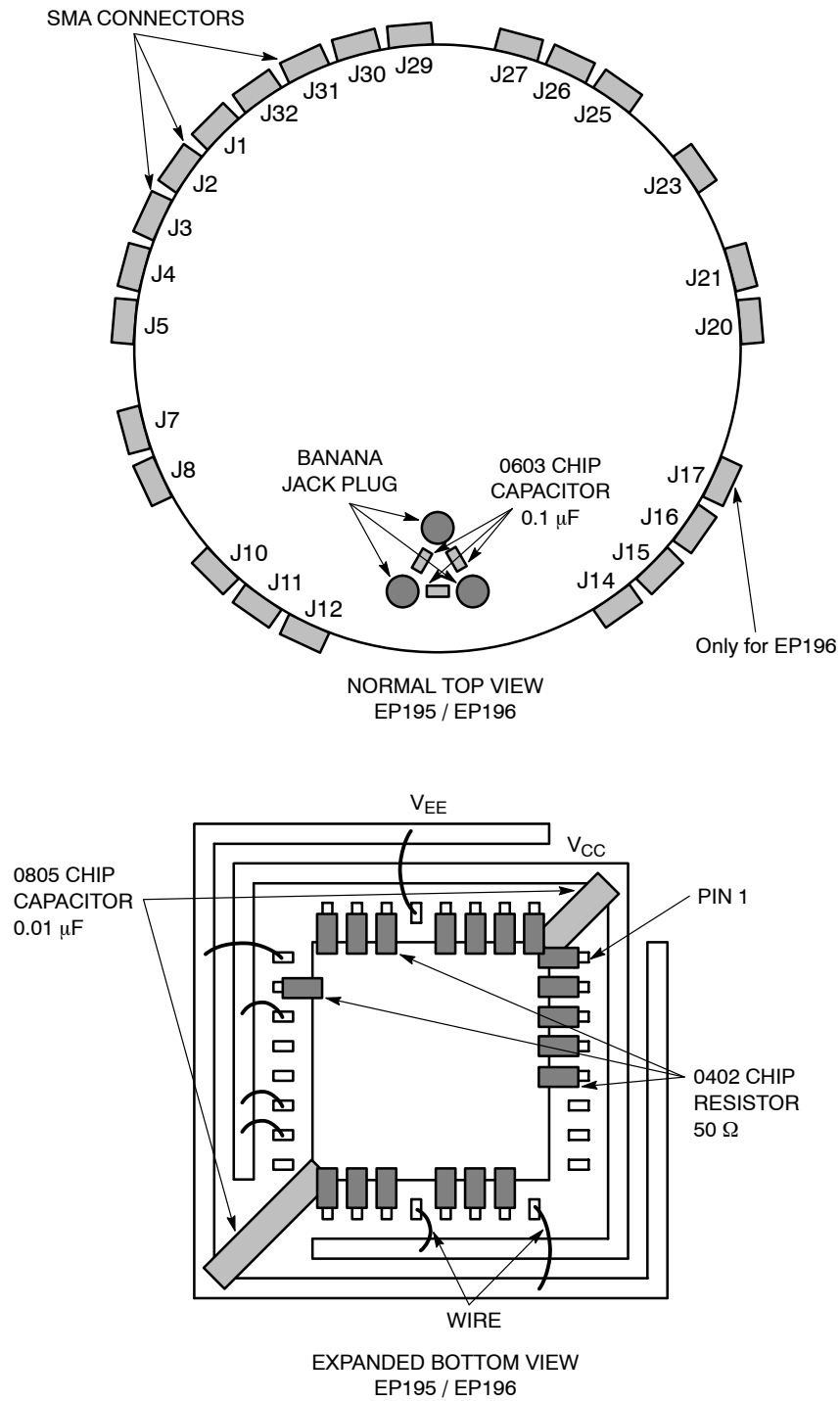


Figure 12. Configuration 7

Table 9. Configuration 7 (Device EP195 and EP196)

| Device    | J1 | J2 | J3 | J4 | J5 | J6 | J7 | J8 | J9 | J10 | J11 | J12 | J13 | J14 | J15 | J16 | J17 | J18 | J19 | J20 | J21 | J22 | J23 | J24 | J25 | J26 | J27 | J28 | J29 | J30 | J31 | J32 |
|-----------|----|----|----|----|----|----|----|----|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| Pin #     | 1  | 2  | 3  | 4  | 5  | 6  | 7  | 8  | 9  | 10  | 11  | 12  | 13  | 14  | 15  | 16  | 17  | 18  | 19  | 20  | 21  | 22  | 23  | 24  | 25  | 26  | 27  | 28  | 29  | 30  | 31  | 32  |
| Connector | Y  | Y  | Y  | Y  | Y  | Y  | Y  | Y  | N  | Y   | Y   | Y   | Y   | N   | Y   | Y   | *   | N   | N   | Y   | Y   | N   | Y   | N   | Y   | Y   | Y   | N   | Y   | Y   | Y   | Y   |
| Resistor  | Y  | Y  | Y  | Y  | Y  | N  | N  | N  | N  | Y   | Y   | Y   | Y   | N   | Y   | Y   | N   | N   | N   | N   | N   | N   | Y   | N   | Y   | Y   | Y   | N   | Y   | Y   | Y   | Y   |
| Power     | N  | N  | N  | N  | N  | N  | N  | N  | Y  | N   | N   | N   | N   | Y   | N   | N   | N   | Y   | Y   | N   | N   | Y   | N   | Y   | N   | N   | N   | Y   | N   | N   | N   | N   |

\* Only for EP196

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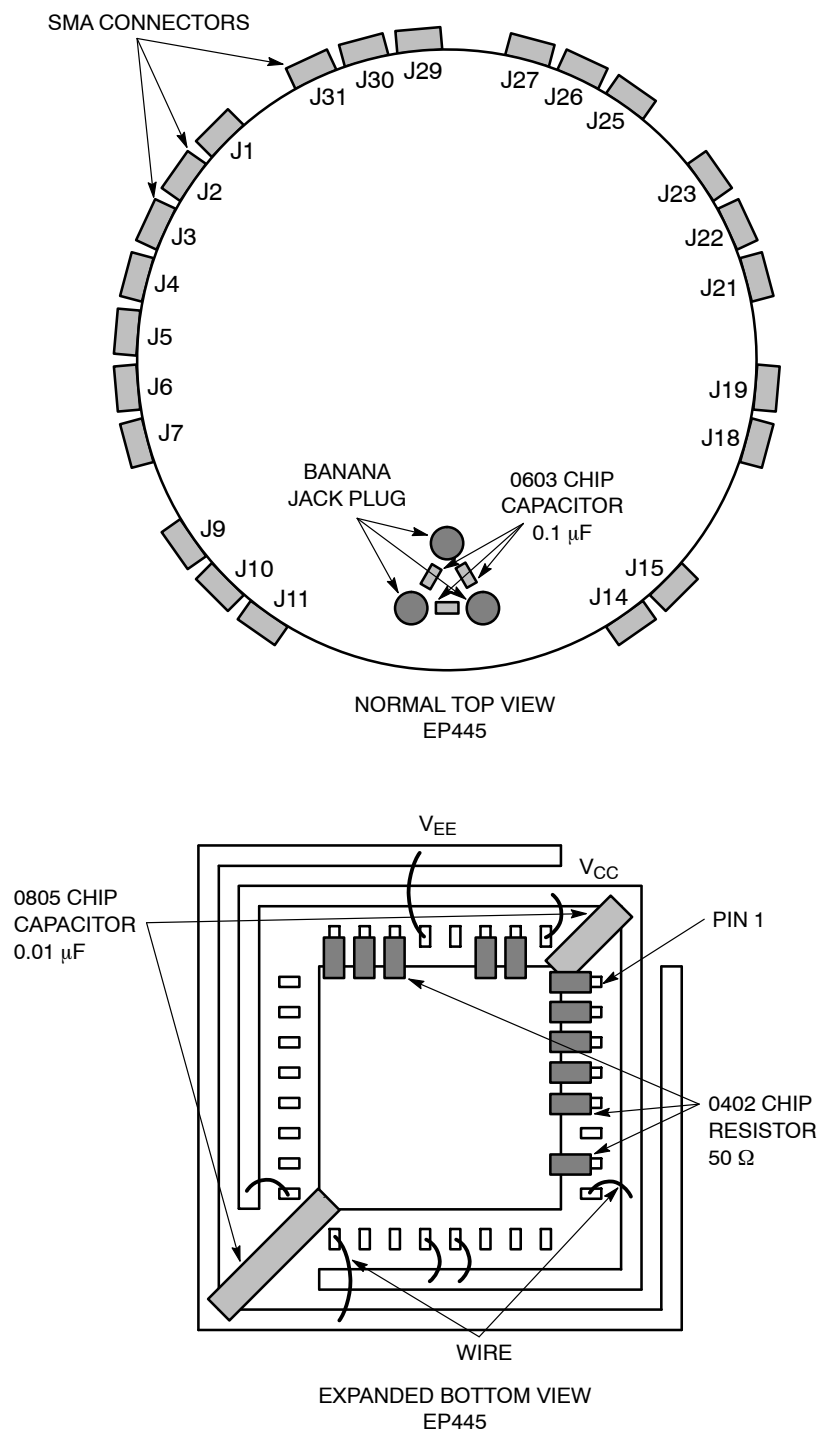


Figure 13. Configuration 8

Table 10. Configuration 8 (Device EP445)

| Device    | J1 | J2 | J3 | J4 | J5 | J6 | J7 | J8 | J9 | J10 | J11 | J12 | J13 | J14 | J15 | J16 | J17 | J18 | J19 | J20 | J21 | J22 | J23 | J24 | J25 | J26 | J27 | J28 | J29 | J30 | J31 | J32 |
|-----------|----|----|----|----|----|----|----|----|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| Pin #     | 1  | 2  | 3  | 4  | 5  | 6  | 7  | 8  | 9  | 10  | 11  | 12  | 13  | 14  | 15  | 16  | 17  | 18  | 19  | 20  | 21  | 22  | 23  | 24  | 25  | 26  | 27  | 28  | 29  | 30  | 31  | 32  |
| Connector | Y  | Y  | Y  | Y  | Y  | Y  | Y  | Y  | Y  | Y   | Y   | N   | N   | Y   | Y   | N   | N   | Y   | Y   | N   | Y   | Y   | Y   | N   | Y   | Y   | Y   | N   | Y   | Y   | Y   | N   |
| Resistor  | Y  | Y  | Y  | Y  | Y  | N  | Y  | N  | N  | N   | N   | N   | N   | N   | N   | N   | N   | N   | N   | N   | N   | Y   | Y   | N   | Y   | Y   | Y   | N   | N   | Y   | Y   | N   |
| Power     | N  | N  | N  | N  | N  | N  | N  | N  | N  | N   | N   | Y   | Y   | N   | N   | Y   | Y   | N   | N   | Y   | N   | N   | N   | Y   | N   | N   | N   | Y   | N   | N   | N   | Y   |

## ECLLQFP32EVB

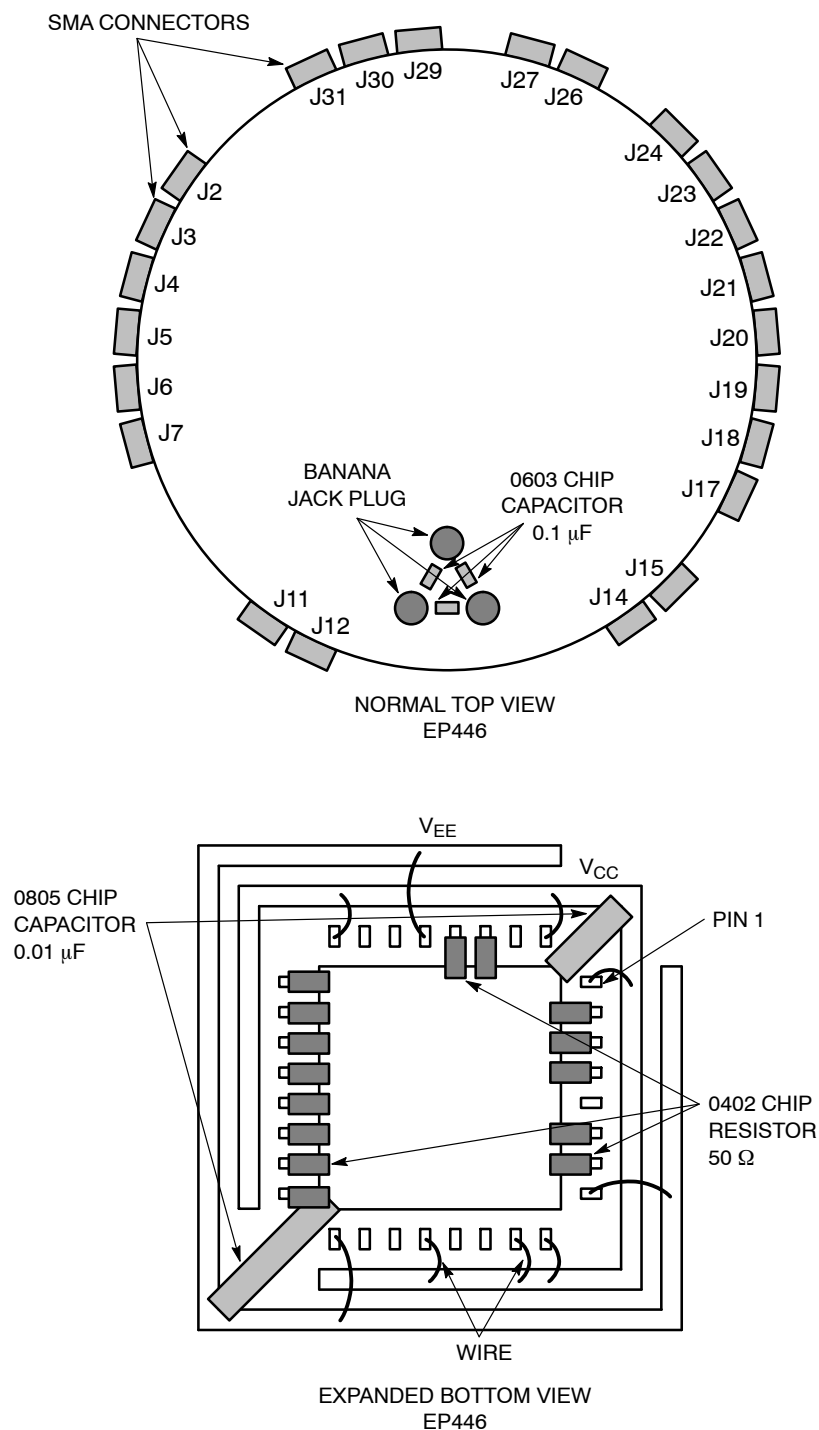


Figure 14. Configuration 9

Table 11. Configuration 9 (Device EP446)

| Device    | J1 | J2 | J3 | J4 | J5 | J6 | J7 | J8 | J9 | J10 | J11 | J12 | J13 | J14 | J15 | J16 | J17 | J18 | J19 | J20 | J21 | J22 | J23 | J24 | J25 | J26 | J27 | J28 | J29 | J30 | J31 | J32 |   |
|-----------|----|----|----|----|----|----|----|----|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|---|
| Pin #     | 1  | 2  | 3  | 4  | 5  | 6  | 7  | 8  | 9  | 10  | 11  | 12  | 13  | 14  | 15  | 16  | 17  | 18  | 19  | 20  | 21  | 22  | 23  | 24  | 25  | 26  | 27  | 28  | 29  | 30  | 31  | 32  |   |
| Connector | N  | Y  | Y  | Y  | Y  | Y  | Y  | N  | N  | N   | Y   | Y   | N   | Y   | Y   | N   | Y   | Y   | Y   | Y   | Y   | Y   | Y   | Y   | N   | Y   | Y   | N   | Y   | Y   | Y   | N   |   |
| Resistor  | N  | Y  | Y  | Y  | N  | Y  | Y  | N  | N  | N   | N   | N   | N   | N   | N   | N   | Y   | Y   | Y   | Y   | Y   | Y   | Y   | Y   | N   | N   | N   | N   | Y   | Y   | N   | N   |   |
| Power     | Y  | N  | N  | N  | N  | N  | N  | Y  | Y  | Y   | N   | N   | Y   | N   | N   | Y   | N   | N   | N   | N   | N   | N   | N   | N   | N   | Y   | N   | N   | Y   | N   | N   | N   | Y |

## ECLLQFP32EVB

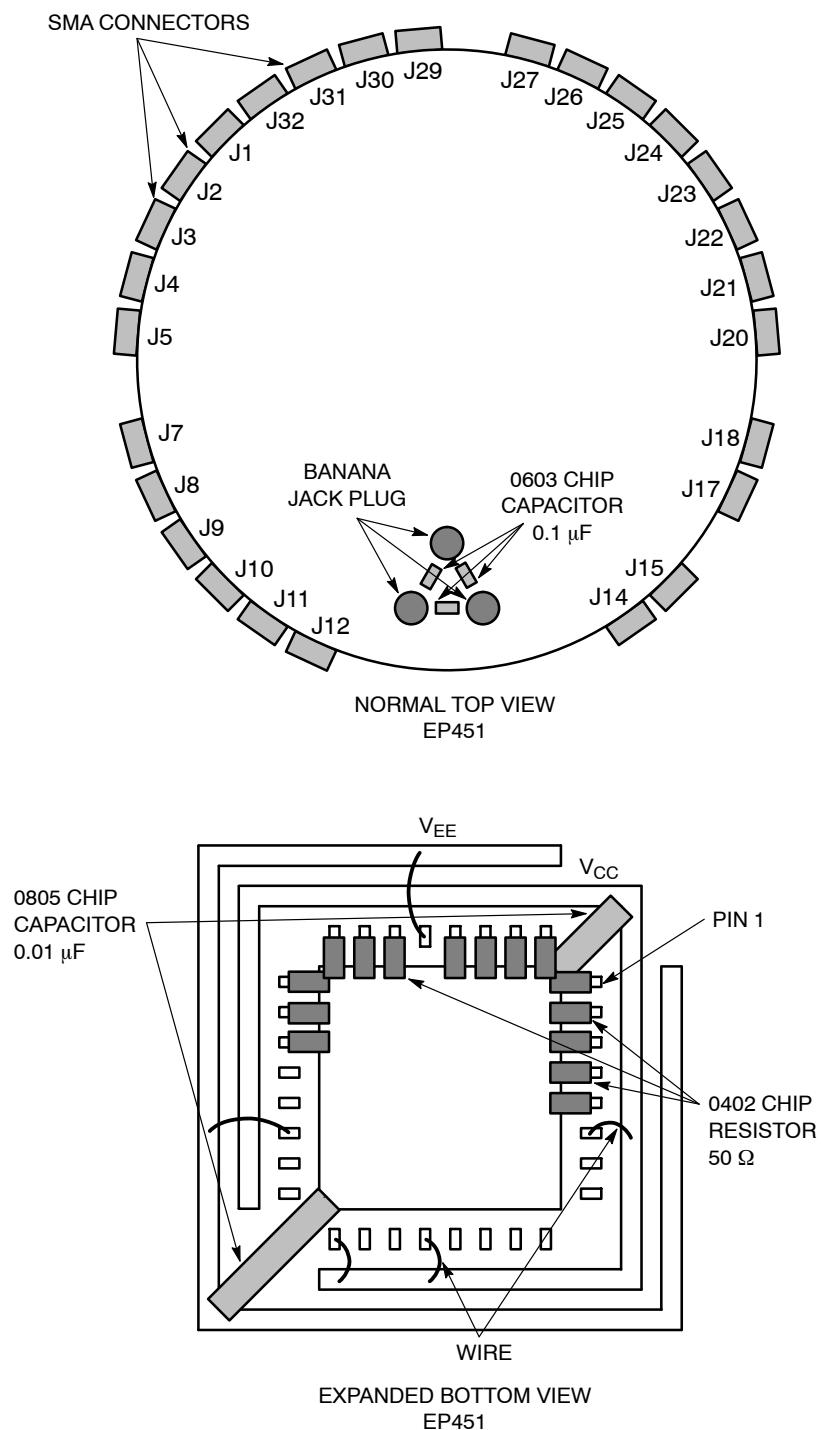


Figure 15. Configuration 10

Table 12. Configuration 10 (Device EP451)

| Device    | J1 | J2 | J3 | J4 | J5 | J6 | J7 | J8 | J9 | J10 | J11 | J12 | J13 | J14 | J15 | J16 | J17 | J18 | J19 | J20 | J21 | J22 | J23 | J24 | J25 | J26 | J27 | J28 | J29 | J30 | J31 | J32 |
|-----------|----|----|----|----|----|----|----|----|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|
| Pin #     | 1  | 2  | 3  | 4  | 5  | 6  | 7  | 8  | 9  | 10  | 11  | 12  | 13  | 14  | 15  | 16  | 17  | 18  | 19  | 20  | 21  | 22  | 23  | 24  | 25  | 26  | 27  | 28  | 29  | 30  | 31  | 32  |
| Connector | Y  | Y  | Y  | Y  | Y  | N  | Y  | Y  | Y  | Y   | Y   | Y   | N   | Y   | Y   | N   | Y   | Y   | N   | Y   | Y   | Y   | Y   | Y   | Y   | Y   | Y   | N   | Y   | Y   | Y   | Y   |
| Resistor  | Y  | Y  | Y  | Y  | Y  | N  | N  | N  | N  | N   | N   | N   | N   | N   | N   | N   | N   | N   | N   | N   | N   | Y   | Y   | Y   | Y   | Y   | Y   | N   | Y   | Y   | Y   | Y   |
| Power     | N  | N  | N  | N  | N  | Y  | N  | N  | N  | N   | N   | N   | Y   | N   | N   | Y   | N   | N   | Y   | N   | N   | N   | N   | N   | N   | N   | N   | Y   | N   | N   | N   | N   |

## ECLLQFP32EVB

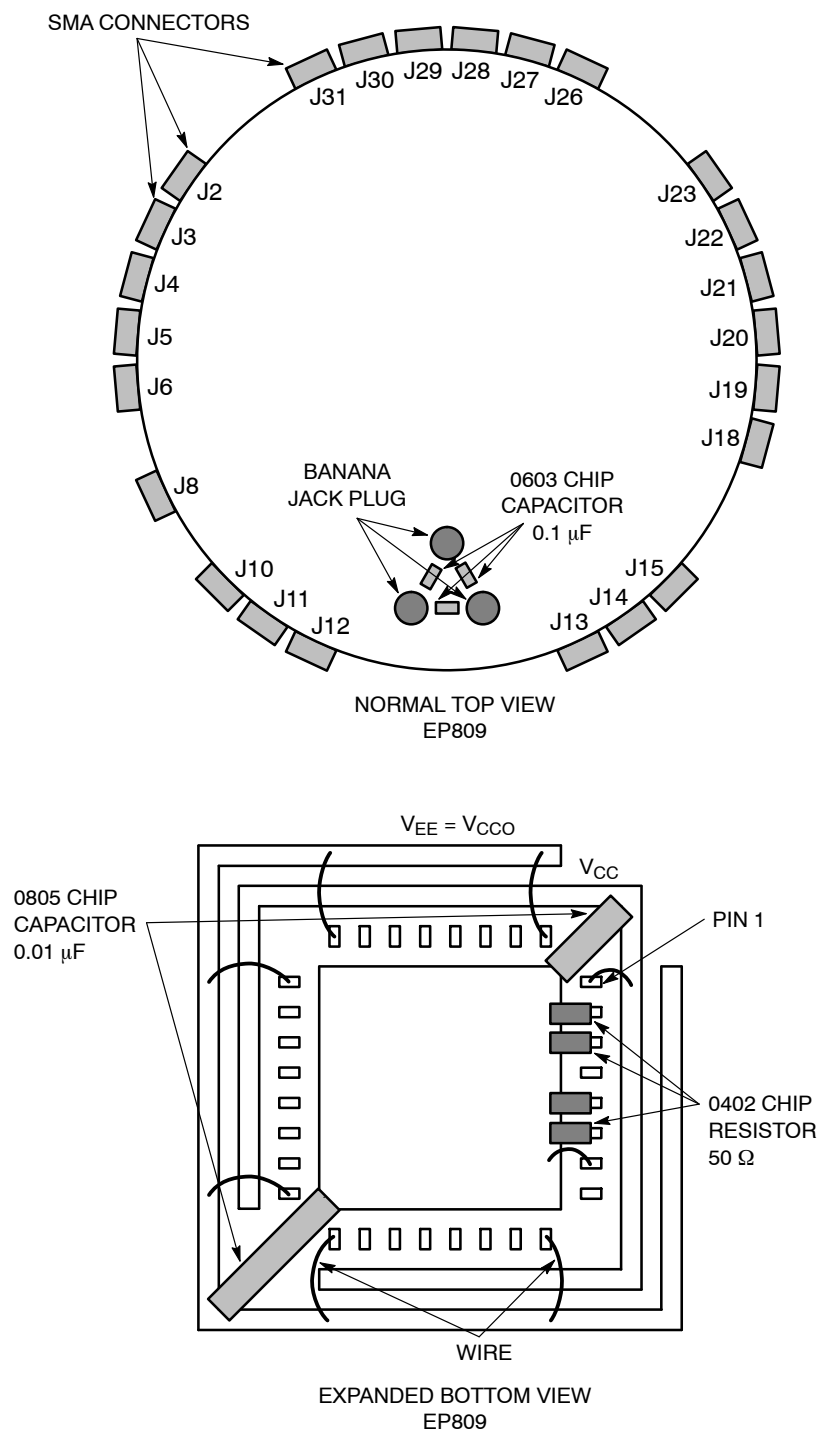
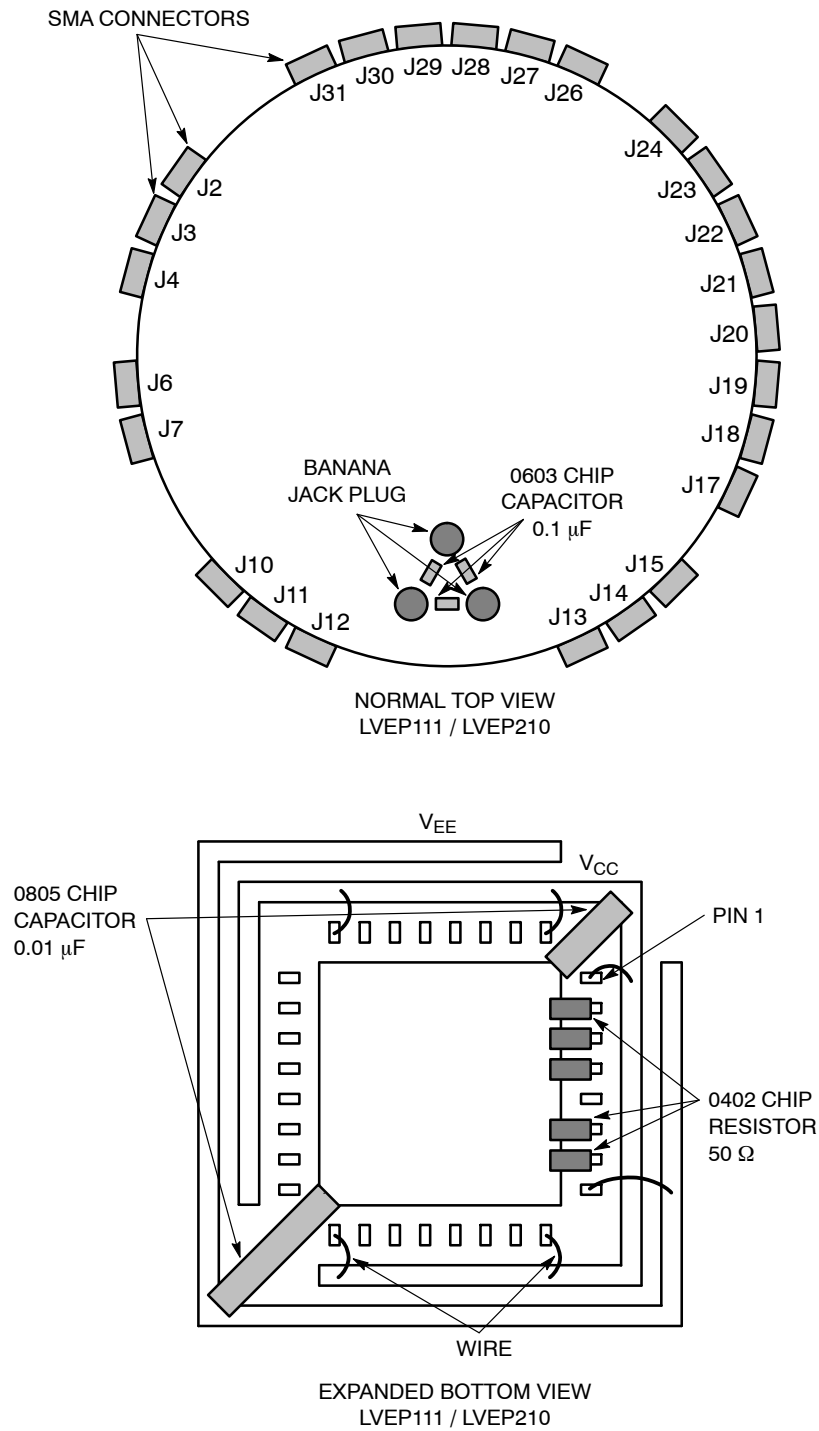


Figure 16. Configuration 11

Table 13. Configuration 11 (Device EP809)

| Device    | J1 | J2 | J3 | J4 | J5 | J6 | J7 | J8 | J9 | J10 | J11 | J12 | J13 | J14 | J15 | J16 | J17 | J18 | J19 | J20 | J21 | J22 | J23 | J24 | J25 | J26 | J27 | J28 | J29 | J30 | J31 | J32 |   |
|-----------|----|----|----|----|----|----|----|----|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|---|
| Pin #     | 1  | 2  | 3  | 4  | 5  | 6  | 7  | 8  | 9  | 10  | 11  | 12  | 13  | 14  | 15  | 16  | 17  | 18  | 19  | 20  | 21  | 22  | 23  | 24  | 25  | 26  | 27  | 28  | 29  | 30  | 31  | 32  |   |
| Connector | N  | Y  | Y  | Y  | Y  | Y  | N  | Y  | N  | Y   | Y   | Y   | Y   | Y   | Y   | N   | N   | Y   | Y   | Y   | Y   | Y   | N   | N   | N   | Y   | Y   | Y   | Y   | Y   | Y   | N   |   |
| Resistor  | N  | Y  | Y  | Y  | Y  | Y  | N  | Y  | N  | N   | N   | N   | N   | N   | N   | N   | N   | N   | N   | N   | N   | N   | N   | N   | N   | N   | N   | N   | N   | N   | N   | N   | N |
| Power     | Y  | N  | N  | N  | N  | N  | Y  | N  | Y  | N   | N   | N   | N   | N   | N   | Y   | Y   | N   | N   | N   | N   | N   | N   | Y   | Y   | N   | N   | N   | N   | N   | N   | N   | Y |

## ECLLQFP32EVB



**Figure 17. Configuration 12**

**Table 14. Configuration 12 (Device LVEP111 and LVEP210)**

| Device    | J1 | J2 | J3 | J4 | J5 | J6 | J7 | J8 | J9 | J10 | J11 | J12 | J13 | J14 | J15 | J16 | J17 | J18 | J19 | J20 | J21 | J22 | J23 | J24 | J25 | J26 | J27 | J28 | J29 | J30 | J31 | J32 |   |
|-----------|----|----|----|----|----|----|----|----|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|---|
| Pin #     | 1  | 2  | 3  | 4  | 5  | 6  | 7  | 8  | 9  | 10  | 11  | 12  | 13  | 14  | 15  | 16  | 17  | 18  | 19  | 20  | 21  | 22  | 23  | 24  | 25  | 26  | 27  | 28  | 29  | 30  | 31  | 32  |   |
| Connector | N  | Y  | Y  | Y  | Y  | Y  | Y  | N  | N  | Y   | Y   | Y   | Y   | Y   | Y   | N   | Y   | Y   | Y   | Y   | Y   | Y   | Y   | Y   | N   | Y   | Y   | Y   | Y   | Y   | Y   | N   |   |
| Resistor  | N  | Y  | Y  | Y  | N  | Y  | Y  | N  | N  | N   | N   | N   | N   | N   | N   | N   | N   | N   | N   | N   | N   | N   | N   | N   | N   | N   | N   | N   | N   | N   | N   | N   | N |
| Power     | Y  | N  | N  | N  | N  | N  | N  | Y  | Y  | N   | N   | N   | N   | N   | N   | Y   | N   | N   | N   | N   | N   | N   | N   | N   | N   | Y   | N   | N   | N   | N   | N   | N   | Y |

\* Pin 2 is No Connect for LVEP210

## ECLLQFP32EVB

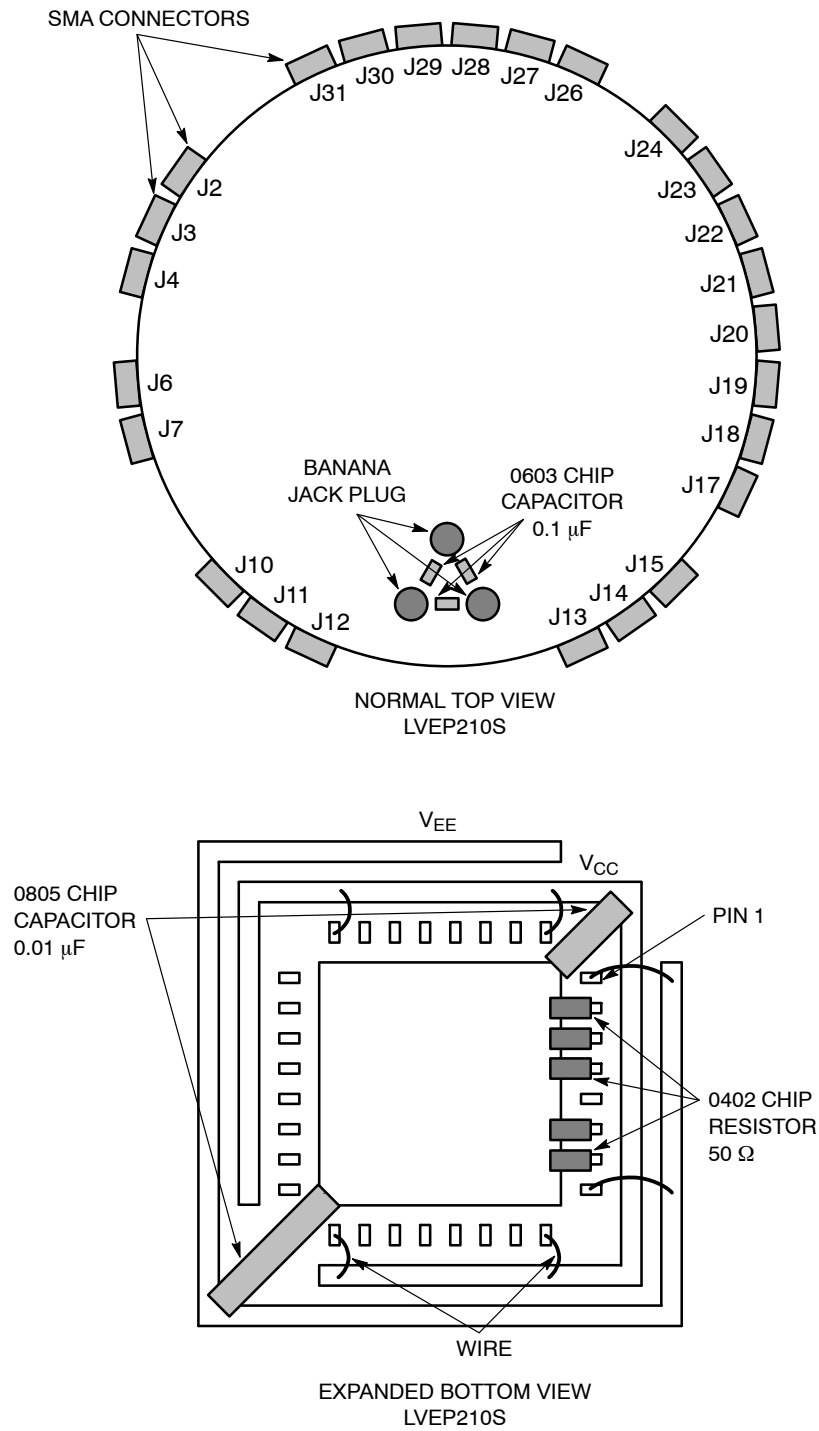


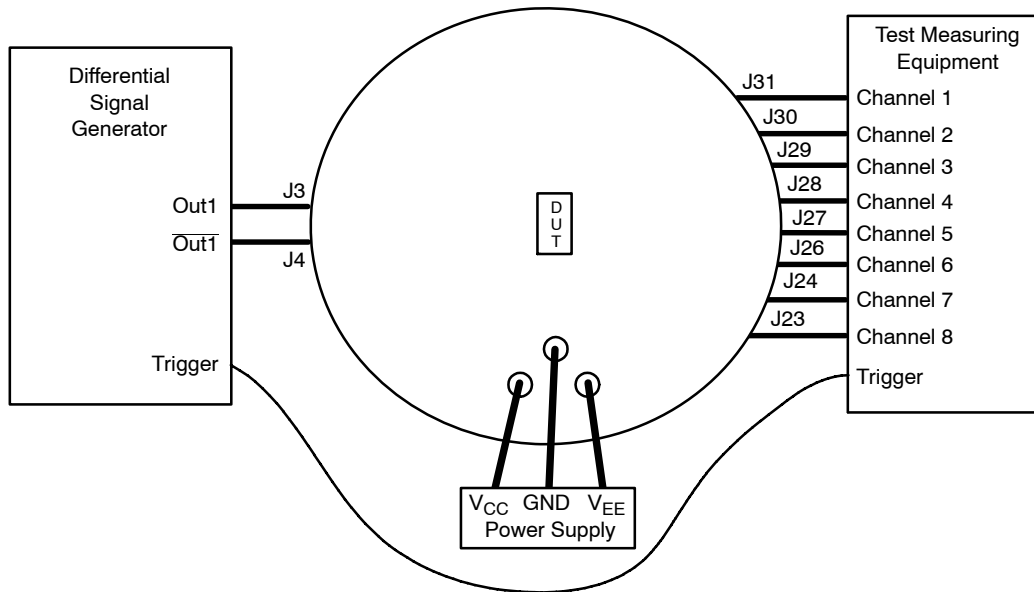
Figure 18. Configuration 13

Table 15. Configuration 13 (Device LVEP210S)

| Device    | J1 | J2 | J3 | J4 | J5 | J6 | J7 | J8 | J9 | J10 | J11 | J12 | J13 | J14 | J15 | J16 | J17 | J18 | J19 | J20 | J21 | J22 | J23 | J24 | J25 | J26 | J27 | J28 | J29 | J30 | J31 | J32 |   |
|-----------|----|----|----|----|----|----|----|----|----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|-----|---|
| Pin #     | 1  | 2  | 3  | 4  | 5  | 6  | 7  | 8  | 9  | 10  | 11  | 12  | 13  | 14  | 15  | 16  | 17  | 18  | 19  | 20  | 21  | 22  | 23  | 24  | 25  | 26  | 27  | 28  | 29  | 30  | 31  | 32  |   |
| Connector | N  | Y  | Y  | Y  | Y  | Y  | Y  | N  | N  | Y   | Y   | Y   | Y   | Y   | Y   | N   | Y   | Y   | Y   | Y   | Y   | Y   | Y   | Y   | N   | Y   | Y   | Y   | Y   | Y   | Y   | N   |   |
| Resistor  | N  | Y  | Y  | Y  | Y  | Y  | Y  | N  | N  | N   | N   | N   | N   | N   | N   | N   | N   | N   | N   | N   | N   | N   | N   | N   | N   | N   | N   | N   | N   | N   | N   | N   | N |
| Power     | Y  | N  | N  | N  | N  | N  | N  | Y  | Y  | N   | N   | N   | N   | N   | N   | Y   | N   | N   | N   | N   | N   | N   | N   | N   | Y   | N   | N   | N   | N   | N   | N   | N   | Y |

# ECLLQFP32EVB

## LAB SETUP



**Figure 19. Example of Standard Lab Setup (Configuration 12)**

1. Connect appropriate power supplies to  $V_{CC}$ ,  $V_{EE}$ , and GND.

For standard ECL lab setup and test, a split (dual) power supply is required enabling the 50  $\Omega$  internal impedance in the oscilloscope to be used as a termination of the ECL signals ( $V_{TT} = V_{CC} - 2.0$  V, in split power supply setup,  $V_{TT}$  is the system ground,  $V_{CC}$  is 2.0 V, and  $V_{EE}$  is -3.0 V or -1.3 V; see Table 16).

2. Connect a signal generator to the input SMA connectors. Setup input signal according to the device data sheet.

3. Connect a test measurement device on the device output SMA connectors.

NOTE: The test measurement device must contain 50  $\Omega$  termination.

**Table 16. Power Supply Levels**

| Power Supply | $V_{CC}$ | $V_{EE}$ | GND   |
|--------------|----------|----------|-------|
| 5.0 V        | 2.0 V    | -3.0 V   | 0.0 V |
| 3.3 V        | 2.0 V    | -1.3 V   | 0.0 V |
| 2.5 V        | 2.0 V    | -0.5 V   | 0.0 V |

**Table 17. Bill of Materials**

| Components       | Manufacturer         | Description                                                  | Part Number   | Web Site                                                                            |
|------------------|----------------------|--------------------------------------------------------------|---------------|-------------------------------------------------------------------------------------|
| SMA Connector    | Johnson Components*  | SMA Connector, Side Launch, Gold Plated                      | 142-0701-851  | <a href="http://www.johnsoncomponents.com">http://www.johnsoncomponents.com</a>     |
| Banana Jack      | Keystone*            | Standard Jack                                                | 6096          | <a href="http://www.keyelco.com">http://www.keyelco.com</a>                         |
|                  |                      | Miniature Jack                                               | 6090          |                                                                                     |
| Chip Capacitor   | Johanson Dielectric* | 0603/0805/1205 0.01 $\mu$ F Chip Capacitor                   | -             | <a href="http://www.johansondielectrics.com">http://www.johansondielectrics.com</a> |
|                  |                      | 0603/0805/1205 0.1 $\mu$ F Chip Capacitor                    | -             |                                                                                     |
| Chip Resistor    | Panasonic*           | 0402 50 $\Omega$ $\pm$ 1% Precision Think Film Chip Resistor | ERJ-2RKF49R9X | <a href="http://www.panasonic.com">http://www.panasonic.com</a>                     |
| Evaluation Board | ON Semiconductor     | LQFP32 Evaluation Board                                      | ECLLQFP32EVB  | <a href="http://www.onsemi.com">http://www.onsemi.com</a>                           |
| Device Samples   | ON Semiconductor     | LQFP32 Package Device                                        | Various       | <a href="http://www.onsemi.com">http://www.onsemi.com</a>                           |

\*Components are available through most distributors, i.e. [www.newark.com](http://www.newark.com), [www.digikey.com](http://www.digikey.com).

## ECLLQFP32EVB

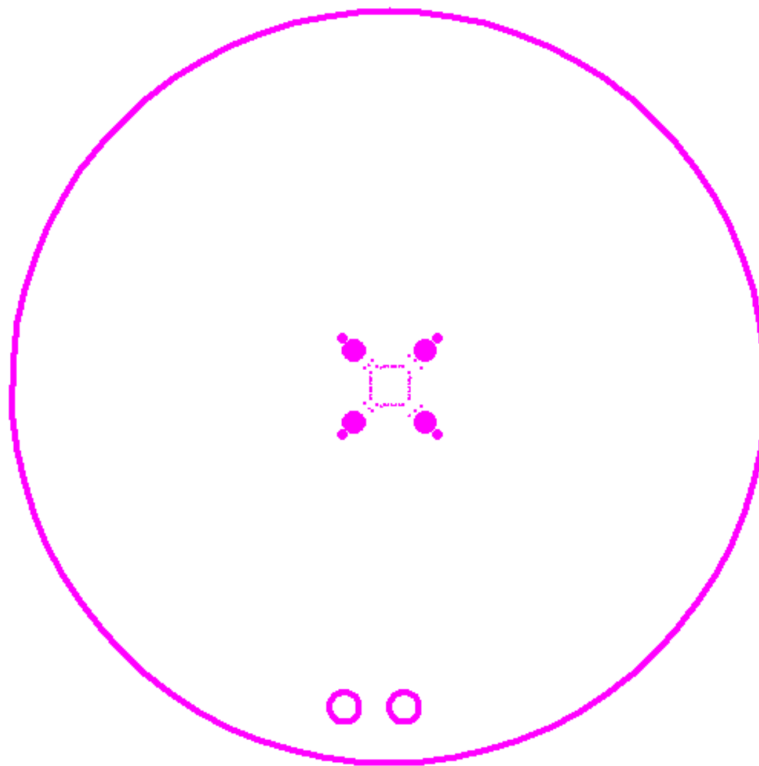
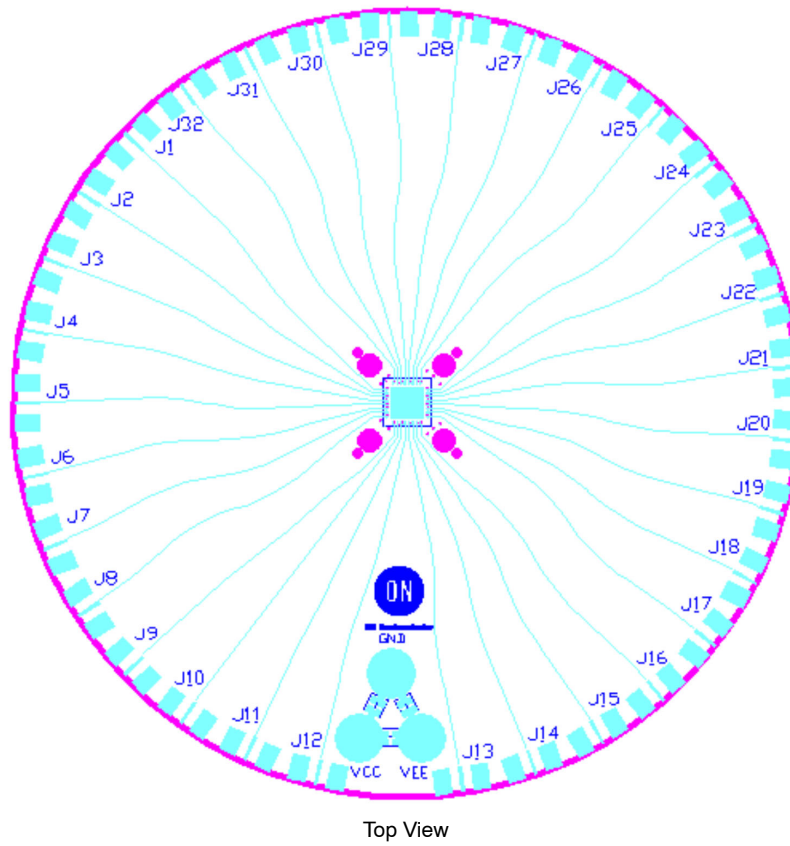
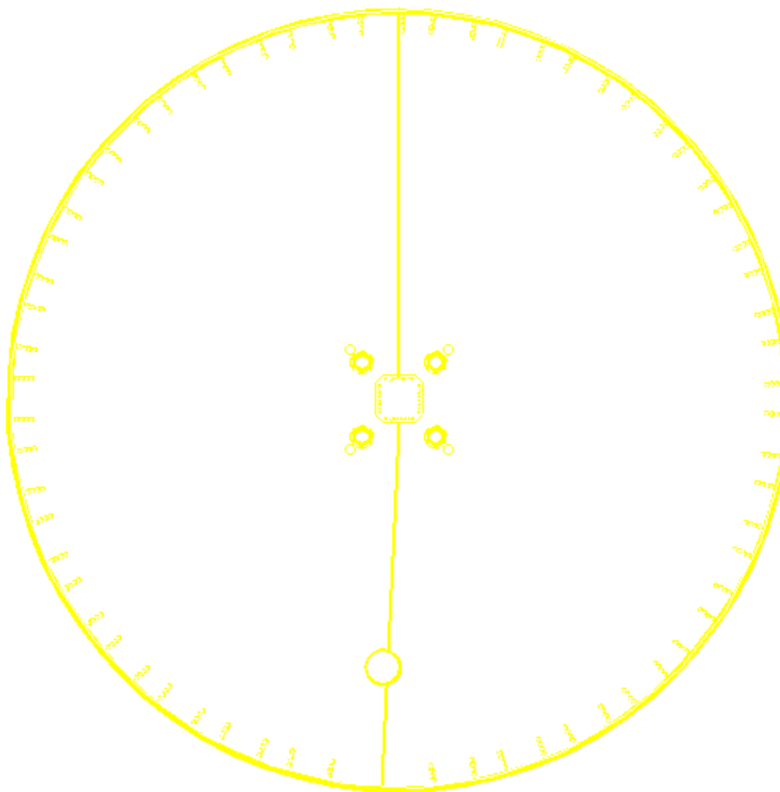
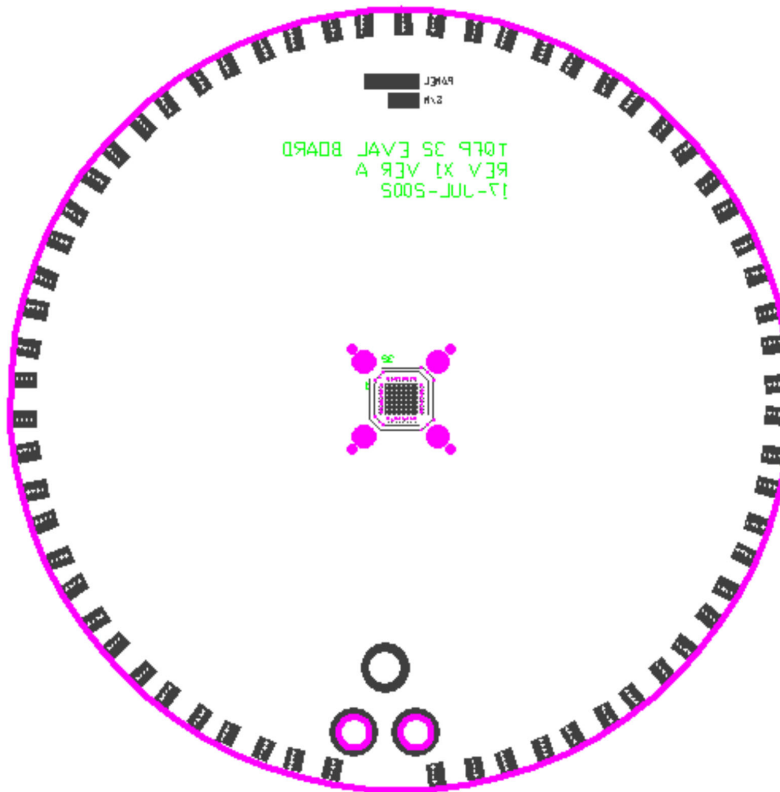


Figure 20. Gerber Files

# ECLLQFP32EVB



Third Layer (Power and Ground Plane)  
(Left side –  $V_{CC}$ , Right side –  $V_{EE}$ , Middle Box – Ground)



Bottom Layer

**Figure 21. Gerber Files**

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