

High Voltage Transistors

PNP Silicon

BSP16T1G

Features

- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	-300	Vdc
Collector-Base Voltage	V_{CBO}	-350	Vdc
Emitter-Base Voltage	V_{EBO}	-6.0	Vdc
Collector Current	I_C	-100	mAdc
Total Device Dissipation @ $T_A = 25^\circ\text{C}$ (Note 1)	P_D	1.5	W
Storage Temperature Range	P_D	-65 to +150	$^\circ\text{C}$
Junction Temperature	T_J	150	$^\circ\text{C}$

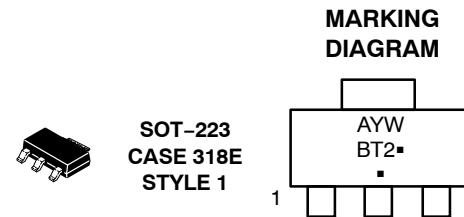
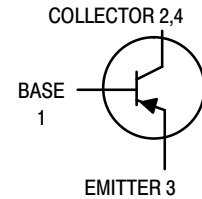
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	83.3	$^\circ\text{C/W}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

- Device mounted on a glass epoxy printed circuit board 1.575 in x 1.575 in x 0.059 in; mounting pad for the collector lead min. 0.93 sq. in.

PNP SILICON HIGH VOLTAGE TRANSISTOR SURFACE MOUNT



A = Assembly Location
 Y = Year
 W = Work Week
 BT2 = Device Code
 ■ = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping [†]
BSP16T1G	SOT-223 (Pb-Free)	1000/Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

BSP16T1G

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
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OFF CHARACTERISTICS

Collector–Emitter Breakdown Voltage ($I_C = -50\text{ mAdc}$, $I_B = 0$, $L = 25\text{ mH}$)	$V_{(BR)CEO}$	-300	–	Vdc
Collector–Base Breakdown Voltage ($I_C = -100\text{ }\mu\text{Adc}$, $I_E = 0$)	$V_{(BR)CBO}$	-300	–	Vdc
Collector–Emitter Cutoff Current ($V_{CE} = -250\text{ Vdc}$, $I_B = 0$)	I_{CES}	–	-50	μAdc
Collector–Base Cutoff Current ($V_{CB} = -280\text{ Vdc}$, $I_E = 0$)	I_{CBO}	–	-1.0	μAdc
Emitter–Base Cutoff Current ($V_{EB} = -6.0\text{ Vdc}$, $I_C = 0$)	I_{EBO}	–	-20	μAdc

ON CHARACTERISTICS

DC Current Gain ($V_{CE} = -10\text{ Vdc}$, $I_C = -50\text{ mAdc}$)	h_{FE}	30	120	–
Collector-Emitter Saturation Voltage ($I_C = -50\text{ mAdc}$, $I_B = -5.0\text{ mAdc}$)	$V_{CE(sat)}$	–	-2.0	Vdc

DYNAMIC CHARACTERISTICS

Current Gain – Bandwidth Product ($V_{CE} = -10\text{ Vdc}$, $I_C = -10\text{ mAdc}$, $f = 30\text{ MHz}$)	f_T	15	–	MHz
Collector–Base Capacitance ($V_{CB} = -10\text{ Vdc}$, $I_E = 0$, $f = 1.0\text{ MHz}$)	C_{obo}	–	15	pF

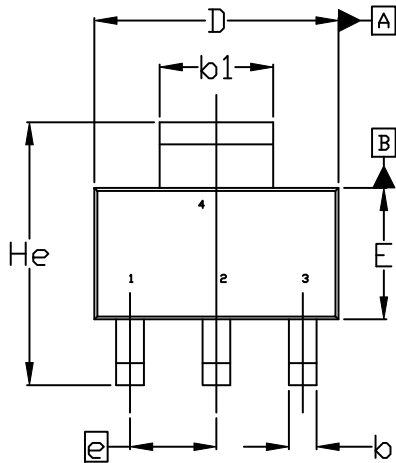
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.



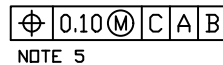
SCALE 1:1

SOT-223 (TO-261)
CASE 318E-04
ISSUE R

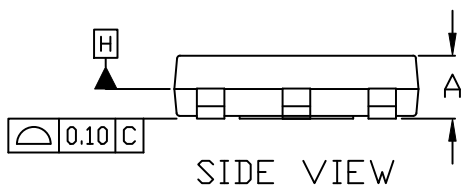
DATE 02 OCT 2018



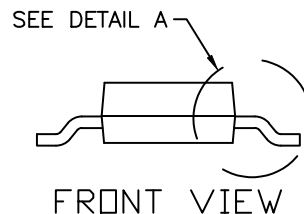
TOP VIEW



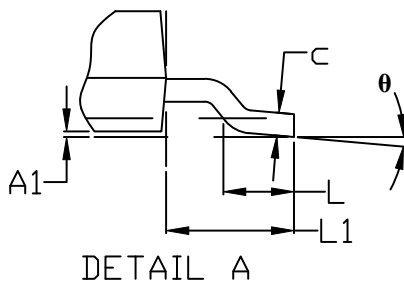
NOTE 5



SIDE VIEW



FRONT VIEW

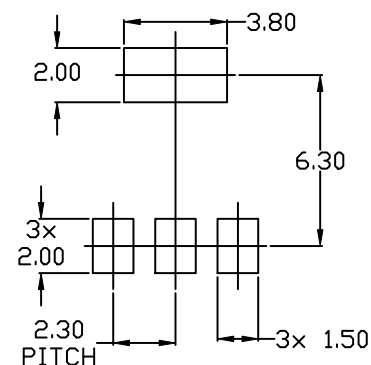


DETAIL A

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D & E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.200MM PER SIDE.
4. DATUMS A AND B ARE DETERMINED AT DATUM H.
5. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
6. POSITIONAL TOLERANCE APPLIES TO DIMENSIONS b AND b1.

MILLIMETERS			
DIM	MIN.	NOM.	MAX.
A	1.50	1.63	1.75
A1	0.02	0.06	0.10
b	0.60	0.75	0.89
b1	2.90	3.06	3.20
c	0.24	0.29	0.35
D	6.30	6.50	6.70
E	3.30	3.50	3.70
e	2.30 BSC		
L	0.20	---	---
L1	1.50	1.75	2.00
He	6.70	7.00	7.30
θ	0°	---	10°



RECOMMENDED MOUNTING
FOOTPRINT

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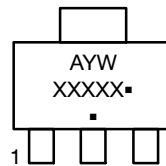
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CASE 318E-04
ISSUE R

DATE 02 OCT 2018

STYLE 1: PIN 1. BASE 2. COLLECTOR 3. EMITTER 4. COLLECTOR	STYLE 2: PIN 1. ANODE 2. CATHODE 3. NC 4. CATHODE	STYLE 3: PIN 1. GATE 2. DRAIN 3. SOURCE 4. DRAIN	STYLE 4: PIN 1. SOURCE 2. DRAIN 3. GATE 4. DRAIN	STYLE 5: PIN 1. DRAIN 2. GATE 3. SOURCE 4. GATE
STYLE 6: PIN 1. RETURN 2. INPUT 3. OUTPUT 4. INPUT	STYLE 7: PIN 1. ANODE 1 2. CATHODE 3. ANODE 2 4. CATHODE	STYLE 8: CANCELLED	STYLE 9: PIN 1. INPUT 2. GROUND 3. LOGIC 4. GROUND	STYLE 10: PIN 1. CATHODE 2. ANODE 3. GATE 4. ANODE
STYLE 11: PIN 1. MT 1 2. MT 2 3. GATE 4. MT 2	STYLE 12: PIN 1. INPUT 2. OUTPUT 3. NC 4. OUTPUT	STYLE 13: PIN 1. GATE 2. COLLECTOR 3. EMITTER 4. COLLECTOR		

**GENERIC
MARKING DIAGRAM***



A = Assembly Location
 Y = Year
 W = Work Week
 XXXXX = Specific Device Code
 ▪ = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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