

TrenchT2™ Power MOSFET

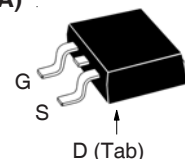
IXTA260N055T2 IXTP260N055T2

N-Channel Enhancement Mode
Avalanche Rated



$$\begin{aligned} V_{DSS} &= 55V \\ I_{D25} &= 260A \\ R_{DS(on)} &\leq 3.3m\Omega \end{aligned}$$

TO-263 (IXTA)



TO-220 (IXTP)



G = Gate D = Drain
S = Source Tab = Drain

Symbol	Test Conditions	Maximum Ratings	
V_{DSS}	$T_J = 25^\circ\text{C}$ to 175°C	55	V
V_{DGR}	$T_J = 25^\circ\text{C}$ to 175°C , $R_{GS} = 1M\Omega$	55	V
V_{GSM}	Transient	± 20	V
I_{D25}	$T_C = 25^\circ\text{C}$	260	A
$I_{L(RMS)}$	External Lead Current Limit	120	A
I_{DM}	$T_C = 25^\circ\text{C}$, Pulse Width Limited by T_{JM}	780	A
I_A	$T_C = 25^\circ\text{C}$	100	A
E_{AS}	$T_C = 25^\circ\text{C}$	600	mJ
P_D	$T_C = 25^\circ\text{C}$	480	W
T_J		-55 ... +175	$^\circ\text{C}$
T_{JM}		175	$^\circ\text{C}$
T_{stg}		-55 ... +175	$^\circ\text{C}$
T_L	Maximum Lead Temperature for Soldering	300	$^\circ\text{C}$
T_{SOLD}	1.6 mm (0.062in.) from Case for 10s	260	$^\circ\text{C}$
F_C	Mounting Force (TO-263)	10..65 / 2.2..14.6	N/lb
M_d	Mounting Torque (TO-220)	1.13 / 10	Nm/lb.in
Weight	TO-263	2.5	g
	TO-220	3.0	g

Symbol	Test Conditions ($T_J = 25^\circ\text{C}$ Unless Otherwise Specified)	Characteristic Values		
		Min.	Typ.	Max.
BV_{DSS}	$V_{GS} = 0V$, $I_D = 250\mu A$	55		V
$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250\mu A$	2.0		4.0 V
I_{GSS}	$V_{GS} = \pm 20V$, $V_{DS} = 0V$			± 200 nA
I_{DSS}	$V_{DS} = V_{DSS}$, $V_{GS} = 0V$ $T_J = 150^\circ\text{C}$			5 μA 150 μA
$R_{DS(on)}$	$V_{GS} = 10V$, $I_D = 50A$, Notes 1 & 2			3.3 m Ω

Features

- International Standard Packages
- Avalanche Rated
- Low Package Inductance
- Fast Intrinsic Rectifier
- 175 $^\circ\text{C}$ Operating Temperature
- High Current Handling Capability
- ROHS Compliant
- High Performance Trench Technology for extremely low $R_{DS(on)}$

Advantages

- High Power Density
- Easy to Mount
- Space Savings

Applications

- Automotive Engine Control
- Synchronous Buck Converter (for Notebook SystemPower & General Purpose Point & Load)
- DC/DC Converters
- High Current Switching Applications
- Power Train Management
- Distributed Power Architecture

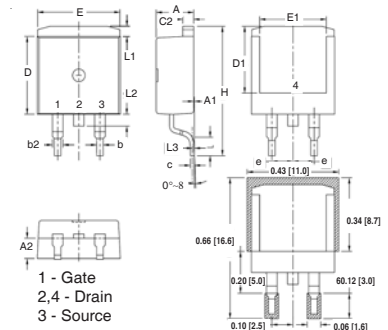
Symbol	Test Conditions ($T_J = 25^\circ\text{C}$ Unless Otherwise Specified)	Characteristic Values		
		Min.	Typ.	Max.
g_{fs}	$V_{DS} = 10\text{V}$, $I_D = 60\text{A}$, Note 1	55	94	S
C_{iss}	$V_{GS} = 0\text{V}$, $V_{DS} = 25\text{V}$, $f = 1\text{MHz}$		10.8	nF
C_{oss}			1460	pF
C_{rss}			215	pF
$t_{d(on)}$	Resistive Switching Times $V_{GS} = 10\text{V}$, $V_{DS} = 28\text{V}$, $I_D = 100\text{A}$ $R_G = 2\Omega$ (External)		20	ns
t_r			27	ns
$t_{d(off)}$			36	ns
t_f			24	ns
$Q_{g(on)}$	$V_{GS} = 10\text{V}$, $V_{DS} = 0.5 \cdot V_{DSS}$, $I_D = 0.5 \cdot I_{DSS}$		140	nC
Q_{gs}			52	nC
Q_{gd}			32	nC
R_{thJC}	TO-220		0.50	0.31°C/W
R_{thCS}				

Source-Drain Diode

Symbol	Test Conditions ($T_J = 25^\circ\text{C}$ Unless Otherwise Specified)	Characteristic Values		
		Min.	Typ.	Max.
I_S	$V_{GS} = 0\text{V}$			260 A
I_{SM}	Repetitive, Pulse Width Limited by T_{JM}			1000 A
V_{SD}	$I_F = 100\text{A}$, $V_{GS} = 0\text{V}$, Note 1			1.3 V
t_{rr}	$I_F = 130\text{A}$, $V_{GS} = 0\text{V}$, $-di/dt = 100\text{A}/\mu\text{s}$, $V_R = 27\text{V}$		60	ns
I_{RM}			3.4	A
Q_{RM}			102	nC

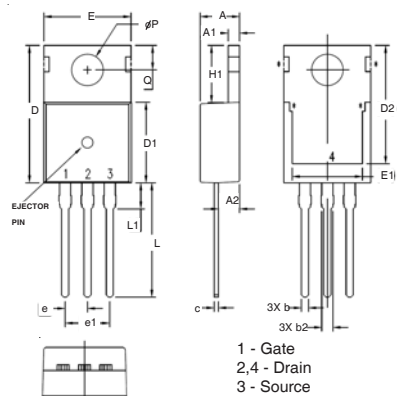
- Notes: 1. Pulse test, $t \leq 300\mu\text{s}$; duty cycle, $d \leq 2\%$.
2. On through-hole packages, $R_{DS(on)}$ Kelvin test contact location must be 5mm or less from the package body.

TO-263 Outline



SYM	INCHES		MILLIMETER	
	MIN	MAX	MIN	MAX
A	.170	.185	4.30	4.70
A1	.000	.008	0.00	0.20
A2	.091	.098	2.30	2.50
b	.028	.035	0.70	0.90
b2	.046	.060	1.18	1.52
C	.018	.024	0.45	0.60
C2	.049	.060	1.25	1.52
D	.340	.370	8.63	9.40
D1	.300	.327	7.62	8.30
E	.380	.410	9.65	10.41
E1	.270	.330	6.86	8.38
[e]	.100 BSC		2.54 BSC	
H	.580	.620	14.73	15.75
L	.075	.105	1.91	2.67
L1	.039	.060	1.00	1.52
L2	—	.070	—	1.77
[L3]	.010 BSC		0.254 BSC	

TO-220 Outline



SYM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.169	.185	4.30	4.70
A1	.047	.055	1.20	1.40
A2	.079	.106	2.00	2.70
b	.024	.039	0.60	1.00
b2	.045	.057	1.15	1.45
c	.014	.026	0.35	0.65
D	.587	.626	14.90	15.90
D1	.335	.370	8.50	9.40
(D2)	.500	.531	12.70	13.50
E	.382	.406	9.70	10.30
(E1)	.283	.323	7.20	8.20
e	.100 BSC		2.54 BSC	
e1	.200 BSC		5.08 BSC	
H1	.244	.268	6.20	6.80
L	.492	.547	12.50	13.90
L1	.110	.154	2.80	3.90
ØP	.134	.150	3.40	3.80
Q	.106	.126	2.70	3.20

IXYS Reserves the Right to Change Limits, Test Conditions, and Dimensions.

IXYS MOSFETs and IGBTs are covered by one or more of the following U.S. patents:	4,835,592	4,931,844	5,049,961	5,237,481	6,162,665	6,404,065B1	6,683,344	6,727,585	7,005,734B2	7,157,338B2
	4,860,072	5,017,508	5,063,307	5,381,025	6,259,123B1	6,534,343	6,710,405B2	6,759,692	7,063,975B2	
	4,881,106	5,034,796	5,187,117	5,486,715	6,306,728B1	6,583,505	6,710,463	6,771,478B2	7,071,537	

Fig. 1. Output Characteristics @ $T_J = 25^\circ\text{C}$

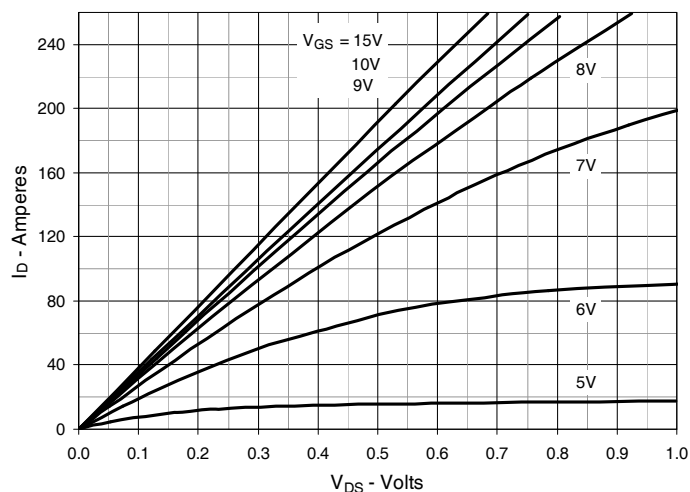


Fig. 2. Extended Output Characteristics @ $T_J = 25^\circ\text{C}$

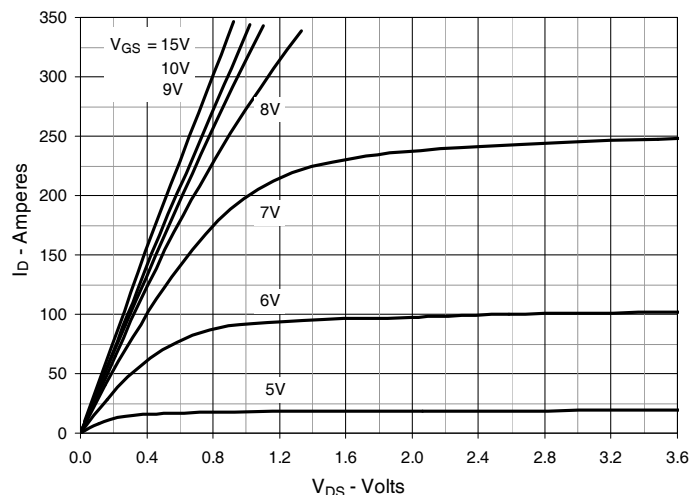


Fig. 3. Output Characteristics @ $T_J = 150^\circ\text{C}$

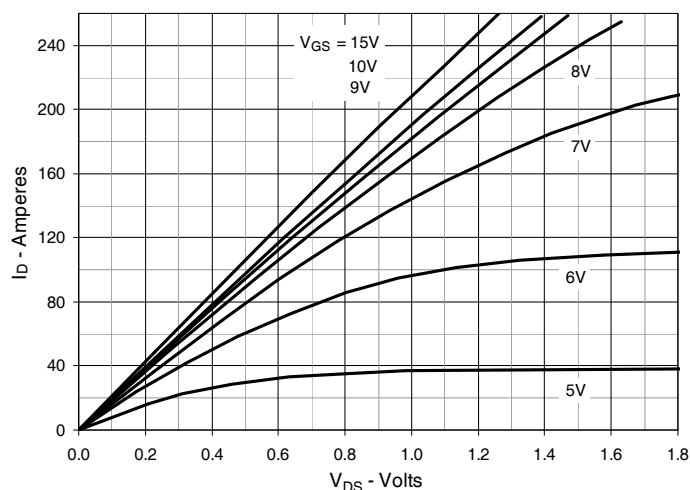


Fig. 4. $R_{DS(on)}$ Normalized to $I_D = 130\text{A}$ Value vs. Junction Temperature

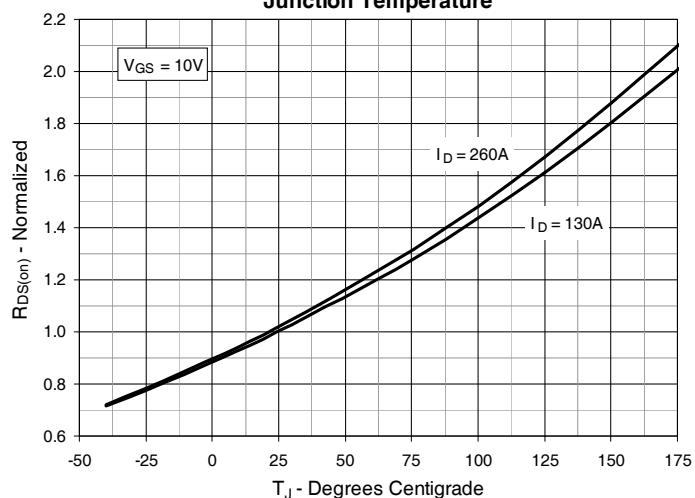


Fig. 5. $R_{DS(on)}$ Normalized to $I_D = 130\text{A}$ Value vs. Drain Current

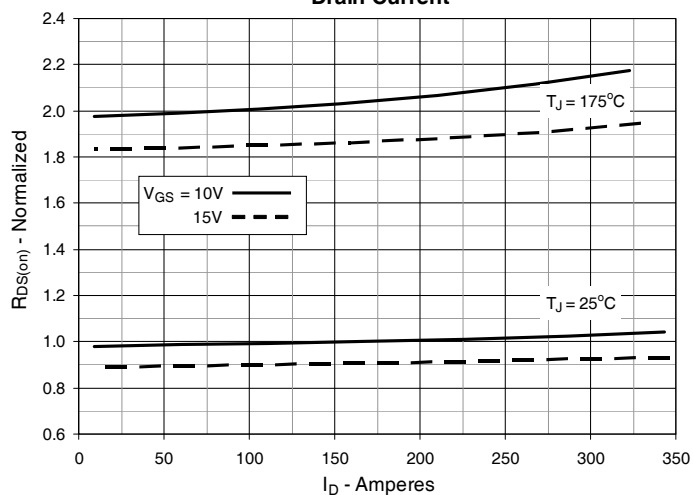


Fig. 6. Drain Current vs. Case Temperature

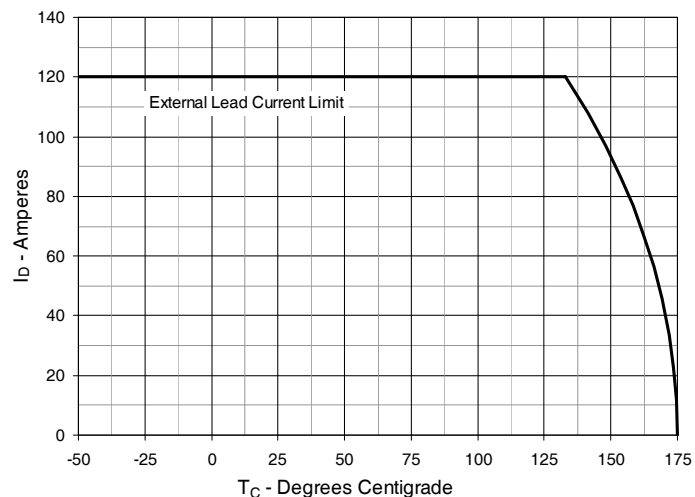


Fig. 7. Input Admittance

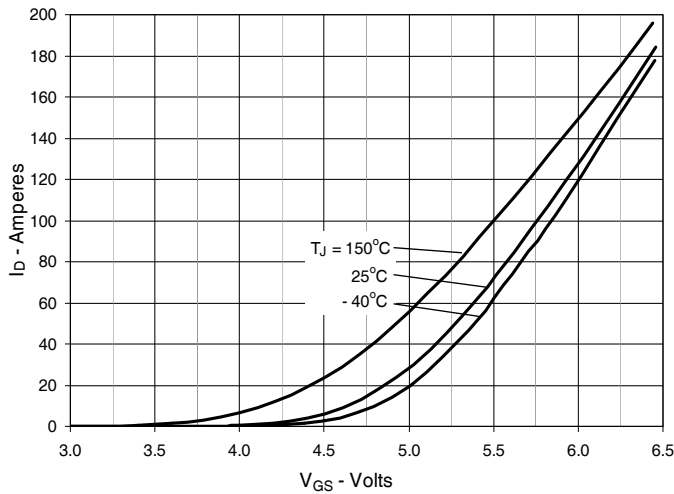


Fig. 8. Transconductance

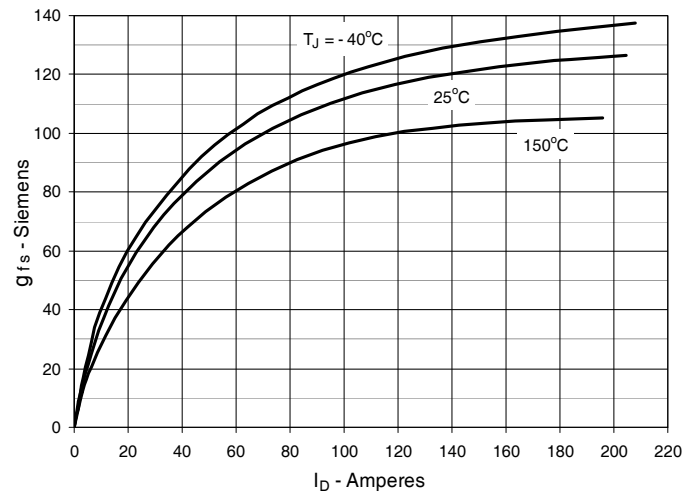


Fig. 9. Forward Voltage Drop of Intrinsic Diode

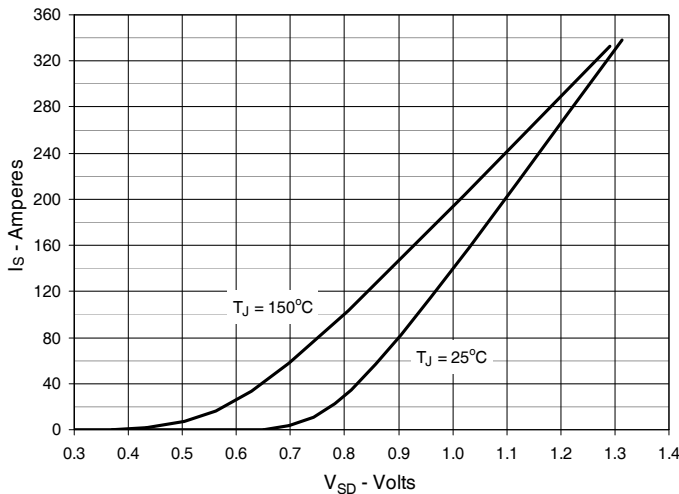


Fig. 10. Gate Charge

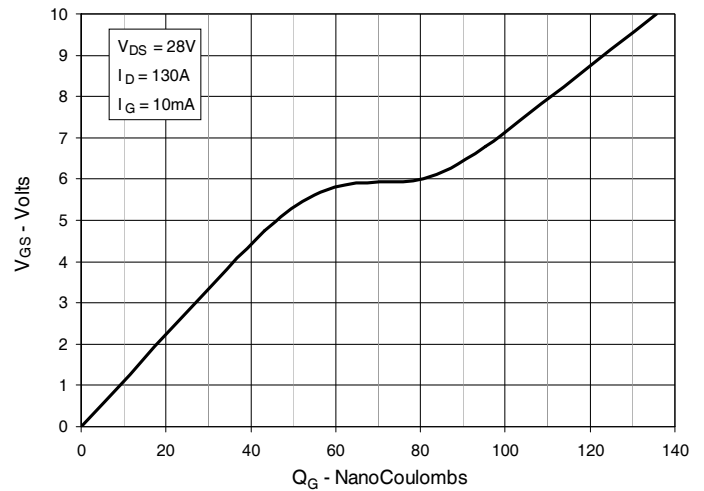


Fig. 11. Capacitance

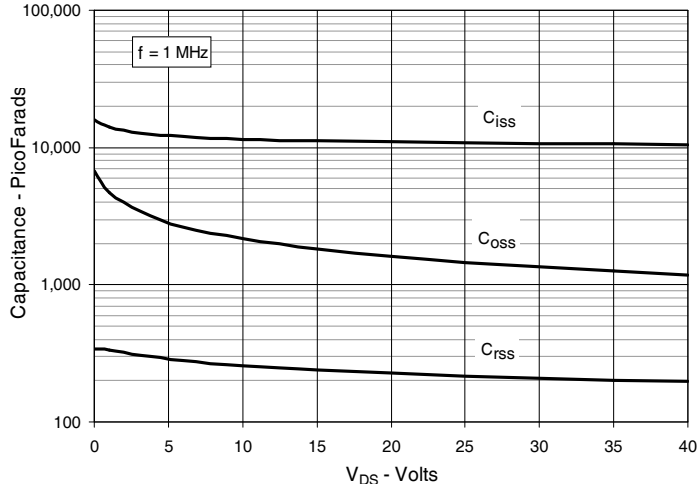


Fig. 12. Forward-Bias Safe Operating Area

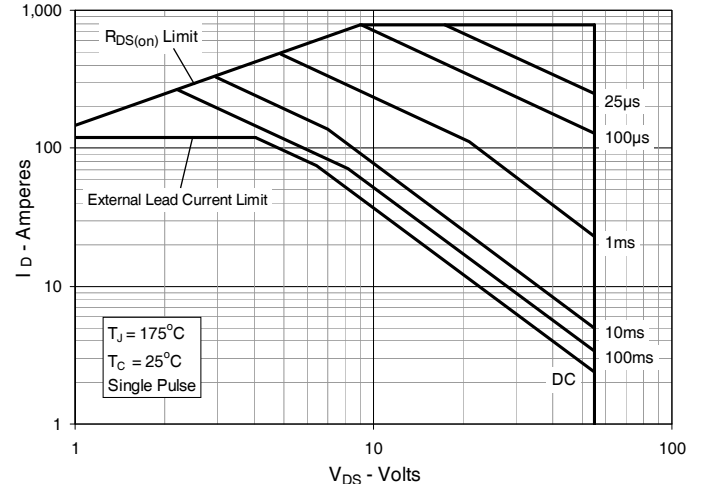


Fig. 13. Resistive Turn-on
Rise Time vs. Junction Temperature

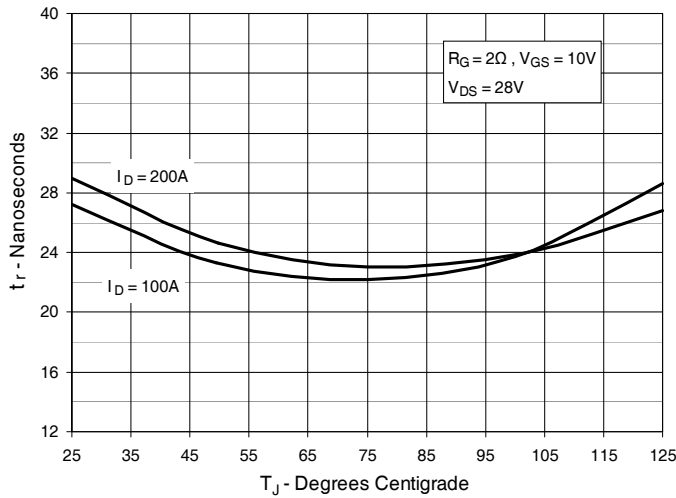


Fig. 14. Resistive Turn-on
Rise Time vs. Drain Current

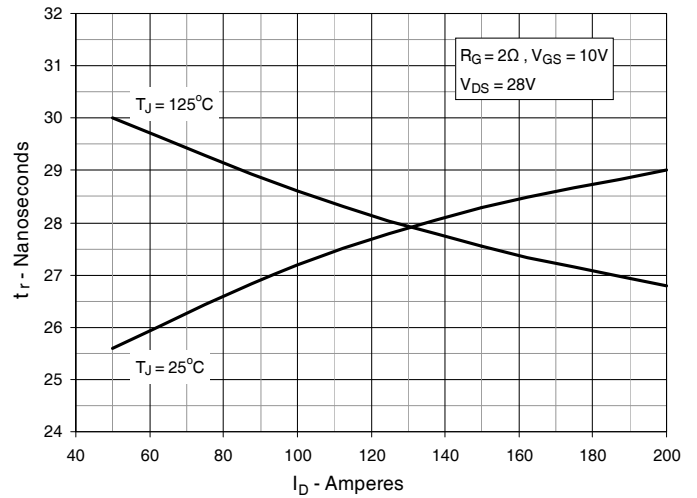


Fig. 15. Resistive Turn-on
Switching Times vs. Gate Resistance

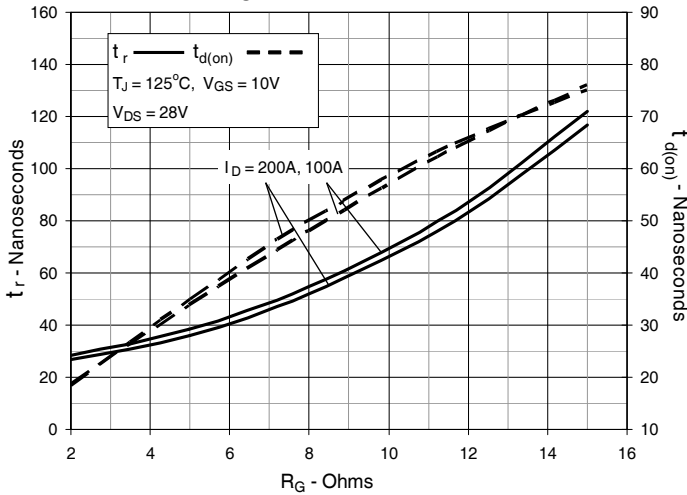


Fig. 16. Resistive Turn-off
Switching Times vs. Junction Temperature

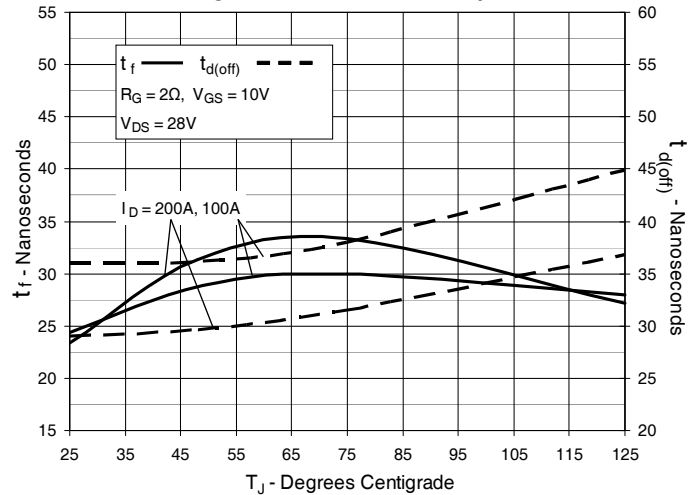


Fig. 17. Resistive Turn-off
Switching Times vs. Drain Current

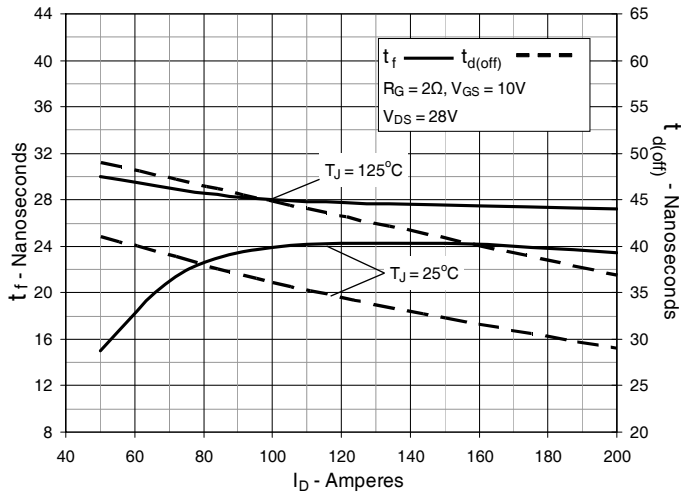


Fig. 18. Resistive Turn-off
Switching Times vs. Gate Resistance

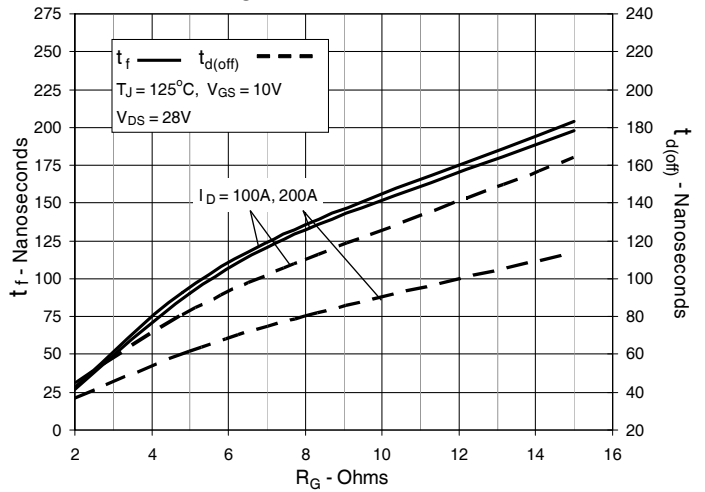
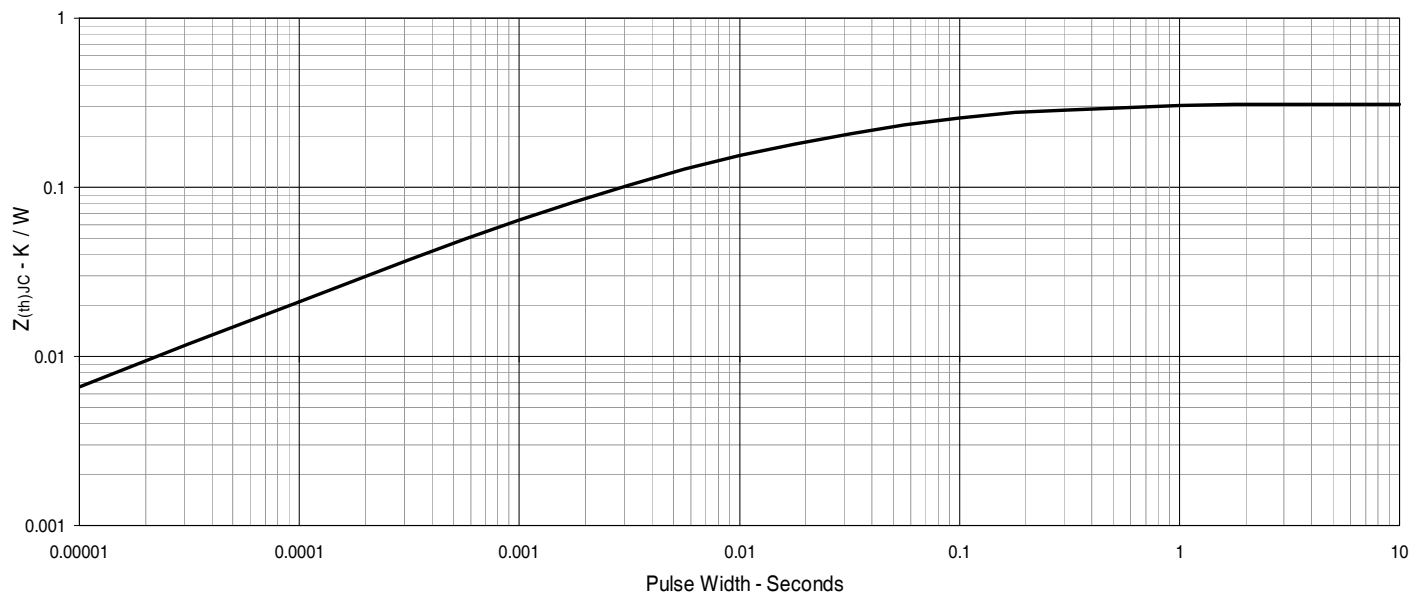


Fig. 19. Maximum Transient Thermal Impedance





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