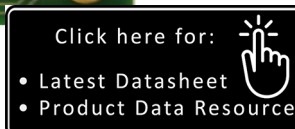
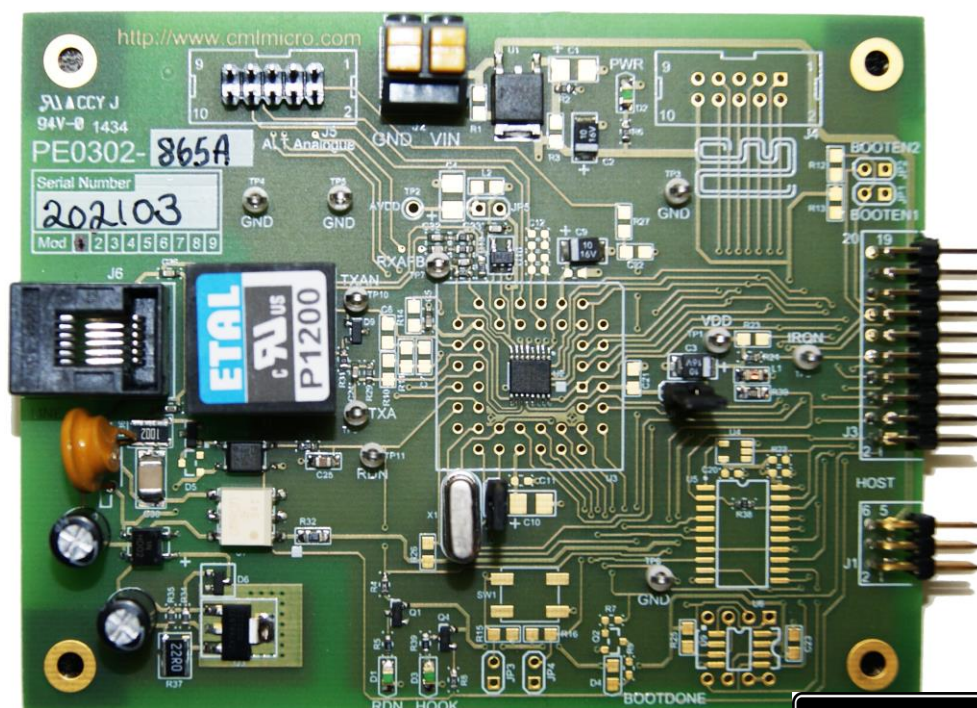


Features

- CMX865A evaluation
- Fully Isolated 2-Wire Line Interface (DAA)
- Designed for use with PE0003 Universal Interface Card and PC control software
- Operates from single 5V dc power supply
- On-board supply regulator



1 Brief Description

The PE0302-865A Evaluation Board features the CMX865A DTMF Codec/FSK Combo. Also included is a line interface.

The board is fitted with a C-BUS connector allowing the PE0302-865A to be operated by connection to either of the two C-BUS ports on a PE0003 Universal Interface Card, and used with the associated PC GUI software. Alternatively, direct connection is possible between the CMX865A C-BUS and the user's μ C development application or emulation system.

The board is operated at 3.3V dc, which is regulated on-board from an external 5 volt supply.

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It is always recommended that you check for the latest product datasheet version from the Datasheets page of the CML website: [www.cmlmicro.com].

History

Version	Changes	Date
2	Minor typographical corrections	Mar 2015
1	Original document	Dec 2014

2 Block Diagram

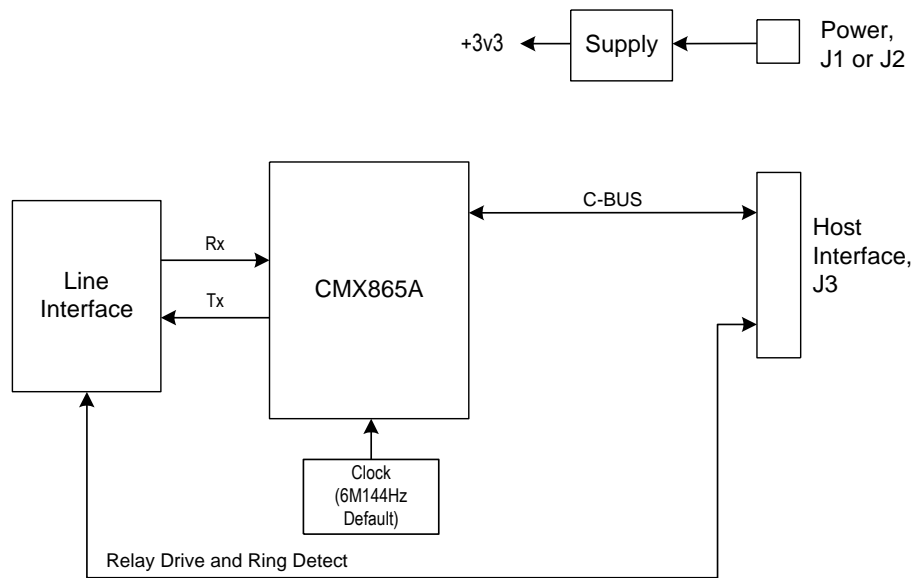


Figure 1 Block Diagram

3 Preliminary Information

3.1 Laboratory Equipment

The following laboratory equipment is needed to use this evaluation kit:

A 5.0 volt dc regulated power supply

If the board is being used with the PE0003 Universal Interface Card, the following items will also be required:

An IBM compatible PC with the following specification:

- One of the following Windows operating systems installed: Windows 7 SP1 or Windows XP SP2
- USB port
- Minimum screen resolution 800 x 600. Recommended screen resolution 1024 x 768

A USB type A male to mini B male cable

Software application **ES000310.exe**, or later version, installed on the PC

3.2 Handling Precautions

Like most evaluation kits, this product is designed for use in office and laboratory environments. The following practices will help ensure its proper operation:

3.2.1 Static Protection



This product uses low-power CMOS circuits that can be damaged by electrostatic discharge. Partially-damaged circuits can function erroneously, leading to misleading results. Observe ESD precautions at all times when handling this product.

3.2.2 Contents – Unpacking

Please ensure that you have received all of the items on the separate Information Sheet (EK0302) and notify CML within seven working days if the delivery is incomplete.

3.3 Approvals

This product is not approved to any EMC or other regulatory standard. Users are advised to observe local statutory requirements, which may apply to this product.

4 Quick Start

This section is divided into two sub-sections. The first is for those users who are using the board with a PE0003 Universal Interface Controller Card and Windows application. The second is for users who are not using the PE0003.

4.1 With PE0003

Note that the C-BUS connector J3 and the power connector J1 are both right-angle headers and are designed to plug directly into sockets J5 (C-BUS1 port) and J9 respectively, or sockets J3 (C-BUS2 port) and J7 respectively, of a PE0003.

4.1.1 Setting-Up

- Refer to the PE0003 User Manual, and follow the instructions given in the quick start section.

The basic arrangement, when used with the PE0003 is shown below:

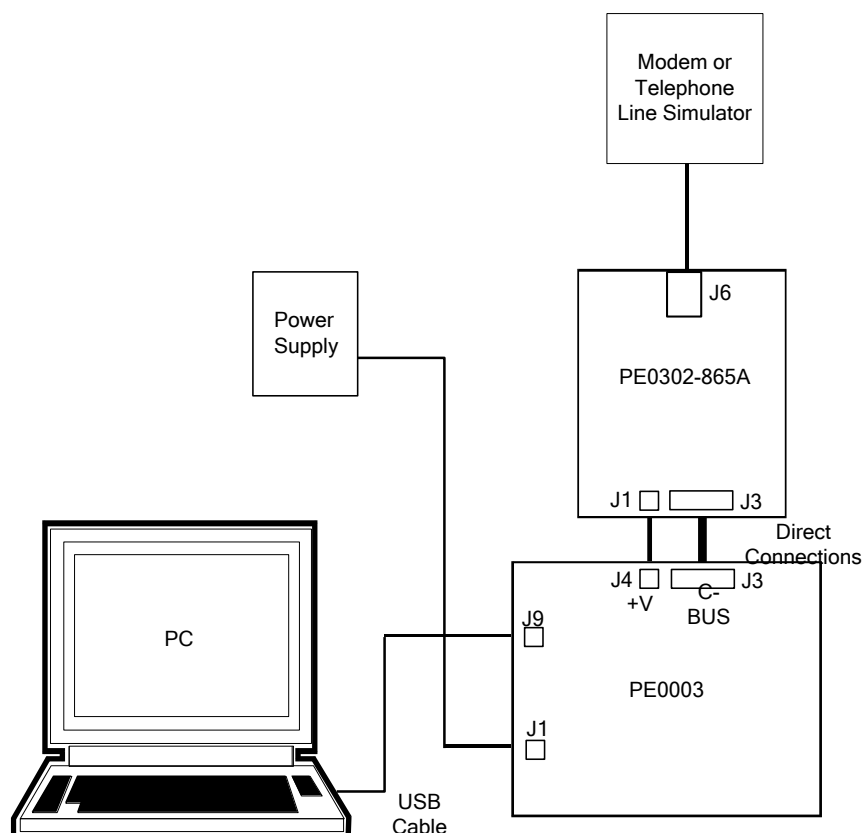


Figure 2 PE0302-865A used with PE0003

4.1.2 Operation

Neither the ring detector output 'RDN' or the hook switch control signal 'RLYDRV' are accessible from the generic PE0003 graphical user interface (GUI). Access can be gained by using PE0003 scripts. RDN and RLYDRV correspond to the signals GPIO2 and GPIO3 respectively, when using C-BUS1 as shown in Figure 2. See also the PE0003 script handler reference document.

4.2 Without PE0003

As an alternative to using the PE0003 controller kit, users may control the target device with their own host controller card. As with the PE0003 the C-BUS serial interface connections are made via connector J3.

5 Signal Lists

Table 1 Signal List

CONNECTOR PINOUT				
Connector Ref.	Connector Pin No.	Signal Name	Signal Type	Description
J1	1, 2	GND	PWR	Supply ground
	3 to 6	+V	PWR	External supply voltage – daisy chained from PE0003
J2		+V	PWR	External supply voltage
		GND	PWR	Supply ground
J3	1	N/C	-	
	2	CSN	I/P	Chip select. Connects to host μ C
	3	-	-	Not used
	4	CDATA	I/P	Serial data input. Connects to host μ C
	5	RDN	O/P	Ring detect, active low
	6	SCLK	I/P	Serial clock input. Connects to host μ C
	7	RLYDRV	I/P	Hook switch control, active low
	8	RDATA	O/P	Serial data output. Connects to host μ C
	9	-	-	Not used
	10	IRQN	O/P	Interrupt request. Connects to host μ C
	11, 12	GND	PWR	Supply ground
	13	-	-	Not used
	14	-	-	Not used
	15, 16, 17, 18, 19, 20	N/C	-	Do not connect these pins
J5	1, 3, 5, 6, 7, 8, 9	N/C	-	
	2	RXALT	I/P	Alternative Rx input, bypassing line Interface
	4, 10	GND	PWR	ground
J6	1, 2	N/C	-	
	3	RING	BI	RJ11 connector – Ring
	4	TIP	BI	RJ11 connector – Tip
	5, 6	N/C	-	

Table 2 Test Points

TEST POINTS		
Test Point Ref.	Default Measurement	Description
TP1	3.3V	Output from on-board regulator. DC supply voltage rail
TP3	0V	GND, digital ground
TP4	0V	GND, digital ground
TP5	0V	GND, digital ground
TP6	0V	GND, digital ground
TP7	-	RXAFB - The output of the evaluation device Rx input amplifier
TP8	3.3V	IRQN – The interrupt output of the evaluation device
TP9	-	TXA - The non-inverted Tx output of the evaluation device
TP10	-	TXAN - The inverted Tx output of the evaluation device
TP11	3.3V	RDN - Ring detect

Table 3 Jumpers

JUMPERS/LINKS			
Link Ref.	Positions	Default Position	Description
JP6	1-2	short	Disconnect to supply external clock source to evaluation device
JP7	1-2	short	Isolates supply rail from CMX865A evaluation device

Table 4 LEDs

LEDs	
LED Ref.	Description
D1	RDN – Indicates ring signal on the line
D2	Indicates that the supply voltage is present
D3	HOOK – Indicates board is off-hook

Notes: I/P = Input
O/P = Output
BI = Bidirectional
N/C = Not connected
PWR = Power supply connection

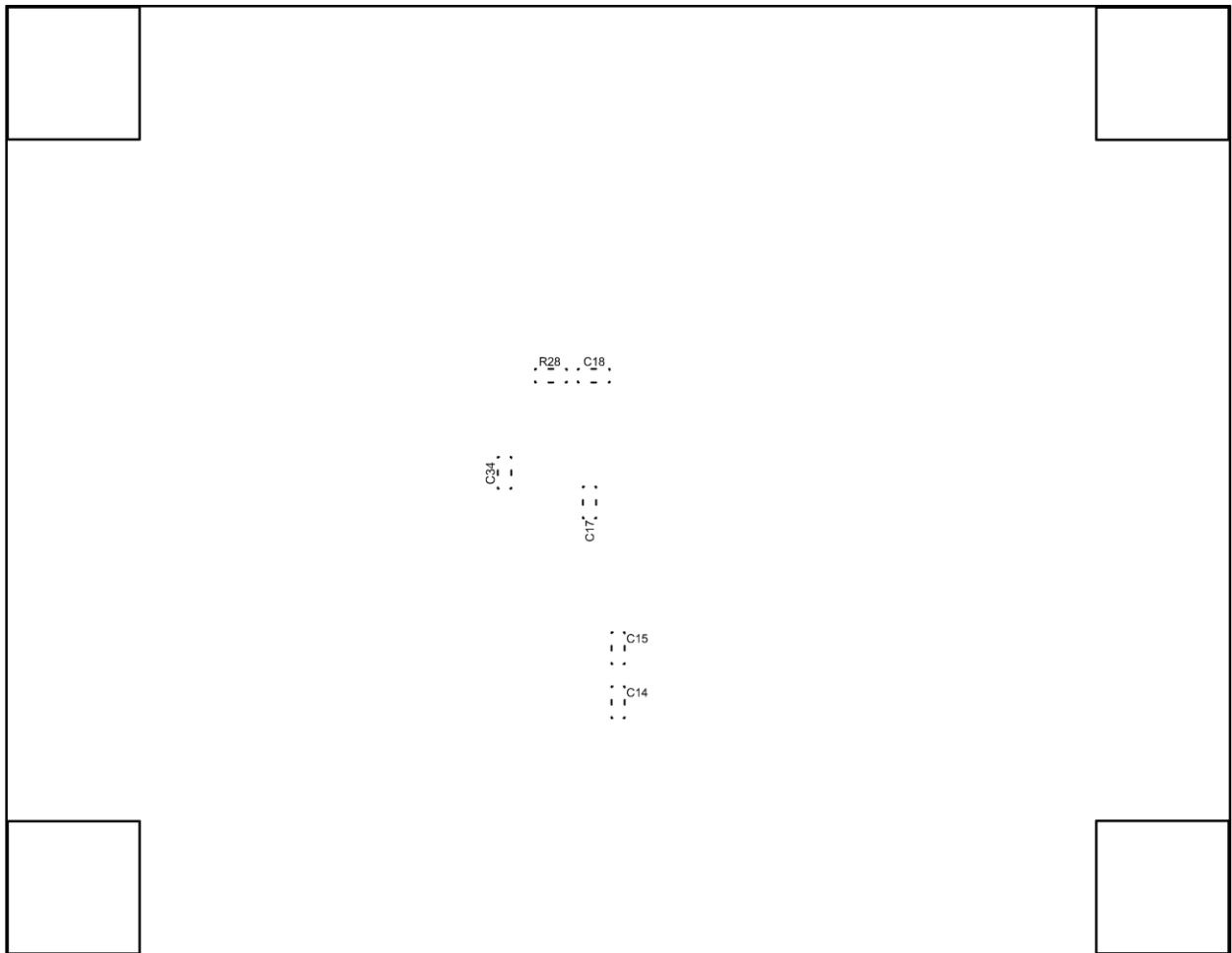


Figure 4 Evaluation Board Layout - Bottom

7 Detailed Description

7.1 Hardware Description

7.1.1 Power Supplies

The board is fitted with a 3.3 volt regulator, U1. The input to this regulator is provided by an external, nominally 5.0 volt dc, power supply, which is connected to the board via connector J2, a snap type connector. Alternatively power may be daisy-chained from a PE0003 via connector J1.

The supply voltage to the CMX865A device can be monitored on test point TP1.

LED illumination confirms the on-board presence of the +3.3 volt dc digital voltage supply.

7.1.2 Clock Options

The board uses the fitted 6.144MHz crystal as the default clock source for the evaluation device. Alternatively, jumper JP6 can be removed and using an appropriate lead, an external clock source with a signal level of less than +3V3D, can be applied between pin 2 of JP1 and GND.

7.1.3 Host Interface

The C-BUS, hook and ring signals are brought out on connector J3. This is a right-angle male header designed to plug directly into the PE0003 which has a matching female header.

7.1.4 Line Interface

The board is shipped with a DAA, which presents an ac line termination of 600Ω resistive when off hook. The user may alter the terminating impedance by fitting alternative values for components C3, C5, C6, R6 and R7. For CTR21 complex matching, the values are:

$C29 = 2.2\mu\text{F}$, $C26 = 56\text{nF}$, $C24 = 150\text{nF}$, $R31 = 220\Omega$, $R29 = 680\Omega$

The board is off-hook when the 'RLYDRV' signal at the host interface, J3, is held low.

There is a direct input receive path that bypasses the line interface at J5 pin 2, 'RXALT'.

On-hook Caller ID

This function provides a high-impedance, on-hook AC path for the routing of Caller ID signals to the CMX865A. Components C28 and R18 provide this signal path. C28 bypasses the optoMOS relay hook switch, allowing AC signals to pass through T1 when the PE0302-865A is in an on-hook state. To compensate for losses incurred in the on-hook state, R18 is switched in circuit by analogue switch U10, thereby increasing the receive path gain. Path gain is set assuming that the TXA output of the CMX865A is set to high impedance.

Ring Detection

The ring detect threshold is approximately 20V rms. The RDN signal at the host interface, J3, will be low when a ring signal is present at the telephone line connector, J6. Additionally, a single pulse low on the RDN line will signal that a line reversal has occurred.

Line Protection

Line protection is provided by an integrated overcurrent/overvoltage protection device, E1.

7.2 Software

The board can be used with the GUI software supplied with the PE0003. The PE0003 includes a script handler and various example scripts are available from the CML website.

Neither the ring detector output 'RDN' or the hook switch control signal 'RLYDRV' are accessible from the generic PE0003 GUI. Access can be gained by using PE0003 scripts. RDN and RLYDRV correspond to the signals GPIO2 and GPIO3 respectively, when using C-BUS1 as shown in Figure 2. See also the User Manual for PE0003 Scripting Language (available from the CML website).

8 Performance Specification

8.1 Electrical Performance

8.1.1 Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the Evaluation Kit.

	Min.	Max.	Units
Supply ($V_{IN} - V_{SS}$)	-0.3	9.0	V
Voltage on any connector pin to V_{SS}	-0.3	3.6	V
Current into or out of V_{IN} and V_{SS} pins	0	+0.45	A
Current into or out of any other connector pin	-20	+20	mA

8.1.2 Operating Limits

Correct operation of the Evaluation Kit outside these limits is not implied.

	Notes	Min.	Max.	Units
Supply (+V - V_{GND})		4.5	5.5	V

8.1.3 Operating Characteristics

For the following conditions unless otherwise specified:

Evaluation Device Clock Frequency = 6.144MHz, $V_{IN} = 5.0V$, $T_{AMB} = +25^{\circ}C$.

For Function Image[™] parameters, see relevant FI datasheet.

	Notes	Min.	Typ.	Max.	Units
DC Parameters					
I_{DD} (on-hook, CMX865A powersaved)	1	-	10	-	mA
I_{DD} (off-hook, CMX865A operating)	1	-	25	-	mA
+3V3 Regulated Supply		3.15	3.3	3.45	Vdc

Notes: 1. Not including any current drawn from pins by external circuitry.

Operating Characteristics - Timing Diagrams

See relevant FI documentation for C-BUS signal timing information.

8.1.4 Physical Dimensions

	Notes	Min.	Typ.	Max.	Units
Width			111		mm
Height			86		mm

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