PE0003
Evaluation Kit Interface Card

UM0003/3 August 2017 Provisional Information

Features

- **Global interface for new generation IC evaluation kits**
- **Target IC C-BUS read and write operations**
- **32-Bit Dual core ARM Microprocessor Cortex-M4/Cortex-M0**
- **Mating interface for wide range of target evkit boards**
- **Micro SD Card to store Function Images and bulk data**
- **PC GUI and hardware provided**
- **Function Image handling for *FirmASIC*®-based projects**
- **High-speed real-time script execution**
- **PC control/communications via USB**
- **Software configurable GPIO lines and LED bank**
- **C Library for fast C development**
- **JTAG port for debugging C applications**

1 Brief Description

The PE0003 Evaluation Kit Interface Card is a global interface system for use with evaluation kits for CML's new generation ICs, including *FirmASIC*®–based products. This greatly simplifies the approach to the evaluation and design-in process.

Based around the NXP ARM microprocessor LPC4330 and using a PC GUI, the information generated is formatted, timed and delivered to the target IC via selected C-BUS serial interfaces or a host port. The supplied control software can be used to perform C-BUS read and write operations, read or write sample data or run scripting functions.

In the case of *FirmASIC*® IC evaluations, the Function Image™ can be loaded onto the CMX{target} device or programmed into serial memory on the {target} card.

Communication with the PE0003 is via high-speed USB 2.0.

The PE0003 provides an environment for C code development and evaluation using NXP's toolchain, LPCXpresso and JTAG. A set of proven C libraries can be downloaded in the PE0003 Support Package to assist with application development.

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It is recommended that you check for the latest product datasheet version from the Datasheets page of the CML website: [www.cmlmicro.com].

History

Version	Changes	Date
3	• Section 7.6: Updated to include instructions for Windows 10 Driver installation.	August 2017

2	• New Figure 8 (C-BUS Frequency Warning Message dialog) and associated new text in Section 7.4 • ES0003 screenshots updated with activation codes control and frequency control (Figures 9 to 15). Associated new text in Section 7.4.1. • Section 8: Maximum operating supply voltage corrected to +6 • Section 8: Absolute maximum supply voltage corrected to +6.8V	January 2016
1	First release	August 2014

2 Block Diagram

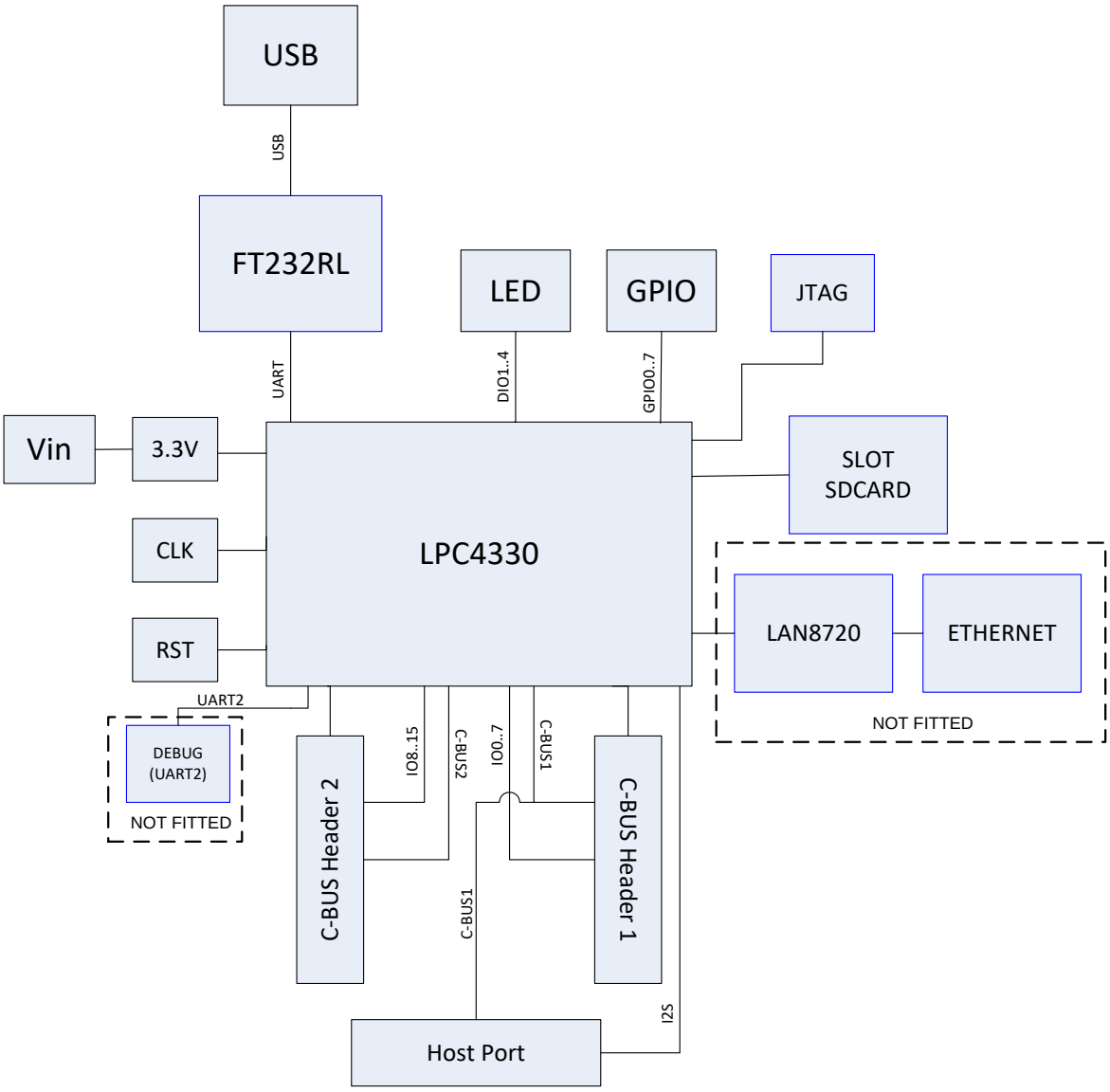

Figure 1 Block Diagram

3 Preliminary Information

3.1 Laboratory Equipment

The following laboratory equipment is needed to use this evaluation kit:

3.1.1 Power Supply

A 5 Volt DC unregulated power supply.

3.1.2 PC

With the following requirements:

- One of the following Windows operating systems installed: XP, Vista, Windows 7 or Windows 8.
- USB port.
- Minimum screen resolution 800 x 600. Recommended minimum resolution 1024 x 768.

3.1.3 USB type A male to mini B male cable

3.2 Handling Precautions

Like most evaluation kits, this product is designed for use in office and laboratory environments. The following practices will help ensure its proper operation.

3.2.1 Static Protection

This product uses low power CMOS circuits that can be damaged by electrostatic discharge. Partially damaged circuits can function erroneously, leading to misleading results. Observe ESD precautions at all times when handling this product.

3.2.2 Contents - Unpacking

Please ensure that you have received all of the items on the separate information sheet (EK9980) and notify CML within seven working days if the delivery is incomplete.

3.2.3 Approvals

This product is not approved to any EMC or other regulatory standard. Users are advised to observe local statutory requirements, which may apply to this product and the radio frequency signals that may emanate from it.

4 Quick Start

This section provides instructions for users who wish to experiment immediately with the evaluation kit. A more detailed description of the kit and its use appears later in this document.

4.1 Setting-Up

- Copy the file 'ES0003xx.zip', which is downloaded from the CML website following registration, to the hard drive of your host PC.
- Extract the files to the hard drive of your host PC.
- Connect the Target Card(s) to the PE0003 C-BUS connectors J3, J7 and/or host connector J6 as required.
- Connect a DC supply to the PE0003 and set the voltage level to 5V.
- Connect a DC supply to the Target Card and set to the voltage level specified in the relevant Target Card User Manual. Some target cards can use the 5 volts supplied through the PE0003 on either J4, J8 and/or J5.
- Attach a USB cable between connector J9 of the PE0003 Interface Card and the USB port of the PC.
- Turn on the power supply. The power-on indicator D8 will light.
- Install the USB driver when requested. See Section 7.6.

4.2 Adjustments

The default C-BUS clock frequency is 10MHz. Change this to the C-BUS speed of the slowest Evaluation Kit connected. The C-BUS clock speed is changed using the Options Dialogue. See Section 7.4.6.

4.3 Operation

- Run the application ES0003xx.exe.
- Press the reset switch, SW1, on the PE0003 board if requested.

When the GUI finishes loading the PE0003 is ready to use.

5 Signal Lists

CONNECTOR PINOUT				
Connector Ref.	**Connector Pin No.**	**Signal Name**	**Signal Type**	**Description**
J1				Ethernet – not fitted
	1	TD+	DP+	Transmit data +
	2	TD-	DP-	Transmit data -
	3	RD+	RD+	Receive data +
	4	unused		
	5	unused		
	6	RD-	RD-	Receive data -
	7	unused		
	8	unused		
	9	NET_ACT	O/P	Net active led
	10			
	11	NET_SPD	O/P	Net speed led
	12			
J2	1	GPIO0	BI	GPIO
	2	GPIO4	BI	GPIO
	3	GPIO1	BI	GPIO
	4	GPIO5	BI	GPIO
	5	GPIO2	BI	GPIO
	6	GPIO6	BI	GPIO
	7	GPIO3	BI	GPIO
	8	GPIO7	BI	GPIO
	9	GND	Power	Ground
	10	3V3	Power	3.3V power suply
J3	1[1]	IO0/RESET1/CSN3	BI	Spare I/O / Reset / C-BUS chip select
	2	CSN1	O/P	C-BUS 1 chip select
	3	IO1	BI	Spare I/O
	4	CDATA1	O/P	C-BUS 1 command data
	5	IO2	BI	Spare I/O

CONNECTOR PINOUT				
Connector Ref.	**Connector Pin No.**	**Signal Name**	**Signal Type**	**Description**
	6	SCLK1	O/P	C-BUS 1 serial clock
	7	IO3	BI	Spare I/O
	8	RDATA1	I/P	C-BUS 1 reply data
	9	IO4	BI	Spare I/O
	10	IRQN1	I/P	C-BUS 1 interrupt request
	11,12	GND	Power	Ground
	13	BOOTEN1_1	O/P	Hardware boot control
	14	BOOTEN1_2	O/P	Hardware boot control
	15	n/c		
	16	IO5	BI	Spare I/O
	17	IO6	BI	Spare I/O
	18	IO7	BI	Spare I/O
	19	n/c		
	20[2]	n/c or Power		
J4[3]	1,2	GND	Power	Ground
	3,4,5,6	5V	Power	+5.0V power supply
J5	1,2	GND	Power	Ground
	3,4,5,6	5V	Power	+5.0V power supply
J6	1	IRQN1	I/P	C-BUS 1 interrupt request
	2	RDATA1	I/P	C-BUS 1 reply data
	3	CDATA1	O/P	C-BUS 1 command data
	4	CSN1	O/P	C-BUS 1 chip select
	5	SCLK1	O/P	C-BUS 1 serial clock
	6	IO0/RESET1/CSN3	BI	Spare I/O / C-BUS chip select
	7	GND	Power	Ground
	8	GND	Power	Ground
	9,10,11,12	n/c		
	13	RXCLK	I/P	I^2S Receive Clock
	14	TXCLK	I/P	I^2S Transmit Clock
	15	RXFS	I/P	I^2S Receive Frame Select

CONNECTOR PINOUT				
Connector Ref.	**Connector Pin No.**	**Signal Name**	**Signal Type**	**Description**
	16	TXFS	I/P	I^2S Transmit Frame Select
	17	RXD	I/P	I^2S Receive Data
	18	TXD	O/P	I^2S Transmit Data
	19, 20	GND	Power	Ground
J7	1	IO8/RESET2	BI	Spare I/O
	2	CSN2	O/P	C-BUS 2 chip select
	3	IO9	BI	Spare I/O
	4	CDATA2	O/P	C-BUS 2 command data
	5	IO10	BI	Spare I/O
	6	SCLK2	O/P	C-BUS 2 serial clock
	7	IO11	BI	Spare I/O
	8	RDATA2	I/P	C-BUS 2 reply data
	9	IO12	BI	Spare I/O
	10	IRQN2	I/P	C-BUS 2 interrupt request
	11,12	GND	Power	Ground
	13	BOOTEN2_1	O/P	Hardware boot control
	14	BOOTEN2_2	O/P	Hardware boot control
	15	n/c		
	16	IO13	BI	Spare I/O
	17	IO14	BI	Spare I/O
	18	IO15	BI	Spare I/O
	19, 20	n/c		
J8	1,2	GND	Power	Ground
	3,4,5,6	5V	Power	+5.0V power supply
J9	1	VBUS		USB Mini B type connector - USB power supply
	2	D-		USB Mini B type connector - USB data signal (-)
	3	D+		USB Mini B type connector - USB data signal (+)
	4	n/c		

CONNECTOR PINOUT				
Connector Ref.	**Connector Pin No.**	**Signal Name**	**Signal Type**	**Description**
	5	GNDD		USB Mini B type connector - Digital ground
	6	SHELL		USB Mini B type connector - USB connector shell
	7	n/c		
J10	1	GND	Power	GND
	2	U2_TXD	O/P	Transmit data UART2
	3	U2_RXD	I/P	Receive data UART2
	4	5V	Power	5V Power supply
J11				
	1	GND	Power	GND
	2	VIN	Power	5V regulated power supply
J13	1	3V3	Power	
	2	SWIO/TMS	I/P	JTAG test mode select
	3	GND	Power	
	4	SWDCLK/TCLK	I/P	JTAG test clock
	5	GND	Power	
	6	SWO/TDO	O/P	JTAG test data output
	7	n/c		
	8	TDI	I/P	JTAG test data In
	9	GND	Power	
	10	RESET#	I/P	Reset. Active low

TEST POINTS		
Test Point Ref.	**Default Measurement**	**Description**
TP1	-	WAKEUP - Wake up from low power mode pin (input).
TP2	-	E_RXER - Ethernet receive error
TP3	+5V	+5V power supply
TP4	+3V3	+3V3 power supply
TP5	GND	Ground
TP6	GND	Ground
TP7	-	TRST
TP8	-	E_TX_CLOCK - ethernet clock input
TP9	12 MHz	XTAL - LPC4330 clock input

SWITCHES		
Switch Ref.	**Default Position**	**Description**
SW1	O/C	Push to reset the LPC4330 microprocessor

Notes:
I/P = Input
O/P = Output
BI = Bi-directional
O/C = Open circuit
DP = Differential Pair +
DM = Differential Pair -

Note[1] : pin J3-1 can be used as an extra CSN for the C-BUS1
Note[2]: used for providing power supply when isolators are fitted
Note[3] : J3 and J4 connectors can be isolated

6 Circuit Schematics and Board Layouts

For clarity, circuit schematics are available as separate high-resolution files. These can be obtained via the CML website.

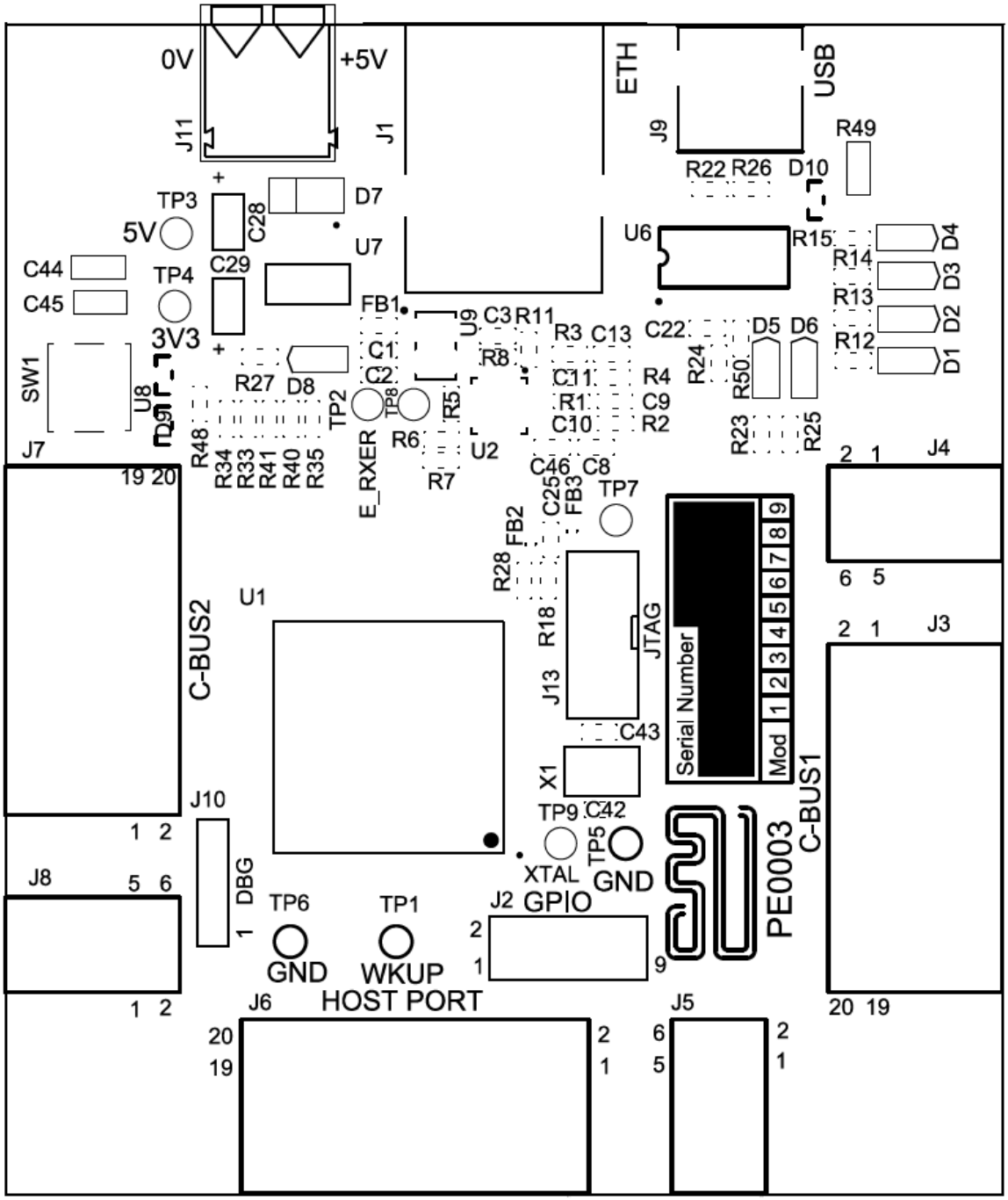

Figure 2 PE0003 Interface Card Top Layout

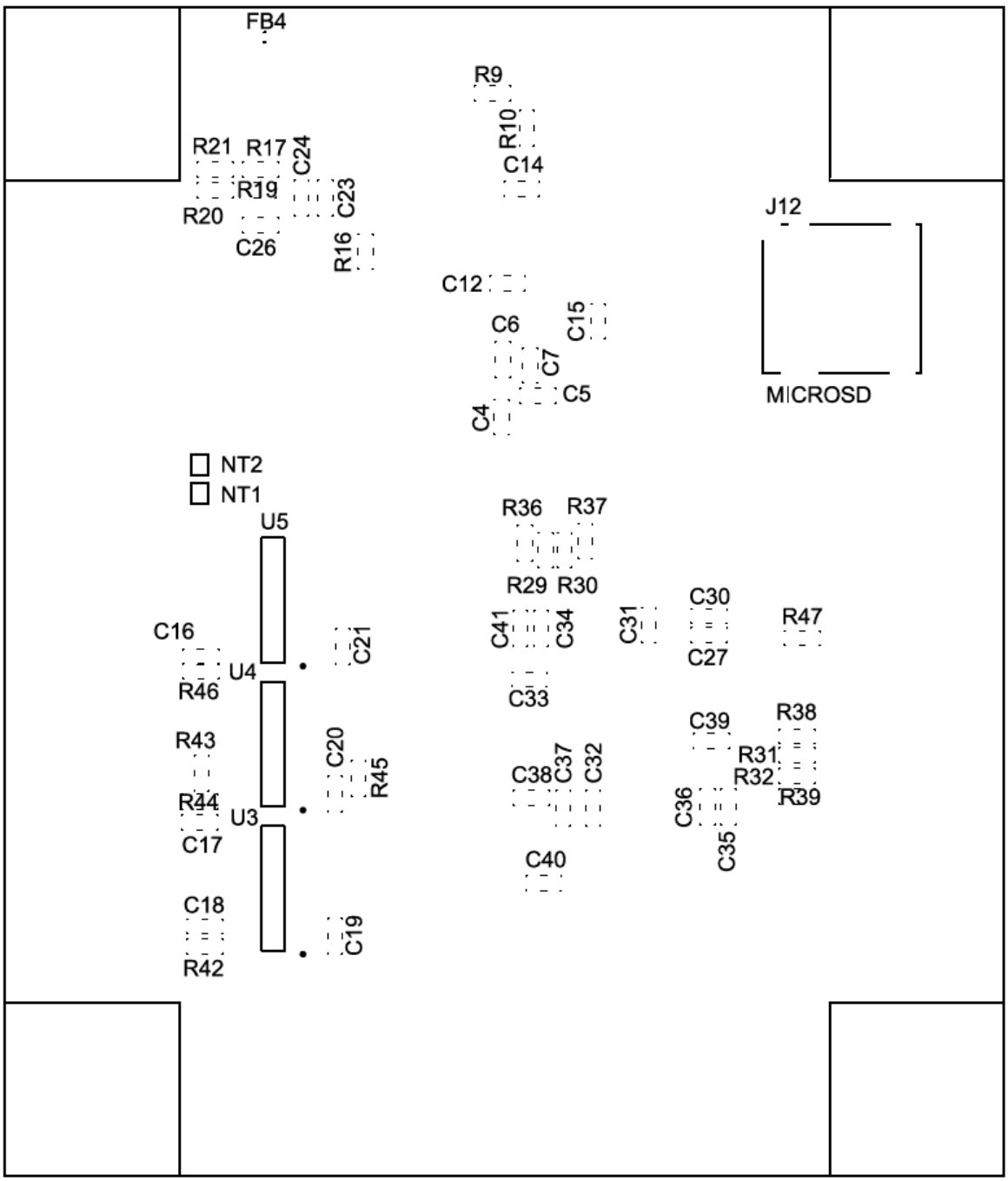

Figure 3 PE0003 Interface Card Bottom Layout

7 Detailed Description

7.1 Hardware Description

The board is fitted with a voltage regulator, U7, providing the +3.3V digital supply rail. The input to this regulator is provided by an external un-regulated power supply at, nominally, 5V DC, which is connected to the board via connector J11 (2-position terminal block). The external unregulated power supply is available at connectors J4 and J8 (right-angle female headers) for mating to target cards at C-BUS1 and C-BUS2 respectively. Similarly connector J5 for the mating to target cards at the host port.

The nominal 5V supply and the +3.3V regulated supply voltage levels can be monitored on test points TP3 and TP4 respectively.

Digital grounds are on test points TP5 and TP6.

D8 will illuminate, confirming presence of the on-board regulated +3.3V DC digital voltage supply.

The PE0003 uses the NXP LPC4330 microprocessor which combines a 32-bit ARM Cortex-M4 and a 32-bit ARM Cortex-M0 co-processor. The LPC4330 runs at 204MHz, has 264 kB of SRAM a USB and Ethernet interface. The LPC4330 toolchain from NXP, including low cost debugging tools, can be used with the PE0003. The board uses a 12MHz integrated crystal as clock source for the LPC4330 processor. The internal PLLs generate the 204MHz clock signals.

Two LPC4330 SSP controllers are utilised for C-BUS1 and C-BUS2 and an I^2S controller, combined with a the C-BUS1 SSP port utilised for the host port. The C-BUS ports have eight independent I/O pins on each C-BUS port. C-BUS 1 and C-BUS 2 operation can be multiplexed onto C-BUS 1 where pin 1 (IO0) of C-BUS1 provides the second CSN signal.

The PE0003 offers improved performance over the PE0002 C-BUS with better processing, and faster and completely independent, not multiplexed, C-BUS ports. The layout has been optimised to reduce both radiated and conducted noise emissions from the board.
Isolators can be fitted at C-BUS1 to galvanically isolate the target card from the PE0003. This can increase the noise immunity, particularly that caused by conducted noise and ground loops.

There are eight software-configurable general purpose I/O signals available at connector J2 and four software-configurable LEDs.

A Micro-SD Card interface has been added to store Function Images and their respective activation codes for convenience. The micro-SD card also stores the logged data from the Trace function. Data captured using the Host port is stored and read from a binary file that is created on the card. It is also possible to use the micro SD-card for data storage. The card is formatted for the FAT-32 file system.

The link to a host PC is via a full speed USB 2.0 port via connector J9. A footprint is provided for an Ethernet port at J1. There is no support for Ethernet.

7.1.1 C-BUS Interface

The C-BUS interfaces transfer data control and status information between the target device's internal registers and the microprocessor over the C-BUS serial bus. Each transaction consists of a single register address byte sent from the microprocessor, which may be followed by one or more data bytes sent from the microprocessor to be written into one of the target device's registers, or one or more bytes of data read out from one of the target device's registers, as illustrated in Figure 4.

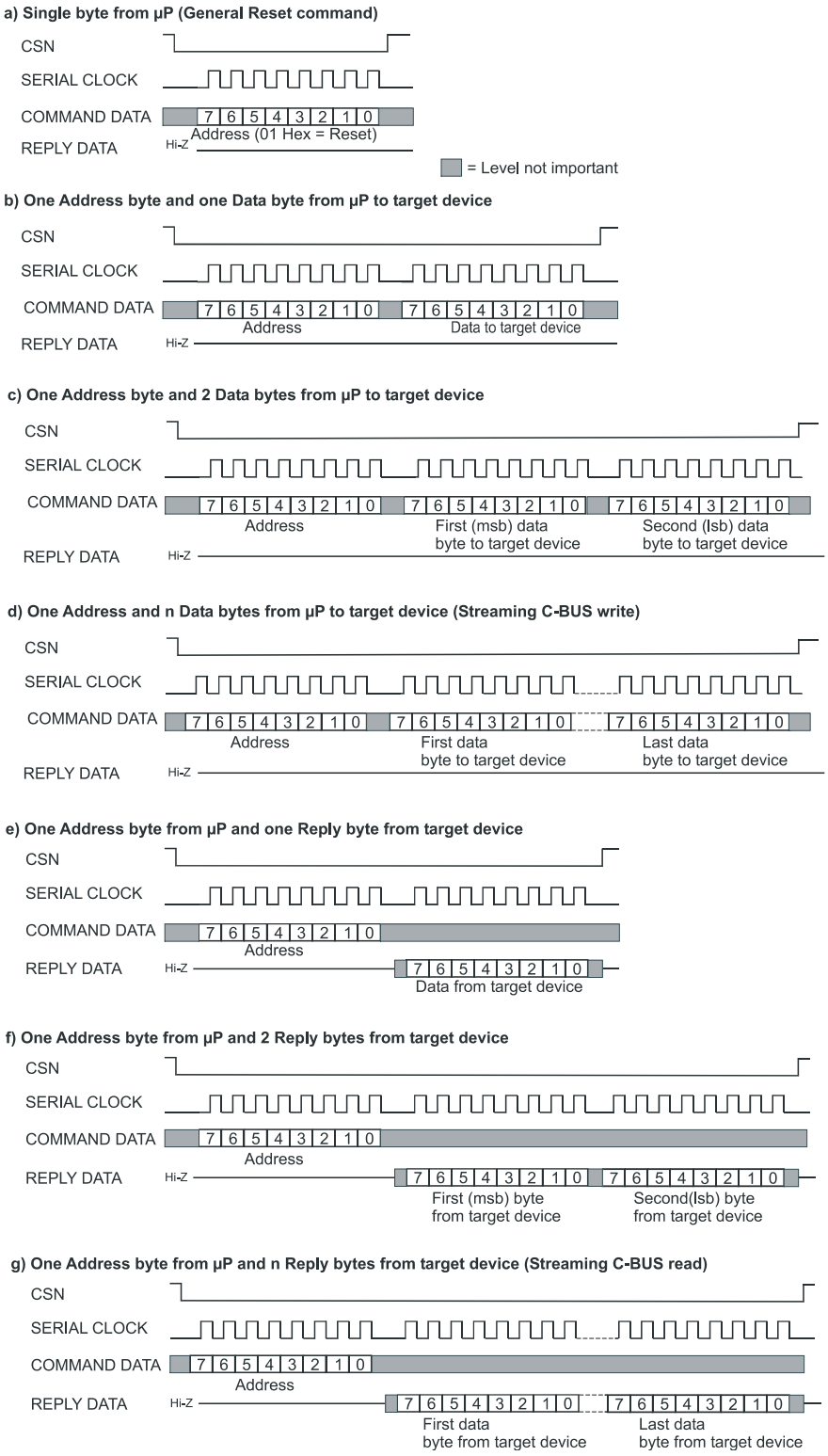

Figure 4 C-BUS Transactions

All writes and reads to C-BUS1/2 occur via the SSP0/1 peripherals of the LPC4330 Microprocessor.

Two different target devices can be selected by taking CSN1 or CSN2 low on connectors J3 and J7 respectively. If C-BUS1 and C-BUS2 are multiplexed, then C-BUS1/2 signals are routed to J3 and CSN2 is routed to J3:1.

The target device can issue an interrupt by taking IRQN1 or IRQN2 low on connectors J3 and J7 respectively.

7.1.2 Galvanic Isolation of C-BUS1

The PE0003 has been designed to minimise radiated and conducted noise. If galvanic isolation is required between the PE0003 and the target card, NVE IL715 and IL716 isolators or equivalent can be fitted at C-BUS1. The following steps must be completed:

- On the bottom side of the board, cut the net ties placed within the footprints for U3, U4 and U5, see Figure 3, to isolate the C-BUS1 port
- If the power connector, J4, mates to the target card, cut net ties NT1 and NT2. Pin 20 of C-BUS 1 must be wired to supply power to the isolated side of the PE0003.
- Fit an IL716 at U4 and a UL715 at both U5 and U3. U3 need only be fitted if the signals BOOTEN1, BOOTEN2, IO5 and IO6 are required.
- Fit decoupling components C16, C17, C18, C19, C20, C21, R42, R44, R46, R43 and R45.

Note that if isolation is used signals IO3, IO4 and IO7, J3 pins 7, 9 and 18 respectively, must NOT be connected on the target card because these IO signals are not isolated.

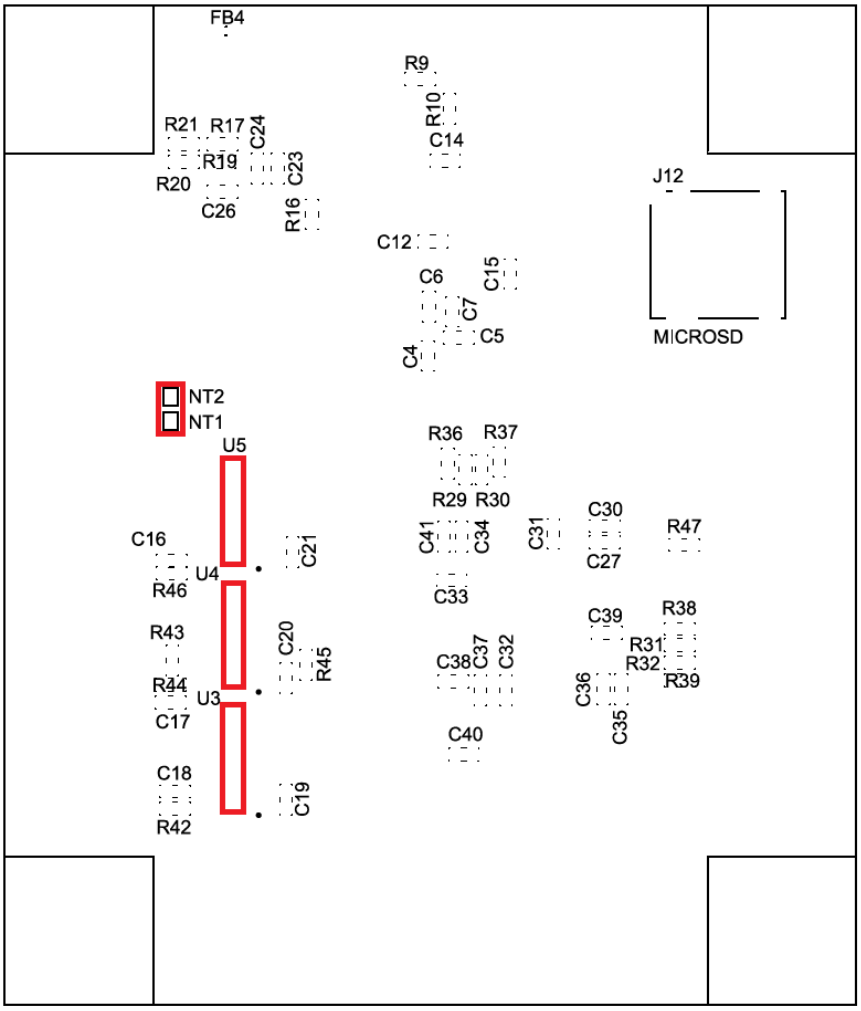

Figure 5 Net Tie Locations

7.1.3 Multiplexing C-BUS2 onto C-BUS1

C-BUS1 and C-BUS2 signals can be multiplexed onto C-BUS1 port, J3. This feature allows two independent C-BUS or SPI devices to be addressed via one C-BUS port. To enable C-BUS multiplexing, check one of the 'Multiplex C-BUS1/2' checkboxes in the PE0003 GUI.

The following C-BUS2 signals are directed to C-BUS1:

CDATA2 multiplexes onto CDATA1
RDATA2 multiplexes onto RDATA1
SCLK2 multiplexes onto SCLK1

Pin 2 of C-BUS1 port J3 will be reconfigured as CSN2. The normal default function, IO0, will be disabled. C-BUS2 on connector J7 will also be disabled. To select C-BUS1 or C-BUS2 when 'multiplex C-BUS1/2' is selected, use the C-BUS checkbox or the Device command in scripts.

7.1.4 Host Port

The Host Port is a merge of C-BUS1 and an I²S port. Pins 1 to 6 are mapped to C-BUS 1 and pins 13 to 19 are mapped to the I²S port. The I²S port consists of three lines for transmission and three

for reception. Those three lines are a continuous serial clock, RXCLK/TXCLK, a Frame Sync, RXFS/TXFS (also known as word select WS) and serial data, RXD/TXD.

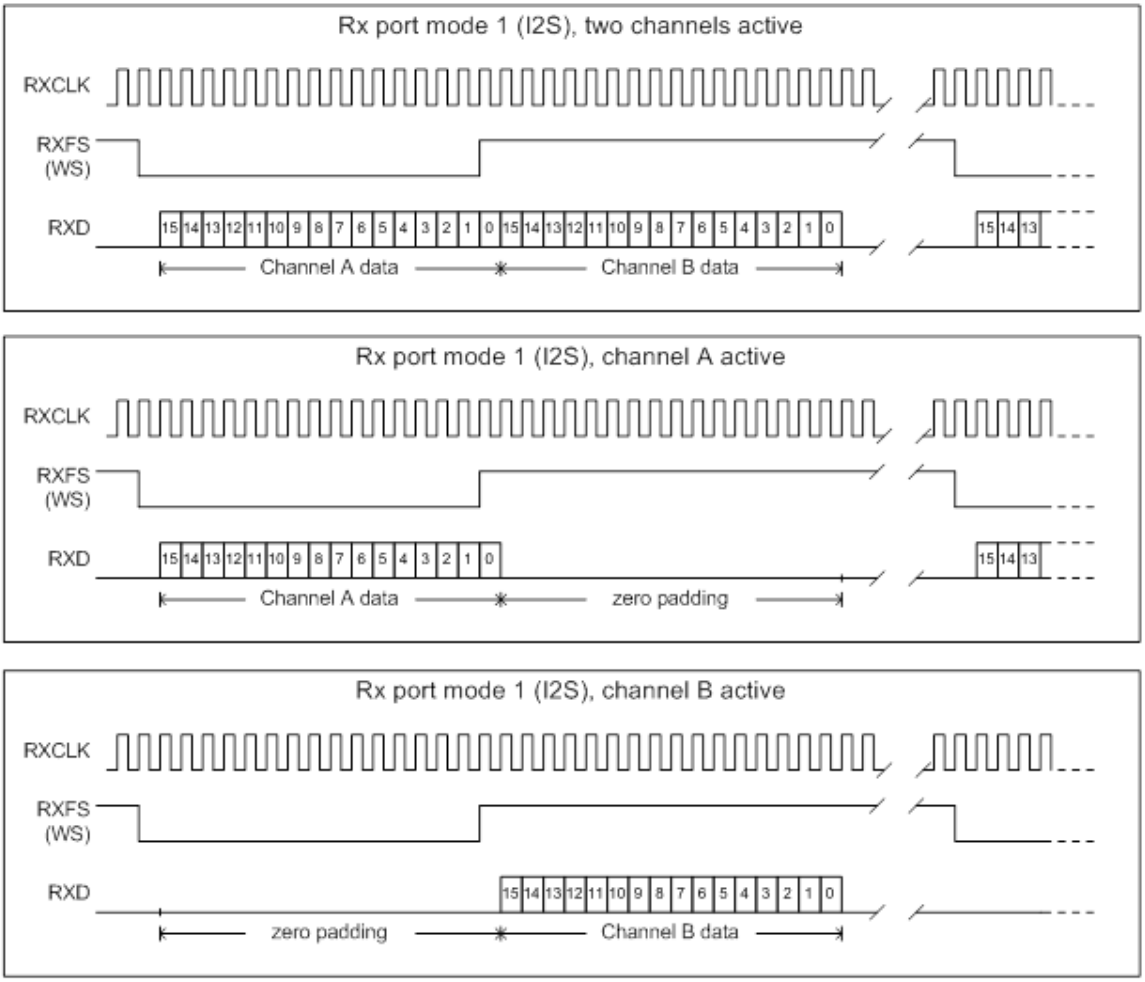

Figure 6 Rx I²S Timing (identical for Tx)

7.2 Adjustments and Controls

There are no adjustments required on the PE0003. All controls are in the GUI.

7.3 Embedded Software Description

On power up the microprocessor will monitor the USB port to download the firmware from the host PC to the internal memory of the microprocessor and will jump to the start address of the firmware when requested by the host PC.

7.4 Software Description

A single application ‘ES0003xx.EXE’ running in a Windows environment supports a range of target cards. Visit the CML website for the latest information.

When the ES0003xx.EXE application is run, if communication cannot be established a message box will be displayed to indicate the failure. If the message box in Figure 7 is displayed, press the Reset Switch SW1 on the PE0003. The firmware is automatically downloaded to the PE0003 board and the application GUI will be displayed.

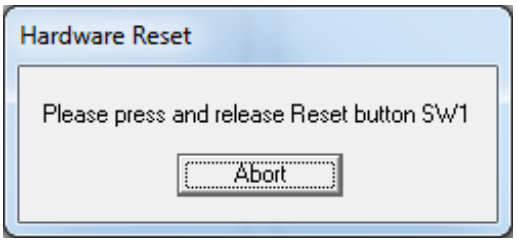

Figure 7 Start Message Box

There are five tabs within the main application dialog and these are described in the following sections.

More than one PE0003 can be connected to a single PC. When plugging in an additional PE0003, Windows will request suitable drivers. Use the 'Let Windows search for drivers' option as these will already be available from the initial installation. A separate instance of the GUI must be started for each PE0003. The PC resources will be shared between each instance. The Options menu allows the PE0003 to be named, with the name shown in the GUI caption.

By default the GUI is configured to operate the C-BUS ports at 10MHz. A pop-up message is displayed to remind the user that the C-BUS operates at 10MHz by default. This message can be removed by clicking on the “Do not show this message again” checkbox. Ensure that the target device supports the C-BUS frequency or change it via the Options menu.

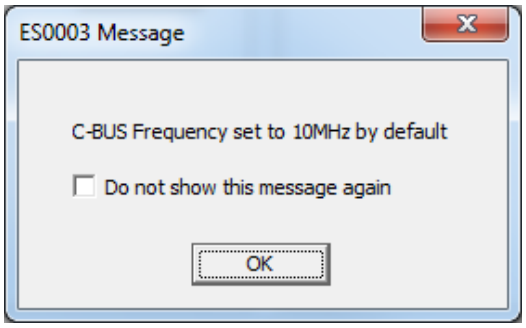

Figure 8 C-BUS Frequency Warning Message

Note: The C-BUS side of the HOST PORT is controlled with C-BUS 1.

7.4.1 The C-BUS Control Tab

This tab provides basic C-BUS read, write and general reset functions. Each character entered into the Register Address and Register Data edit boxes is checked to ensure that it is a valid

hexadecimal value. The radio buttons select an 8-bit or 16-bit read/write operation. The lengths of the entered values are limited to 2 hexadecimal characters (1 byte) for read or write register addresses and 2 or 4 hexadecimal characters (1 or 2 bytes) for the register write data. The General Reset button writes 01_H to the Target Device. The radio buttons select read/write operation to the CMX{target} device 1 using CSN1 on connector J5 or to the Target Device 2 using CSN2 on connector J3.

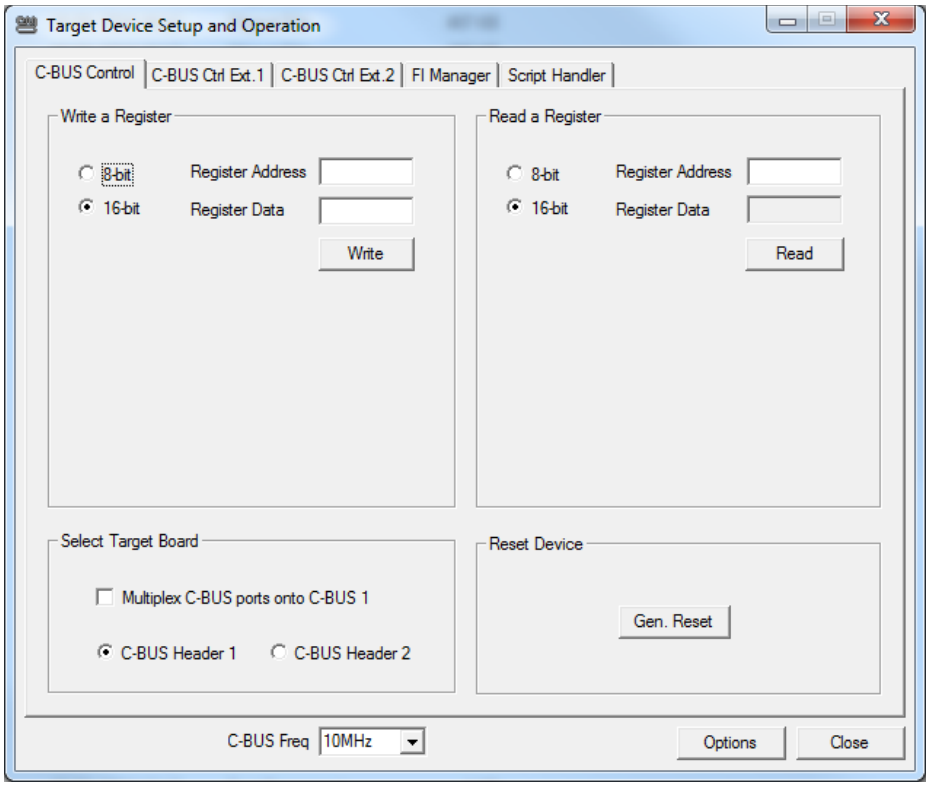

Figure 9 C-BUS Control Tab

The C-BUS frequency can be set in the small drop-down selection box at the bottom of the dialog or by clicking on the options button.

7.4.2 The C-BUS Control Extended Tab (C-BUS Ctrl Ext. 1 and 2)

This tab provides multiple C-BUS read and write functions. Each row in the table represents a single C-BUS register. Select the C-BUS register type from the drop down list. The Update button and the Data edit box will be configured according to the selection. Each character entered into the Address and Data edit boxes is checked to ensure that it is a valid hexadecimal value. The lengths of the entered values are limited to 2 hexadecimal characters (1 byte) for register addresses and 2 or 4 hexadecimal characters (1 or 2 bytes) for the register data. Click the Update button to read or write a single C-BUS register. For multiple C-BUS read or write operations select the C-BUS registers using the Selected checkboxes and click on the 'Wr all', 'Rd all' or 'Wr\Rd all' buttons. Click on the 'Wr all' button to write all the selected write type C-BUS registers. Click on the 'Rd all' button to read all the selected read type C-BUS registers. Click on the 'Wr\Rd all' button to read or write all the selected C-BUS registers.

Click on the 'Clear all' button to reset the table. Click on the 'Clear data' button to reset the Data edit boxes.

When the ‘Lock’ button is selected the Description, Address and Type controls are disabled, preventing accidental changes.

Use the ‘Save Config…’ button to save the current table. The Description, Address, Type, Data and Enable columns are saved in the specified file. Use the ‘Open Config…’ button to load a previously saved table.

The radio buttons select read/write operation to the Target Device 1 using CSN1 on connector J3 or to the Target Device 2 using CSN2 on connector J7.

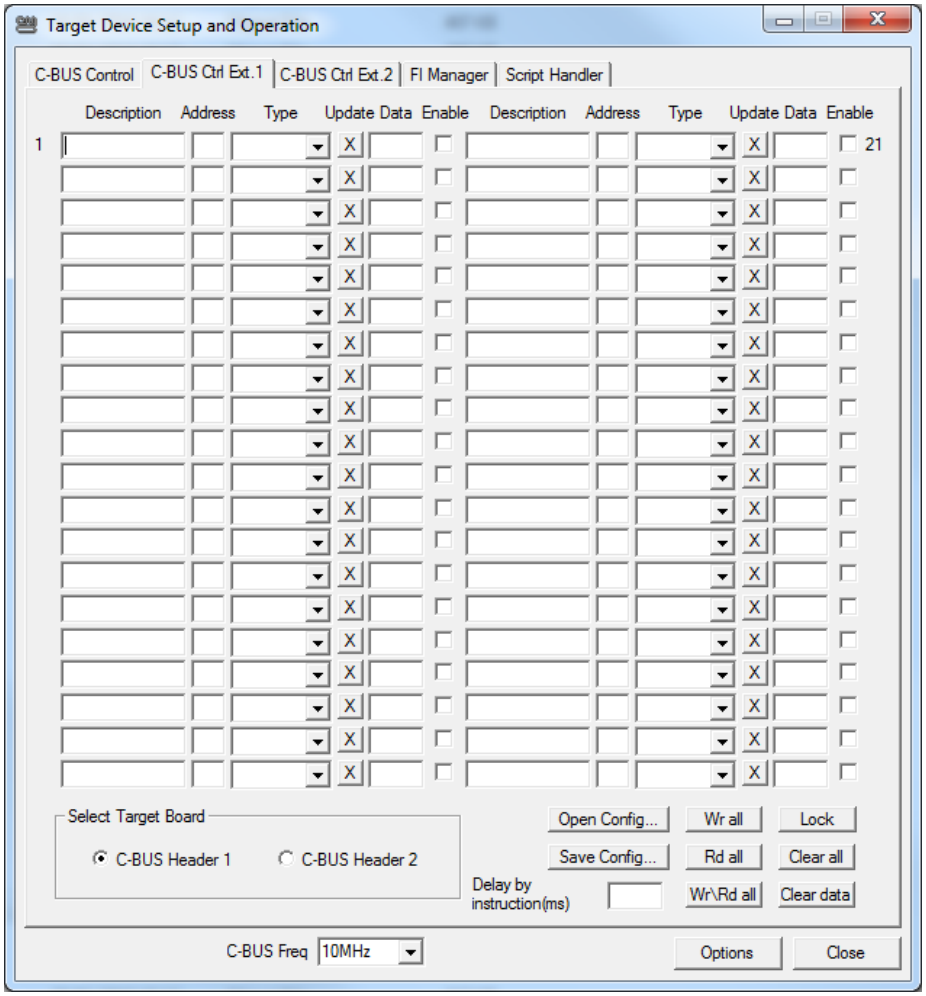

Figure 10 C-BUS Control Extended Tab

7.4.3 The FI Manager Tab

This tab provides Function Image load and activation utilities for *FirmASIC*® products. The operation of this tab is described in the user manuals of the Target Cards to which it applies. The source and the destination of the Function Image must be initially selected. The GUI will limit the options to those that are available depending on the selected source. The selected destination may limit the choices further. The GUI de-activates and greys out incorrect configurations.

Source is PC:

Select the Destination (Target C-BUS 1, Target C-BUS 2 or SD Card).

Enter the filename and path of the required Function Image. Alternatively, use the file browser by clicking the Browse button.
Enter the Activation Code, if required**.** The Activation code can be typed in, selected from the drop-down list or selected from a previously created list using the Activation Codes button.
Click Load. The GUI will load the Function Image to the selected destination and signal success or failure. A progress bar will be displayed for longer operations.

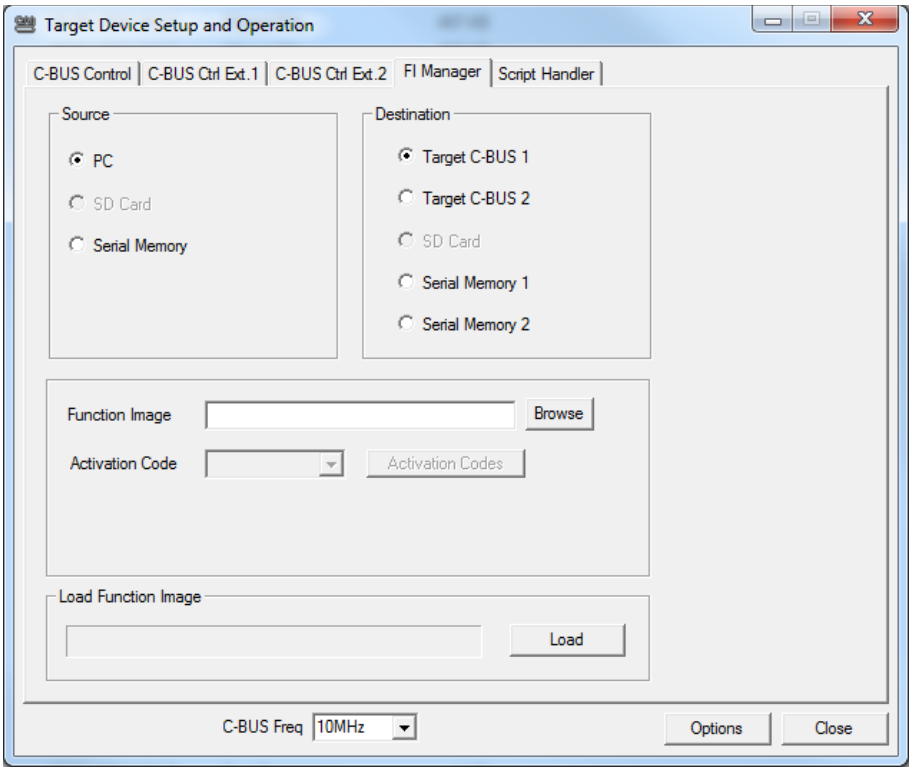

Figure 11 FI Manager Tab (PC as source)

Source is PC:

Select the Destination (Serial Memory 1 or Serial Memory 2).
If the destination is the serial memory (only for ev kits with serial memory available), the GUI asks for the file with the FI and a thick stub (snippet of code to take the data through the Target Device to the memory).

Enter the filename and path of the required Function Image. Alternatively, use the file browser by clicking the Browse button.
Enter the filename and path of the Thick Stub for the *FirmASIC* device and serial memory type. Alternatively, use the file browser by clicking the Browse button.
Click Load. The GUI will load the Thick Stub and then the Function Image to the selected destination and signal success or failure. A progress bar will be displayed for longer operations.

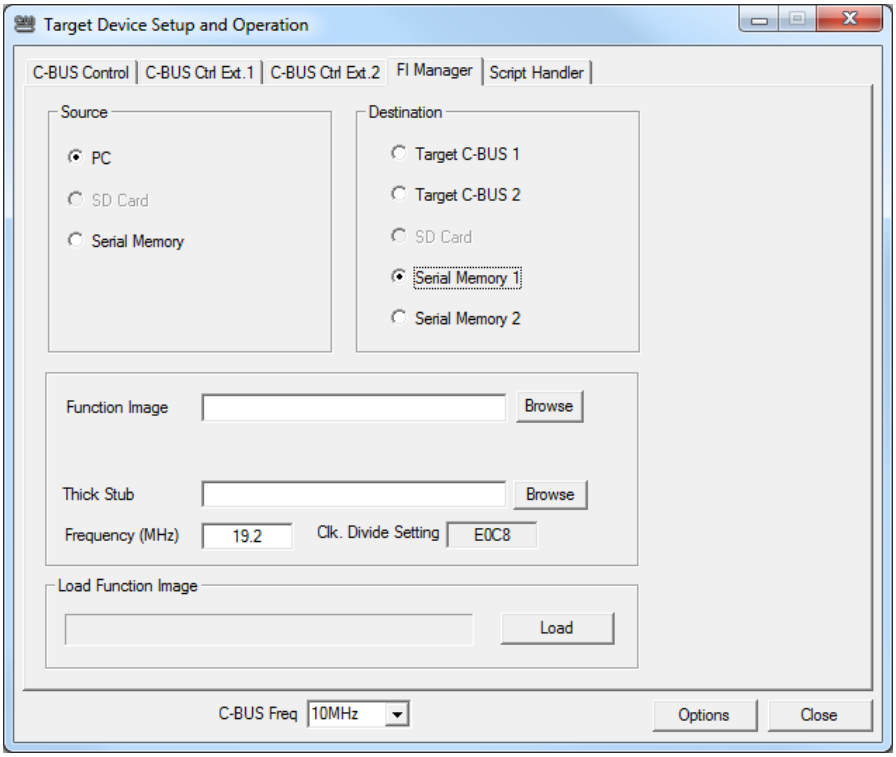

Figure 12 FI Manager Tab (serial memory as destination)

For loading the FI from serial memory, select source Serial Memory and destination the C-BUS port which the Target Card is connected.

Source is Serial Memory:

To program the target from serial memory the previous step is required.
Select the Destination, Target C-BUS 1 or Target C-BUS 2.
Enter the filename and path of the required Function Image.
Enter the Activation Code (if required)**.** The Activation code can be typed in, selected from the drop-down list or selected from a previously created list using the Activation Codes button.
Function Images normally come with an activation .txt file. This file can be loaded into the activation codes table when the Activation Codes button is clicked.
Click Load. The GUI will load the Function Image to the selected destination, activate the Function Image and signal success or failure. A progress bar will be displayed for longer operations.

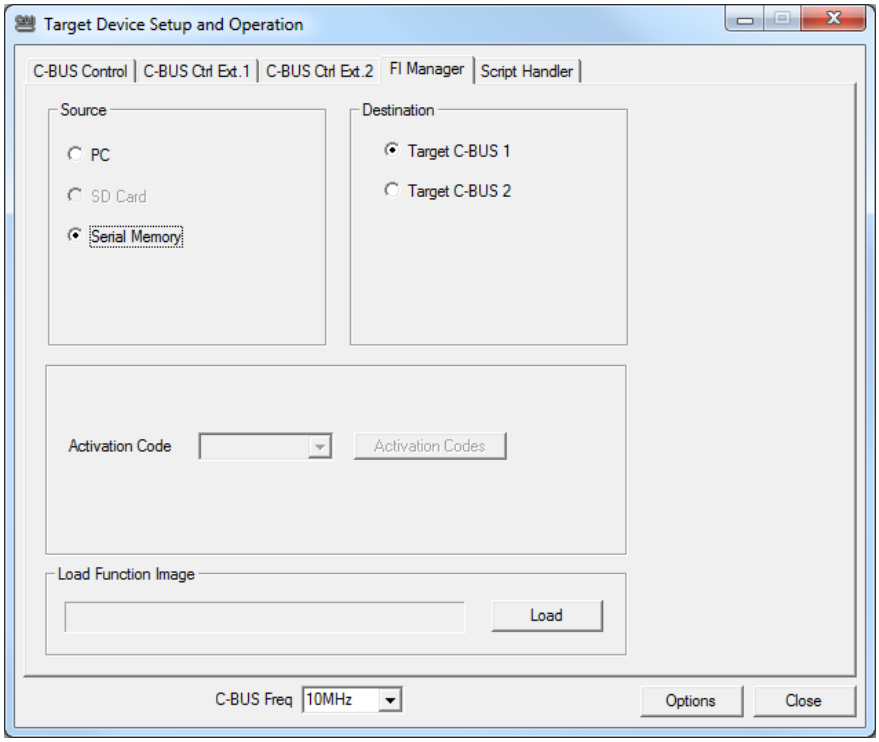

Figure 13 FI Manager Tab (serial memory as source)

Loading the Function Image from the SD card

A Function Image should have been loaded into the SD card by selecting PC as source and SD card as destination. It may also be necessary to store the activation codes. The FI is stored on the SD card as an enhanced binary file (with extension .ebi). This is basically a binary file with small changes of the data. The activation code is stored with the prefix 'act_'.

The required FI can then be loaded by selecting it from the list. Double click the FI name or select it and click the Load button. If there is a file containing the prefix 'act_' with the same filename as the selected FI (activation code file) the GUI loads the FI and activation codes. If the 'act_' file is not present only the FI will be loaded.

Note: if an activation code is required, but not provided, the FI will not run and the Target Device will be inactive.

Source is SD card:

Select the Destination, Target C-BUS 1 or Target C-BUS 2
Select the required Function Image™ from the displayed list. Function Images will only be displayed if they have been previously saved to the SD Card. Activation Codes will only be displayed if they have been previously saved to the SD Card. The activation code is loaded if the file 'act_filename' is present. If the FI does not require an activation code that file should be removed. If the FI uses a different activation code the file must be reloaded with the new activation code.

Click Load. The GUI will load the Function Image™ directly into the Target Card at the selected destination, activate the Function Image™ and signal success or failure. A progress bar will be displayed for longer operations.

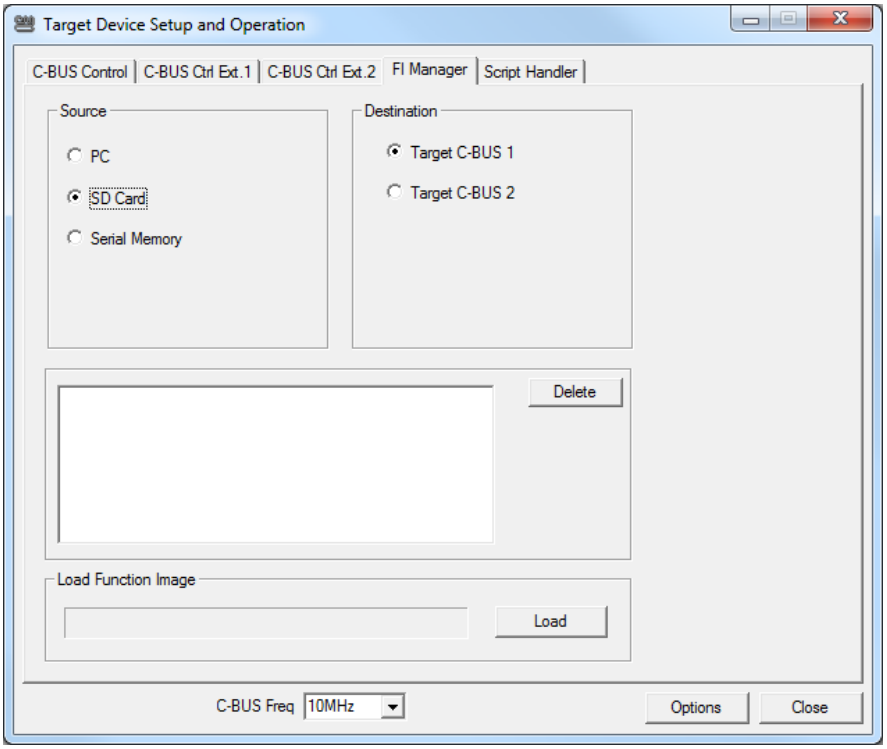

Figure 14 FI Manager Tab (SD card as source)

7.4.4 The Script Handler Tab

The Script Handler tab allows the execution of scripts. These are plain text files on the PC which are compiled by the GUI, but executed by the LPC4330 Microprocessor on the board. The script language is documented separately in the “Script Language Reference” document, which can be downloaded with the PE0003 support package from the CML website.

To select a script file, click on the ‘Select Script’ button. The Open File Dialog is displayed. Browse and select the script file. The folder that contains the script file will be the working folder of the script (i.e. all the files referenced in the script will be searched in this folder). Alternatively, select a script file from the recent files list. Click on the ‘>’ button to display the list.

The results window displays the values returned by the script. These results can be saved to a text file or discarded by clicking on the ‘Save Results’ or ‘Clear Results’ buttons, respectively. When a script file is being executed the ‘Run Script’ button will change to be the ‘Abort’ button, the rest of the tab will be disabled and the other tabs cannot be selected.

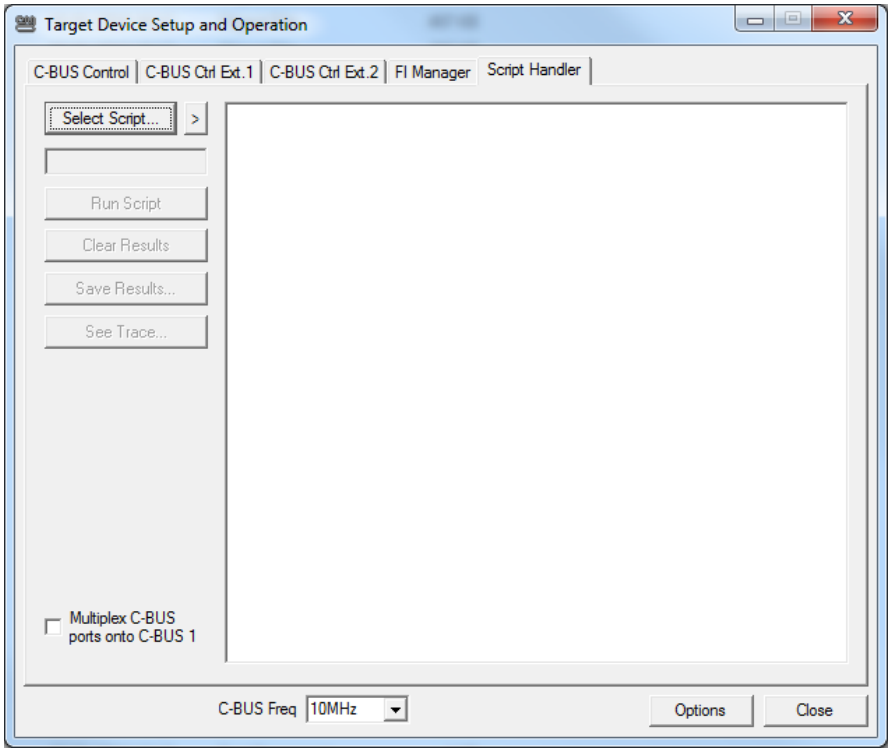

Figure 15 Script Handler Tab

7.4.5 The Trace Function

After a script has finished running and when trace data is available, the 'See Trace…' button will be enabled. Up to 131072 C-BUS transactions can be logged in the PE0003 board. Click in the 'See Trace…' button to display the Trace dialog box. Note that the C-BUS transactions are only logged if the feature has been enabled in the script. See the "Script Language Reference" document for details.

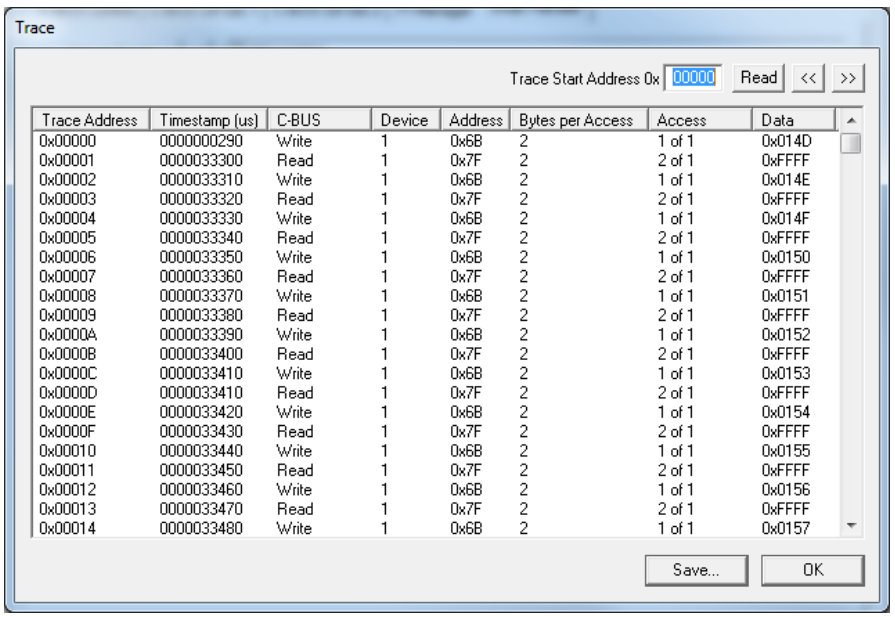

Figure 16 Trace Dialog Box

Click on the '<<' or '>>' buttons to upload and display the next or previous C-BUS transaction data block. Click on the 'Read' button to upload and display the C-BUS transaction data block starting at the address displayed in the Trace Start Address edit box. Use the 'Save…' button to save the trace data to a file.

7.4.6 The Options Dialog Box

Click on the 'Options' button on the main application dialog to display the 'Options' dialog box.

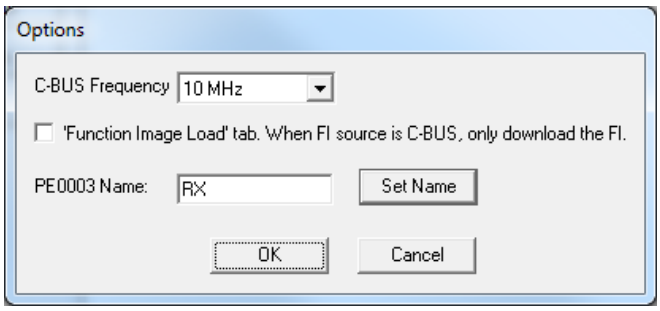

Figure 17 Options Dialog Box

Use the 'C-BUS Frequency' drop down list to select the C-BUS clock frequency for all C-BUS transactions between the PE0003 and the Target Card. This option is set to 10MHz by default.

With the 'Function Image Load tab. When the FI source is C-BUS, only download the FI' checkbox selected, no Activation Code, Checksum or Status register checking is performed when a Function Image™ is downloaded to the Target Card using the C-BUS source in the Function Image™ Load tab.

The PE0003 Name option allows the software to give a name to the PE0003 board. The name is displayed in the caption of the main window.

7.5 Evaluation Tests

Details of any Target Card specific tests are included in the relevant Target Card User Manual.

7.6 USB Driver Installation

Installation support is provided for Windows XP, Windows 7, Windows 8, Windows 8.1 and Windows 10. Windows XP is supported only via a legacy, unsigned driver because Microsoft has ended support for that operating system.

7.6.1 Windows 7 Driver Installation

Connect the PE0003 USB port, then power up the PE0003. A message will appear on the screen indicating that Windows has found new hardware and is attempting to install it. The automatic installation will fail and the following message will be displayed.

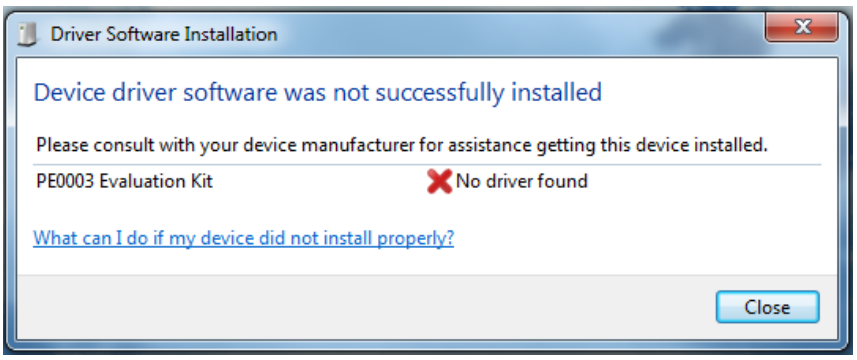

Figure 18 Windows 7 Automatic Installation Fail

Click Close. Open the Device Manager and locate the PE0003 Evaluation Kit as shown below.

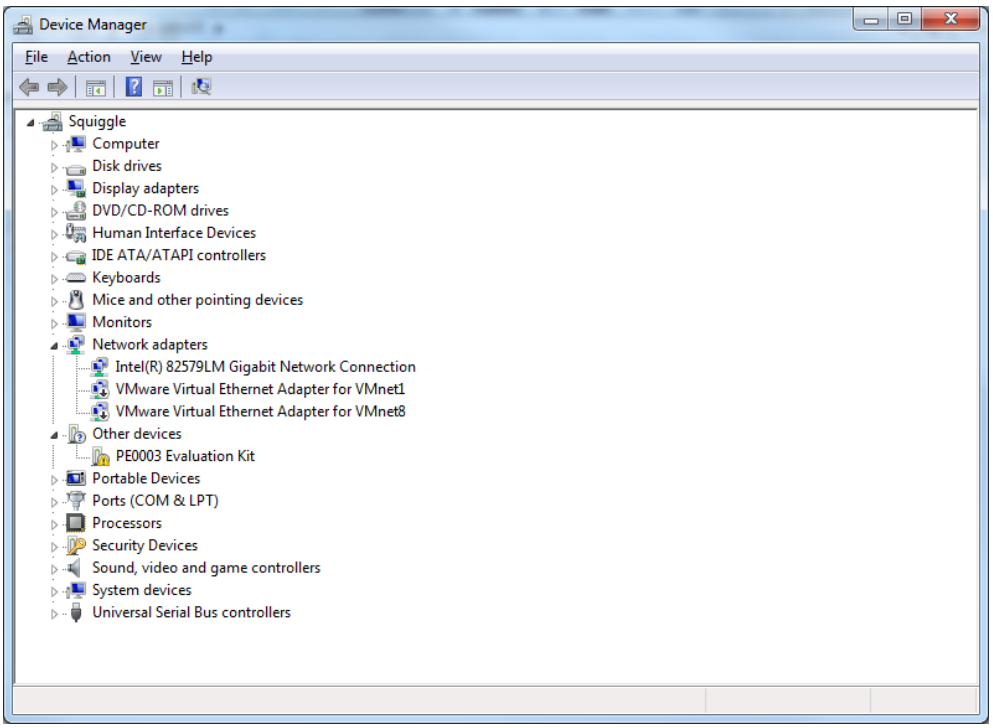

Figure 19 Device Manager List

Right click on the PE0003 Evaluation Kit and select Update Driver Software….

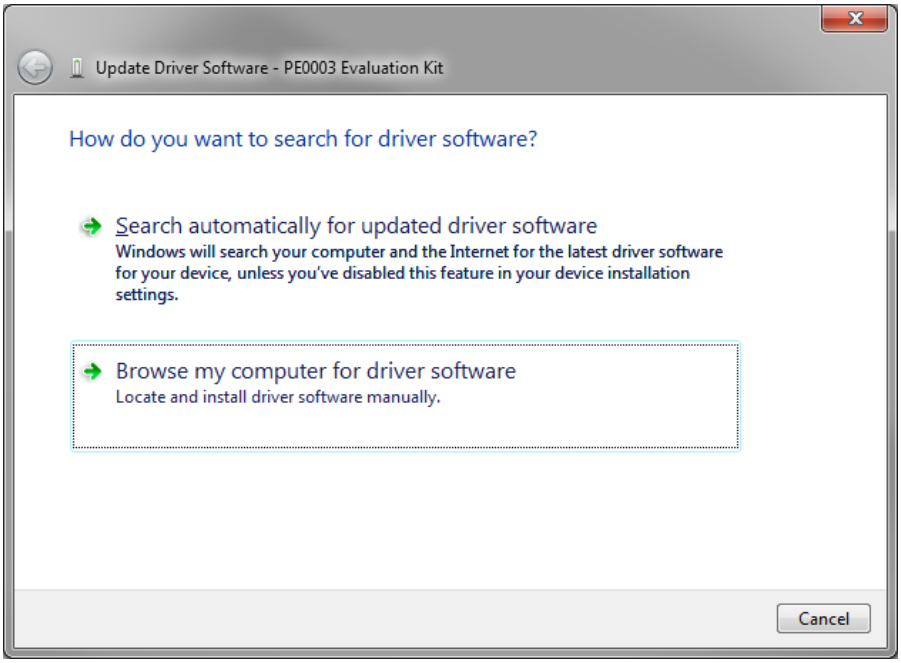

Figure 20 Update Driver Software (1)

Click Browse my computer for driver software and navigate to the location of the \ES0003\Driver folder.

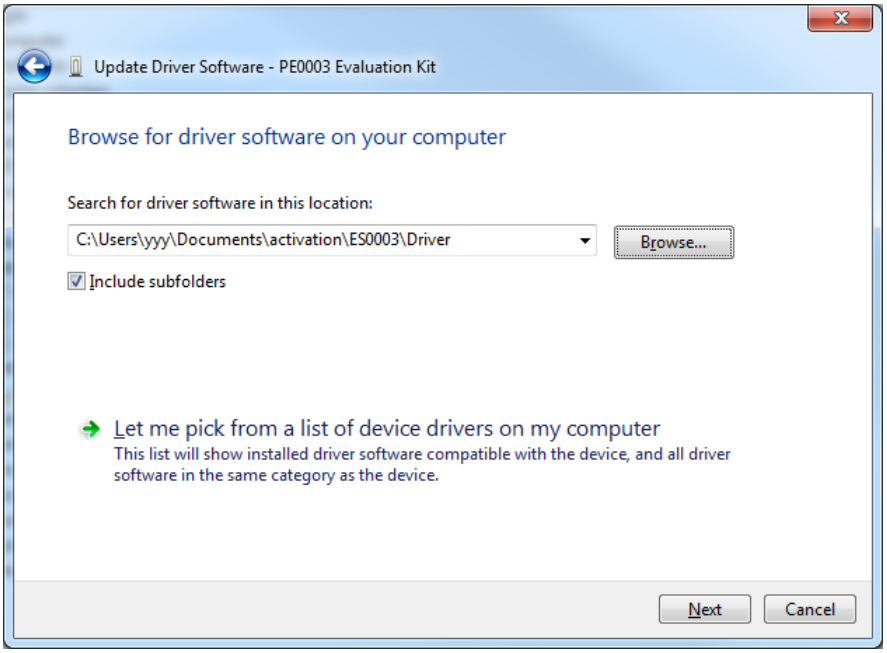

Figure 21 Update Driver Software (2)

Check Include subfolders and then click Next

Windows will now install the device driver and the PE0003 should be registered in the Device Manager under “Universal Serial Bus Controllers”. More than one PE0003 can be registered.

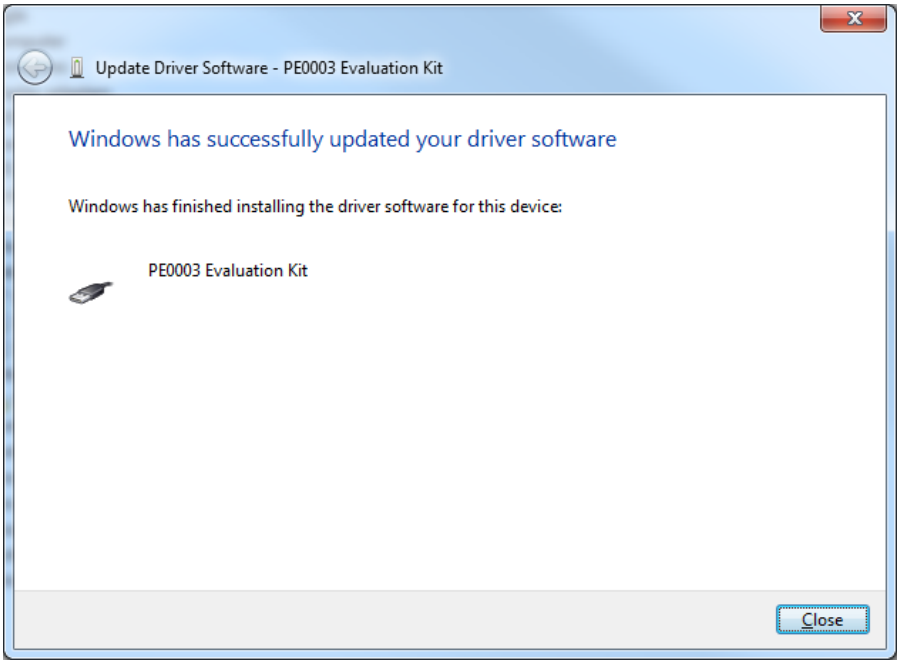

Figure 22 Update Driver Software (3)

7.6.2 Windows 8.x and Windows 10 Driver Installation

The process for installing Windows 8 and Windows 8.1 is similar to that for Windows 10.

Connect the PE0003 USB port, then power up the PE0003. A message will appear on the screen indicating that Windows has found new hardware and is attempting to install it. The automatic installation will fail and a message will be displayed in the sys tray reporting “Setup incomplete”.

Figure 23 Windows 10 Initial Connection Message

Click Close. Open the Device Manager and locate the PE0003 Evaluation Kit as shown below.

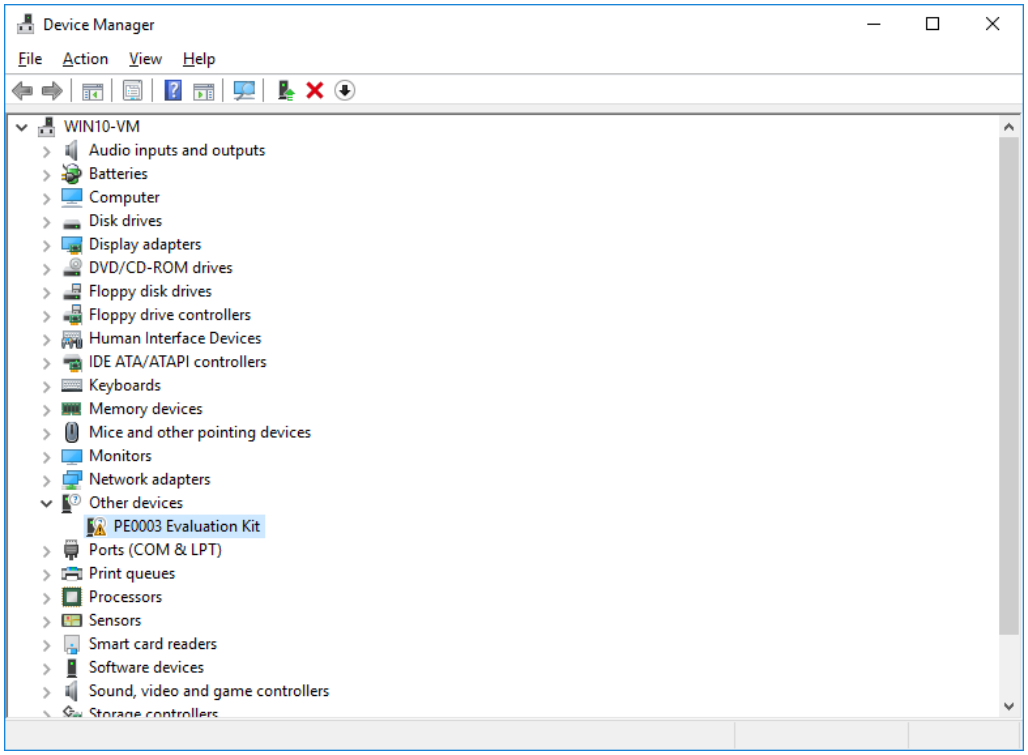

Figure 24 Windows 10 Device Manager List

Right click on the PE0003 Evaluation Kit and select Update Driver Software….

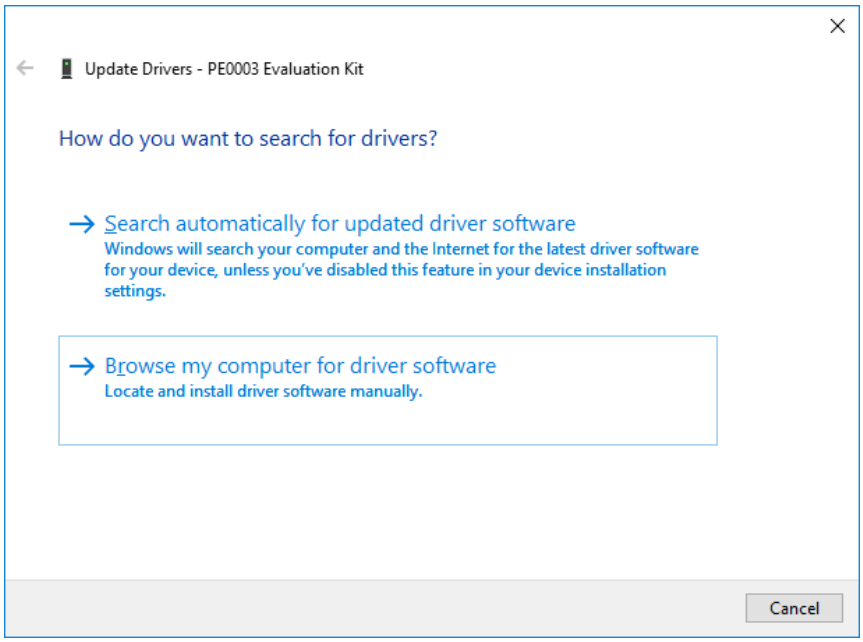

Figure 25 Windows 10 Update Driver Software (1)

Click Browse my computer for driver software and navigate to the location of the \ES0003\Driver folder.

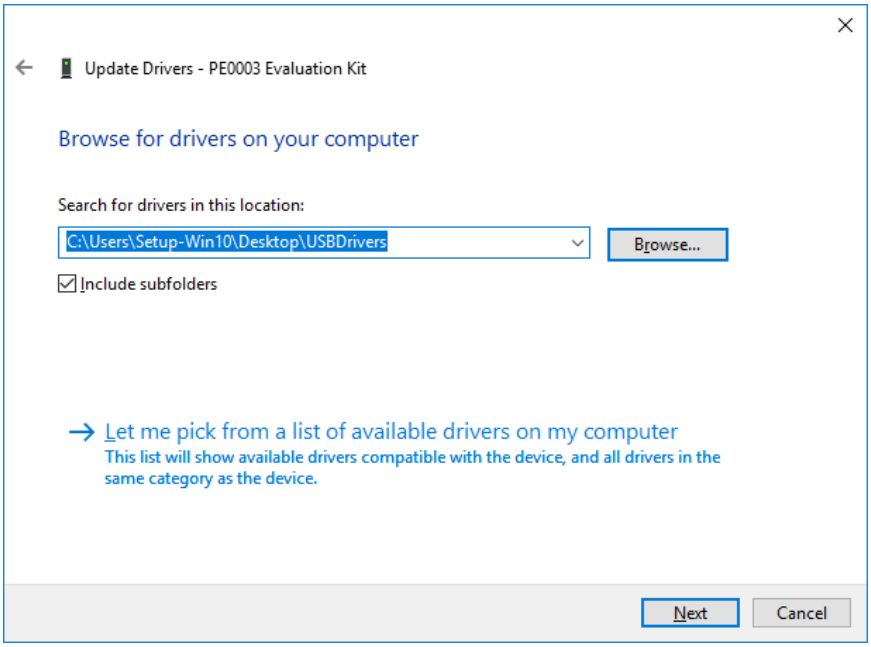

Figure 26 Windows 10 Update Driver Software (2)

Check Include subfolders and then click Next

Windows will now install the device driver and the PE0003 should be registered in the Device Manager under “Universal Serial Bus Controllers”. More than one PE0003 can be registered.

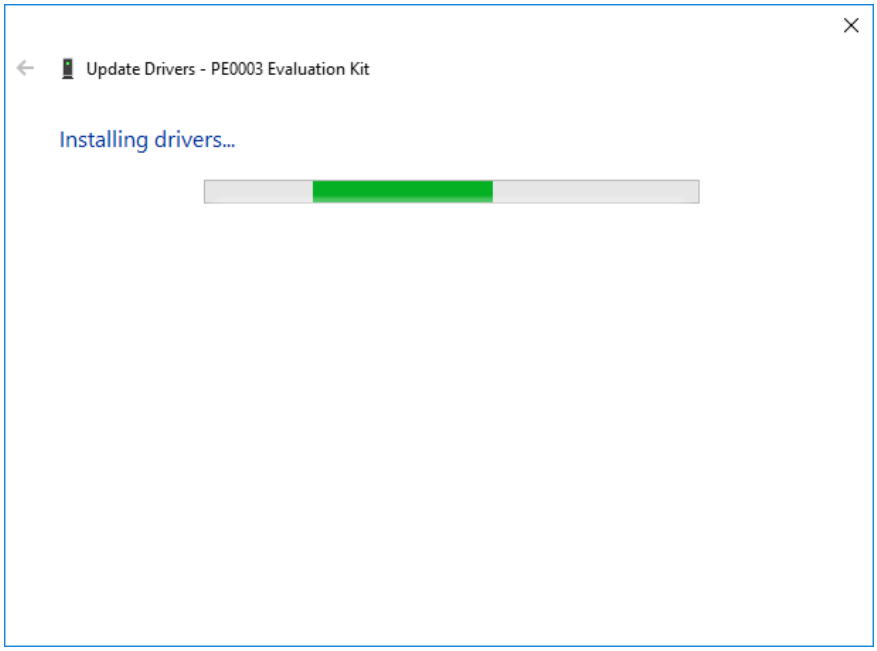

Figure 27 Windows 10 Update Driver Software (4)

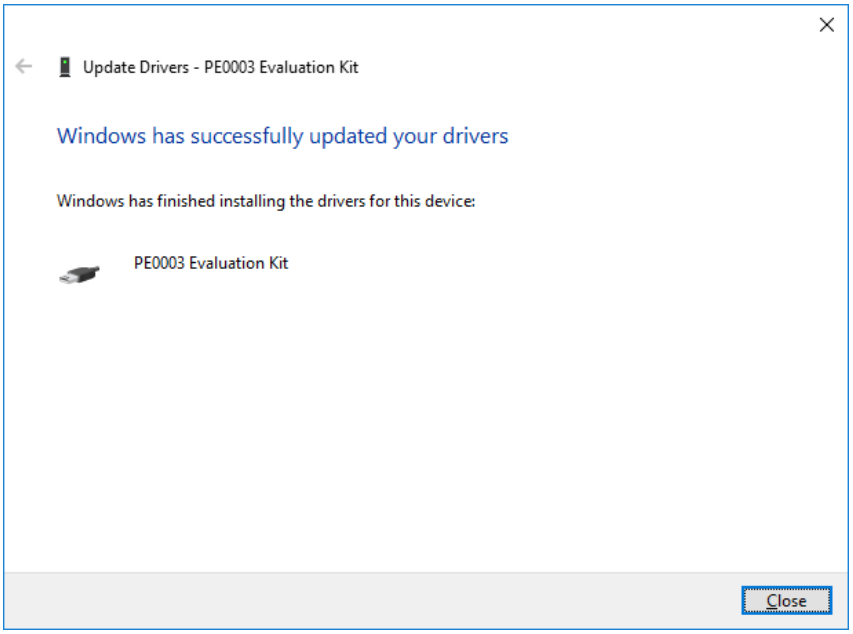

Figure 28 Windows 10 Update Driver Software (3)

7.6.3 Windows XP Driver Installation

For Windows XP users download the XP driver from the CML website.
Connect the PE0003 USB port to the PC and then power up the PE0003. The Found New Hardware Wizard will appear.

Figure 29 Found New Hardware Wizard (1)

Select No, not this time then click Next.

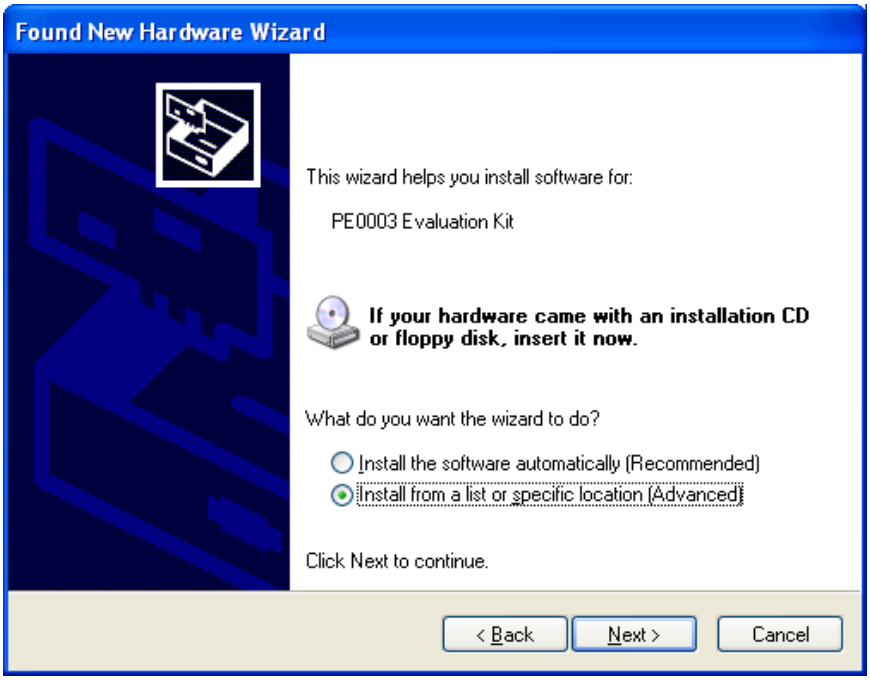

Figure 30 Found New Hardware Wizard (2)

Select Install from a list or specific location then click Next.

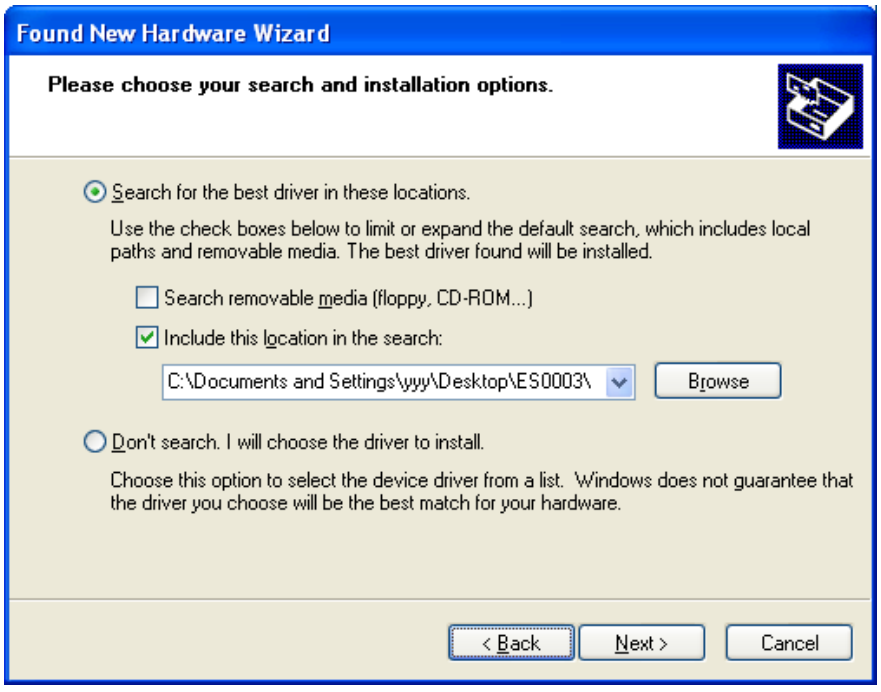

Figure 31 Found New Hardware Wizard (3)

Select Include this location in the search. Enter the location of the ES0003\Driver folder or click Browse and navigate to it. Click Next.

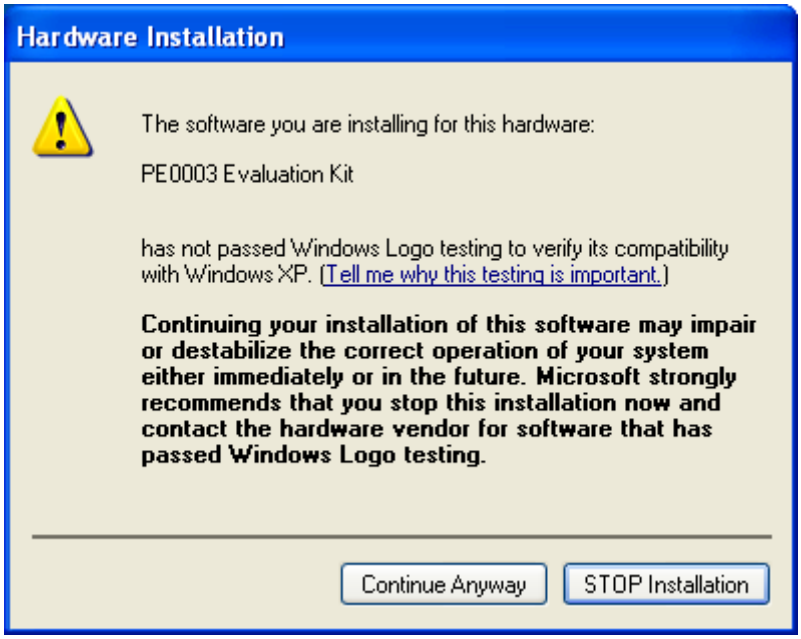

Figure 32 Hardware Installation Dialog Box

Click Continue Anyway.

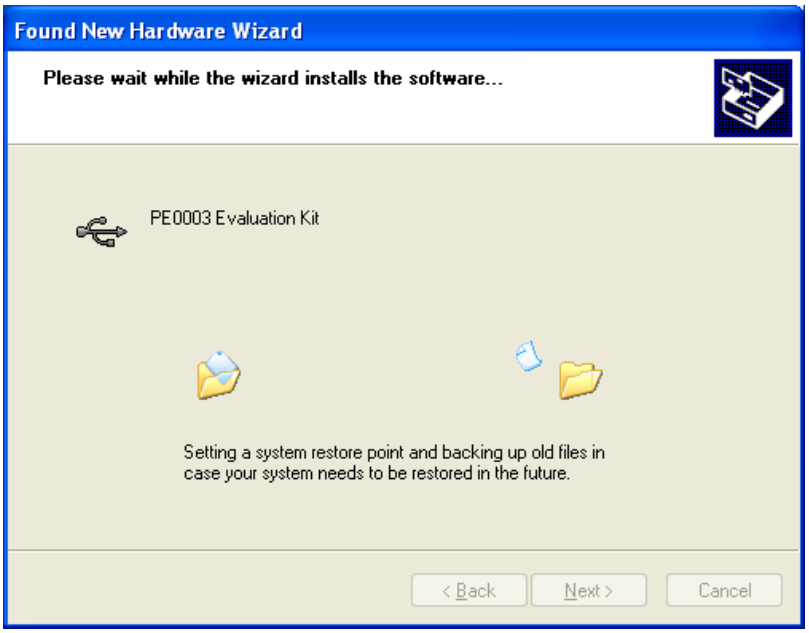

Figure 33 Found New Hardware Wizard (4)

Windows will now install the device driver and the PE0003 should be registered in the Device Manager under “Universal Serial Bus Controllers”. More than one PE0003 can be registered.

Figure 34 Found New Hardware Wizard (5)

Click Finish. The driver is now loaded and the PE0003 is ready for use.

8 Performance Specification

8.1 Electrical Performance

8.1.1 Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the Evaluation Kit.

	Min.	Max.	Units
Supply (VCCIN - GNDD)	4.8	6.8	V
Voltage on any connector pin to GNDD	2.2	3.6	V
Current into or out of VCCIN and GNDD pins	-50	+300	mA
Current into or out of any other connector pin	-20	+20	mA
Storage Temperature	-10	+70	°C
Operating Temperature	+10	+35	°C

8.1.2 Operating Limits

Correct operation of the Evaluation Kit outside these limits is not implied.

	Notes	Min.	Max.	Units
Supply (VCCIN - GNDD)		4.8	6	V
Operating Temperature		+10	+35	°C
Xtal Clock Frequency		11.99	12.01	MHz

8.1.3 Operating Characteristics

For the following conditions unless otherwise specified:

Xtal Frequency = 12MHz
VCCIN = 5.0V, T_{AMB} = +25°C.

	Notes	Min.	Typ.	Max.	Units
DC Parameters					
I_{CCIN} (5V) LPC4330 M4 only, all peripherals disabled, 204MHz	1, 2		96		mA
I/O pins					
V_{IH}	3	2.33		5.5	V
V_{IL}	3	0		1	V
V_{OH} (I_{OH}=-6mA)	3	2.9			V
V_{OL} (I_{OL}=6mA)	3			0.4	V
I_{OH}	3	-6			mA
I_{OL}	3	6			mA
I_{OHS} (short-circuit)	3			86.5	mA
I_{OLS} (short-circuit)	3			76.5	mA
I_{pd} (pull-down current) (V_I = 5V)	3		93		µA
I_{pu} (pull-up current)(V_I = 0V)	3		-62		µA
V_{IH}	4	2.33		5.5	V
V_{IL}	4	0		1	V
V_{OH} (I_{OH}=-8mA)	4	2.9			V
V_{OL} (I_{OL}=8mA)	4			0.4	V
I_{OH}	4	-8			mA
I_{OL}	4	8			mA
I_{OHS} (short-circuit)	4			86	mA
I_{OLS} (short-circuit)	4			76	mA
I_{pd} (pull-down current) (V_I = 3.3V)	4		62		µA
I_{pu} (pull-up current)(V_I = 0V)	4		-62		µA
Input/Output Capacitance	4			2	pF
C-BUS clock frequency		1.0	10.0		MHz
I2S Interface					
V_{IH}	5	2.33		5.5	V
V_{IL}	5	0		1	V
V_{OH} (I_{OH}=-8mA)	5	2.9			V
V_{OL} (I_{OL}=8mA)	5			0.4	V
I_{OH}	5	-8			mA
I_{OL}	5	8			mA
I_{OHS} (short-circuit)	5			86	mA
I_{OLS} (short-circuit)	5			76	mA
I_{pd} (pull-down current) (V_I = 3.3V)	5		62		µA
I_{pu} (pull-up current)(V_I = 0V)	5		-62		µA
Input/Output Capacitance	5			2	pF
I^2S clock frequency				12.6	MHz

Notes:

1. Not including any current drawn from the output pins by external circuitry.
2. No Target Card connected.
3. BOOTEN1, BOOTEN2, GPIO0, GPIO1, GPIO2, GPIO3, GPIO4, GPIO5, GPIO6, GPIO7, IO0, IO1, IO2, IO3, IO4, IO5, IO6, IO7, IO8, IO9, IO10, IO11, IO12, IO13, IO14 and IO15. Normal drive strength. The IO pins have another option for high currents. In case of using the Isolators the pins IO0,IO1, IO2, IO5 and IO6 do not follow the values of the table (depends on the isolator fitted).
4. CSN1, CSN2, IRQN1, IRQN2, RDATA1, RDATA2, CDATA1, CDATA2 SCLK1 and SCLK2 pins.
5. TXD, RXD, TXFS, RXFS, RXCLK and TXCLK.

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CML's proprietary *FirmASIC*® component technology reduces cost, time to market and development risk, with increased flexibility for the designer and end application. *FirmASIC*® combines Analogue, Digital, Firmware and Memory technologies in a single silicon platform that can be focused to deliver the right feature mix, performance and price for a target application family. Specific functions of a *FirmASIC*® device are determined by uploading its Function Image™ during device initialization. New Function Images™ may be later provided to supplement and enhance device functions, expanding or modifying end-product features without the need for expensive and time-consuming design changes. *FirmASIC*® devices provide significant time to market and commercial benefits over Custom ASIC, Structured ASIC, FPGA and DSP solutions. They may also be exclusively customised where security or intellectual property issues prevent the use of Application Specific Standard Products (ASSP's).

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