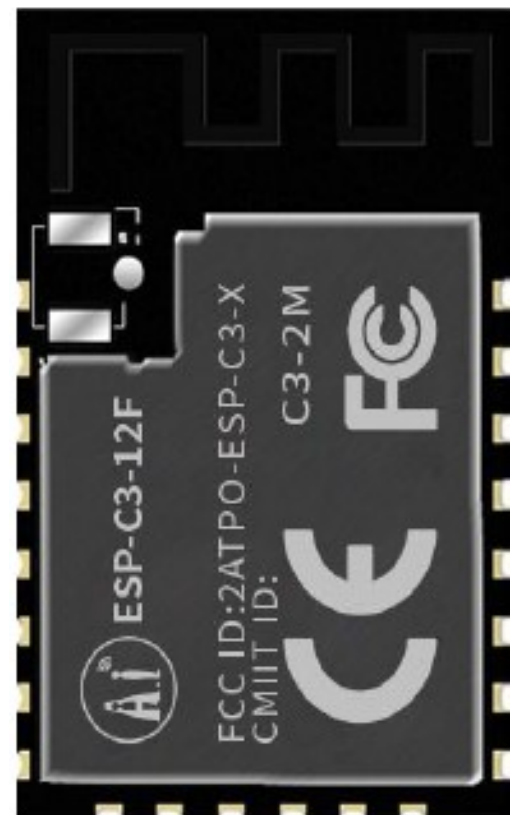




ESP WIFI MODULE

Features

- Complete Wi-Fi 802.11b/g/n, 1T1R mode data rate up to 150Mbps
- Support BLE5.0 and rate support: 125Kbps, 500Kbps, 1Mbps, 2Mbps
- 32-bit RISC-V single-core processor, supports a clock frequency of up to 160 MHz with 400 KB SRAM, 384 KB ROM, 8KB RTC SRAM
- Support UART/PWM/GPIO/ADC/I2C/I2S interface, temperature sensor, pulse counter
- SMD-22 package
- Support multiple sleep modes, deep sleep electric current is less than 5uA
- UART rate up to 5Mbps
- Support STA/AP/STA+AP mode and mix mode
- Support Smart Config (APP)/AirKiss (WeChat) of Android and IOS One-click network configuration
- Support UART port local upgrade and remote firmware upgrade (FOTA)
- General AT commands can be better understand
- Support secondary development, integrated Linux development environment
- About Flash configuration—Acquiesce in using the built-in 4MByte Flash.



Product Overview

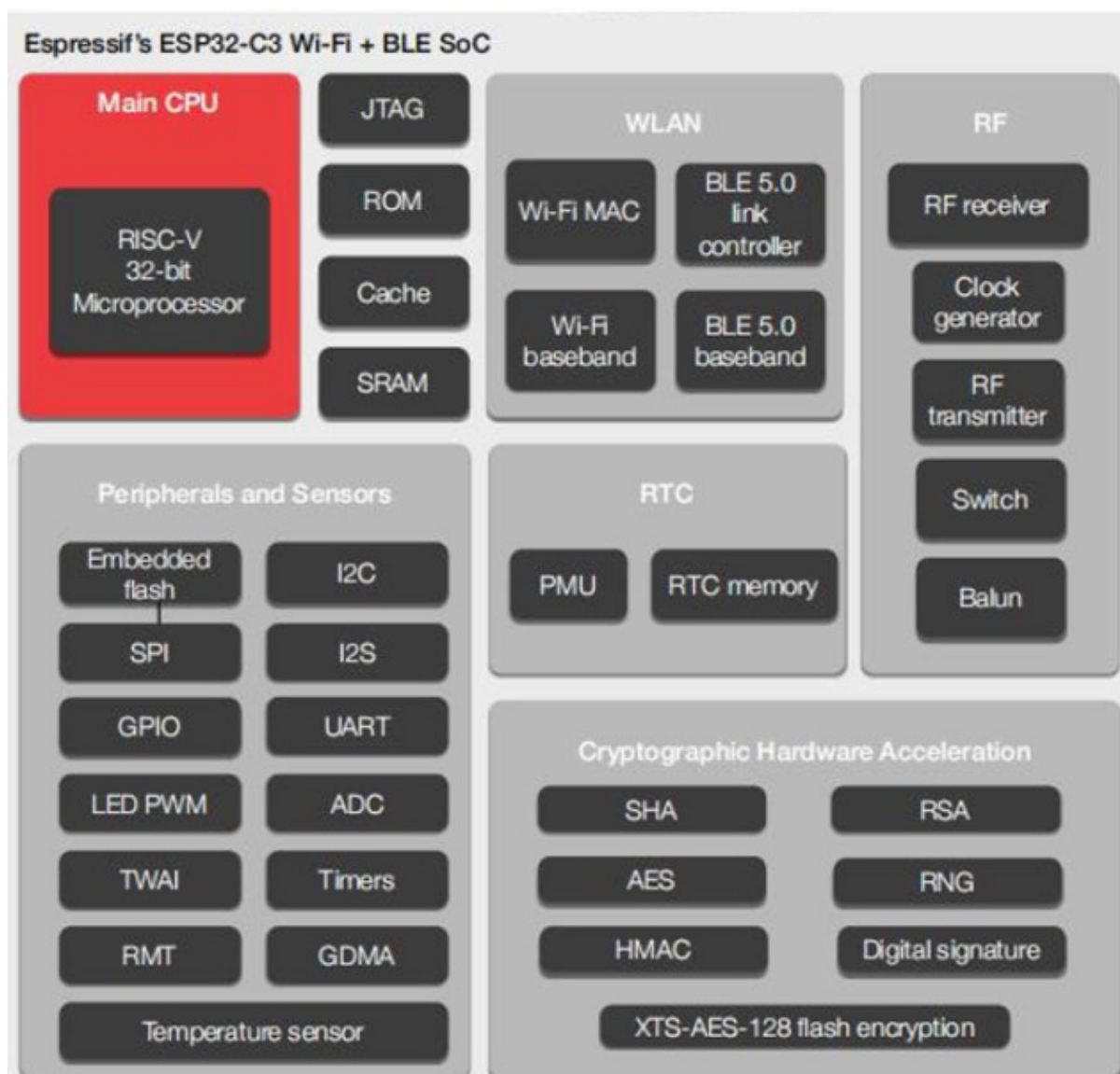
This module core processor ESP32-C3 is a Wi-Fi+ BLE combination of system-level chips (SoC), designed for various applications such as internet of things (IoT), mobile devices, wearable electronics, smart home, etc. ESP32-C3 with industry-leading low power and RF performance, supporting Wi-Fi IEEE802.11b/g/n agreements and BLE 5.0. ESP32-C3 chip is equipped with 32-bit RISC-V single-core processor, operating frequency up to 160 MHz. The chip is support to have secondary development without using other microcontrollers or processors.

The chip has a built-in 400 KB SRAM, 384 KB ROM, 8KB RTC SRAM. Also, the chip supports external Flash while it has built-in 4Mbit Flash. ESP32-C3 chip supports a variety of low-power consumption working states, which can meet the power consumption requirements of various application scenarios. The chip's unique features such as fine clock gating function, dynamic voltage clock frequency adjustment function, and RF output power adjustable function can achieve the best balance between communication distance, communication speed and power consumption.

ESP-C3-12F provides a wealth of peripheral interfaces, including UART, PWM, SPI, I2S, I2C, ADC, temperature sensor and there are 15 GPIOs.

ESP-C3-12F has a variety of unique hardware safety mechanisms. The hardware encryption accelerator supports AES, SHA and RSA algorithm. Among them, RNG, HMAC and Digital Signature modules provide more security features. Other security features include flash encryption and secure boot signature verification, etc. The perfect security mechanism enables the chip to be perfectly applied to various encryption products.

ESP-C3-12F module supports low-power Bluetooth: Bluetooth5 and Bluetooth mesh. Bluetooth rate support: 125Kbps, 500Kbps, 1Mbps, 2Mbps. Support broadcast extension, multi-broadcasting, channel selection.



1.2 Main Parameters

Table 1 Main Parameter Descriptions

Model Name	ESP-C3-12F
Package	SMD-22
Size	24.0*16.0*3.1(±0.2)mm
Antenna	On-board PCB antenna/IPEX
Frequency Range	2400 ~ 2483.5MHz
Operating Temperature	-40 °C ~ 85 °C
Store Temperature	-40 °C ~ 125 °C , < 90%RH
Power supply range	Voltage 3.0V ~ 3.6V, Electrical current >500mA
Support Interface	UART/GPIO/ADC/PWM/I2C/I2S
IO	IO0,IO1,IO2,IO3,IO4,IO5,IO6,IO7,IO8,IO9,IO10,IO18,IO19, IO20,IO21
UART Rate	Support 110 ~ 4608000 bps , default 115200 bps
Bluetooth	BLE 5.0
Security	WEP/WPA-PSK/WPA2-PSK
SPI Flash	Default allocation 4MByte, support 2MByte version

2 Electrical Parameters

ESP-C3-12F module is electrostatic sensitive devices and special precautions need to be taken when handling



2.1 Electrical Characteristics

Parameters		Conditions	Min	Typical values	Max	Unit
Supply voltage		VDD	3.0	3.3	3.6	V
I/O	V _{IL} /V _{IH}	-	-0.3/0.75VDD	-	0.25VDD/VDD+0.3	V
	V _{OL} /V _{OH}	-	N/0.8VIO	-	0.1VIO/N	V
	I _{MAX}	-	-	-	12	mA

2.2 WIFI RF Performance

Description	Typical values	Unit
Operating frequency	2400 - 2483.5	MHz
Output Power		
11n mode HT40, PA output power	15±2	dBm
11n mode HT20, PA output power	15±2	dBm
11g mode, PA output power	16±2	dBm
11b mode, PA output power	18±2	dBm
Receiving sensitivity		
CCK, 1 Mbps	-96±2	dBm
CCK, 11 Mbps	-88±2	dBm
6 Mbps (1/2 BPSK)	-92±2	dBm
54 Mbps (3/4 64-QAM)	-75±2	dBm
HT20 (MCS7)	-73±2	dBm
HT40 (MCS7)	-70±2	dBm

2.3 BLE RF Performance

Description	Typical values	Unit
Output power		
Transmit power	0±2	dBm
Receiving sensitivity Low Energy consumption BLE: 1M		
Sensitivity@30.8%PER	-96±2	dBm

2.4 Power Consumption

The following power consumption data are based on a 3.3 V power supply, 25°C ambient temperature and measured using an internal voltage regulator.

- All measurements were completed at the antenna interface without SAW filters
- All emission data are based on a duty cycle of 100%, measured in the mode of continuous emission.

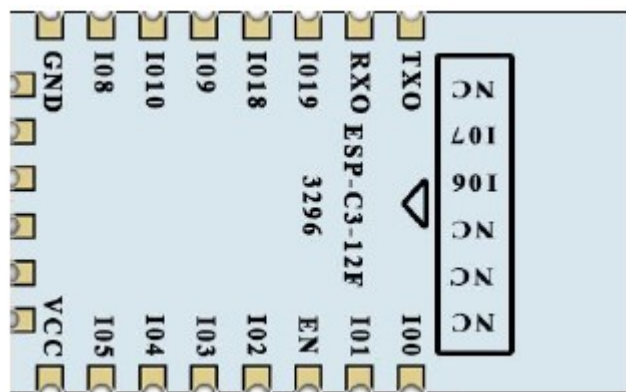
Mode	Mix	Typical values	Max	Unit
Tx 802.11b, CCK 1Mbps, POUT=+20dBm	-	345	-	mA
Tx 802.11g, OFDM 54Mbps, POUT =+18dBm	-	285	-	mA
Tx 802.11n, MCS7, POUT =+17dBm	-	280	-	mA
Rx 802.11b, 1024 bit	-	82	-	mA
Rx 802.11g, 1024 bit	-	82	-	mA
Rx 802.11n, 1024 bit	-	84	-	mA
Modem-Sleep ^①	-	20	-	mA
Light-Sleep ^②	-	130	-	μA
Deep-Sleep ^③	-	5	-	μA
Power Off	-	1	-	μA

3 Appearance Dimensions

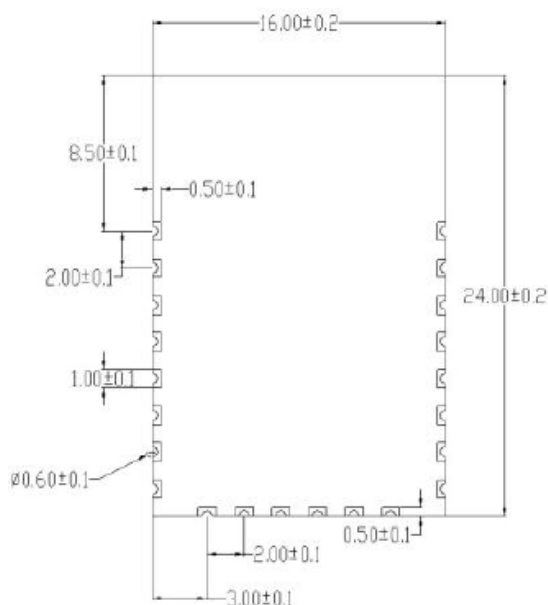
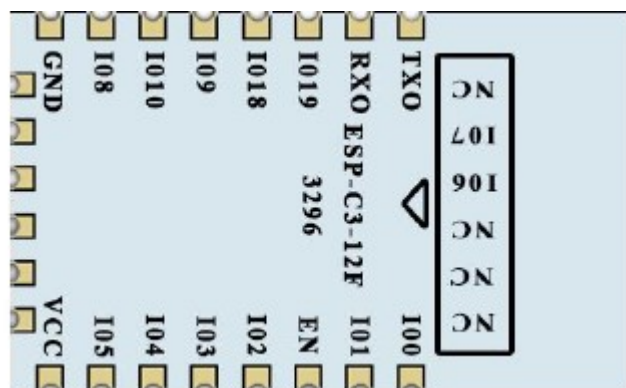
ESP-C3-12F have two FLASH, including external FLASH and build-in FLASH

(The rendering is for reference only, the actual product shall prevail)

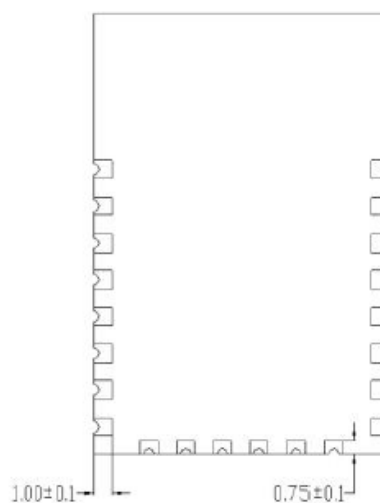
External 2MByte FLASH:



Build-in 4MByte FLASH:

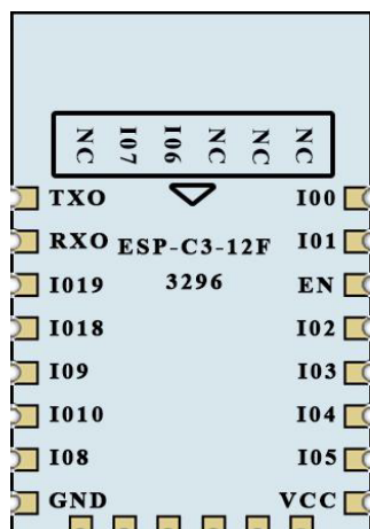


正面



背面

4 Pin Definition



ESP-C3-12F Diagram of Pin

ESP-C3-12F module is connected to 22 interfaces, refer to pin diagram, pin function definition table is interface definition.

Table ESP-C3-12F Pin function definition

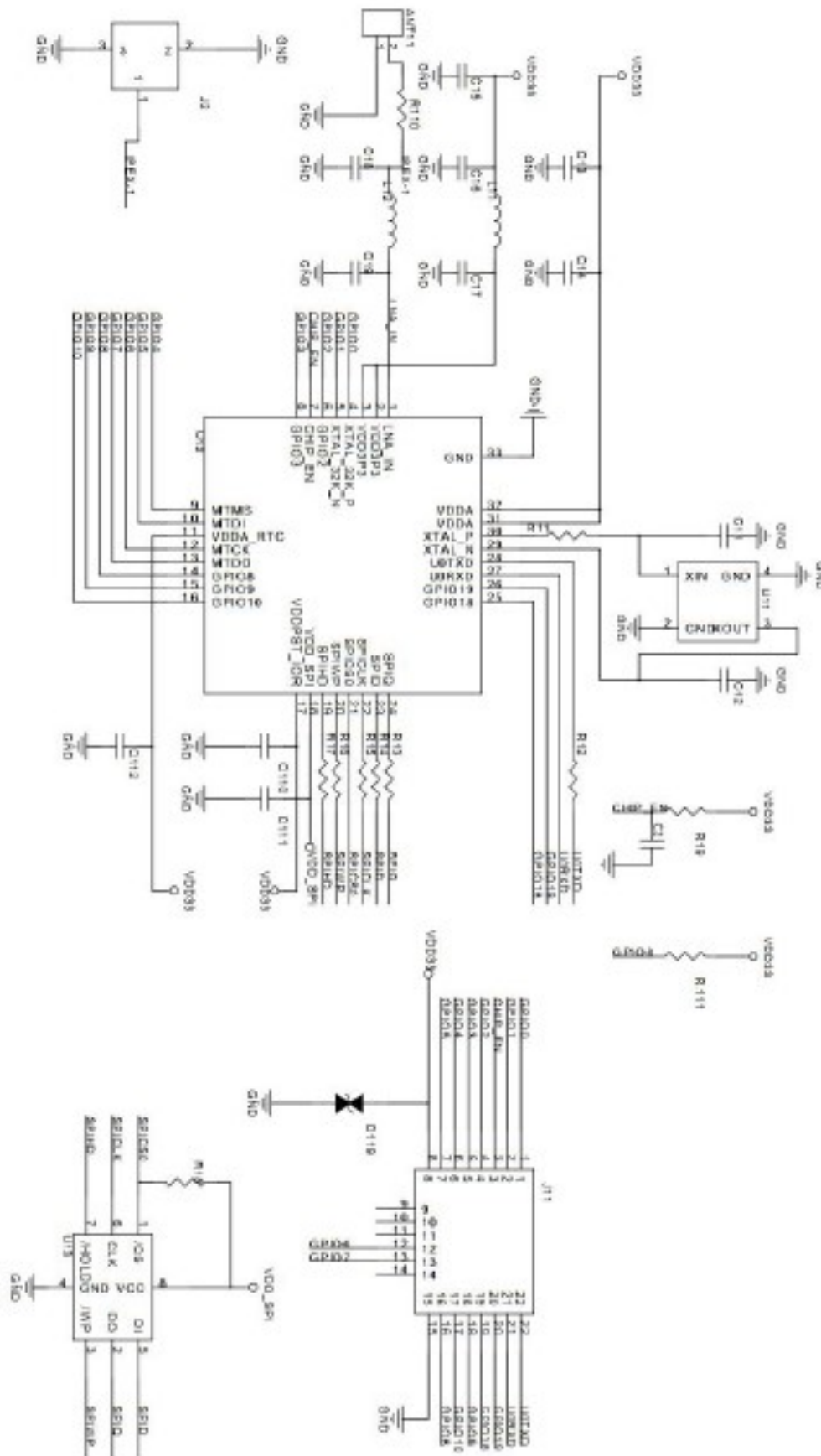
No.	Name	Function
1	IO0	GPIO0,ADC1_CH0,XTAL_32K_N
2	IO1	GPIO1,ADC1_CH1,XTAL_32K_N
3	EN	High level: chip enabled; Low level: chip shutdown; Pay attention not to leave the CHIP_PU pin floating:
4	IO2	GPIO2,ADC1_CH2,FSPIQ
5	IO3	GPIO03,ADC1_CH3
6	IO4	GPIO04,ADC1_CH4,FSPIHD,MTMS
7	IO5	GPIO05,ADC2_CH0,FSPIWP,MTDI
8	VCC	VCC
9	NC	NC
10	NC	NC
11	NC	NC
12	IO6	GPIO6,FSPICLK,MTCK
13	IO7	GPIO7,FSPID,MTDO
14	NC	NC
15	GND	GND
16	IO8	GPIO8
17	IO10	GPIO10,FSPICSO
18	IO9	GPIO9
19	IO18	GPIO18
20	IO19	GPIO19
21	RX	UART0_RX,GPIO20
22	TX	UART0_TX,GPIO21

Table Module Start-up Mode Description

System start-up mode			
Pin	Default	SPI Start up mode	Download Start up Mode
IO8	non	/	1
IO9	Pull up	1	0

Note: Some pins have been internally pulled up, please refer to the schematic

5 Schematic Diagrams



6 Design Guidance

6.1. Note:

(1) When GPIO20 is used as U1RXD, a pull-up resistor needs to be added externally.

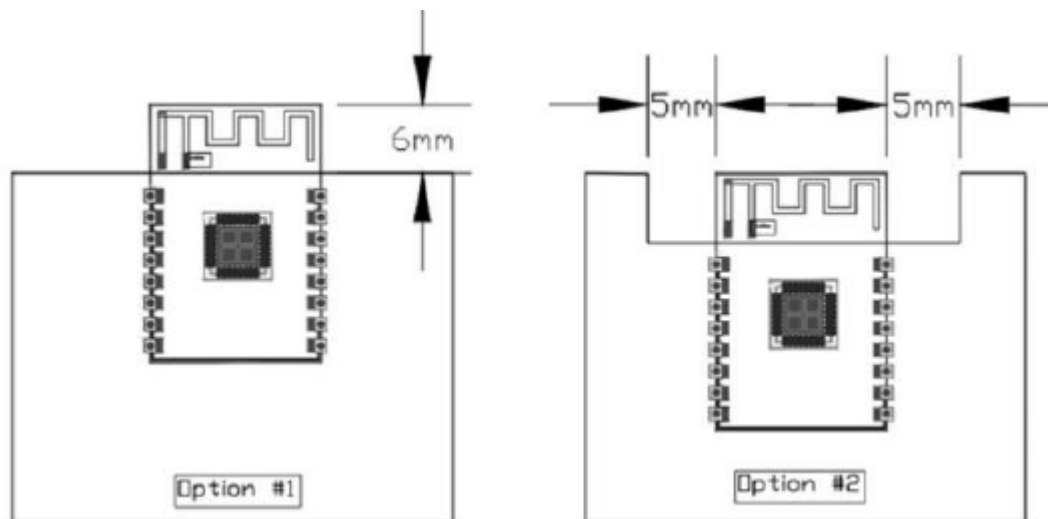
6.2. Antenna layout requirements

(1) For the installation position on the motherboard, the following two methods are recommended:

Solution 1: Put the module on the edge of the main board, and the antenna area extends out of the edge of the main board.

Solution 2: Put the module on the edge of the main board, and hollow out an area at the antenna position on the edge of the main board.

(2) In order to meet the performance of the on-board antenna, metal parts are forbidden to be placed around the antenna, away from high frequency devices.



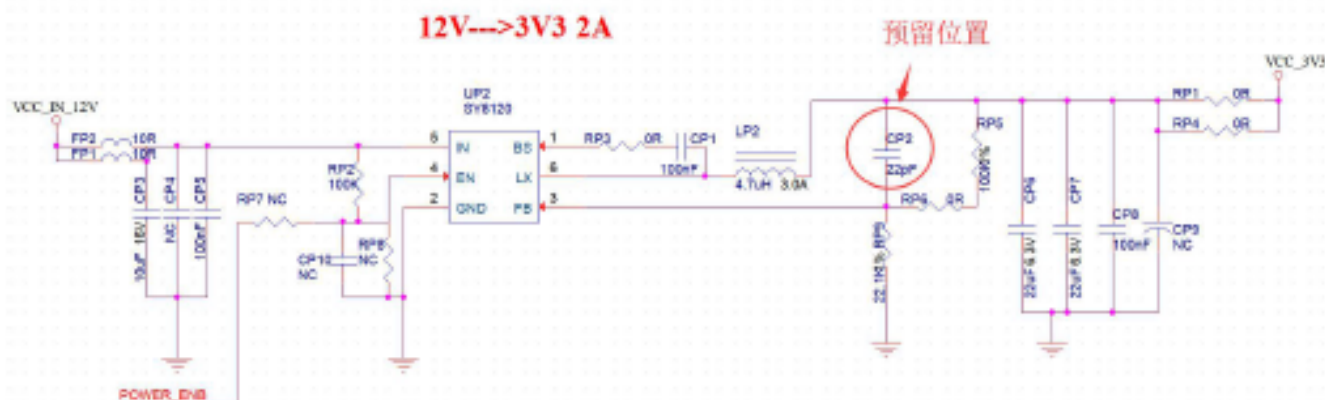
6.3. Power supply

(1) Recommend 3.3V voltage, peak current above 500mA

(2) It is recommended to use LDO for power supply; if DC-DC is used, the ripple is recommended to be controlled within 30mV.

(3) DC-DC the power supply circuit, it is suggested to reserve the position of output ripple can be optimized when the load changes greatly.

(4) It is recommended to add ESD devices to the 3.3V power interface.



6.4. GPIO Interface

- (1) The module periphery leads to some GPIO ports, such as the recommended resistance of 10-100 Ohms in series on the IO port. This can suppress overshoot, to ensure both sides of the level more stable. helpful for both EMI and ESD.
- (2) For special IO, please refer to the specification, which will affect the starting configuration of the module.
- (3) The IO port of the module voltage is 3.3 V, if the main control does not match the IO level of the module, require to add the level conversion circuit.
- (4) When the IO port is connected directly to the peripheral interface, or the pin header and other terminals, it is recommended to reserve ESD device near the terminal.

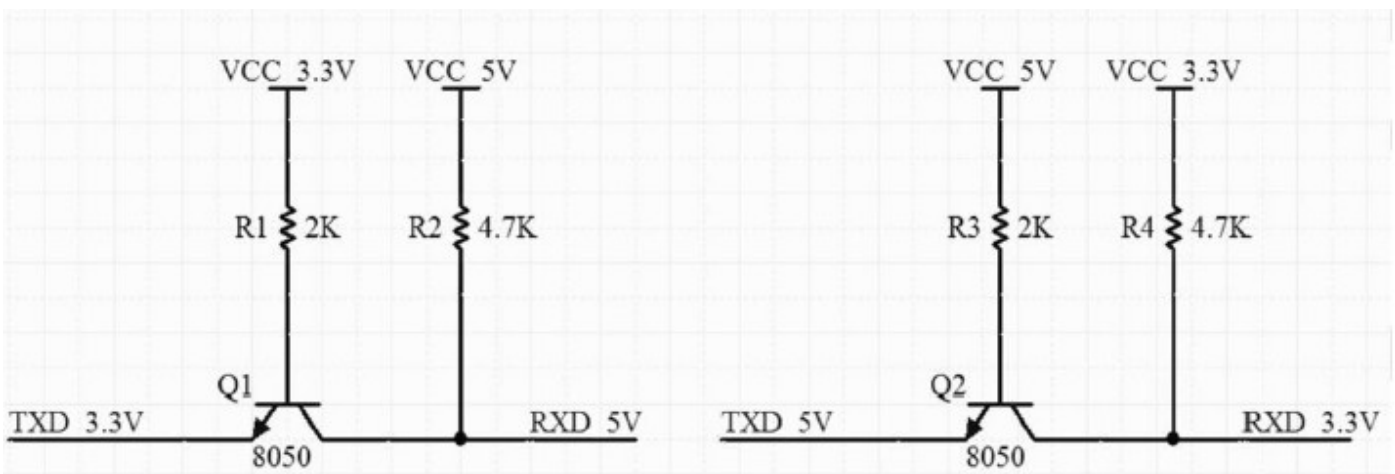
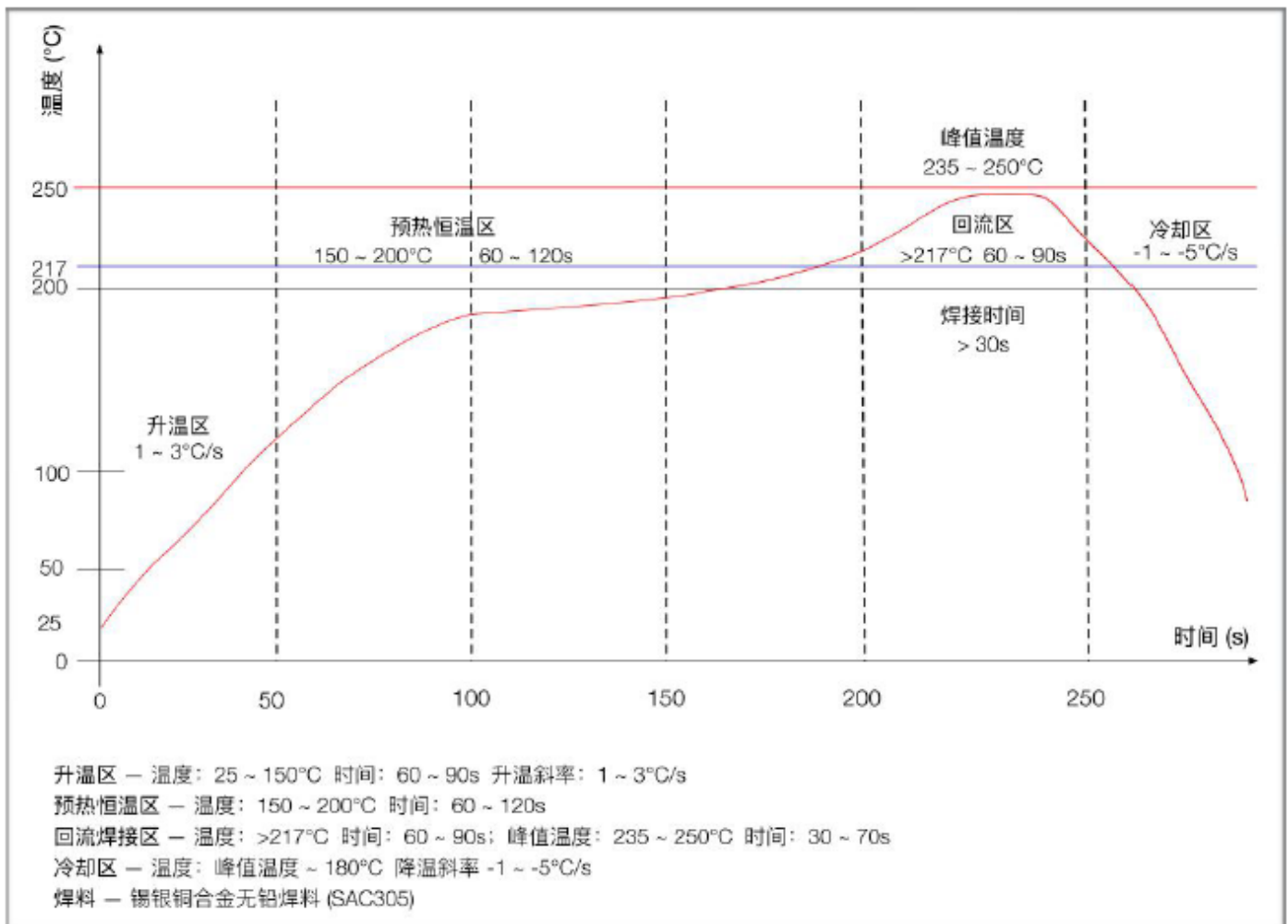


Table Electrical level conversion circuit

7 Reflow Soldering



8 Packaging Information

Refer to below image,ESP-C3-12F package is in Tape/Reel.



Simplified Declaration of Conformity (RED)

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