transphorm

User Guide

TDTTP4000W065AN_0V1: 4kW Analog Bridge-less Totem-pole PFC Evaluation Board

Overview

This user guide describes the TDTTP4000W065AN_0v1 4kW Analog Bridge-less totem-pole power factor correction (PFC) evaluation board. Very high efficiency single-phase AC-DC conversion is achieved with the TP65H035G4WS, a diode-free Gallium Nitride (GaN) FET bridge with low reverse-recovery charge. Using Transphorm GaN FETs in the fast-switching leg of the circuit and low-resistance MOSFETs in the slow-switching leg of the circuit results in improved performance and efficiency. For more information and complete design files, please visit transphormusa.com/TDTTP4000W065AN.

The TDTTP4000W065AN_0v1-KIT is for evaluation purposes only.

The evaluation board is shown in Fig. 1.

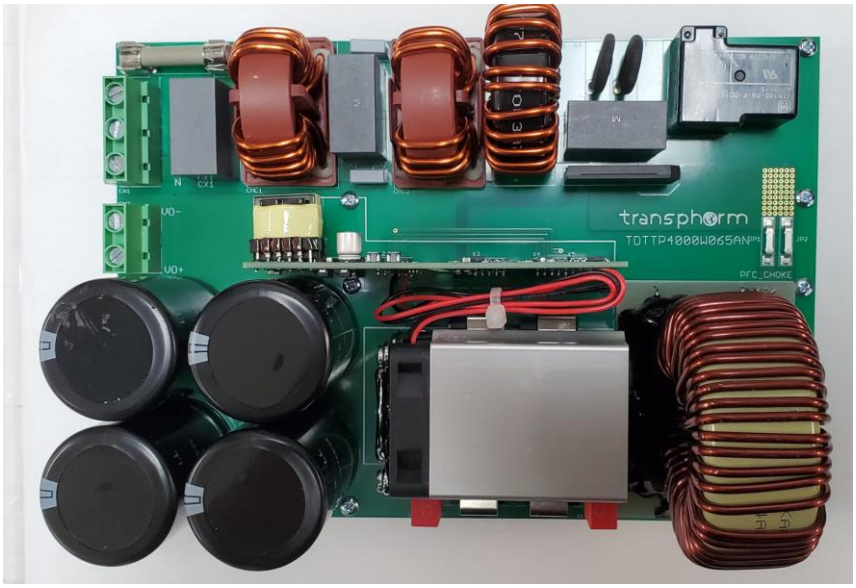


Figure 1. TDTTP4000W065AN_0v1 4kW analog totem-pole PFC evaluation board

Warning

This EV demo board is intended to validate GaN FET technology and is for demonstration purposes only and no guarantees are made for standards compliance. There are areas of this evaluation board that have exposed access to hazardous high voltage levels. Implement caution to avoid contact with those voltages. Also note that the evaluation board may retain high voltage temporarily after input power has been removed. **Exercise caution when handling**. When testing converters on an evaluation board, ensure adequate cooling. Apply cooling air with a fan blowing across the converter or across a heat sink attached to the converter. Monitor the converter temperature to ensure it does not exceed the maximum rated per the datasheet specification.

TDTTP4000W065AN_0V1 input/output specifications

Input Voltage: 90 Vac to 265 Vac, 47 Hz to 63 Hz

Max Input Current: 18 A (rms) : (2000W at 115 Vac, 4000W at 230 Vac)

Ambient temperature: < 65 C at high power operation

Output Voltage: 387 Vdc +/- 5 Vdc

PWM Frequency: 65 kHz

Power dissipation in the GaN FET is limited by the maximum junction temperature. Refer to the TP65H035G4WS datasheet

Figure 2 shows the input and output connections. To reduce EMI noise, adding a ferrite core at the input and output cable is recommended.

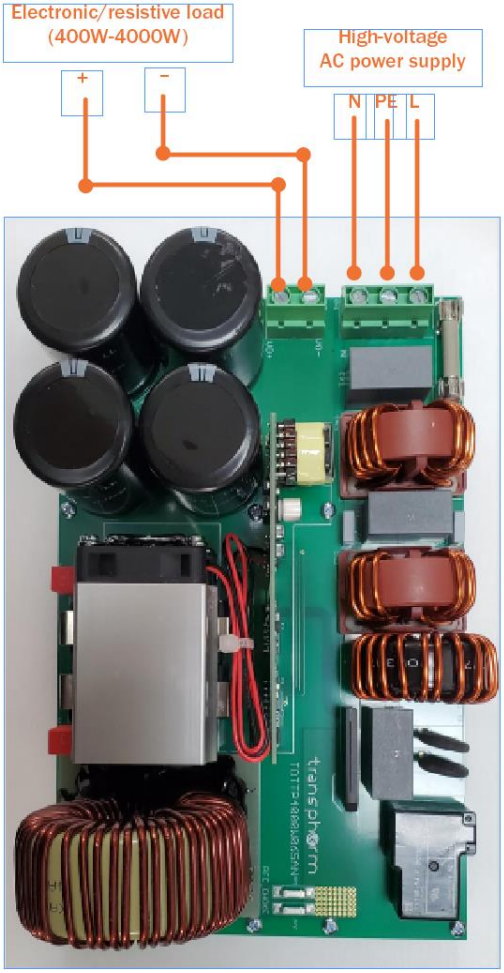


Figure 2. Input and output cable connections

Circuit description for Bridge-Less Totem-Pole PFC based on GaN FET

The Bridge-less totem-pole topology is shown in Fig 3 below. As shown in Fig 3(a), two GaN FETs and two diodes are used for the line rectification, while in Fig 3(b), the circuit is modified and the diodes are replaced by two low resistance silicon MOSFETs to eliminate diode drops and improve the efficiency. Further information and discussion on the performance and the characteristics of Bridge-less PFC circuit is provided in [1].

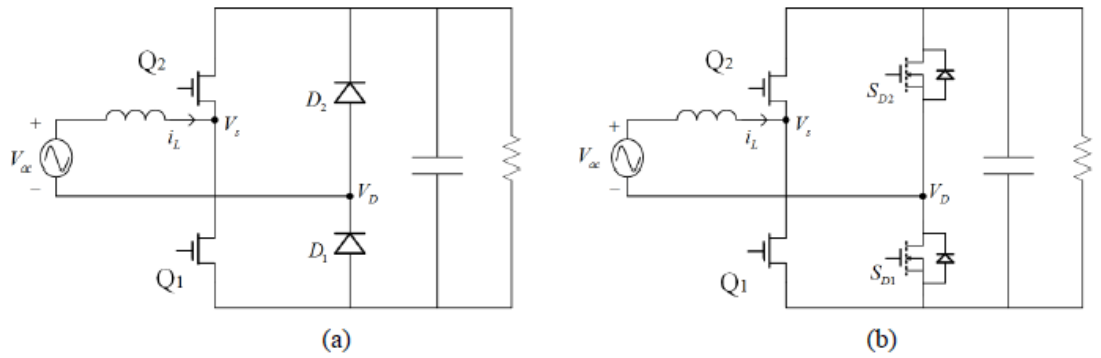


Fig.3 Totem-pole bridgeless PFC boost converter based on GaN FET (a) Diode for line rectification (b) MOSFET for line rectification

The large recovery charge (Qrr) of existing silicon MOSFETs makes CCM operation of a silicone totem-pole Bridge-less PFC impractical and reduces the total efficiency..

Figure 4(a) is a simplified schematic of a totem-pole PFC in continuous conduction mode (CCM) mode, focused on minimizing conduction losses. It comprises two fast-switching GaN FETs (Q1 and Q2) operating at a high pulse-width-modulation (PWM) frequency and two very low-resistance MOSFETs (S1 and S2) operating at a much slower line frequency (50Hz/60Hz). The primary current path includes one fast switch and one slow switch only, with no diode drop. The function of S1 and S2 is that of a synchronized rectifier as illustrated in Figures 4(b) and 4(c). During the positive AC cycle, S1 is on and S2 is off, forcing the AC neutral line tied to the negative terminal to the DC output. The opposite applies for the negative cycle.

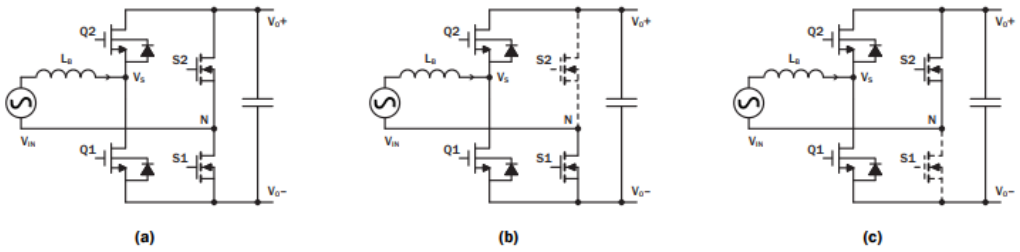


Figure 4. Totem-pole PFC with GaN FETs (a) simplified schematic, (b) during positive AC cycle and (c) during negative AC cycle

In either AC polarity, the two GaN FETs form a synchronized boost converter with one transistor acting as a master switch to allow energy intake by the boost inductor (LB), and another transistor as a slave switch to release energy to the DC output. The roles of the two GaN devices interchange when the polarity of the AC input changes; therefore, each transistor must be able to perform both master and slave functions. To avoid shoot-through a dead time is built in between two switching events, during

which both transistors are momentarily off. To allow CCM operation, the body diode of the slave transistor must function as a flyback diode for the inductor current to flow during dead time. The diode current; however, must quickly reduce to zero and transition to the reverse blocking state once the master switch turns on. This is the critical process for a totem-pole PFC which, with the high Qrr of the body diode of high-voltage Si MOSFETs, results in abnormal spikes, instability, and associated high switching losses. The low Qrr of the GaN switches allows designers to overcome this barrier.

As seen in Figure 5, inductive tests at 430V bus show healthy voltage waveforms up to inductor current exceeding 35A using either a high-side (Figure 5(a)) or low-side (Figure 5(b)) GaN transistor as a master switch. With a design goal of 4.4kW output power in CCM mode at 230VAC input, the required inductor current is 20A. This test confirms a successful totem-pole power block with enough current overhead.

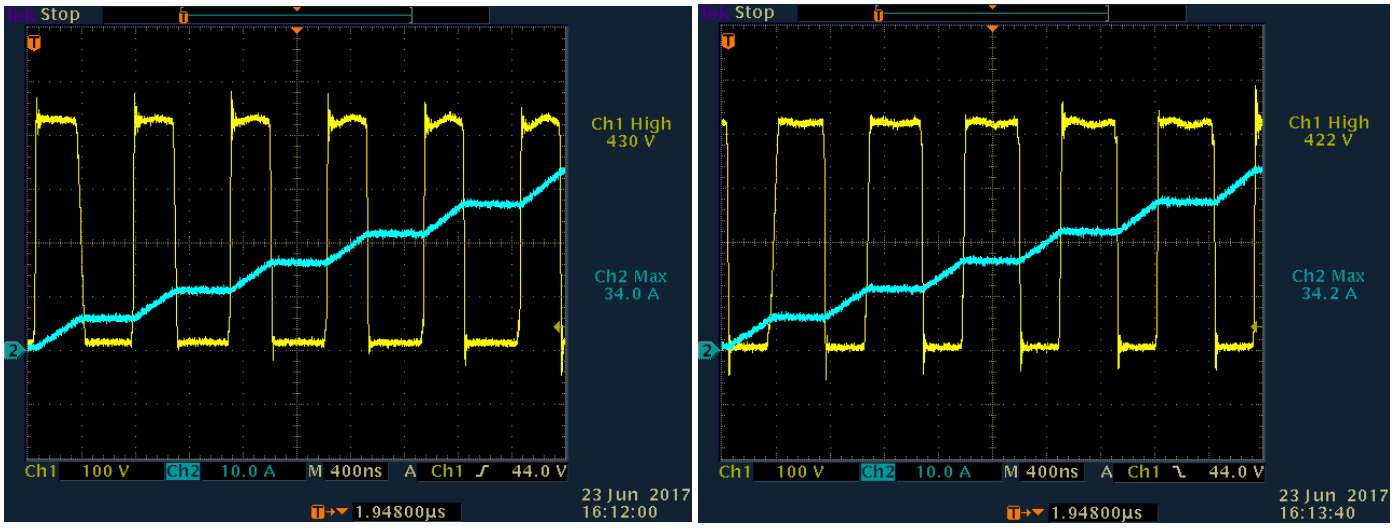


Fig 5. Hard-switched waveforms of a pair of GaN FET switches when setting a) high side as master and b) low side as master

One issue inherent in the bridgeless totem-pole PFC is the operation mode transition at AC voltage zero-crossing. For instance, when the circuit operation mode changes from positive half-line to negative half-line at the zero-crossing, the duty ratio of the high-side GaN switch changes abruptly from almost 100% to 0% and the duty ratio of low-side GaN switch changes from 0% to 100%. Due to the slow reverse recovery of diodes (or body diode of a MOSFET), the voltage VD cannot jump from ground to VDC instantly; a current spike will be induced. To avoid the problem, a soft-start at every zero-crossing is implemented to gently reverse duty ratio (a soft-start time of a few switching cycles is enough). The TDTTP4000W065AN evaluation board is designed to run in CCM and the larger inductance alleviates the current spike issue at zero-crossing.

While a typical Si MOSFET has a maximum dV/dt rating of 50V/ns, the TP65H035G4WS GaN FET will switch at dV/dt of 100V/ns or higher to achieve the lowest possible switching loss. At this level of operation, even the layout becomes a significant contributor to performance. As shown in Figure 8, the recommended layout keeps a minimum gate drive loop and keeps the traces between the switching nodes very short--with the shortest practical return trace to the power bus and ground. The power ground plane provides a large cross-sectional area to achieve an even ground potential throughout the circuit. The layout carefully separates the power ground and the IC (small signal) ground, only joining them at the source pin of the FET to avoid any possible ground loop. Note that the Transphorm GaN FETs in TO-247 packages have pinout configuration of G-S-D, instead of the traditional G-D-S of a MOSFET. The G-S-D configuration is designed with thorough consideration to minimize the gate source driving loop, reducing parasitic inductance and to separate the driving loop (gate source) and power loop (drain source) to minimize noise. All PCB layers of the TDTTP4000W065AN_0V1 design are shown Figure 8(a-c) and available in the design files.

Design details

A detailed circuit schematic for the main board is shown in Figures 7a and 7b. A detailed circuit schematic for the controlboard is shown in figures 8a, 8b, and 8c.

The PCB layers in Figure 9, and the parts list in Table 1 (also included in the design files).

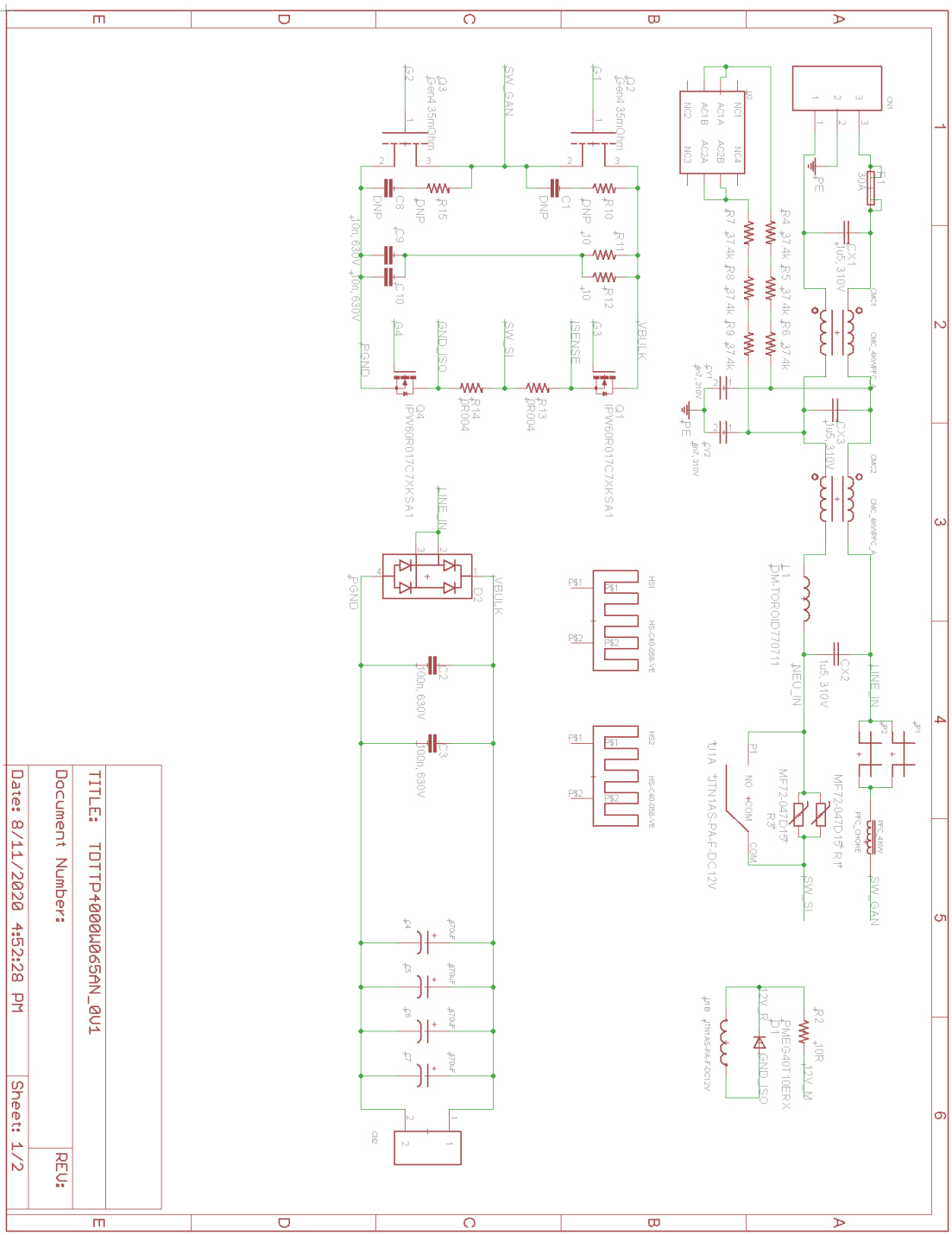


Fig 7a

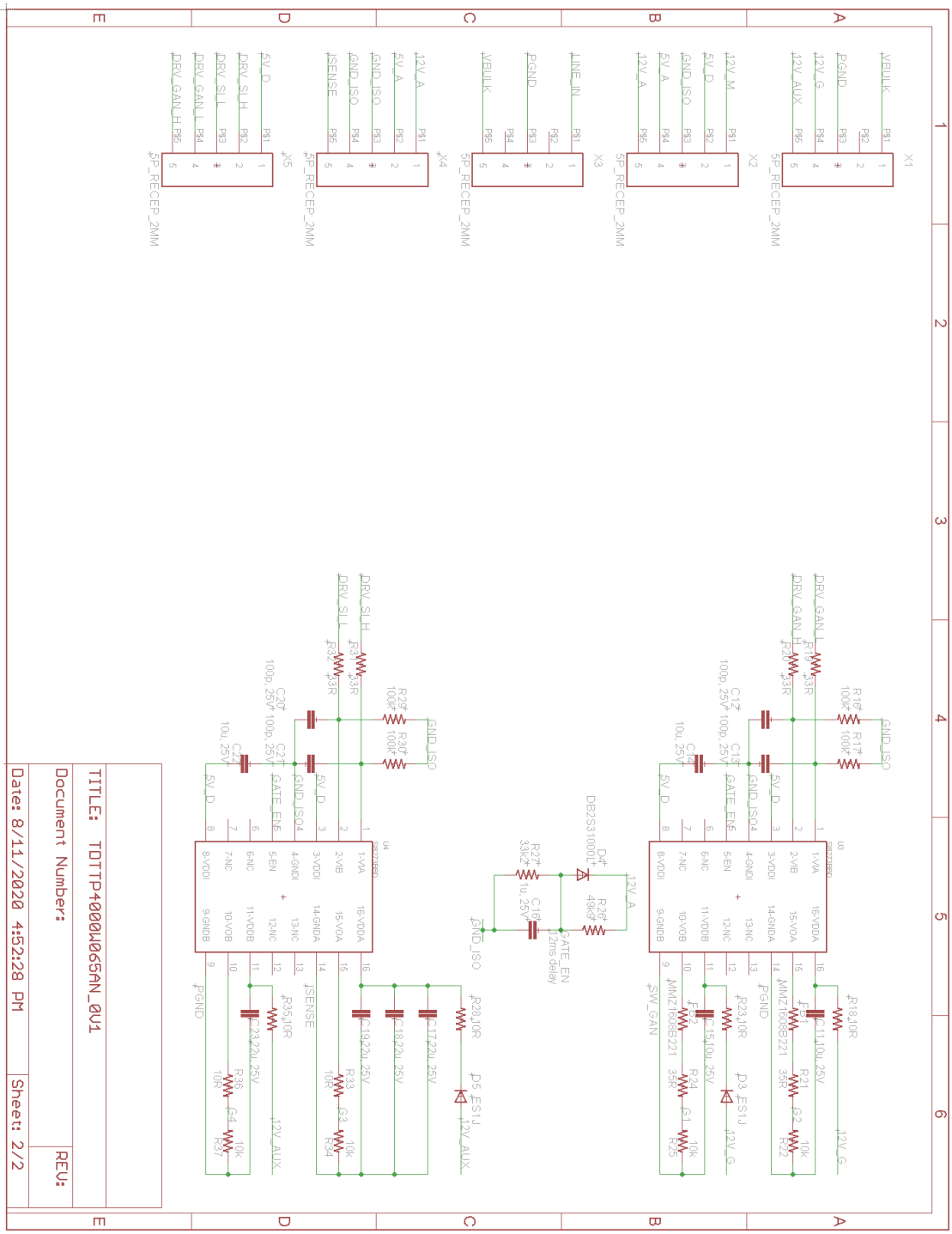


Fig 7b

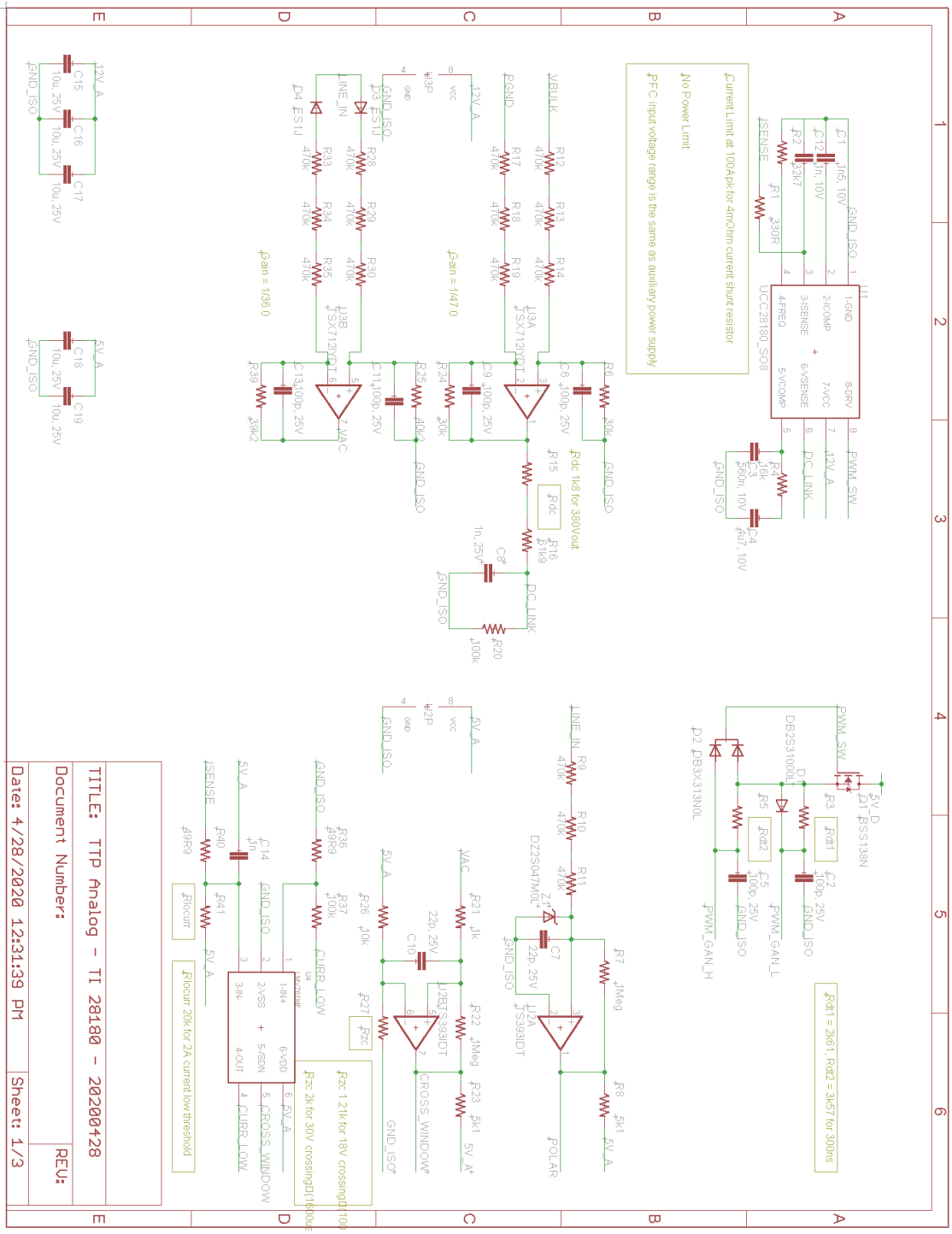


Fig 8a

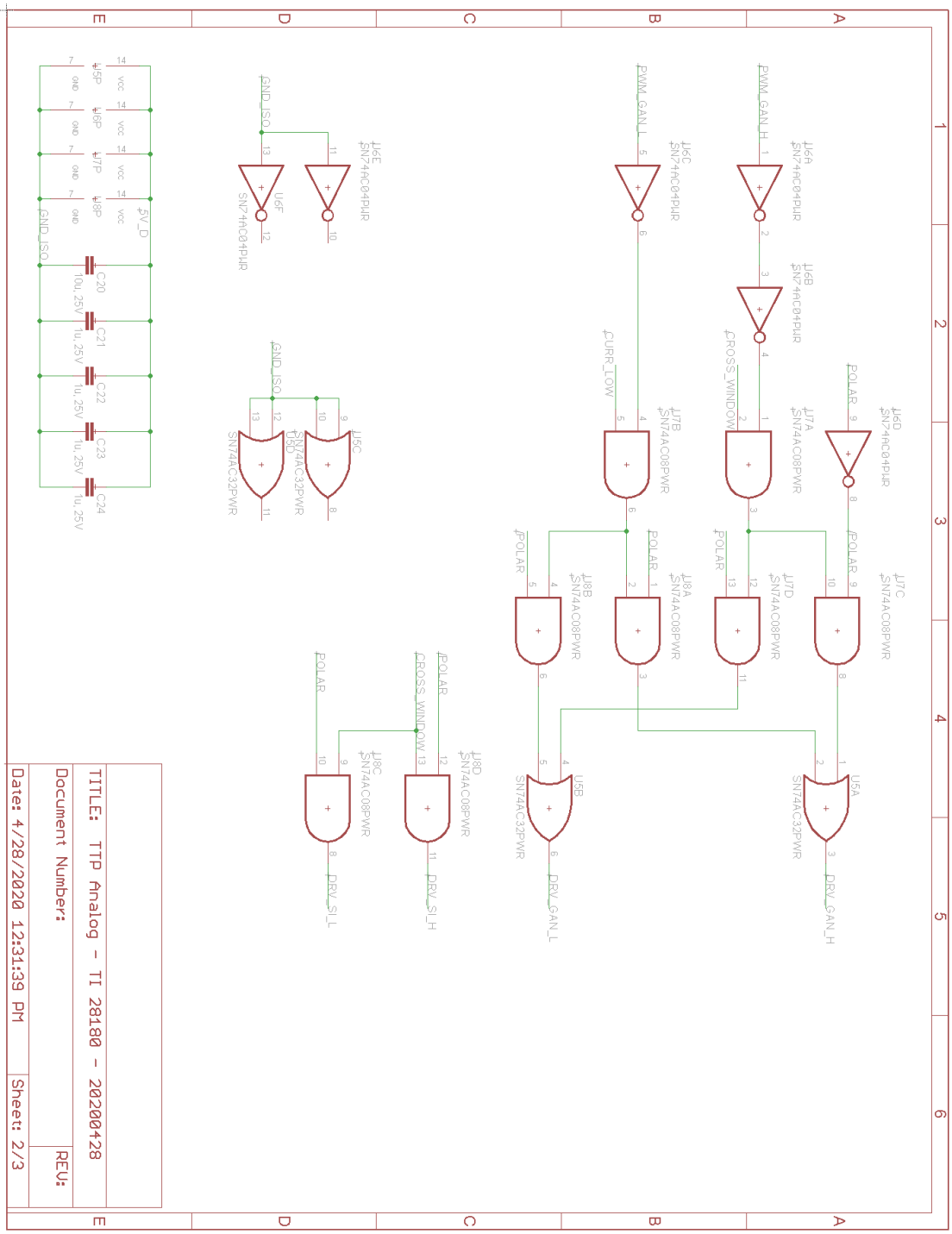


Fig 8b

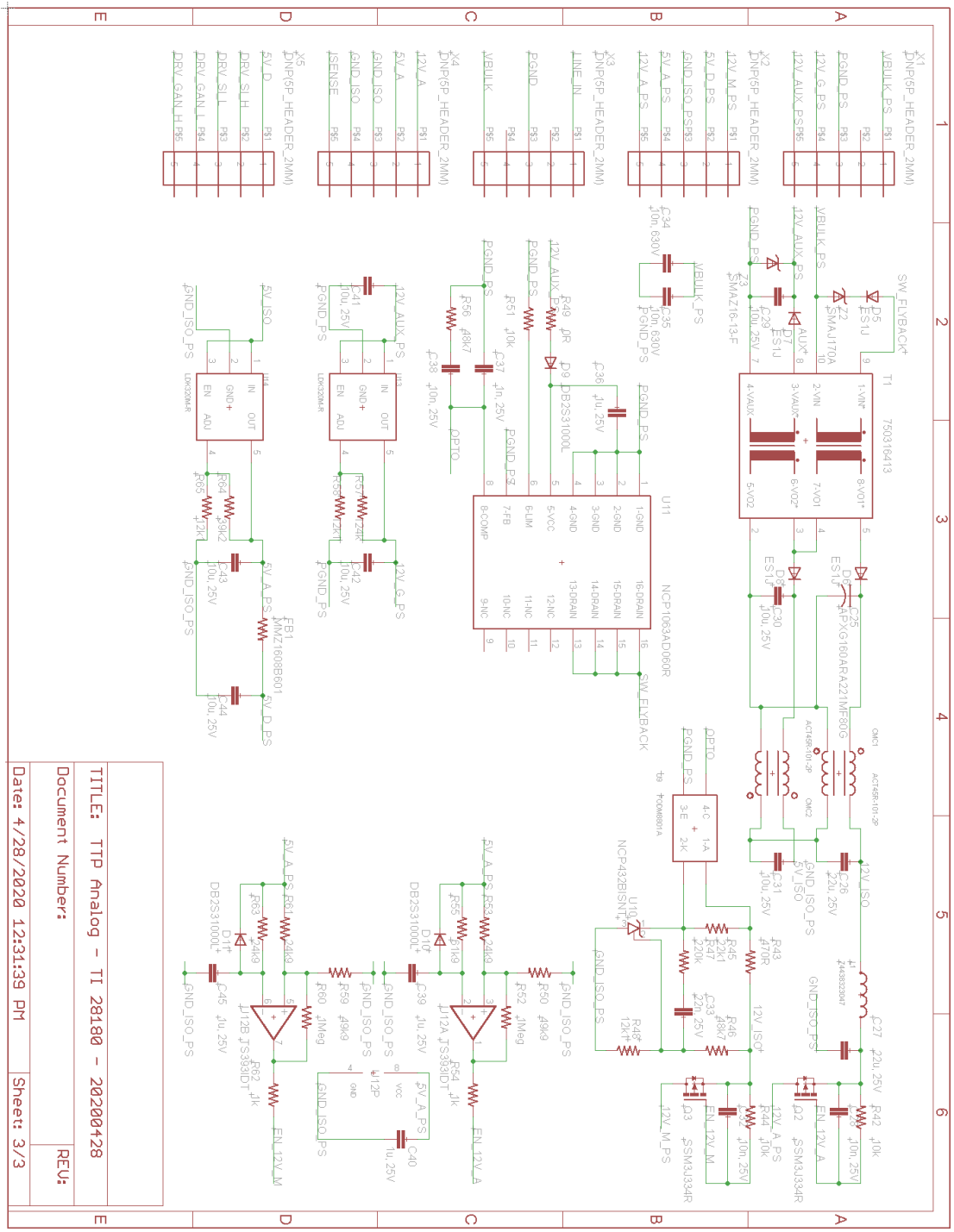


Fig 8c

Table 1. TDTTP4000W065AN_0V1 main board bill of materials (BOM)

TDTTP4000W065AN_MAINBOARD - BOM				
Qty	Value	Device	Parts	Manufacturing PN
2	JUMPER TIN SMD	JUMPER TIN SMD	JP1, JP2	S1621-46R
5	CONN RCPT 5POS 0.079 GOLD PCB	CONN RCPT 5POS 0.079 GOLD PCB	X1, X2, X3, X4, X5	MMS-105-01-L-SV
1	TERM BLK 3P SIDE ENT 9.53MM PCB	TERM BLK 3P SIDE ENT 9.53MM PCB	CN1	OSTT7032150
1	TERM BLK 2P SIDE ENT 9.53MM PCB	TERM BLK 2P SIDE ENT 9.53MM PCB	CN2	OSTT7022150
2	FUSE CLIP	CARTRIDGE PCB	F1 - Holder	BK/1A1907-06-R
1	FUSE CERM 30A	250VAC 125VDC 3AB	F1 - Fuse	BK/ABC-30-R
1	LAM 4K 50mm mit Motor 12V	LAM 4K 50mm mit Motor 12V	HS1, HS2 - One Piece Heat Sink	10038775
4	THFU 2	THFU 2	Clips for Mounting Devices onto Heat Sink	10065593
4	Thermal Pad	Thermal Pad	Thermal Pad for Mounting Devices onto Heat Sink	SPK10-0.006-00-104
1	FAN AXIAL	40X10MM VAPO 12VDC	Fan	CFM-4010V-185-314
1	FINGER GUARD 40MM METAL	FINGER GUARD 40MM METAL	Finger guard for Fan	8149
1	DIODE SCHOTTKY	40V 1A SOD123W	D1	PMEG40T10ERX
1	BRIDGE RECT 1PHASE	600V 25A GBJ	D2	GBJ2506-F
2	DIODE GEN PURP	DIODE GEN PURP	D3, D5	ES1J
1	DIODE SCHOTTKY	DIODE SCHOTTKY	D4	DB2S31000L
2	MOSFET N-CH 650V	MOSFET N-CH 650V	Q1, Q4	IPW60R017C7XKSA1
2	TP65H035G4WS	TP65H035G4WS	Q2, Q3	TP65H035G4WS
1	RELAY GEN PURPOSE SPST 30A 12V	RELAY GEN PURPOSE SPST 30A 12V	U1	JTN1AS-PA-F-DC12V

1	IC CAPACITOR DISCHARGE 8SO	IC CAPACITOR DISCHARGE 8SO	U2	CAP019DG-TL
2	DGTL ISO 2.5KV GATE DRVR 16SOIC	DGTL ISO 2.5KV GATE DRVR 16SOIC	U3, U4	SI8273BBD-IS1R
2	FERRITE BEAD 220 OHM	0603 1LN	FB1, FB2	MMZ1608B221CTAH0
4	RES SMD 100K OHM	1% 1/10W 0603	R16, R17, R29, R30	RC0603FR-07100KL
2	RES SMD 15 OHM	5% 1/10W 0603	R33, R36	RC0603JR-0715RL
4	RES SMD 10K OHM	1% 1/10W 0603	R22, R25, R34, R37	RC0603FR-0710KL
4	RES SMD 33 OHM	1% 1/10W 0603	R19, R20, R31, R32	RC0603FR-0733RL
1	RES SMD 33K OHM	1% 1/10W 0603	R27	RC0603FR-0733KL
2	RES SMD 36 OHM	1% 1/10W 0603	R21, R24	RC0603FR-0736RL
1	RES SMD 49.9K OHM	1% 1/10W 0603	R26	RC0603FR-0749K9L
7	RES SMD 10 OHM	1206 3/4W 5%	R2, R11, R12, R18, R23, R28, R35	SR1206JR-7T10RL
6	RES SMD 37.4K OHM	1% 1/4W 1206	R4, R5, R6, R7, R8, R9	RC1206FR-0737K4L
2	RES SMD 1206	RES SMD 1206	R10, R15	DNP
2	RES 0.004 OHM	1% 3W 2512	R13, R14	PA2512FKE7T0R004E
2	ICL 47 OHM	20% 3A 17.5MM	R1, R3	MF72-047D15
4	CAP CER 100PF	25V NP0 0603	C12, C13, C20, C21	CC0603JRNP08BN101
1	CAP CER 1UF	25V X5R 0603	C16	CC0603KRX5R8BB105
4	CAP CER 10UF	25V X5R 0805	C11, C14, C15, C22	GRM21BR61E106KA73L
2	CAP CER 10000PF	630V X7R 1206	C9, C10	CC1206KKX7RZBB103
4	CAP CER 22UF	25V X6S 1206	C17, C18, C19, C23	GRM31CC81E226ME11L
2	CAP CER SMD 1206	CAP CER SMD 1206	C1, C8	DNP
2	CAP FILM 4700PF	20% 630VDC RAD	CY1, CY2	BFC233820472
2	CAP FILM 0.22UF	10% 310VAC RAD	C2, C3	890334023028
3	CAP FILM 1.5UF	20% 630VDC RAD	CX1, CX2, CX3	R463N415040N1M
4	CAP ALUM 470UF	20% 450V SNAP	C4, C5, C6, C7	ALC10A471DF450

2	CMC_42X27MM_SM	CMC_42X27MM_SM	CMC1, CMC2	T60405-R6128-X225
1	DM-77071B	DM-77071B	L1	CWS-1SN-12606 - CWS
1	PFC_4KW INDUCTOR	PFC_4KW INDUCTOR	PFC_CHOKE	T91880B - SUMIDA
11	stand off (nylon 1/2)	stand off (nylon 1/2)	standoff for pcb board	1902C
11	machine screw (ss 1/2)	machine screw (ss 1/2)	screw for stand off for pcb board	9902
4	machine screw (ss 5/8)	machine screw (ss 5/8)	screw for FAN to Heatsink	29316

Table 2. TDTTP4000W065AN_0V1 control board bill of materials (BOM)

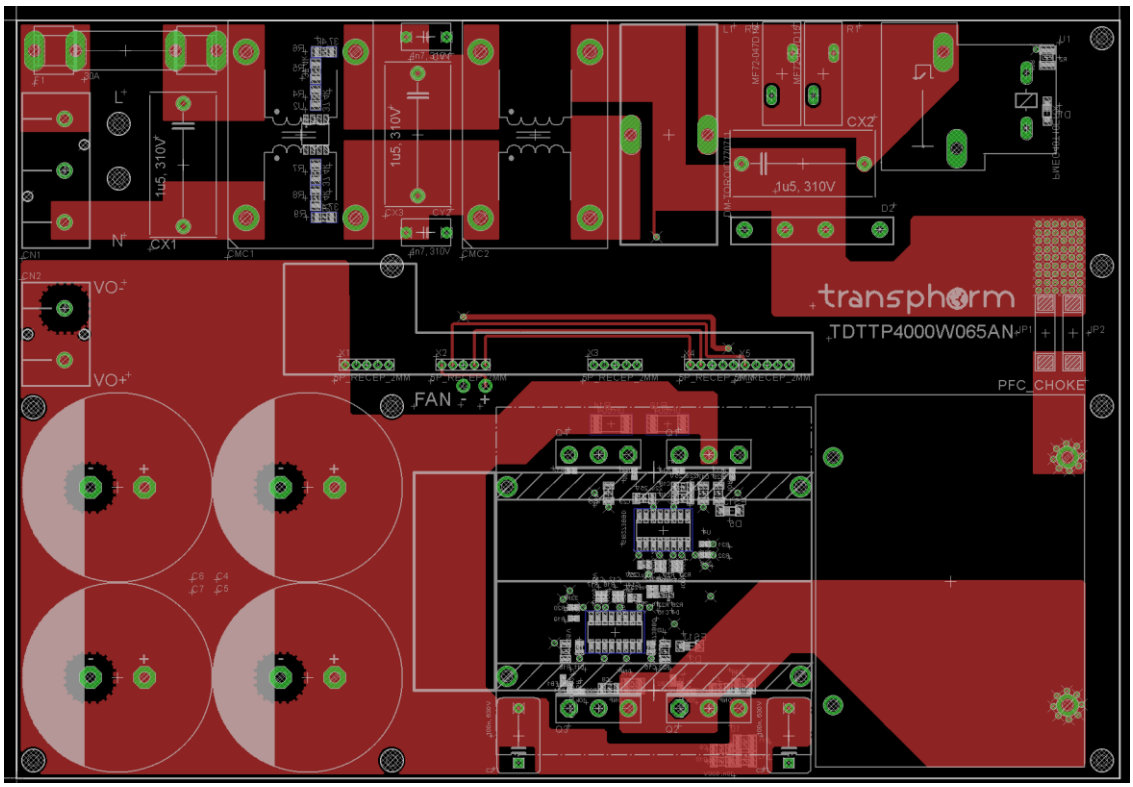
TDTTP4000W065AN_CTRLCARD - BOM				
Qty	Value	Device	Parts	Manufacturing PN
1	0R	RES0603	R49	RC0603JR-070RL
4	1Meg	RES0603	R7, R22, R52, R60	RC0603FR-071ML
3	1k	RES0603	R21, R54, R62	RC0603FR-071KL
1	1n	CAP0603	C14	C0603C102K3RACTU
1	1n, 10V	CAP0603	C12	
2	1n, 25V	CAP0603	C8, C37	C0603C102K3RACTU
1	1n5, 10V	CAP0603	C1	C0603C152J8RACTU
8	1u, 25V	CAP0603	C21, C22, C23, C24, C36, C39, C40, C45	C0603C105K3RACTU
1	4u7, 10V	CAP0603	C4	CC0603MRX5R6BB475
2	5k1	RES0603	R8, R23	RC0603FR-075K1L
4	10k	RES0603	R26, R42, R44, R51	RC0603FR-0710KL
3	10n, 25V	CAP0603	C28, C32, C38	C0603C103J3GACTU
2	10n, 630V	CAP1206	C34, C35	CC1206KKX7RZBB103

13	10u, 25V	CAP0805	C15, C16, C17, C18, C19, C20, C29, C30, C31, C41, C42, C43, C44	C0805C106K3PAC7800
3	12k1	RES0603	R48, R58, R65	RC0603FR-0712K1L
1	16k	RES0603	R4	RC0603FR-0716KL
1	22k1	RES0603	R45	RC0603FR-0722K1L
1	22n, 25V	CAP0603	C33	C0603C223K3RACTU
2	22p, 25V	CAP0603	C7, C10	C0603C220K3GACTU
2	22u, 25V	CAP1206	C26, C27	GRM31CC81E226ME11L
3	24k9	RES0603	R53, R61, R63	RC0603FR-0724K9L
2	30k	RES0603	R6, R24	RC0603FR-0730KL
1	33k	RES0603	R2	RC0603FR-0733KL
2	39k2	RES0603	R39, R64	RC0603FR-0739K2L
1	40k2	RES0603	R25	RC0603FR-0740K2L
2	48k7	RES0603	R46, R56	RC0603FR-0748K7L
2	49R9	RES0603	R36, R40	RC0603FR-0749R9L
2	49k9	RES0603	R50, R59	RC0603FR-0749K9L
2	61k9	RES0603	R16, R55	RC0603FR-0761K9L
2	100k	RES0603	R20, R37	RC0603FR-07100KL
6	100p, 25V	CAP0603	C2, C5, C6, C9, C11, C13	C0603C101J3GACTU
1	124k	RES0603	R57	RC0603FR-07124KL
1	220k	RES0603	R47	RC0603FR-07220KL
1	330R	RES0603	R1	RC0603JR-07330RL
1	470R	RES0603	R43	RC0603JR-07470RL
15	470k	RES1206	R9, R10, R11, R12, R13, R14, R17, R18, R19, R28, R29, R30, R33, R34, R35	RC1206FR-07470KL
1	560n, 10V	CAP0603	C3	C0603C564K8PACTU

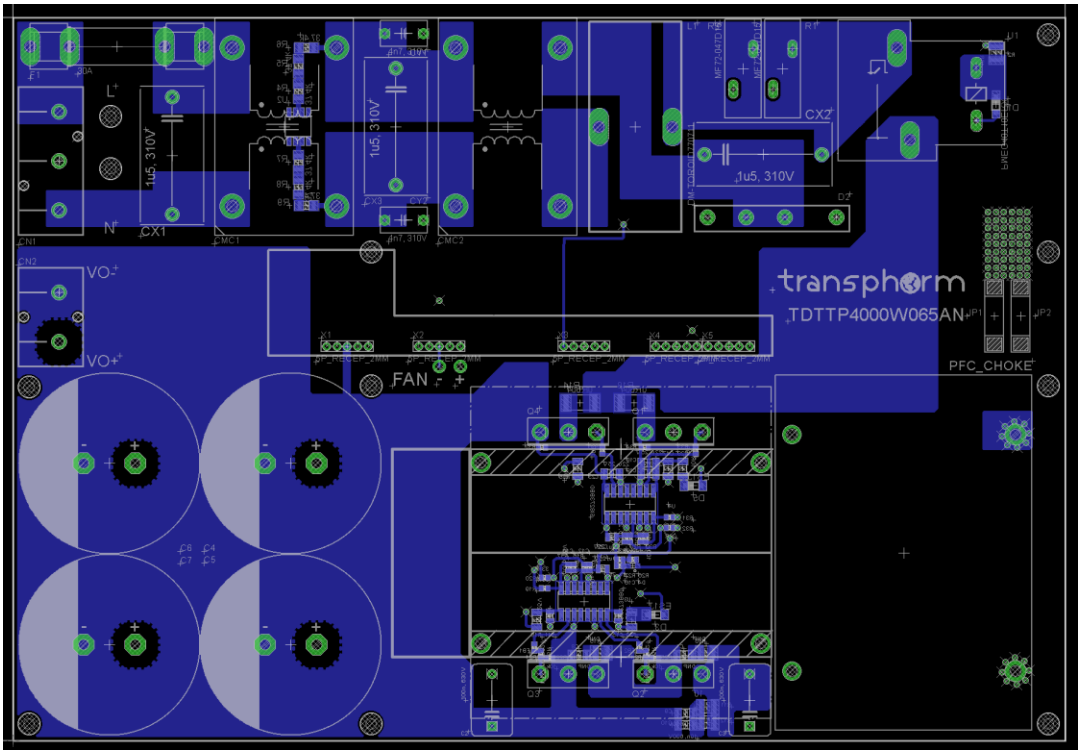
1	750316413	750314352_750314352	T1	750316413
1	74438323047	INDUCTOR_SMD1008	L1	74438323047
4	DB2S31000L	DIODE_SSMINI2	D1, D9, D10, D11	DB2S31000L
1	DB3X313N0L	DIODE_CC_SOT23	D2	DB3X313N0L
2	CMC_ACT45	CMC_ACT45	CMC1, CMC2	CMC_ACT45
1	APXG160ARA221MF80G	APXG160ARA221MF80G	C25	APXG160ARA221MF80G
1	BSS138N	BSS138-7-F	Q1	BSS138NH6327XTSA2
5	5P_HEADER_2MM	5P_HEADER_2MM	X1, X2, X3, X4, X5	TMM-105-01-L-S-RA
1	CZRU52C4V7	CZRU52C4V7	Z1	CZRU52C4V7
6	ES1J	DIODE_DO214	D3, D4, D5, D6, D7, D8	ES1J
1	FODM8801A	FODM8801A_MINIFLAT04	U9	FODM8801A
2	LDK320M-R	LDK320M_SOT23-5L	U13, U14	LDK320M-R
1	LMV761MF	MAX9030	U4	LMV761MF
1	MMZ1608B601	RES0603	FB1	MMZ1608B601
1	NCP432BISNT	TL431	U10	NCP432BISNT
1	NCP1063AD060R	NCP1063_SO16	U11	NCP1063AD060R
1	Rdc: 1.8k	RES0603	R15	RC0603JR-071K8L
1	Rdt1: 2.61k	RES0603	R3	RC0603FR-072K61L
1	Rdt2: 3.57k	RES0603	R5	RC0603FR-073K57L
1	Rlocurr: 20k	RES0603	R41	RC0603FR-0720KL
1	Rzc: 1.21k	RES0603	R27	AC0603FR-071K21L
1	SMAJ170A	ZENER_DO214AC	Z2	SMAJ170A
1	SMAZ16-13-F	ZENER_DO214AC	Z3	SMAZ16-13-F
1	SN74AC04PWR	SN74AC04_PW	U6	SN74AC04PWR
2	SN74AC08PWR	SN74AC08_PW	U7, U8	SN74AC08PWR
1	SN74AC32PWR	SN74AC32_PW	U5	SN74AC32PWR
2	SSM3J334R	PMOS_SOT23	Q2, Q3	SSM3J334R,LF

2	TS393IDT	LM293_SO8	U2, U12	TS393IDT
1	TSX712IYDT	LMX58_DT	U3	TSX712IYDT
1	UCC28180_SO8	UCC28180_SO8	U1	UCC28180DR

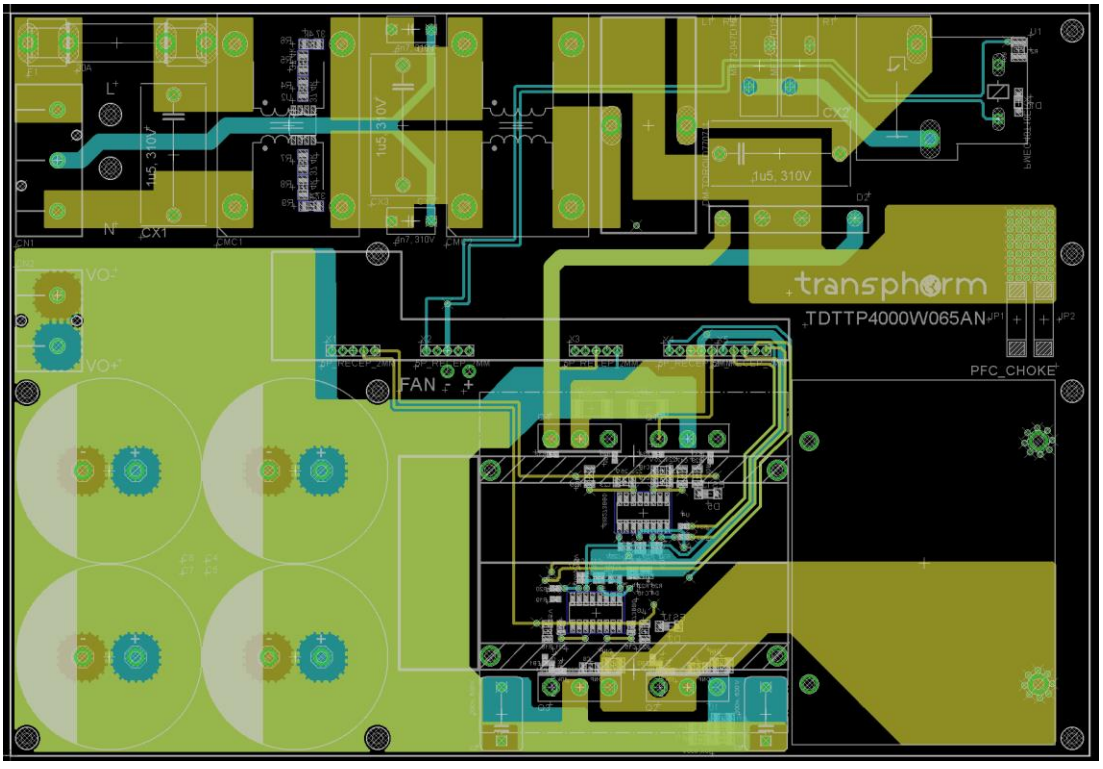
For this evaluation board, the PFC circuit has been implemented on a 4-layer PCB. The GaN FET half-bridge is built with TP65H035G4WS (0.035 ohm) devices by Transphorm, Inc. The slow Si switches are IPW60R017C7XKSA1super junction MOSFETs with 0.017 ohm on-resistance. The inductor is made of a High Flux core with the inductance of 480 uH and a dc resistance of 0.025 Ohm, designed to operate at 65 kHz. A simple 2 A rated high/low side driver IC (Si8273) with 0/12 V as on/off states directly drives each GaN FETs. A TI UCC28180DR controller handles the control algorithm. The voltage and current loop controls are similar to conventional boost PFC converter. The feedback signals are dc output voltage (VO), ac input potentials (V_{ACP} and V_{ACN}) and inductor current (I_L). The input voltage polarity and RMS value are determined from V_{ACP} and V_{ACN}. The outer voltage loop output multiplied by $|V_{AC}|$ gives a sinusoidal current reference. The current loop gives the proper duty ratio for the boost circuit. The polarity determines how PWM signal is distributed to drive Q1 and Q2. A soft-start sequence with a duty ratio ramp is employed for a short period at each ac zero-crossing for better stability.



(a) PCB top layer



(b) PCB bottom layer



(c) PCB inner layer 2 (ground plane) + inner layer 3 (power plane)

Figure 9. PCB layers

Using the board

The board can be used for evaluation of Transphorm GaN 0.035 ohm FETs in a Bridge-less totem-pole PFC circuit. It is not a complete circuit, but rather a building block.

Turn on Sequences:

1) Connect an Electronic / resistive load to the corresponding marking (CN2).

The requirement for the resistive load:

– At 115 Vac input: 0 W and ≤ 2000 W

– At 230 Vac input: 0 W and ≤ 4000 W

2) With HV power off, connect the high-voltage AC power input to the corresponding marking (CN1) on the PCB;

-N and L (PE: potential ground)

3) Turn on the AC power input (85 Vac to 265 Vac; 50 – 60Hz)

a. Minimum recommended power load for turn-on sequence is 400W.

Monitor CN2 output voltage with Vdc meter to verify 385V +/- 5V is generated.

b. Electronic / resistive load can be increased while AC supply is ON and board is functional.

Turn off sequences:

1) Switch off the high-voltage AC power input;

2) Verify Input and Output voltage = 0.

Operational Waveforms

Fig 10a and 10b below shows the converter start-up procedure at 0W and 350W for Low line input:

CH1 shows the DC input current; CH2 is the DC bus voltage waveform and CH3 is the PWM, and CH4 is the Vac input voltage. For the start-up, there are three phases to charge the DC bus to a reference voltage. In the beginning, the relay K1 is open, and DC bus capacitors are charged by input voltage through NTC and Diode Bridge. When the Vdc is over 100V, the relay K1 is closed to bypass the NTC, and the Vdc increase to the peak of the input voltage. After 100ms, the GaN FETs leg is engaged in voltage closed-loop control, in which the DC bus voltage reference slowly increases to the rated voltage 385V. The NTC and diode bridge are applied in this circuit to avoid high inrush current flow through the GaN FETs.

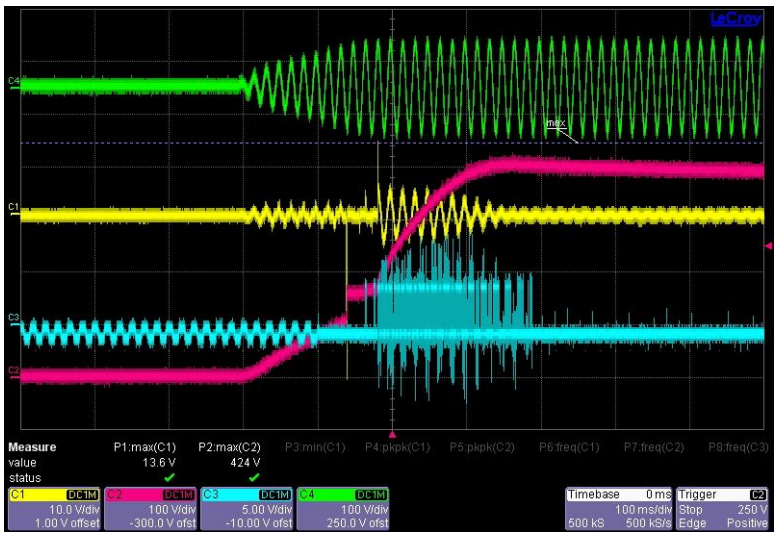


Fig 10a. Start-up of the Bridge-less totem-pole PFC (CH1: Iac(in), Ch2: Vdc(out), CH3: PWM, Ch4: Vac(in)) 120Vac with 0W load

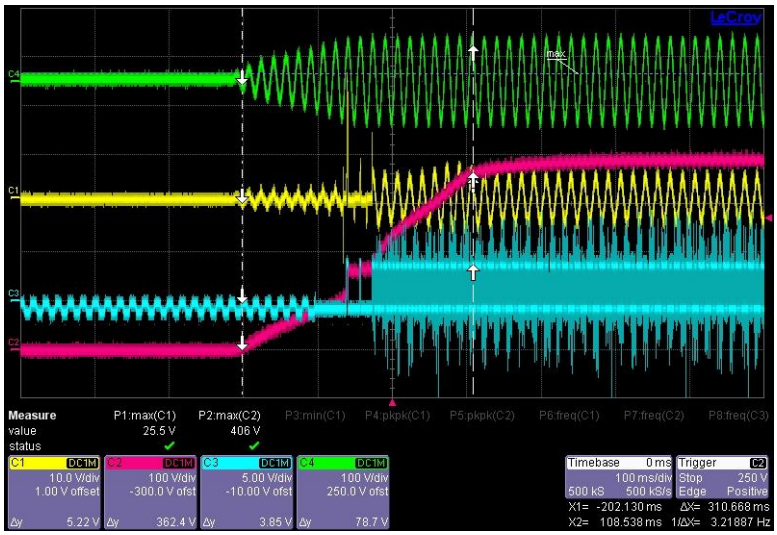


Fig 10b. Start-up of the Bridge-less totem-pole PFC (CH1: Iac(in), Ch2: Vdc(out), CH3: PWM, Ch4: Vac(in)) 120Vac with 350W load

Fig 11a and 11b below shows the converter start-up procedure at 0W and 350W for High line input:

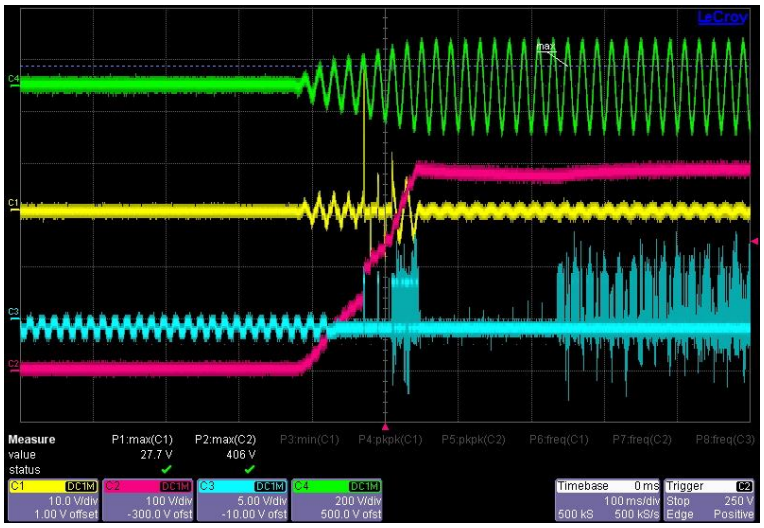


Fig 11a. Start-up of the Bridge-less totem-pole PFC (CH1: Iac(in), Ch2: Vdc(out), CH3: PWM, Ch4: Vac(in)) 230Vac with 0W load

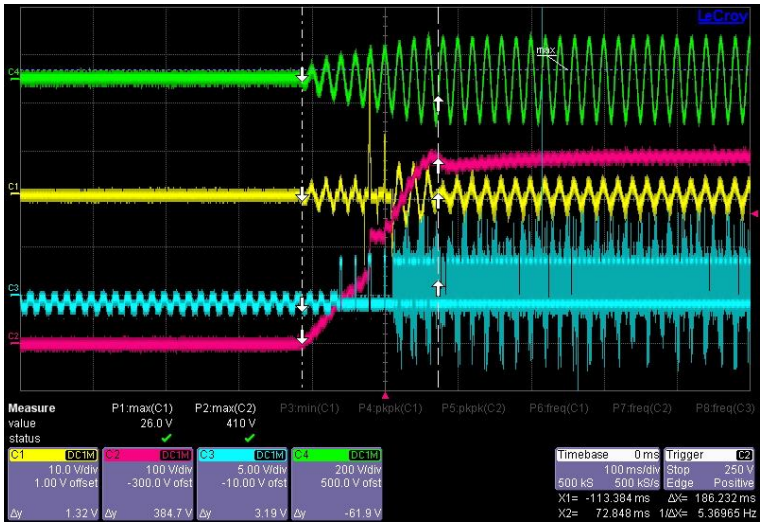


Fig 11b. Start-up of the Bridge-less totem-pole PFC (CH1: Iac(in), Ch2: Vdc(out), CH3: PWM, Ch4: Vac(in)) 230Vac with 350W load

Fig 12 below shows the Vds of Q2 at 3.5k. It can be seen that the voltage spike is 56V at iL = 20A. In this circuit, the RC snubber and Rg help to reduce voltage spikes.

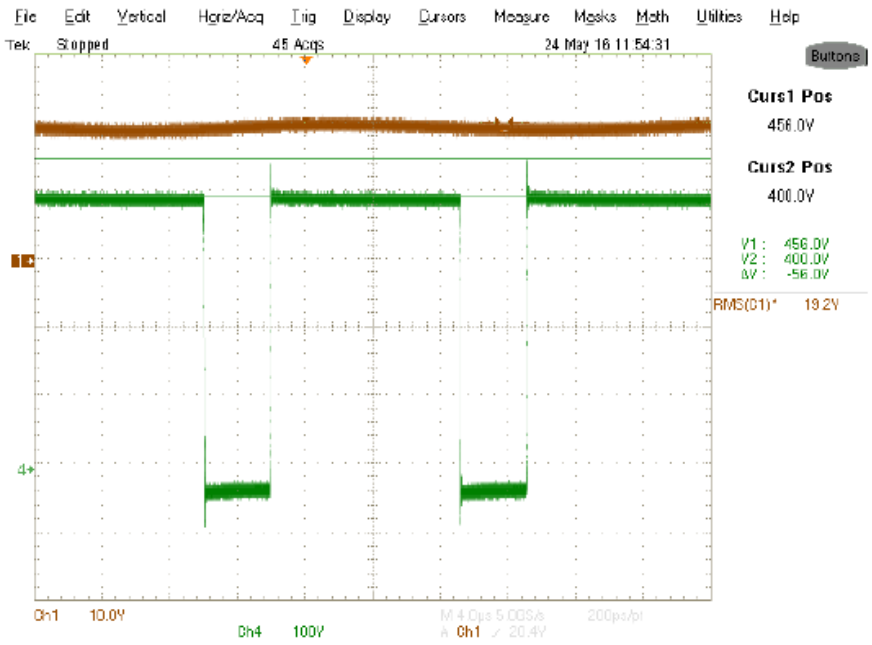


Fig 12. Waveforms of Vds of Q2 at iL = 20A. CH1: input current Iin (10A/div) ; CH4: (a) Vds (100V/div)

Efficiency Sweep and THDi

For the efficiency measurement, the input/output voltage and current will be measured for the input/output power calculation with a power analyzer. Efficiency has been measured at 120 Vac or 230 Vac input and 400 Vdc output using the WT1800 precision power analyzer from Yokogawa. The efficiency results for this Totem Pole PFC board are shown in Fig.13. The extremely high efficiency of 99% at 230Vac input, and > 98% at 120V ac input is the highest among PFC designs with similar PWM frequency; this high efficiency will enable customers to reach peak system efficiency to meet and exceed Titanium standards.

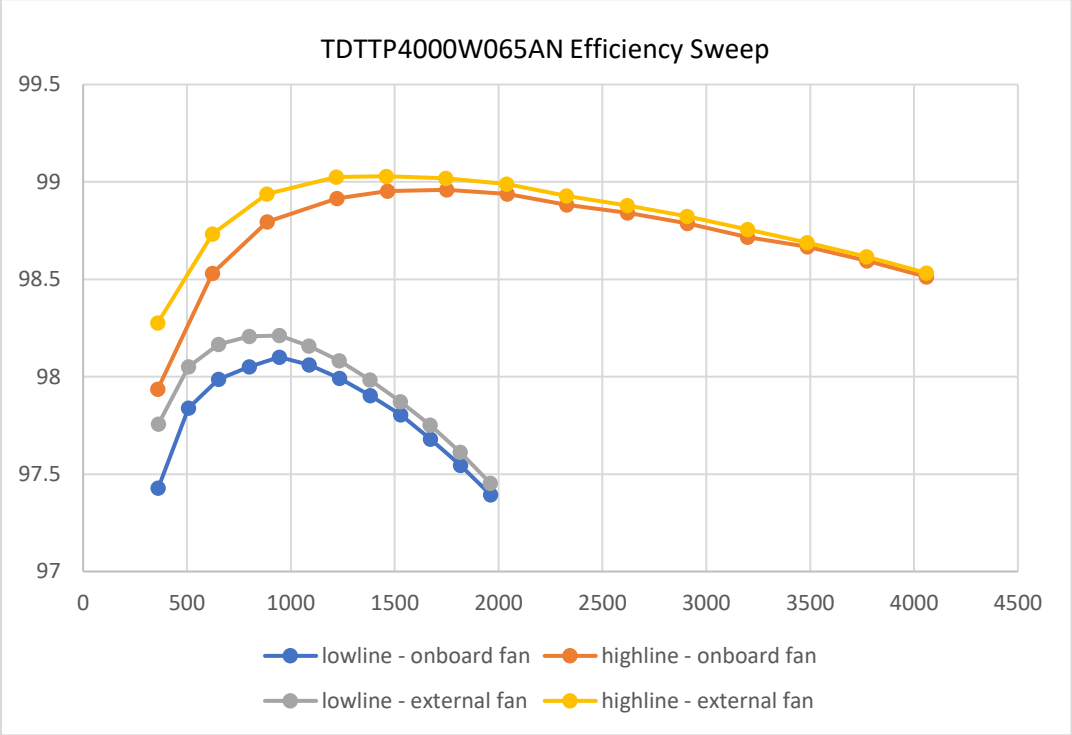


Figure 13. The efficiency results for Bridge-less Totem-pole PFC Evaluation Board.

The THDi is measured using WT1800 at the condition of input THDv 3.8%. As shown in Fig 14 below, it meets the standard of IEC61000-3-12.

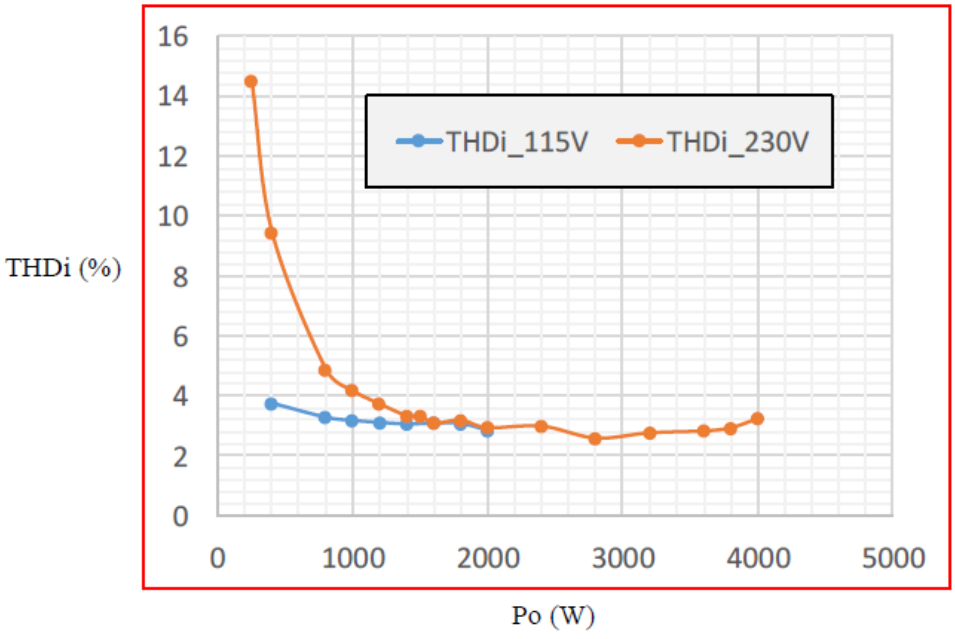


Fig 14. THDi meets IEC61000-3-12 (>16A)

Maximum Load Limit:

The TDTTP4000W065AN Bridge-less totem-pole PFC eval board is allowed to run overload in a short time. The rated input current for < 230Vac input is 18A, and the 10% overload current can be 19.8A. The input OCP will be triggered when the current is over 21A.

Fig 15 below shows the input voltage and current waveforms at max power for low line and high line operation

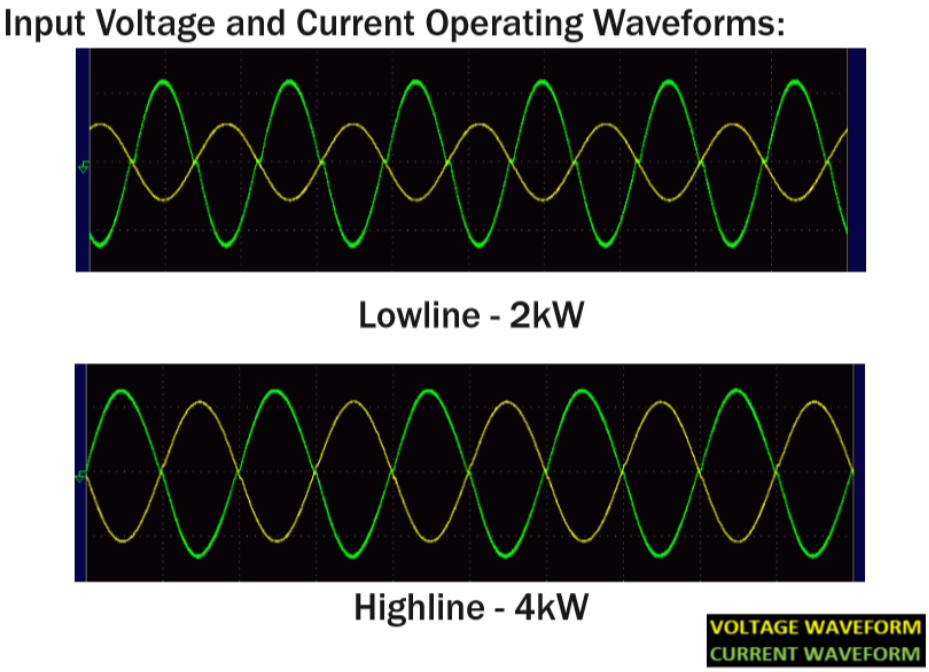


Fig 15. Input voltage and current operating waveforms – max power (low line and high line)

WARNINGS:

This demo board is intended to demonstrate GaN FET technology. While it provides the main features of a totem-pole PFC, it is not intended to be a finished product and does not have all the protection features found in commercial power supplies. Along with this explanation go a few warnings which should be kept in mind:

1. An isolated AC source should be used as input; an isolated lab bench grade power supply or the included AUX DC supply should also be used for the 12V DC power supply. Float the oscilloscope by using an isolated oscilloscope or by disabling the PE (Protective Earth) pin in the power plug. Float the current probe power supply (if any) by disabling the PE pin in the power plug.

2. Use a resistive load only. The Totem-pole PFC kit can work at zero load with burst mode. The output voltage will be swinging between 375V and 385V during burst mode.

3. The demo board is not fully tested at large load steps. **DO NOT** apply a very large step in the load (>2000W) when it is running.

4. **DO NOT** manually probe the waveforms when the demo is running. Set up probing before powering up the demo board.

5. The auxiliary Vdc supply must be 12 V. The demo board will not work under, for example, 10 V or over 15V Vdc.

6. **DO NOT** touch any part of the demo board when it is running.

7. When plugging the control cards into the socket, make sure the control cards are fully pushed down with a clicking sound.

8. If the demo circuit goes into protection mode it will work as a diode bridge by shutting down all PWM functions. Recycle the bias power supply to reset the DSP and exit protection mode.

9. **DO NOT** use a passive probe to measure control circuit signals and power circuit signals in the same time. GND1 and AGND are not the same ground.

10. To get clean Vgs of low side GaN FET, it is recommended not to measure the Vds at the same time.

11. It is not recommended using passive voltage probe for Vds, Vgs measurement and using differential voltage probe for Vin measure measurement at the same time unless the differential probe has very good dv/dt immunity.

REFERENCE:

[1]. Liang Zhou, Yi-Feng Wu and Umesh Mishra, “True Bridge-less Totem-pole PFC based on GaN FETs”, PCIM Europe 2013, 14-16 May, 2013, pp.1017-1022.

[2]. L. Huber, Y. Jang, and M. M. Jovanovic, “Performance evaluation of Bridge-less PFC boost rectifiers,” IEEE Transactions on Power Electronics, Vol. 23, No. 3, pp. 1381-1390, May 2008.

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