

VECP Starter Kit

- *Xilinx Zynq UltraScale+ ZU3EG MPSoC based on 1.2 GHz Quad Arm Cortex-A53 and 600MHz Dual Cortex-M4 Cores*
- *4GB DDR4 SDRAM (64-bit, 2400MHz)*
- *4GB eMMC Flash, 128MB QSPI Flash*
- *1 x USB 3.0 Host, 1 x USB 3.0 Device, 1 x USB-UART, 2 x Gigabit Ethernet, MIPI-CSI, HDMI, TF...*
- *SONY imx334 4K Sensor*
- *Ready to Run Linux OS*
- *Built-in 4k/30fps Image Signal Processing IP Core*
- *Built-in GigE Vision 2.0 IP Core*
- *Built-in Machine Vision USB3 Vision IP Core*



Figure 1-1 VECP Starter Kit

The **VECP Starter Kit** is an affordable and complete **Vision Edge Computing Platform** to provide an excellent image processing solution for computer vision development based on [Xilinx Zynq UltraScale+ ZU3EG MPSoC](#) which features a 1.2 GHz quad-core ARM Cortex-A53 64-bit application processor, a 600MHz dual-core real-time ARM Cortex-R5 processor, a Mali400 embedded GPU and rich FPGA fabric. The kit comes with a **MYD-CZU3EG-ISP development board** and some necessary cable accessories to help users start their development rapidly.

The **MYD-CZU3EG-ISP development board** is capable of handling **4K video at 30fps** through the built-in **ISP core** and can implement **ultra-low delay video transmission at maximum 0.7ms**. The input videos support **Bayer, YCbCr and RGB** formats to meet the demand of high frame rate and high-resolution image acquisition. The image can be output through diversified image output interfaces including **HDMI, Gigabit Ethernet and USB 3.0**. The integrated **GigE vision IP core** supports Machine Vision **GenICam V2.4.0** standard and user-defined XML files. The **USB3 vision IP core** also meets the industrial machine vision standard.

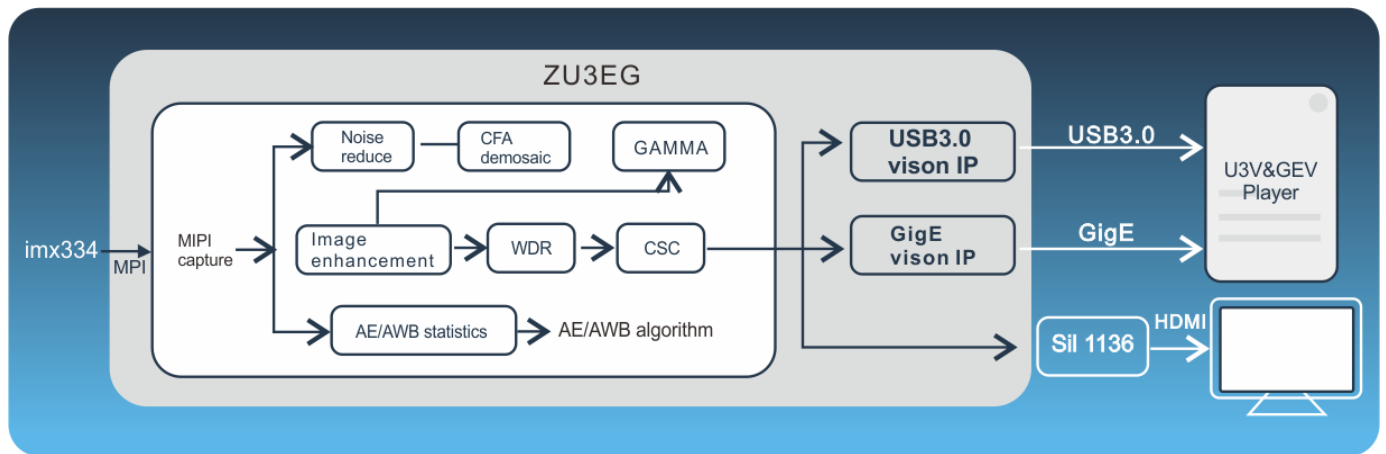


Figure 1-2 VECP Data Processing Frame

The **MYD-CZU3EG-ISP development board** consists of a [MYC-CZU3EG CPU Module](#) with installed **active heatsink**, a **base board** and a **SONY imx334 4K Sensor** which is installed on the rear of the base board and connected to the **MIPI-CSI** interface through an FPC cable. From the CPU PL part, the board has extended **one Gigabit Ethernet**, **one USB 3.0 device** and **one HDMI interface** for image output. From the PS part, the board has extended **one USB-to-UART interface**, **one USB 3.0 Host**, **one TF card slot** and **one Gigabit Ethernet** for data communication purpose. The board is ready to run **Linux** operating system provided with plenty of software resources.

MYIR also offer custom design services for board design based on the **MYD-CZU3EG-ISP** development board or customized image sensors or customized IP cores according to customers' requirements.

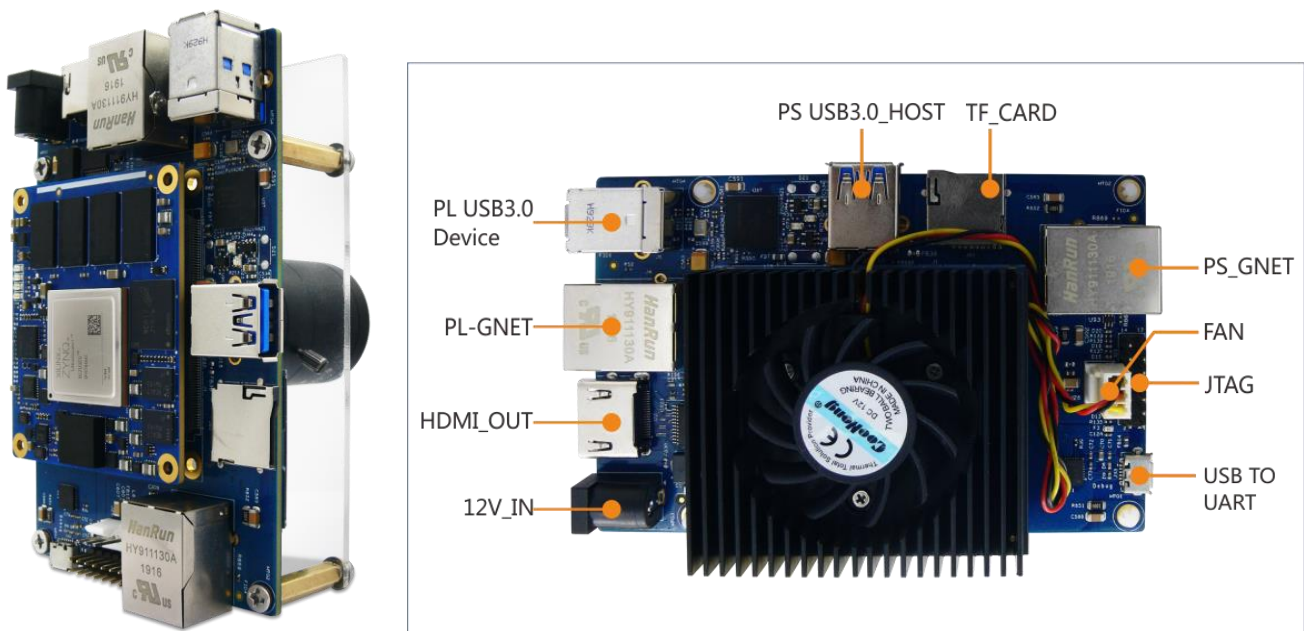


Figure 1-3 MYD-CZU3EG-ISP Development Board Top-View (delivered with installed active heatsink by default)



Figure 1-4 MYD-CZU3EG-ISP Development Board Base Board Bottom-View

The built-in ISP core of the **MYD-CZU3EG-ISP development board** has excellent image processing capabilities. It has outstanding intelligent noise reduction effect and can separate from motion area and background accurately. The digital WDR function and super 3D denoise technology of the ISP core can restore information from ultra-low illuminance precisely. The automatic exposure strategy can be adopted according to different usage scenarios and the color reduction is strong. The right images below are processed through the IP cores of the MYD-CZU3EG-ISP development board which may make you feel some difference.



Figure 1-5 Image Effect Comparison

Hardware Specification

Zynq® UltraScale+™ MPSoC devices provide 64-bit processor scalability while combining real-time control with soft and hard engines for graphics, video, waveform, and packet processing. Built on a common real-time processor and programmable logic equipped platform, three distinct variants include dual application processor (CG) devices, quad application processor and GPU (EG) devices, and video codec (EV) devices.

	CG Devices	EG Devices	EV Devices
Application Processor	Dual-core ARM® Cortex™-A53 MPCore™ up to 1.3GHz	Quad-core ARM Cortex-A53 MPCore up to 1.5GHz	Quad-core ARM Cortex-A53 MPCore up to 1.5GHz
Real-Time Processor	Dual-core ARM Cortex-R5 MPCore up to 533MHz	Dual-core ARM Cortex-R5 MPCore up to 600MHz	Dual-core ARM Cortex-R5 MPCore up to 600MHz
Graphics Processor		Mali™-400 MP2	Mali™-400 MP2
Video Codec			H.264 / H.265
Programmable Logic	103K–600K System Logic Cells	103K–1143K System Logic Cells	192K–504K System Logic Cells
Applications	<ul style="list-style-type: none"> • Sensor Processing & Fusion • Motor Control • Low-cost Ultrasound • Traffic Engineering 	<ul style="list-style-type: none"> • Flight Navigation • Missile & Munitions • Military Construction • Secure Solutions • Networking • Cloud Computing Security • Data Center • Machine Vision • Medical Endoscopy 	<ul style="list-style-type: none"> • Situational Awareness • Surveillance/Reconnaissance • Smart Vision • Image Manipulation • Graphic Overlay • Human Machine Interface • Automotive ADAS • Video Processing • Interactive Display

Figure 1-6 Zynq UltraScale+ MPSoCs

The Zynq UltraScale+ family provides footprint compatibility to enable users to migrate designs from one device to another. Any two packages with the same footprint identifier code (last letter and number sequence) are footprint compatible. MYiR is using the **XCZU3EG-1SFVC784E** MPSoC for VECP Starter Kit by default, the C784 package covers the widest footprint compatibilities that enable users to select devices among CG, EG and EV.

Pkg	mm	Zynq® UltraScale+™																				
		CG Devices							EG Devices							EV Devices						
		ZU2CG	ZU3CG	ZU4CG	ZU5CG	ZU6CG	ZU7CG	ZU9CG	ZU2EG	ZU3EG	ZU4EG	ZU5EG	ZU6EG	ZU7EG	ZU9EG	ZU11EG	ZU15EG	ZU17EG	ZU19EG	ZU4EV	ZU5EV	ZU7EV
A484	19	■	■						■	■												
A625	21	■	■						■	■												
C784	23	■	■	■	■				■	■	■	■								■	■	
B900	31			■	■		■				■	■		■						■	■	■
C900	31					■		■					■		■		■					
B1156	35					■		■					■		■		■					
C1156	35						■							■								■
B1517	40														■	■	■	■				
F1517	40														■							■
C1760	42.5															■	■	■	■			
D1760	42.5																■	■	■			
E1924	45																	■	■			

Figure 1-7 Zynq® UltraScale+™ MPSoC Device Migration Table

Device	XCZU2CG	XCZU3CG	XCZU3EG	XCZU4EV	XCZU5EV
Logic cells (k)	103	154	154	192	256
CLB Flip-Flops (K)	94	141	141	176	234
CLB LUTs (K)	47	71	71	88	117
Block RAM (Mb)	5.3	7.6	7.6	4.5	5.1
UltraRAM (Mb)	-	-	-	13.5	18.0
DSP Slices	240	360	360	728	1,248
GTX transceivers	PS-GTR4x (6Gb/s)	PS-GTR4x (6Gb/s)	PS-GTR4x (6Gb/s)	PS-GTR4x (6Gb/s), GTH4x (16.3Gb/s)	PS-GTR4x (6Gb/s), GTH4x (16.3Gb/s)
Processor Units					
Application Processor Unit	Dual-core ARM® Cortex™-A53 MPCore™ up to 1.3GHz		Quad-core ARM® Cortex™-A53 MPCore™ up to 1.5GHz		
Memory w/ECC	L1 Cache 32KB I / D per core, L2 Cache 1MB, on-chip Memory 256KB				
Real-Time Processor Unit	Dual-core ARM Cortex-R5 MPCore™ up to 600MHz				
Memory w/ECC	L1 Cache 32KB I / D per core, Tightly Coupled Memory 128KB per core				
Graphics Processing Unit	-	-	Mali™-400 MP2 up to 667MHz		
Video Codec	-	-	-	H.264 / H.265	
Memory L2 Cache	64KB				
External Memory, Connectivity, Integrated Block Functionality					
Dynamic Memory Interface	x32/x64: DDR4, LPDDR4, DDR3, DDR3L, LPDDR3 with ECC				
Static Memory Interfaces	NAND, 2x Quad-SPI				
High-Speed Connectivity	PCIe® Gen2 x4, 2x USB3.0, SATA 3.1, DisplayPort, 4x Tri-mode Gigabit Ethernet				
General Connectivity	2 x USB 2.0, 2 x SD/SDIO, 2 x UART, 2 x CAN 2.0B, 2 x I2C, 2 x SPI, 4 x 32b GPIO				
Power Management	Full / Low / PL / Battery Power Domains				
Security	RSA, AES, and SHA				
AMS - System Monitor	10-bit, 1MSPS – Temperature and Voltage Monitor				

Table 1-1 MPSoC device selection guide

The MYD-CZU3EG-ISP development board takes full advantages of the Xilinx Zynq UltraScale+ ZU3EG MPSoC. The main features are listed in below table.

Features	Description
CPU	Xilinx Zynq UltraScale+ XCZU3EG-1SFVC784E (ZU3EG, 784 Pin Package) MPSoC
RAM	4GB DDR4 (64-bit, 2400MHz)
Flash	4GB eMMC, 128MB QSPI
PS unit	One USB 3.0 Host
	One USB-UART interface
	One TF card slot
	One 10/100/1000Mbps Ethernet interface
	One 2.54mm pitch 14-pin JTAG interface (PS, PL reused)
PL unit	One HDMI interface
	One 10/100/1000Mbps Ethernet interface
	One USB 3.0 device
	One MIPI-CSI interface (0.5mm pitch 40-pin FPC connector, on the rear of the base board)
	IO Expansion interface (0.5mm pitch 50-pin FPC connector, on the rear of the base board)
Image Sensor SONY IMX334LLR	Resolution: 3840 (H) x 2160 (V)
	Mega Pixels: 8.42 MP
	Frame Rate: 60 to 120 fps
	ADC Resolution: 12-bit
	Pixel Size: 2.0 μm \times 2.0 μm
	Interface: MIPI CSI-2
Dimensions	106.71mm x 69.98mm (base board)
Power supply	12V/2A
Working temp.	0~70 Celsius (commercial grade)
Target applications	IoT, Medical, Machine Vision, Industry, etc.

Table 1-2 MYD-CZU3EG-ISP Development Board Feature

Function Block Diagram

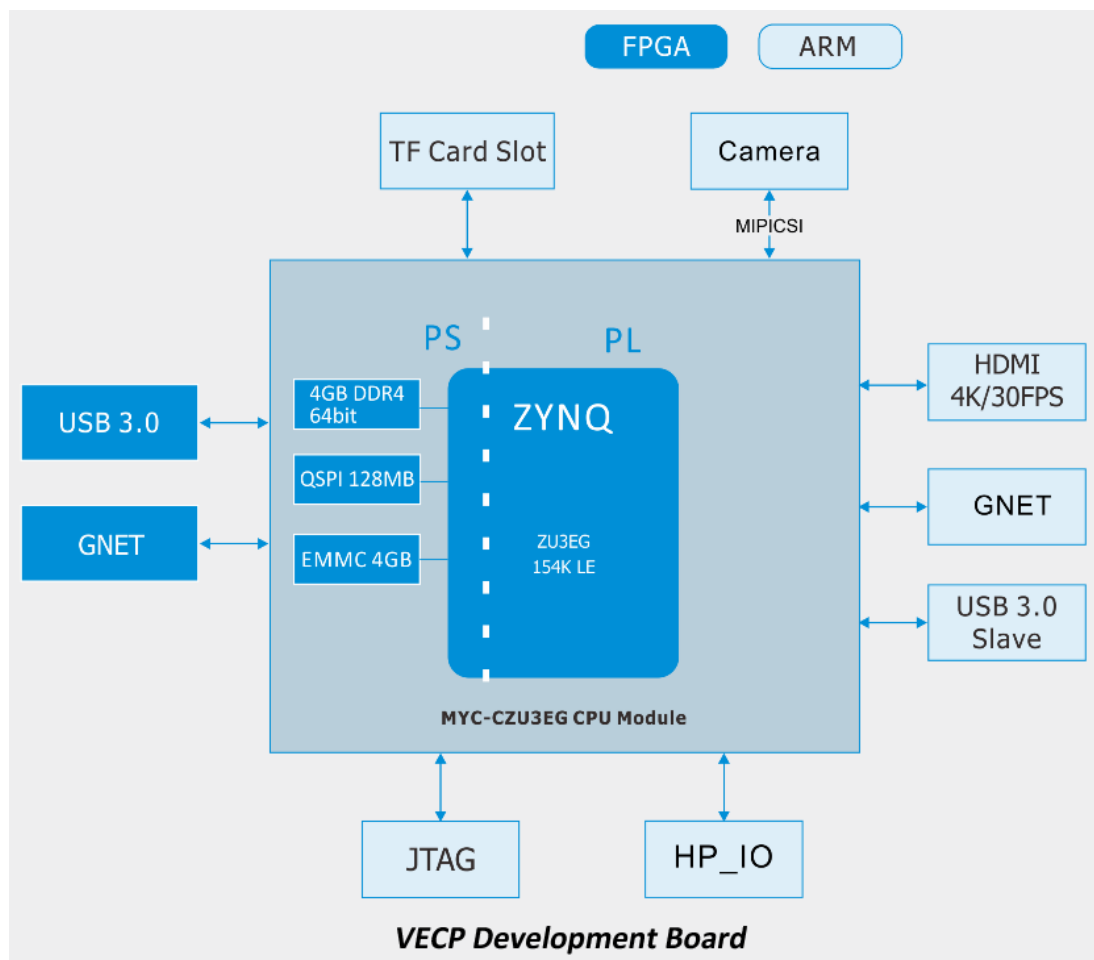


Figure 1-8 Function Block Diagram of MYD-CZU3EG-ISP Development Board

Dimension Chart

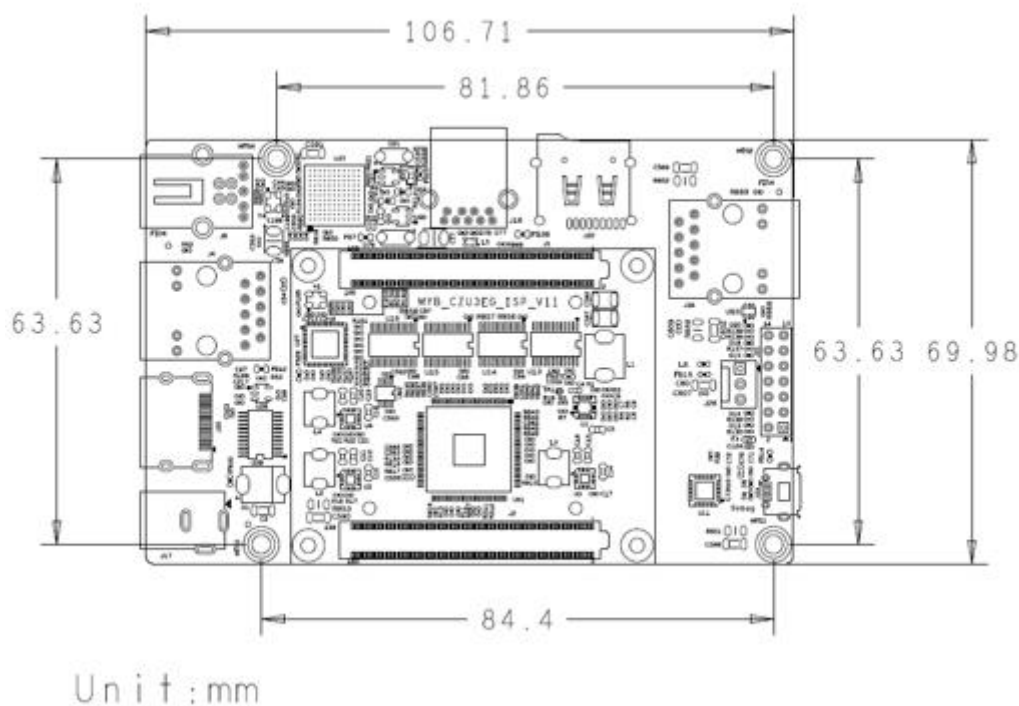


Figure 1-9 Dimension Chart of MYD-CZU3EG-ISP Development Board

Software Features

The MYD-CZU3EG-ISP Development Board is preloaded with Linux OS. MYIR provides software package in a product disk along with the goods delivery. The software package features as below:

Item	Features	Description	Remark
Cross compiler	gcc 7.2.1	gcc version 7.2.1 (Linaro GCC7.2)	
Boot program	BOOT.BIN	First boot program including FSBL, u-boot2018.01	Source code provided
Linux Kernel	Linux 4.14.0	Customized kernel for VECP Starter Kit	Source code provided
Drivers	USB Host	USB2.0/USB3.0 Host driver	Source code provided
	Ethernet	Gigabit Ethernet driver	Source code provided
	MMC/SD/TF	MMC/SD/TF card driver	Source code provided
	Camera	Camera driver	Source code provided
	HDMI	HDMI (Si1136 X chip) driver	Source code provided
	Button	Button driver	Source code provided
	UART	UART driver	Source code provided
	I2C	I2C driver	Source code provided
	LED	LED driver	Source code provided
	GPIO	GPIO driver	Source code provided
	QSPI	QSPI Flash MT25QU512ABB driver	Source code provided
	Watch dog	Watch dog driver	Source code provided
Applications	Net	Socket program	Source code provided
File System	Ramdisk	Ramdisk system image	File System
	Rootfs.tar	Buildroot, including QT	Source code provided

Table 1-3 Software Features of VECP Starter Kit

Order Information

Item	Packing List
<p>VECP Starter Kit (Part No.: MYD-CZU3EG-4E4D-1200-C-ISP)</p>	<ul style="list-style-type: none"> ➤ One VECP Development Board (including MYC-CZU3EG CPU Module with installed active heatsink and base board with installed SONY imx334 image Sensor) ➤ One HDMI cable ➤ One 12V/2A Power adapter ➤ One Mini USB 2.0 cable ➤ One 16GB TF card ➤ One Product disk <p>(Including user manual, datasheet, base board schematic in PDF format and software packages)</p>
<p>VECP Development Board (Part No.: MYD-CZU3EG-4E4D-1200-C-ISP-S)</p>	<ul style="list-style-type: none"> ➤ One VECP Development Board (including MYC-CZU3EG CPU Module with installed active heatsink and base board with installed SONY imx334 image Sensor) <p>Production recommended</p>
<p>MYC-CZU3EG CPU Module (Part No.: MYC-CZU3EG-4E4D-1200-C)</p>	<ul style="list-style-type: none"> ➤ MYC-CZU3EG CPU Module



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