



Differential LVPECL VCXO

CVPD-940 Model

9×14 mm SMD, 3.3V, LVPECL

Frequency Range:

50 MHz to 212.500 MHz

Temperature Range:

0°C to 70°C

(Option X)

-40°C to 85°C

Storage:

-45°C to 90°C

Input Voltage:

3.3V ±0.3V

Control Voltage:

1.65V ±1.65V

Settability At Nominal:

1.65V ±0.25V

Input Current:

88mA Max

Output:

Differential LVPECL

Symmetry:

49/51% Typical, 45/55% Max @ zero crossing point

Rise/Fall Time:

550ps Max (20% to 80%)

Pullability APR:

±50ppm Min

Linearity:

±10% Max

Load: Terminated to Vdd-2V into 50 ohms

Logic "1" Level:

Vcc-0.96V Min, Vcc-0.81V Max

Logic "0" Level:

Vcc-1.85V Min, Vcc-1.65V Max

Disable Time:

100ns Max

Start-up time:

2ms Typical, 10ms Max

Modulation BW:

>10kHz @ -3dB

Sub-harmonics:

none

Period Jitter: (20,000 periods)

<5ps RMS (1-sigma) Max

Phase Jitter: 12kHz~20MHz

<1ps RMS (1-sigma) Max,

50kHz~80MHz

<1ps RMS (1-sigma) Max,

Phase Noise Max:

100Hz

-80 dBc/Hz

1kHz

-108 dBc/Hz

10kHz

-132 dBc/Hz

100kHz

-140 dBc/Hz

Aging:

<3ppm 1st year, <2ppm every year thereafter



Applications:

10 Gigabit Ethernet

OC48: Forward Error Correction

Broadband Networks

SONET/SDH/DWD

ATM

Network/switch

Telecom

Designed using FR5 PCB & HFF crystal technology to provide a Low Noise, Low Jitter Voltage Controlled Crystal Oscillator solution at a competitive price.



Specifications subject to change without notice.

Rev: K

Date: 15-Sep-2017

Page 1 of 2





Differential LVPECL VCXO



CVPD-940 Model 9×14 mm SMD, 3.3V, LVPECL

Crystek Part Number Guide

CVPD - 940 - X - 155.520

#1 #2 #3 #4

- #1 Crystek SMD PECL VCXO
- #2 Model 940 = 9×14 High Frequency 3.3V
- #3 Temp. Range: Blank = 0/70°C, X = -40/85°C
- #4 Frequency in MHz: 3 or 6 decimal places

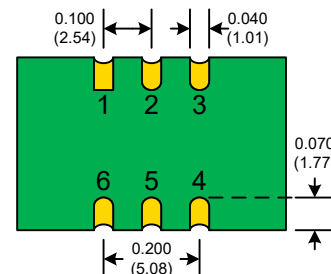
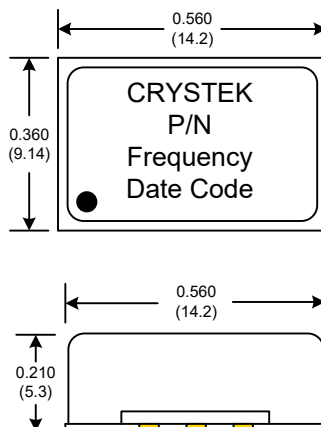
Example:
CVPD-940X-155.520 = 3.3V, -40/85°C, 155.520 MHz

Standard Frequencies MHz

74.175800	161.132800
74.250	166.628600
77.760	167.331700
155.520	212.500
156.250	

RECOMMENDED REFLOW SOLDERING PROFILE 900034 (See App Note listed on website)

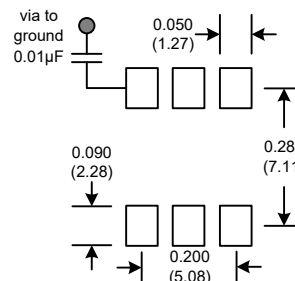
<http://www.crystek.com/specification/reflow/900034.pdf>



PAD FINISH: Immersion Gold (ENIG); 5 micro inches maximum

PIN	Function
1	Vcont
2	E/D
3	GND
4	OUT
5	COUT
6	Vdd

SUGGESTED PAD LAYOUT



Enable/Disable Function	
Pin 2	Output pin
Open	Active
"0" level Vcc-1.620V Max	Active
"1" level Vcc-1.025V Min	Disabled
Disabled State:	
Pin 4 will assume a fixed level of logic "0"	
Pin 5 will assume a fixed level of logic "1"	

Mechanical:

Shock:
Solderability:
Vibration:
Solvent Resistance:
Resistance to Soldering Heat:

MIL-STD-883, Method 2002, Condition B
MIL-STD-883, Method 2003
MIL-STD-883, Method 2007, Condition A
MIL-STD-202, Method 215
MIL-STD-202, Method 210, Condition I or J

Environmental:

Thermal Shock:
Moisture Resistance:

MIL-STD-883, Method 1011, Condition A
MIL-STD-883, Method 1004

Packaging:

Tape/Reel:

100ea, 250ea, 500ea 24mm Tape

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Page 2 of 2



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