BLF981; BLF981S

Power LDMOS transistor

Rev. 1 — 10 January 2025

AMPLEON

Product data sheet

1. Product profile

1.1 General description

A 170 W LDMOS transistor for broadcast, ISM, avionics and non-cellular communications applications. The excellent ruggedness of this device makes it ideal for digital and analog transmitter applications in the frequency range from HF to 1400 MHz.

Table 1. Application information

Test signal	f	V_{DS}	P_L	G_p	η_D
	(MHz)	(V)	(W)	(dB)	(%)
pulsed RF	700	50	170	24	71

1.2 Features and benefits

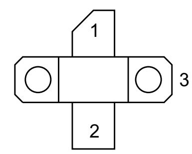
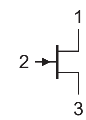
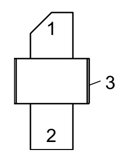
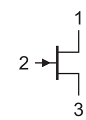
- Designed for broadband operation
- High efficiency
- Integrated dual sided ESD protection
- Excellent ruggedness
- High power gain
- Excellent reliability
- Easy power control
- Excellent stability
- For RoHS compliance see the product details on the Ampleon website

1.3 Applications

- Broadcast transmitter applications
- Industrial, scientific and medical applications
- Avionics applications up to 1400 MHz
- Non-cellular communications applications

2. Pinning information

Table 2. Pinning

Pin	Description		Simplified outline	Graphic symbol
BLF981 (SOT467C)				
1	drain			 amp01464
2	gate			
3	source	[1]		
BLF981S (SOT467B)				
1	drain			 amp01464
2	gate			
3	source	[1]		

[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Package name	Orderable part number	12NC	Packing description	Min. orderable quantity (pieces)
SOT467C	BLF981U	934961037112	Tray; 20-fold; non-dry pack	60
SOT467B	BLF981SU	934961038112	Tray; 20-fold; non-dry pack	60

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	108	V
V_{GS}	gate-source voltage		–6	+11	V
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature	[1]	-	225	°C

[1] Continuous use at maximum temperature will affect the reliability, for details refer to the online MTF calculator.

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-c)}$	thermal resistance from junction to case	T_{case} = 60 °C; V_{DS} = 50 V; P_L = 170 W	0.61	K/W

6. Characteristics

Table 6. DC characteristics

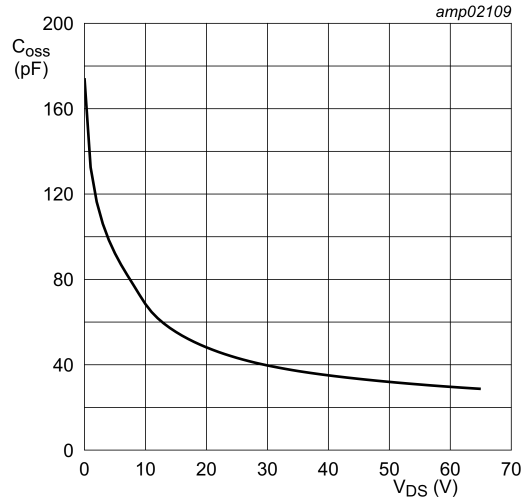
T_j = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 V; I_D = 1.11 mA	108	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 10 V; I_D = 111 mA	1.5	2.0	2.5	V
V_{GSq}	gate-source quiescent voltage	V_{DS} = 50 V; I_D = 25 mA	1.5	1.9	2.5	V
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 50 V	-	-	1.4	μA
I_{DSX}	drain cut-off current	V_{GS} = $V_{GS(th)}$ + 3.75 V; V_{DS} = 10 V	-	20	-	A
I_{GSS}	gate leakage current	V_{GS} = 11 V; V_{DS} = 0 V	-	-	140	nA
$R_{DS(on)}$	drain-source on-state resistance	V_{GS} = $V_{GS(th)}$ + 3.75 V; I_D = 3.885 A	-	0.19	-	Ω

Table 7. AC characteristics

T_j = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_{rs}	feedback capacitance	V_{GS} = 0 V; V_{DS} = 50 V; f = 1 MHz	-	0.43	-	pF
C_{iss}	input capacitance	V_{GS} = 0 V; V_{DS} = 50 V; f = 1 MHz	-	111	-	pF
C_{oss}	output capacitance	V_{GS} = 0 V; V_{DS} = 50 V; f = 1 MHz	-	31.9	-	pF



V_{GS} = 0 V; f = 1 MHz

Fig 1. Output capacitance as a function of drain-source voltage; typical values per section

Table 8. RF characteristics

Test signal: pulsed RF: t_p = 100 μs; δ = 10 %; f = 700 MHZ; RF performance at V_{DS} = 50 V; I_{Dq} = 25 mA; T_{case} = 25 °C; unless otherwise specified; in a class-AB production test circuit.

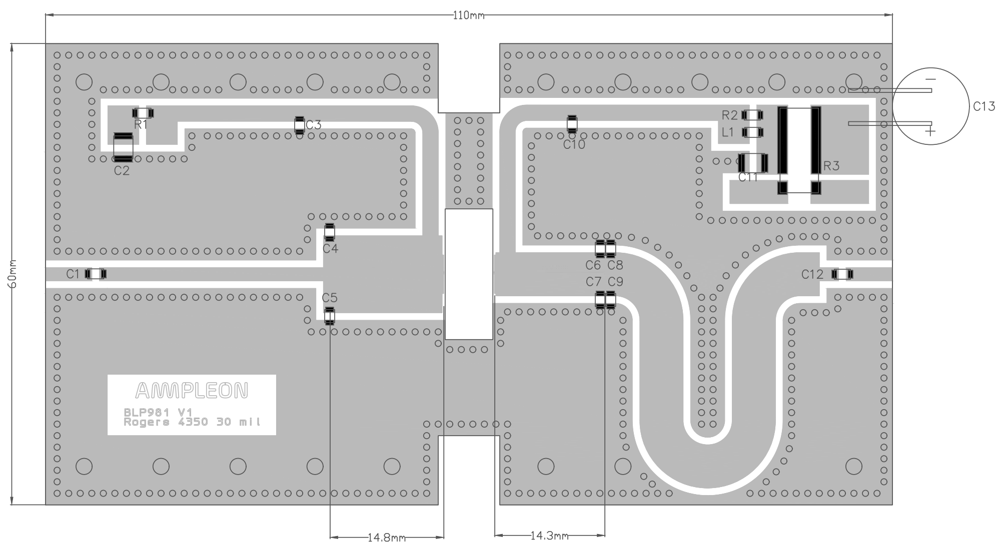
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
G_p	power gain	P_L = 170 W	22.5	24	-	dB
RL_{in}	input return loss	P_L = 170 W	-	-13	-8	dB
η_D	drain efficiency	P_L = 170 W	67	71	-	%

7. Test information

7.1 Ruggedness in class-AB operation

The BLF981 and BLF981S are capable of withstanding a load mismatch corresponding to VSWR = 40 : 1 through all phases under the following conditions: V_{DS} = 50 V; I_{Dq} = 50 mA; P_L = 170 W; f = 700 MHz; pulsed CW (t_p = 100 μs; δ = 10 %).

7.2 Test circuit



Printed-Circuit Board (PCB): Rogers RO4350B; thickness = 0.762 mm. See Table 9 for a list of components.

Fig 2. Component layout for class-AB production test circuit

Table 9. List of components
For test circuit see Figure 2

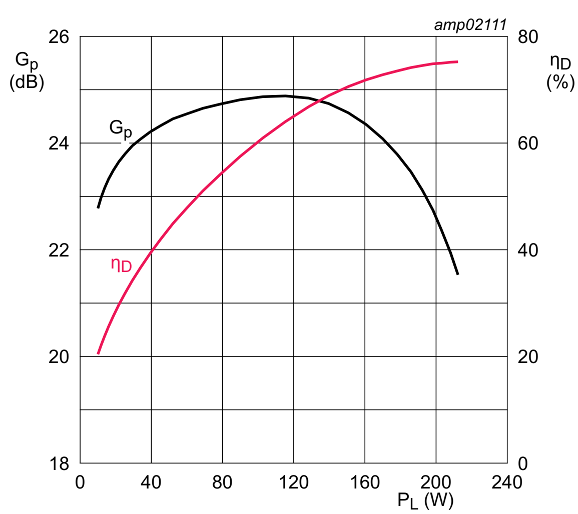
Component	Description	Value	Remarks
C1	multilayer ceramic chip capacitor	10 pF	[1] [2]
C3, C12	multilayer ceramic chip capacitor	30 pF	[1] [2]
C4, C5	multilayer ceramic chip capacitor	22 pF	[1] [2]
C6, C7	multilayer ceramic chip capacitor	6.8 pF	[1] [2]
C8, C9	multilayer ceramic chip capacitor	10 pF	[1] [2]
C10	multilayer ceramic chip capacitor	47 pF	[1] [2]
C2, C11	multilayer ceramic chip capacitor	4.7 μF	100 V
C13	electrolytic capacitor	470 μF	64 V
R1	chip resistor	9.1 Ω	SMD 1206
R2	chip resistor	4.7 Ω	SMD 1206
R3	shunt resistor	10 mΩ	
L1	inductor	9 nH	Coilcraft 1508-9N0GLB

[1] American Technical Ceramics type 800A or capacitor of same quality

[2] Vertical mounted

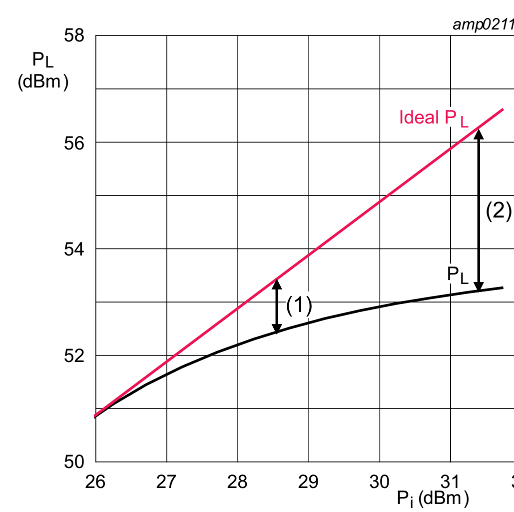
7.3 Graphical data

7.3.1 Pulsed CW performance measured in production RF test circuit



V_{DS} = 50 V; I_{Dq} = 25 mA; f = 700 MHz; t_p = 100 μs; δ = 10 %

Fig 3. Power gain and drain efficiency as a function of output power; typical values

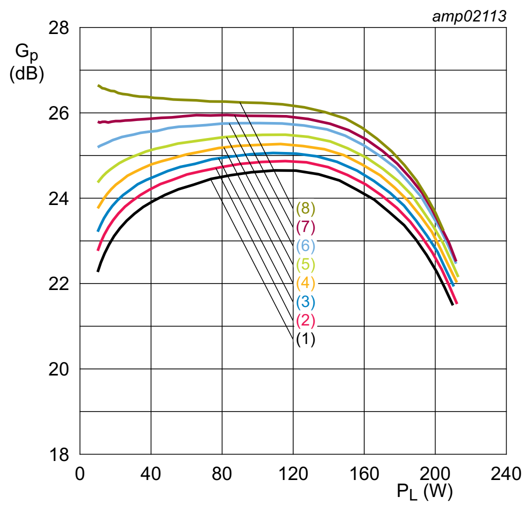


V_{DS} = 50 V; I_{Dq} = 25 mA; f = 700 MHz; t_p = 100 μs; δ = 10 %

(1) $P_{L(1\ dB)}$ = 52.4 dBm (176 W)

(2) $P_{L(3\ dB)}$ = 53.2 dBm (209 W)

Fig 4. Output power as a function of input power; typical values



V_{DS} = 50 V; f = 700 MHz; t_p = 100 μs; δ = 10 %

(1) I_{Dq} = 10 mA

(2) I_{Dq} = 25 mA

(3) I_{Dq} = 50 mA

(4) I_{Dq} = 100 mA

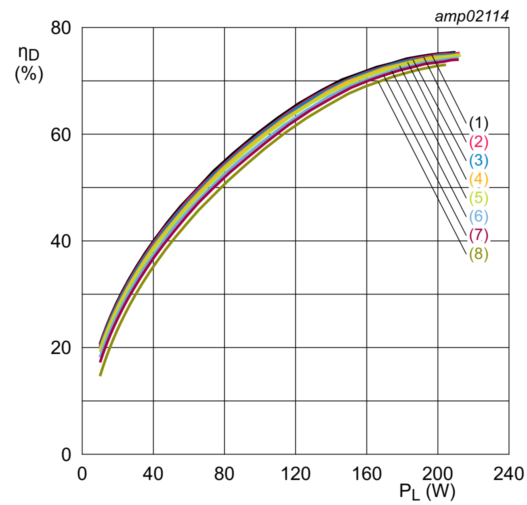
(5) I_{Dq} = 200 mA

(6) I_{Dq} = 400 mA

(7) I_{Dq} = 600 mA

(8) I_{Dq} = 1000 mA

Fig 5. Power gain as a function of output power; typical values



V_{DS} = 50 V; f = 700 MHz; t_p = 100 μs; δ = 10 %

(1) I_{Dq} = 10 mA

(2) I_{Dq} = 25 mA

(3) I_{Dq} = 50 mA

(4) I_{Dq} = 100 mA

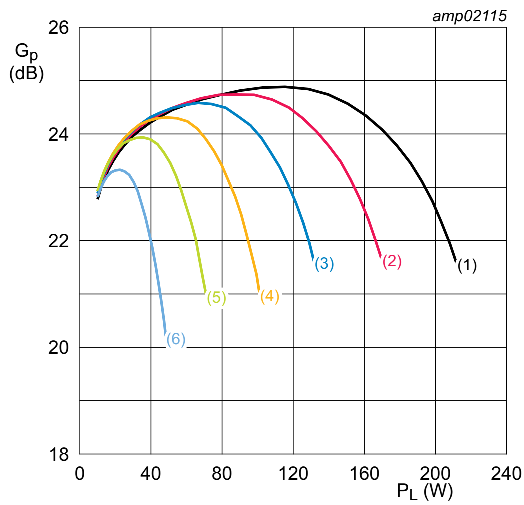
(5) I_{Dq} = 200 mA

(6) I_{Dq} = 400 mA

(7) I_{Dq} = 600 mA

(8) I_{Dq} = 1000 mA

Fig 6. Drain efficiency as a function of output power; typical values



I_{Dq} = 25 mA; f = 700 MHz; t_p = 100 μs; δ = 10 %

(1) V_{DS} = 50 V

(2) V_{DS} = 45 V

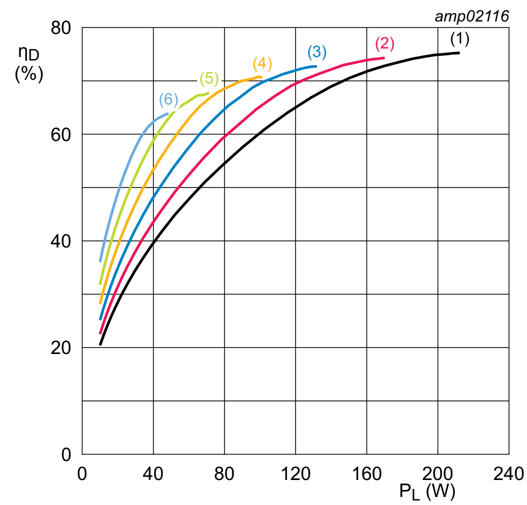
(3) V_{DS} = 40 V

(4) V_{DS} = 35 V

(5) V_{DS} = 30 V

(6) V_{DS} = 25 V

Fig 7. Power gain as a function of output power; typical values



I_{Dq} = 25 mA; f = 700 MHz; t_p = 100 μs; δ = 10 %

(1) V_{DS} = 50 V

(2) V_{DS} = 45 V

(3) V_{DS} = 40 V

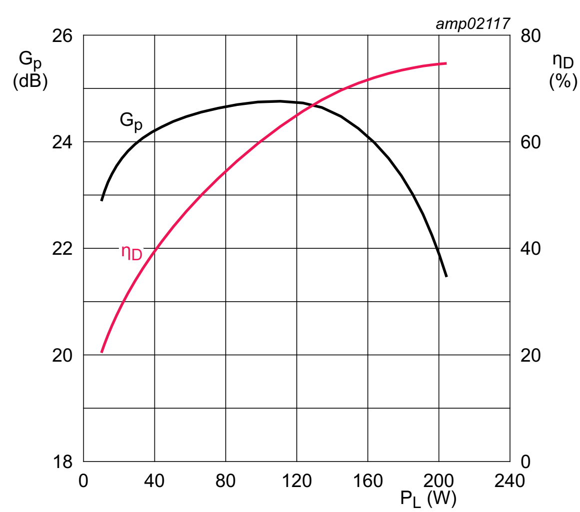
(4) V_{DS} = 35 V

(5) V_{DS} = 30 V

(6) V_{DS} = 25 V

Fig 8. Drain efficiency as a function of output power; typical values

7.3.2 CW performance measured in production RF test circuit

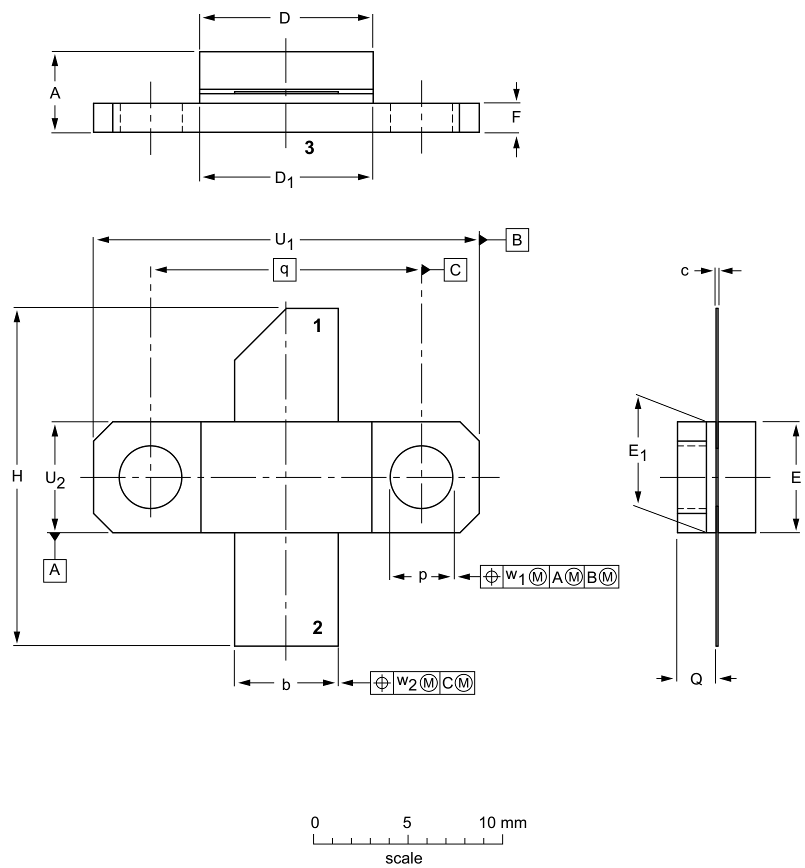


V_{DS} = 50 V; I_{Dq} = 25 mA; f = 700 MHz

Fig 9. Power gain and drain efficiency as a function of output power; typical values

8. Package outline

Flanged ceramic package; 2 mounting holes; 2 leads **SOT467C**



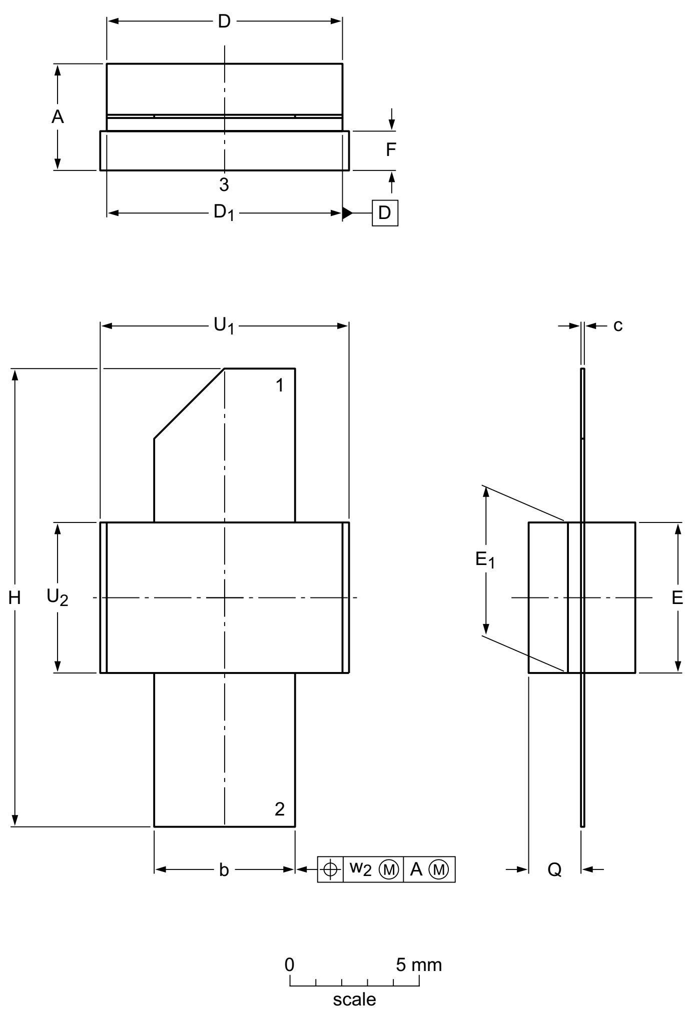
DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D_1	E	E_1	F	H	p	Q	q	U_1	U_2	w_1	w_2
mm	4.67 3.94	5.59 5.33	0.15 0.10	9.25 9.04	9.27 9.02	5.92 5.77	5.97 5.72	1.65 1.40	18.54 17.02	3.43 3.18	2.21 1.96	14.27	20.45 20.19	5.97 5.72	0.25	0.51
inch	0.184 0.155	0.220 0.210	0.006 0.004	0.364 0.356	0.365 0.355	0.233 0.227	0.235 0.225	0.065 0.055	0.73 0.67	0.135 0.125	0.087 0.077	0.562	0.805 0.795	0.235 0.225	0.010	0.020

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT467C						~~99-12-28~~ 12-05-02

Fig 10. Package outline SOT467C

Earless ceramic package; 2 leads **SOT467B**



Dimensions

Unit(1)		A	b	c	D	D_1	E	E_1	F	H	Q	U_1	U_2	w_2
mm	max	4.67	5.59	0.15	9.25	9.27	5.92	5.97	1.65	18.29	2.21	9.78	5.97	
	nom													0.25
	min	3.94	5.33	0.10	9.04	9.02	5.77	5.72	1.40	17.27	1.96	9.53	5.72	
inches	max	0.184	0.22	0.006	0.364	0.365	0.233	0.235	0.065	0.72	0.087	0.385	0.235	
	nom													0.01
	min	0.155	0.21	0.004	0.356	0.355	0.227	0.225	0.055	0.68	0.077	0.375	0.225	

Note
1. millimeter dimensions are derived from the original inch dimensions.

sot467b_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT467B						~~11-08-18~~ 12-05-01

Fig 11. Package outline SOT467B

9. Handling information

CAUTION

This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

Table 10. ESD sensitivity

ESD model	Class
Charged Device Model (CDM); According to ANSI/ESDA/JEDEC standard JS-002	C2A
Human Body Model (HBM); According to ANSI/ESDA/JEDEC standard JS-001	2

10. Abbreviations

Table 11. Abbreviations

Acronym	Description
CW	Continuous Wave
DVB-T	Digital Video Broadcast - Terrestrial
ESD	ElectroStatic Discharge
HF	High Frequency
ISM	Industrial, Scientific, Medical
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
MTF	Median Time to Failure
RoHS	Restriction of Hazardous Substances
VSWR	Voltage Standing Wave Ratio

11. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLF981_BLF981S v1	20250110	Product data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.ampleon.com.

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14. Contents

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