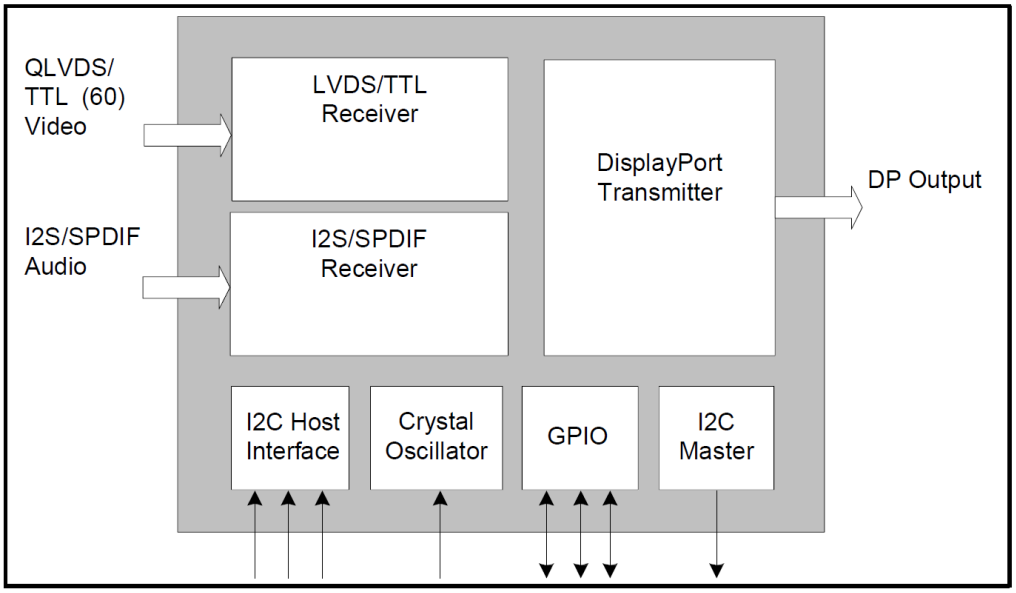
STDP4028
DisplayPort Transmitter

Features

- Enhanced DisplayPort™ (DP) transmitter
  - DP 1.1a compliant
  - Embedded DisplayPort (eDP) compliant
  - 1, 2, or 4 lanes
- Higher bandwidth “Turbo mode” (3.24 Gbps) per lane, supports:
  - 1920 x 1080 (FHD) 120 Hz/10-bit color video standard timings and 7.1 Ch audio
  - 2560 x 1600 (WQXGA), 2560 x 2048 (QSXGA) 60 Hz/10-bit color graphics and 7.1 Ch audio
- Interface compatibility with wide range of display controller ICs
  - LVTTL (60 wide) and LVDS (quad bus) video interface
  - 8-Ch I2S and SPDIF audio interface
- Robust AUX channel
  - Link service, maintenance
  - I2C-over-AUX (MCCS, DDC)
  - IR, full duplex UART protocol
- Configurable through I2C host interface
- Supports HDCP 1.3 with on-chip keys
- HDCP repeater capability
  - Acts as downstream transmitter
- Spread spectrum on DisplayPort, LVDS, and TTL interfaces for EMI reduction
- Supports deep color and color format conversion
  - RGB/YUV (4:4:4) – 10-bit color
  - YUV (4:2:2/4:2:0) – 12-bit color
  - RGB (4:4:4) to YUV (4:4:4) conversion and vice-versa
- Low power operation; 18 mW standby
- I2C to AUX bridge for EDID, MCCS pass through
- Supports HBR/“Turbo” speed over HBR/RBR-rated long cables (15 m and more)
- Package
  - 164 LFBGA (12 x 12 mm / 0.8 mm)
    - Power supply voltages
      - 3.3 V I/O; 1.2 V core

Applications

- Digital TV, docking station, STB, game console, etc.



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1. Description

The STDP4028 is a DisplayPort transmitter IC for the secure transmission of high-bandwidth, uncompressed digital audio-video signals targeted for applications such as DTV, LCD monitor, docking station, STB and other types of consumer audio-video systems. STDP4028 is VESA DP 1.1a and eDP compliant device, implementing a single link DisplayPort output port comprising four main lanes, auxiliary channel, and HPD. In addition to the standard HBR (2.7 Gbps) and RBR (1.62 Gbps) speeds, this device supports “turbo” speed of 3.24 Gbps per lane with a total link bandwidth of 12.96 Gbps. The higher bandwidth provides unique benefits to users over other commercial DP transmitters for embedded applications by offering additional margin to support higher color depth, resolution, and refresh rate. For example, STDP4028 supports FHD non-reduced blanking video (1080p 30-bit color per pixel) at 120 Hz, plus 7.1 Ch audio in two-box TV applications. The high-speed auxiliary channel in STDP4028 acts as a bidirectional communication link, supporting application-specific protocols such as MCCS, DDC, UART, IR, as well as, the dedicated DisplayPort link training and device management functions. The STDP4028 supports RGB and YUV video color formats with color depth of 12 (YUV 4:2:2 only), 10, and 8 bits.

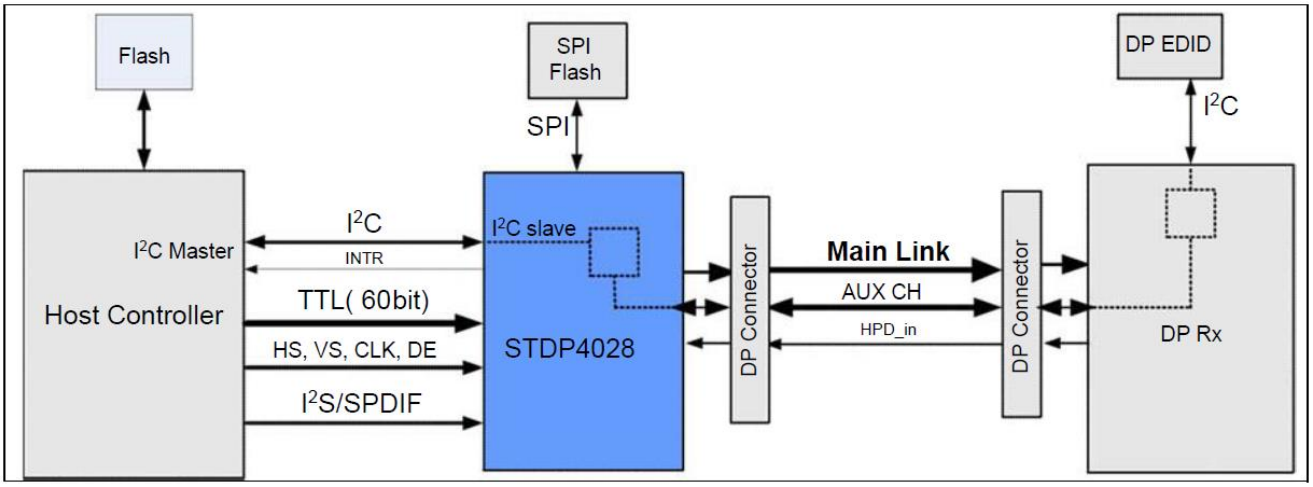
This device offers LVDS and LVTTL input interface configurable to map a wide range of display controller products. The Quad LVDS interface supports video signals up to 400 MHz pixel rate with flexible channel and lane swapping options. The 60-bit LVTTL input ports on STDP4028 can be mapped to transfer video data either in two pixels per clock or single pixel per clock of a chosen color depth. The STDP4028 also supports both compressed and uncompressed audio formats.

This device comprises four I2S audio inputs, supporting up to 8 channels LPCM audio and a single wire SPDIF input for encoded audio. The STDP4028 features HDCP 1.3 content protection scheme with an embedded key option for secure transmission of digital audio-video content. In addition, it supports the HDCP repeater function and, thus acts as a downstream transmitter suitable for two-box TV and HDMI/DVI to DP converter applications. The STDP4028 is configurable from an external host through the I2C host interface. This IC also includes general-purpose inputs/outputs for controlling system components. The STDP4028 features a color space converter (RGB to YUV and YUV to RGB) for flexible interface with external video processing devices.

2. Application overview

The STDP4028 is designed as DisplayPort transmitter device for transferring high bandwidth video and audio in PC and CE applications. Typical audio-video source system has a graphics or video processing device that acts as system master (host). The host controller configures STDP4028 through an I2C host interface. The host and STDP4028 also use interrupt mechanism whenever the slave needs attention. The STDP4028 requires an external SPI Flash to store firmware for supporting optimal performance. The audio and video signal from the host controller is converted into DisplayPort streams through STDP4028 and transfer to an external display system over standard DisplayPort cable. The I2C to AUX bypass channel handles the I2C traffic between STDP4028 and host controller as shown in the figure below.

Figure 1. System interface block diagram



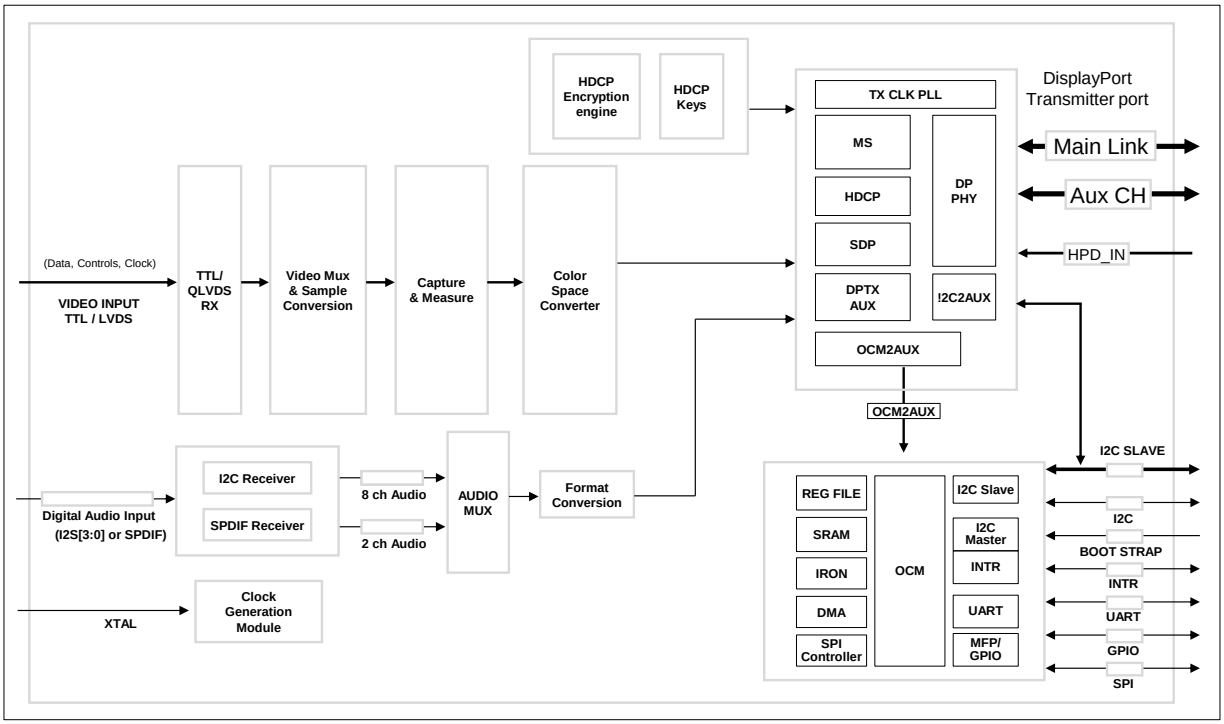
3. Feature attributes

- Video
  - Up to 2560 x 2048-60 Hz, 2560 x 1600-60 Hz, FHD 120 Hz at 10-bits per color
  - 8/10/12 bits per color option
  - RGB/YUV color format
- Audio
  - 8-Ch I2S; word length up to 64 x Fs; bit depth up to 24 bits, sample rate up to 192 kHz
  - SPDIF; 2-Ch LPCM, AC3, DTS, bit depth up to 24 bits, sample rate up to 192 kHz
- Input interface
  - Video: TTL 60/48 bits wide; QLVDS 8/10 bits per color
  - Audio: I2S 8-Ch, SPDIF x1
- Output interface
  - DP 1.1a (4 lanes, AUX, HPD); supported link speed 3.24 Gbps, 2.7 Gbps, 1.62 Gbps
- Spread spectrum
  - Supported on DP output and LVDS/TTL inputs
- AUX capabilities
  - UART, I2C-over-AUX (MCCS, DDC, etc.) IR
- HDCP
  - On-chip keys, HDCP repeater
- Color format conversion
  - RGB 4:4:4 to YUV 4:4:4 and vice-versa
- System configuration
  - I2C host interface for control by an external system microprocessor
- Package
  - 164 LFBGA (12 x 12 mm), 1 mm thickness, 0.8 pitch
- Power
  - Standby power 18 mW
- ESD
  - 2 kV HBM, 200 V MM, 750 V CDM

4. Functional block description

4.1 Block diagram

Figure 2. STDP4028 block diagram



4.2 Power sequence

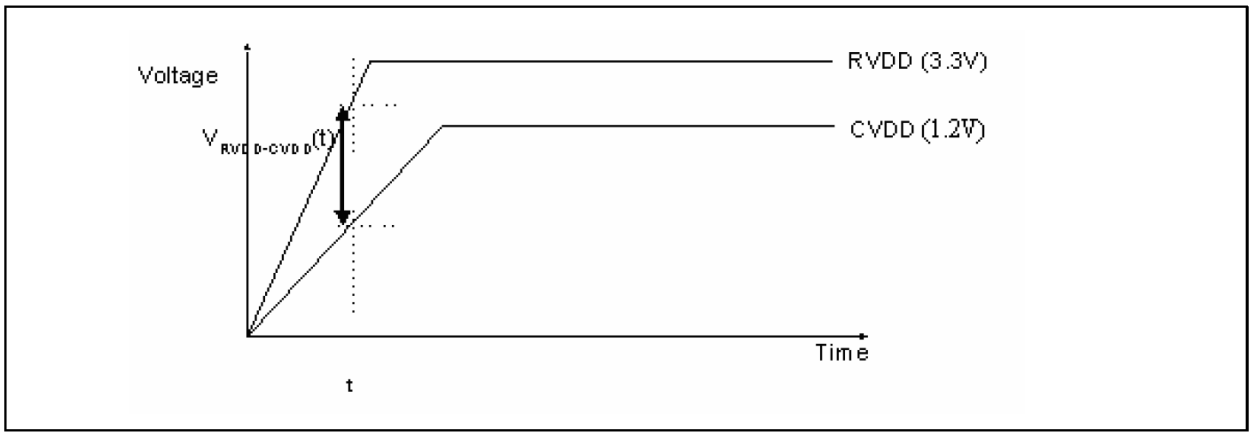
When using linear regulators for the 3.3 V and 1.2 V supplies, precautions must be taken in designing the power supply system to meet the following requirements.

At any time during the power-up sequence, the actual voltage of the 3.3 V ring VDD (RVDD) power supply should always be equal to or higher than the actual voltage of the 1.2 V core VDD (CVDD). In mathematical terms, VRVDD >= VCVDD at all times.

Table 1. Power sequencing requirements

Parameter	Min	Typ	Max
VRVDD-VCVDD (for all t>0)	0 V	1.50 V	

Figure 3. Correct power sequencing



4.3 Power-on reset

The STDP4028 device has an integrated reset pulse generator. The internal reset pulse generator performs hardware reset under the following conditions:

- During system power-up, after the RVDD_3V3 voltage has reached reset threshold voltage V_T
- In the event RVDD_3V3 voltage drops below threshold V_T for more than approximately 150 ns
- Manually holding the RESETn pin low for a minimum of 1 ms

The active-low reset pulse on the RESETn pin generated by the internal reset pulse generator is described in the table below. During the reset period, all internal circuits and logic are reset to the default power-on state. To ensure proper chip operation, TCLK (generated by crystal oscillator or from the external clock source) must be applied during and after the reset.

The following figure shows the relationship between RVDD_3V3 and RESETn during system power-up.

Figure 4. Power-up reset sequence between RVDD_3.3V and RESETn pin

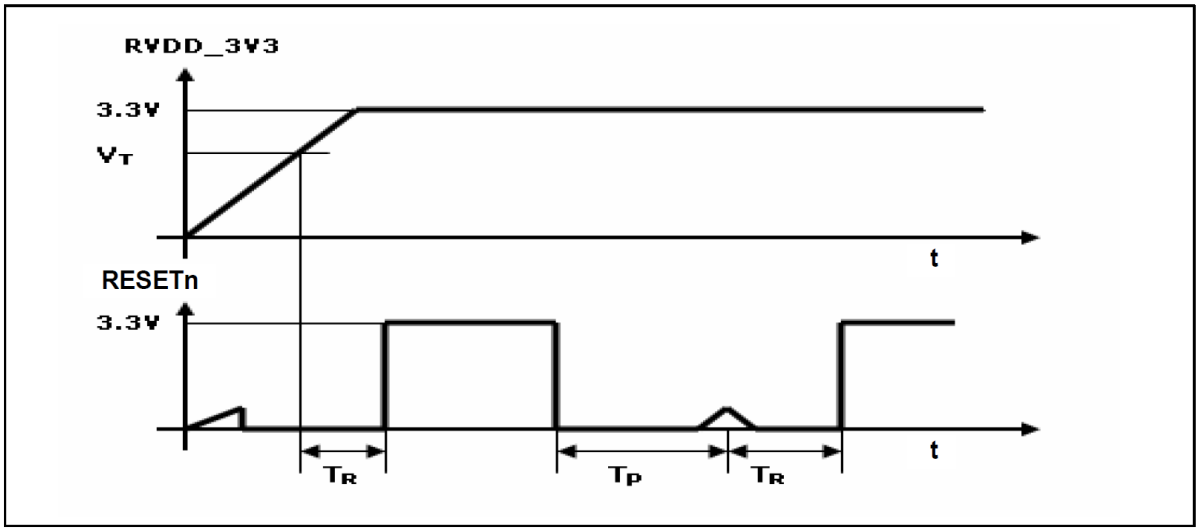


Table 2. Power-on reset characteristics

Description	Symbol	Min	Typ	Max
Power-on reset threshold voltage	V_T	2.60 V	2.70 V	2.80 V
Reset pulse duration	T_R	80 ms	150 ms	200 ms
Push-button hold time	T_P	1 ms	-	-

The glitch filter inside the internal reset pulse generator ignores the RVDD_3V3 power line glitch if the duration of the glitch is shorter than approximately 150 ns. However, if RVDD_3V3 voltage drops below the threshold V_T for more than 150 ns in duration, reset will be asserted and RESETn signal will go low. The following figure illustrates the RVDD_3V3 glitch.

Figure 5. RVDD_3V3 glitch

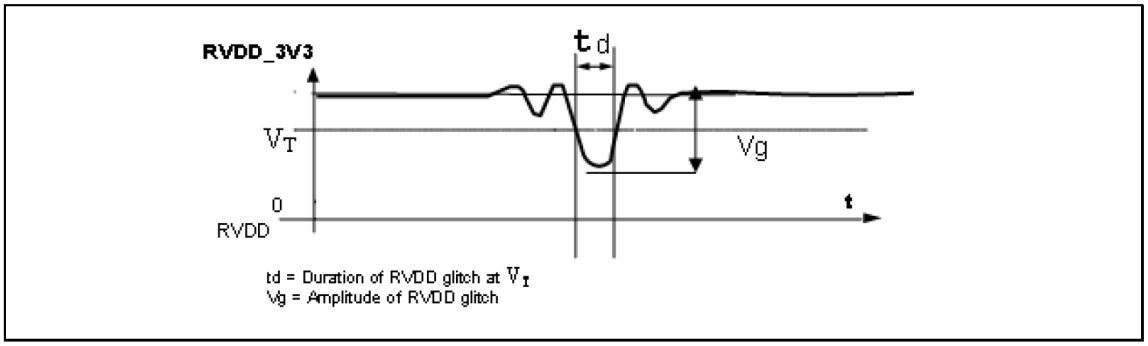


Table 3. RVDD_3.3V glitch-induced reset specifications

Description	Symbol	Min	Typ	Max
RVDD_3V3 glitch duration	td	150 ns		
RVDD_3V3 glitch amplitude	Vg	0.9 V(1)		1.2 V(1)

1. The RESETn pin must connect to RVDD with a pull-up resistor of 2.7 K.

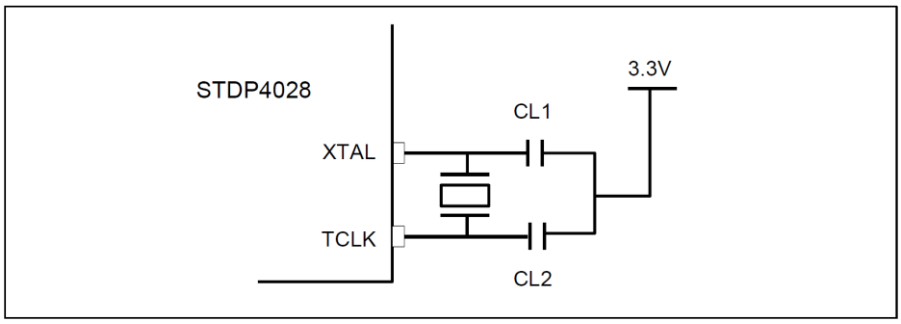
The RVDD_3V3 voltage must fall by more than Vg below the supply voltage (3.3 V nominal) for the reset to assert (RESETn becomes low). For example, RVDD_3V3 voltage level must fall below at least 2.4 V (3.3 V - 0.9 V) in order for reset to assert.

4.4 Clock generation

TCLK is the main timing clock of the STDP4028. All other internal clocks are generated from the TCLK. The STDP4028 TCLK oscillator circuitry is a custom designed circuit to support the use of an external oscillator (27 MHz) or a crystal resonator (27 MHz). This generates a reference frequency source for the STDP4028 device, as shown in the figure below.

The recommended operation uses an external crystal, which in turn, uses an internal oscillator circuit to generate the main chip clock. The internal oscillator provides a low jitter and low harmonic clock to the analog and digital circuitry of the STDP4028. The internal oscillator circuit also minimizes the overdrive of the crystal, which reduces the aging of the crystal. An Automatic Gain Control (AGC) circuit insures proper startup and operation over a wide range of conditions.

Figure 6. STDP4028 clock generation using a crystal resonator



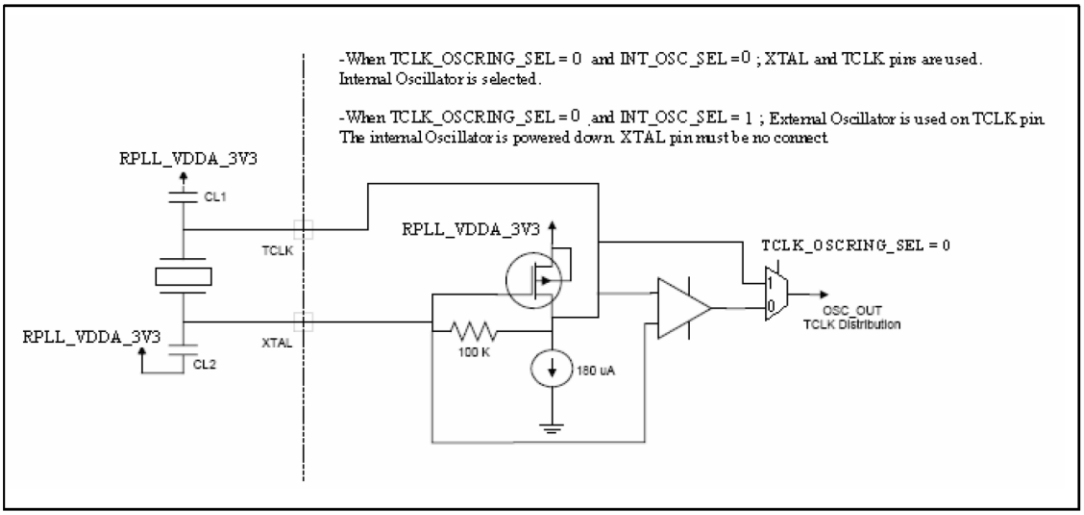
The STDP4028 internal oscillator operation:

The bootstrap pin Boot[0] (XTAL_TCLK_SEL) during chip reset determines the clock source selection. If the bootstrap pin is pulled HIGH (by connecting the pin to Vdd through a pull-up resistor), the internal oscillator is enabled. The maximum value of the pull-down resistor is 15 K (typical value 4.7 K) Ohm. In

this mode, a crystal resonator is connected between the XTAL pin and the TCLK pin with the appropriately sized loading capacitors CL1 and CL2.

Note: *The size of CL1 and CL2 are determined from the crystal manufacturer's specification and by compensating for the parasitic capacitance of the STDP4028 device and the printed circuit board traces. Terminate the loading capacitors to the RPLL_VDDA_3V3 power supply to increase the "power supply rejection ratio" against terminating to the ground plane.*

Figure 7. Using the internal oscillator with an external crystal



The internal oscillator circuit is a Pierce Oscillator circuit and a simplified schematic is shown in the figure above. The output of the oscillator circuit, measured at the TCLK pin, is an approximate sine wave with a bias of about 2 volts above ground (see figure below). The peak-to-peak voltage of the output can range from 250 mV to 1000 mV, depending on the specific characteristics of the crystal and variation in the oscillator characteristics. The output of the oscillator feeds to a comparator that converts the sine wave to a square wave. The comparator requires a minimum signal level of about 50-mV peak to peak to function correctly. The buffered output signal of the comparator distributes to the rest of STDP4028 circuits.

Figure 8. Internal oscillator output

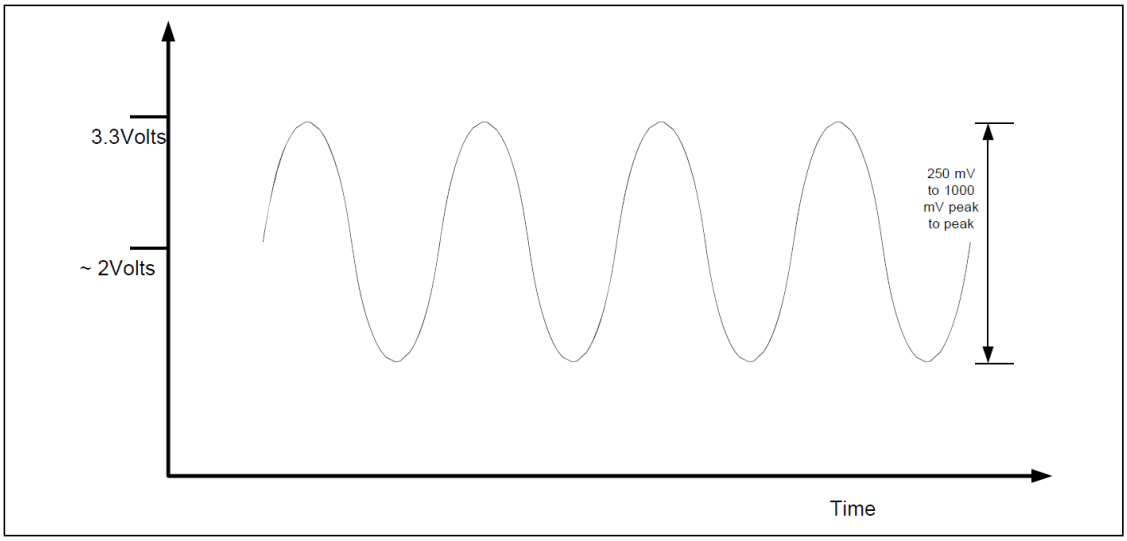
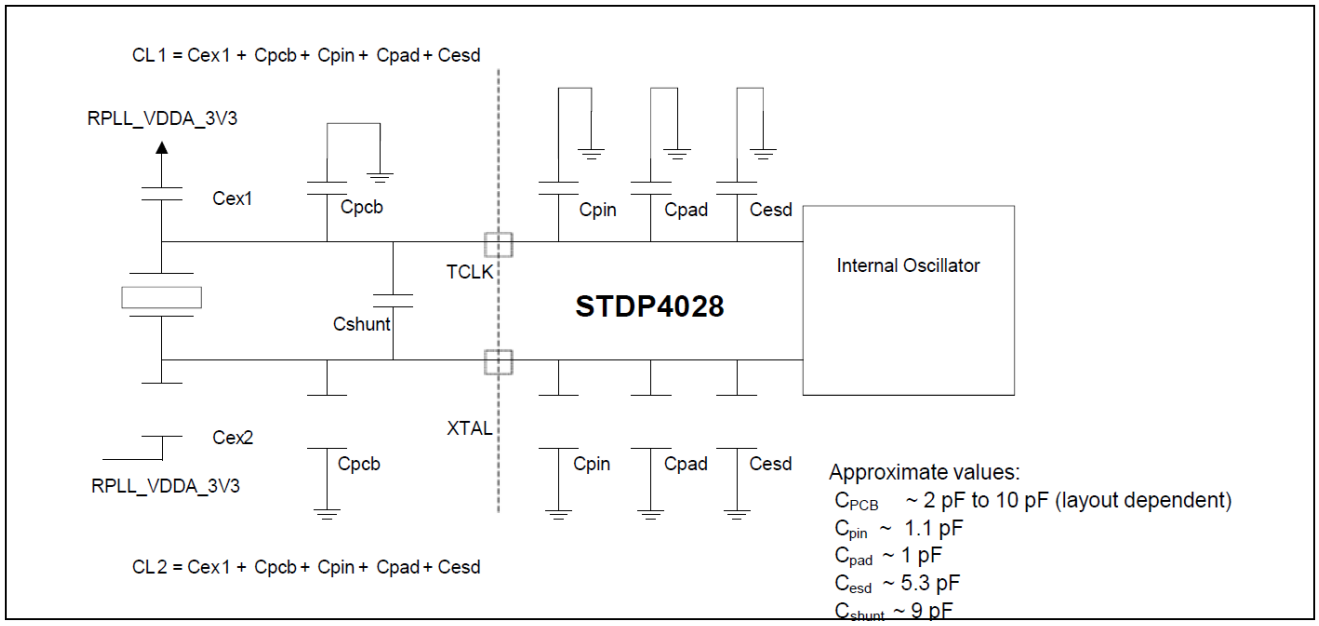


Figure 9. Parasitic capacitance sources



One of the design parameters that must be given some consideration is the value of the loading capacitors used with the crystal. Referring to the figure above, the load capacitance (Cload) on the crystal is the combination of CL1 and CL2 and is calculated by: Cload = ((CL1 * CL2) / (CL1 + CL2)) + Cshunt. The shunt capacitance Cshunt is the effective capacitance between the XTAL and TCLK pins. For the STDP4028, it is approximately 9 pF. CL1 and CL2 are a parallel combination of the external loading capacitors (Cex), the PCB board trace capacitance (CPCB), the pin capacitance (Cpin), the pad capacitance (Cpad), and the ESD protection capacitance (CESD). The capacitances are symmetrical so

that CL1 = CL2 = Cex + CPCB + Cpin + Cpad + CESD. The correct value of Cex must be calculated given the value of the parasitics.

CPCB ~ Layout dependent. Approximately 2 pF to 10 pF Cpin

~ 1.1 pF

Cpad ~ 1 pF CESD

~ 5.3 pF

Cshunt ~ 9 pF

Some attention must be given to the details of the oscillator circuit when used with a crystal resonator. The PCB traces should be as short as possible. The value of Cload that is specified by the manufacturer should not be exceeded to avoid potential start-up problems with the oscillator. Additionally, the crystal should be a fundamental mode AT-cut and the value of the equivalent series resistance must be less then 80 Ohms.

4.4.1 General recommendations for crystal specifications

While the selection of a crystal mainly depends on the specific PCB layout and the crystal manufacturer's specifications, the following are general recommendations.

Table 4. Recommended crystal specifications

Parameters	Specifications
Frequency	27.000 MHz
Operation mode	Fundamental
Operating temperature	-10 ^{0}C to +70 ^{0}C
Frequency tolerance @25 ^{0}C	+/- 50 ppm Max
Frequency stability over temperature	+/- 100 ppm Max
Load capacitance CL Shunt capacitance C0	8 pF to 18 pF 0.5 pF to 7 pF
Equivalent series resistance	< 80 Ohms
Crystal cut	AT-cut

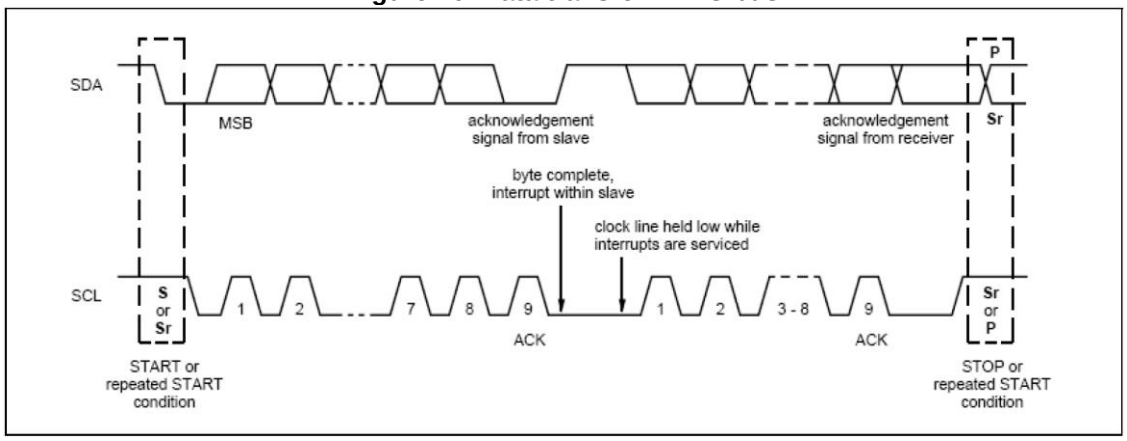
4.5 I2C interface

The STDP4028 has two I2C interface ports for inter-device communication: one I2C master port and a slave port (also referred to as host interface). The communication protocol is compatible with standard I2C protocol. Every byte on the SDA line is 8-bits long and the number of bytes in each transfer is unrestricted. Data is transferred with MSB first. If a slave cannot make or take a complete transfer until it has performed some other function, such as servicing an internal interrupt, it can hold the clock line SCL

LOW (stretch) to force the master into wait state. Data transfer can resume when the slave is ready for another byte of data and releases the clock line SCL.

A brief description of the I2C line activity is shown in the waveform below.

Figure 10. Data transfer in I2C bus



4.5.1 I2C slave interface (host interface)

The I2C slave port is intended for host communication purposes. In a typical monitor or TV application, the host controller communicates with STDP4028 through this interface. The STDP4028 contains a set of host interface registers that are directly read and written by the host controller. Whenever the host controller intends to configure or change the behavior of STDP4028, it writes into the corresponding host register. The STDP4028 responds to the host instruction by executing the intended function and updating the status flag or result register. The host then reads the status or result registers. The host controller must provide the clocks on SCL for both read and write transactions. The port pins used for host interface are AUX_I2C_SCL and AUX_I2C_SDA. When the chip power is turned off, AUX_I2C_SCL and AUX_I2C_SDA lines are tri-stated allowing other I2C devices to continue communication over common I2C bus. Refer to the bootstrap section for I2C slave address selection.

The host controller can receive the EDID information over the I2C slave interface of STDP4028. The STDP4028 in turn receives this EDID information from the connected sink via the DisplayPort AUX channel.

Read sequence

(SLAVE ADDRESS+R), ACK, DATA, (ACK), DATA, (ACK), DATA,…… (#ACK), (Stop)
Command in bracket is set by I2C master.

Write sequence

(SLAVE ADDRESS+#W), ACK, (DATA), ACK, (DATA), …. #ACK/ACK, (Stop)
Command in bracket is set by I2C master. Here

#ACK means no-acknowledge.

The following types of bus transactions are supported in STDP4028.

Note: S - start condition, P - stop condition

Device addressing

S	DevID with R/W	Address

Word write

STDP4028 sends an ACK after every byte.

S	DevID with R/W = 0	Address	Data (H)	Data (L)	P

Page write

The STDP4028 sends an ACK after every byte. The address is auto-incremented for every word received from the host. If the address reaches 0xFF in the middle of the transaction, it rolls over to 0x00. Up to 256 words can be written in one transaction.

S	DevID with R/W = 0	Address	Data0 (H)	Data0 (L)	Data1 (H)	Data1 (L)	…	DataN-1 (H)	DataN-1 (L)	P

Word read

Host controller writes the register address in the first transaction. The STDP4028 sends an ACK after every byte received.

S	DevID with R/W = 0	Address	P

The data is sent out in the second transaction. Host controller provides the clocks and sends an ACK after every byte, except the last one. The stop condition marks the end of the transaction.

S	DevID with R/W = 1	Data (H)	Data (L)	P

Sequential read

Host controller writes the address of the first register to be read in the sequential read operation. The STDP4028 sends an ACK after every byte received.

S	DevID with R/W = 0	Address	P

The data is sent out in the second transaction. Host controller provides the clock and sends an ACK after every byte, except the last one. The address is auto-incremented after every word sent out on the bus. If the address reaches 0xFF in the middle of the transaction, it rolls over to 0x00. The stop condition marks the end of the transaction.

S	DevID with R/W = 1	Data0 (H)	Data0 (L)	Data1 (H)	Data1 (L)	…	DataN-1 (H)	DataN-1 (L)	P

Short read

This is similar to the sequential read, except the first write transaction with the address is omitted. The data is read from the current address in the address register. Host controller provides the clock and sends an ACK after every byte, except the last one. The address is auto-incremented after every word sent out on the bus. If the address reaches 0xFF in the middle of the transaction, it rolls over to 0x00. The stop condition marks the end of the transaction.

S	DevID with R/W = 1	Data0 (H)	Data0 (L)	Data1 (H)	Data1 (L)	…	DataN-1 (H)	DataN-1 (L)	P

4.5.2 I2C master interface

The I2C master port is intended for host communication purposes with other I2C slave devices. In standalone applications, the STDP4028 can act as a host and communicate with other I2C slave devices through this interface.

4.6 Digital video input port

The STDP4028 interfaces with an on-board video processing device through LVTTL digital video port. The LVTTL video input port comprises a total of 60 data pins and two sets of Hsync, Vsync, DE and clock pins. The digital video pins can be grouped into one port (with even and odd bus) or two separate ports. The input data can be in RGB or YUV color format at 12, 10, and 8 bits depth. The port can be configured

to receive data at two pixel per clock or single pixel per clock rate. The digital video input port has the following capabilities:

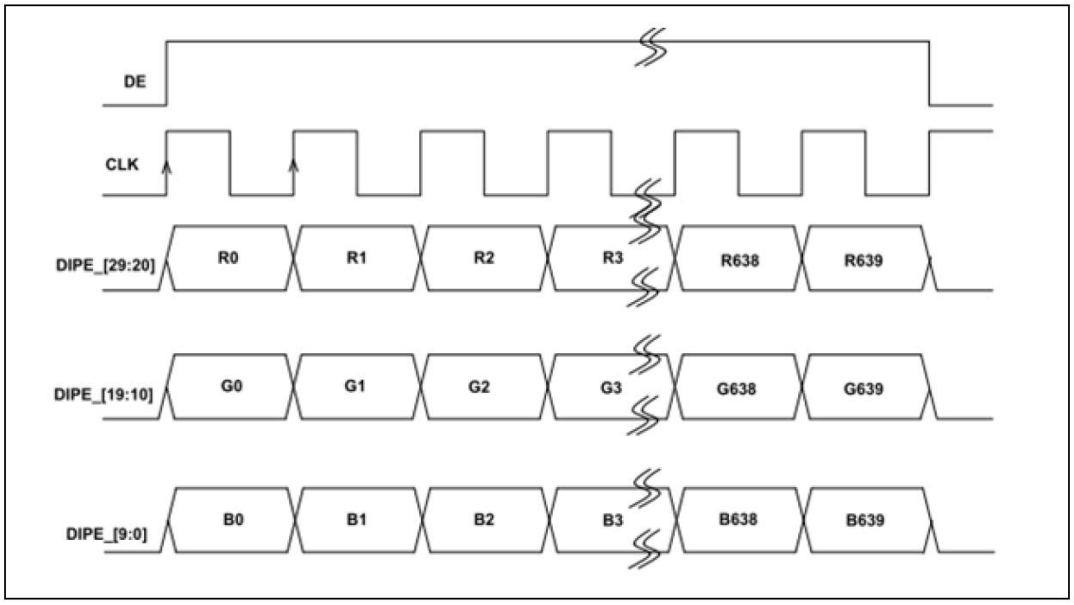
- Highest input clock on the pin is 165 MHz (max data rate up to 330 MHz in dual pixel per clock configuration)
- One input video stream, received as alternative even-odd pixels on a single bus of 30 bit wide or separate even-odd pixels on two ports (60 bit wide)
- RGB or YCbCr (YUV) input color format:
  - RGB 444/YUV 444 with 60 or 48 bits using display input Port E (Even) & port O (Odd) combined
  - RGB 444/YUV 444 with 30, 24 bits using either Port E or Port O
  - YUV 4:2:2 with 24, 20, or 16 bits using either Port E or Port O
- Clocking can be single bus or dual bus
- Supports RGB, SMPTE 170M, ITU-R BT.601-5, full and reduced range colorimetric
- The TTL video input signal mapping is fully configurable. The following table describes the default settings.

Table 5. Digital video input format RGB/YUV 4:4:4

DIPE	DIPO	4:4:4 RGB/YUV Formats	
		10 bit	8 bit
DIPE_29	DIPO_29	R/V/Cr[9]	R/V/Cr[7]
DIPE_28	DIPO_28	R/V/Cr[8]	R/V/Cr[6]
DIPE_27	DIPO_27	R/V/Cr[7]	R/V/Cr[5]
DIPE_26	DIPO_26	R/V/Cr[6]	R/V/Cr[4]
DIPE_25	DIPO_25	R/V/Cr[5]	R/V/Cr[3]
DIPE_24	DIPO_24	R/V/Cr[4]	R/V/Cr[2]
DIPE_23	DIPO_23	R/V/Cr[3]	R/V/Cr[1]
DIPE_22	DIPO_22	R/V/Cr[2]	R/V/Cr[0]
DIPE_21	DIPO_21	R/V/Cr[1]	0
DIPE_20	DIPO_20	R/V/Cr[0]	0
DIPE_19	DIPO_19	G/Y/Y[9]	G/Y/Y[7]
DIPE_18	DIPO_18	G/Y/Y[8]	G/Y/Y[6]
DIPE_17	DIPO_17	G/Y/Y[7]	G/Y/Y[5]
DIPE_16	DIPO_16	G/Y/Y[6]	G/Y/Y[4]
DIPE_15	DIPO_15	G/Y/Y[5]	G/Y/Y[3]
DIPE_14	DIPO_14	G/Y/Y[4]	G/Y/Y[2]
DIPE_13	DIPO_13	G/Y/Y[3]	G/Y/Y[1]
DIPE_12	DIPO_12	G/Y/Y[2]	G/Y/Y[0]
DIPE_11	DIPO_11	G/Y/Y[1]	0
DIPE_10	DIPO_10	G/Y/Y[0]	0
DIPE_9	DIPO_9	B/U/Cb[9]	B/U/Cb[7]
DIPE_8	DIPO_8	B/U/Cb[8]	B/U/Cb[6]
DIPE_7	DIPO_7	B/U/Cb[7]	B/U/Cb[5]
DIPE_6	DIPO_6	B/U/Cb[6]	B/U/Cb[4]
DIPE_5	DIPO_5	B/U/Cb[5]	B/U/Cb[3]
DIPE_4	DIPO_4	B/U/Cb[4]	B/U/Cb[2]
DIPE_3	DIPO_3	B/U/Cb[3]	B/U/Cb[1]
DIPE_2	DIPO_2	B/U/Cb[2]	B/U/Cb[0]
DIPE_1	DIPO_1	B/U/Cb[1]	0
DIPE_0	DIPO_0	B/U/Cb[0]	0
CLOCK		CLK	CLK
HSYNC		HS	HS
DATA ENABLE		DE	DE
VSYNC		VS	VS

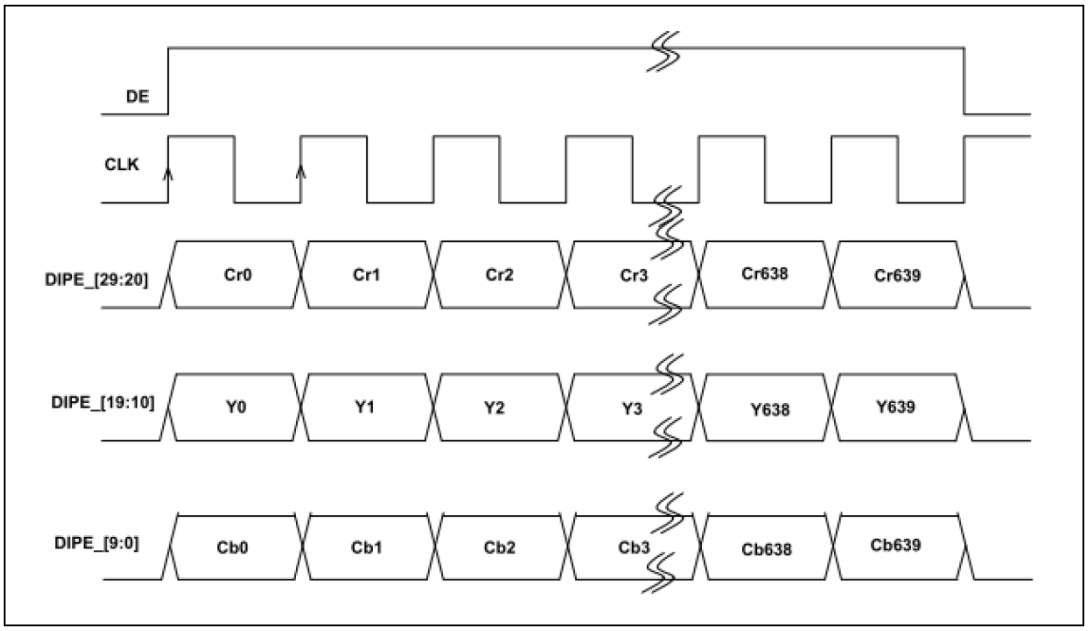
Note: Refer to the pinout description table (Table 16) for the corresponding pin names of DIPE0-29 and DIPO0-29.

Figure 11. Digital video input data on DIPE for 4:4:4 RGB format



Note: DIPO data is identical to the data above.

Figure 12. Digital video input data on DIPE for 4:4:4 YUV format



Note: DIPO data is identical to the data above.

Table 6. Digital video input format YUV 4:2:2 (24/20/16 bit bus)

DIPE	DIPO	4:2:2 YUV ITU-R601 Formats		
		12 bit	10 bit	8 bit
DIPE_29	DIPO_29	0	0	0
DIPE_28	DIPO_28	0	0	0
DIPE_27	DIPO_27	CbCr[1]	0	0
DIPE_26	DIPO_26	CbCr[0]	0	0
DIPE_25	DIPO_25	0	0	0
DIPE_24	DIPO_24	0	0	0
DIPE_23	DIPO_23	Y[1]	0	0
DIPE_22	DIPO_22	Y[0]	0	0
DIPE_21	DIPO_21	0	0	0
DIPE_20	DIPO_20	0	0	0
DIPE_19	DIPO_19	CbCr[11]	CbCr[9]	CbCr[7]
DIPE_18	DIPO_18	CbCr[10]	CbCr[8]	CbCr[6]
DIPE_17	DIPO_17	CbCr[9]	CbCr[7]	CbCr[5]
DIPE_16	DIPO_16	CbCr[8]	CbCr[6]	CbCr[4]
DIPE_15	DIPO_15	CbCr[7]	CbCr[5]	CbCr[3]
DIPE_14	DIPO_14	CbCr[6]	CbCr[4]	CbCr[2]
DIPE_13	DIPO_13	CbCr[5]	CbCr[3]	CbCr[1]
DIPE_12	DIPO_12	CbCr[4]	CbCr[2]	CbCr[0]
DIPE_11	DIPO_11	CbCr[3]	CbCr[1]	0
DIPE_10	DIPO_10	CbCr[2]	CbCr[0]	0
DIPE_9	DIPO_9	Y[11]	Y[9]	Y[7]
DIPE_8	DIPO_8	Y[10]	Y[8]	Y[6]
DIPE_7	DIPO_7	Y[9]	Y[7]	Y[5]
DIPE_6	DIPO_6	Y[8]	Y[6]	Y[4]
DIPE_5	DIPO_5	Y[7]	Y[5]	Y[3]
DIPE_4	DIPO_4	Y[6]	Y[4]	Y[2]
DIPE_3	DIPO_3	Y[5]	Y[3]	Y[1]
DIPE_2	DIPO_2	Y[4]	Y[2]	Y[0]
DIPE_1	DIPO_1	Y[3]	Y[1]	0
DIPE_0	DIPO_0	Y[2]	Y[0]	0
CLOCK		CLK	CLK	CLK
HSYNC		HS	HS	HS
DATA ENABLE		DE	DE	DE
VSYNC		VS	VS	VS

Figure 13. Digital video input data on DIPE for 4:2:2 YUV format

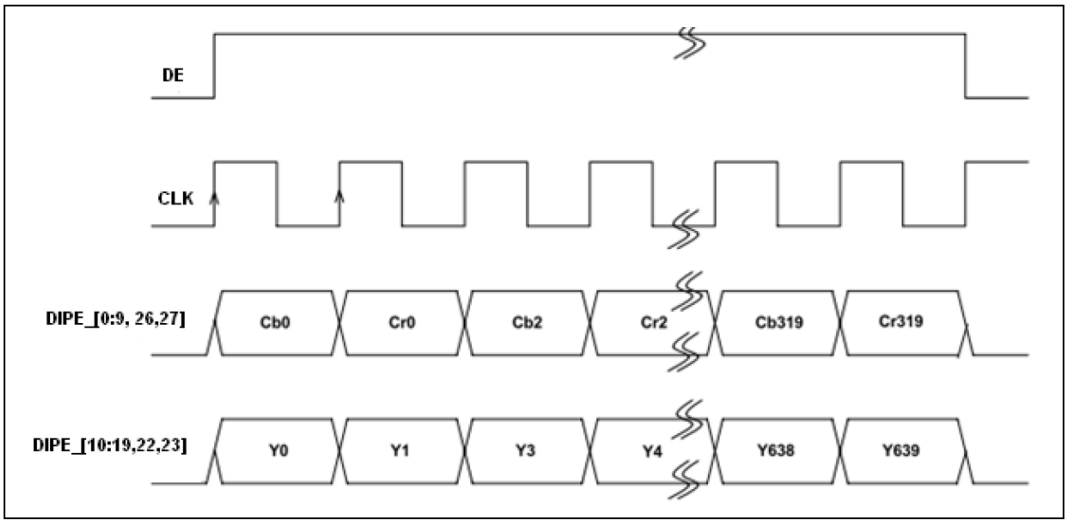
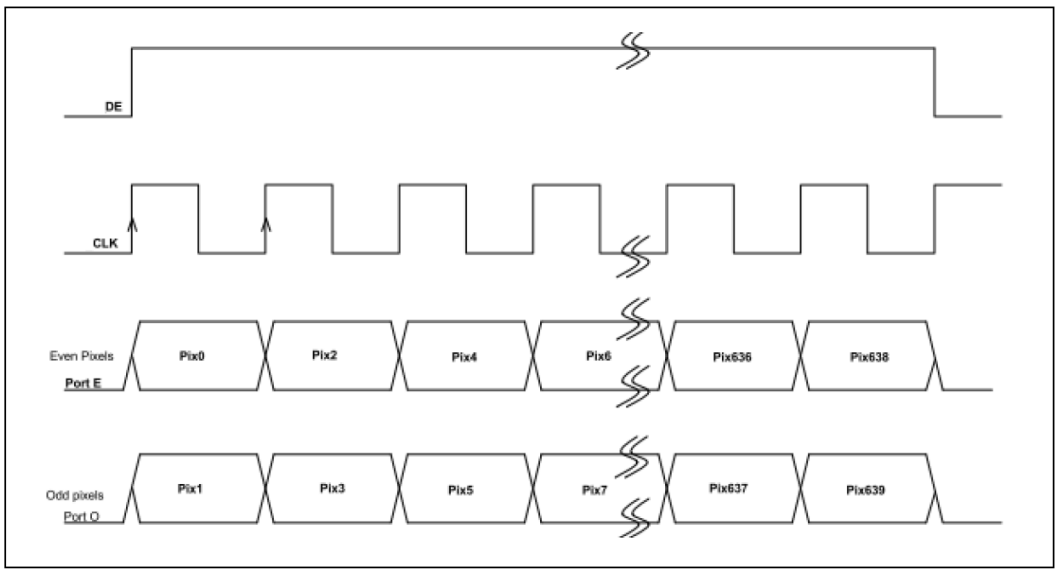


Table 7. Digital video input format for DIPE and DIPO combined (60 bit bus)

DIPE/DIPO		
DIPEB_SWAP --->	0	1
DIPE_[29..0]	First pixel (Even)	Second pixel (Odd)
DIPO_[29..0]	Second pixel (Odd)	First pixel (Even)
CLOCK	Pixel clock (1/2 Freq)	Pixel clock (1/2 Freq)
HSYNC	H Sync	H Sync
DATA ENABLE	Data enable	Data enable
VSYNC	V Sync	V Sync

Figure 14. Digital video input data on combined configuration



4.7 Digital audio receivers

The STDP4028 provides an I2S receiver and an SPDIF receiver. These receiver inputs are available on multifunction (MFP) pins. I2S and SPDIF receivers share the input pins. The I2S receiver input has four serial data pins, a word clock pin, and a bit clock pin. It is capable of receiving up to eight channels of LPCM audio stream. The SPDIF input can handle up to 2ch LPCM or multi-channel compressed audio formats, such as AC3 and DTS. The I2S and SPDIF audio pins are shared, and thus, the device can only be configured to receive audio either in I2S or SPDIF format for multi-channel audio. The received audio streams are then directed to a DisplayPort transmitter packed as secondary streams. The I2S receiver of STDP4028 does not require “MCLK” input for transporting I2S audio over DisplayPort. The SPDIF receiver is capable of receiving IEC60958 audio streams, as well as IEC61937 audio streams. Audio path in the chip provides necessary format conversion required to transport the audio from these receivers to DisplayPort transmitter and to DisplayPort link. SPDIF audio input can be received on any one of the I2S_0, I2S_1, I2S_2, or I2S_3 pins.

Digital audio input formats supported in STDP4028 are shown below.

Table 8. I2S audio formats

Sampling rate	32 K, 44.1 K, 48 K, 88.2 K, 96 K, 192 kHz		
Bit depth	16 bps, 20 bps, 24 bps		
Word length	**Bit depth**	**Left justified**	**I2S (Philips)**
64xFs	24 bits	Yes	Yes
	20 bits	Yes	Yes
	16 bits	Yes	Yes
48xFs	24 bits	Yes	Yes
	20 bits	Yes	Yes
	16 bits	Yes	Yes
32xFs	16 bits	Yes	Yes

Table 9. S/PDIF audio formats

Sampling rate	44.1 K,48 K, 88.2 K, 96 K, 176.4 K, 192 kHz
Bit depth	16-/20-/24 bits per sample
Supported audio formats	2 Ch LPCM, AC3, DTS

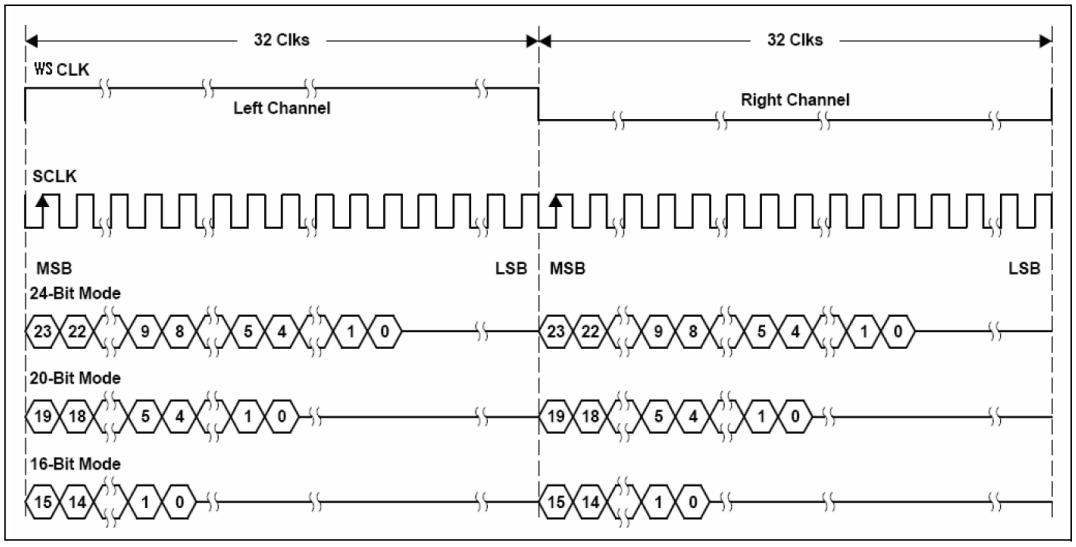
4.7.1 I2S format examples

As shown in the tables above, STDP4028 supports different word lengths within I2S audio format. The word length is measured in number of I2S clocks fit within one word clock period. The factors determine the word clock period range from 16 to 32. For example, 32x2 number of I2C bit clocks (referred to as SLCK) can fit within 1 word clock period. This particular mode is called 64xFs clock mode, where Fs refers to audio sampling frequency. Similarly, there are other clock modes, such as 48xFs and 32xFs in I2S standard.

64xFs clock mode

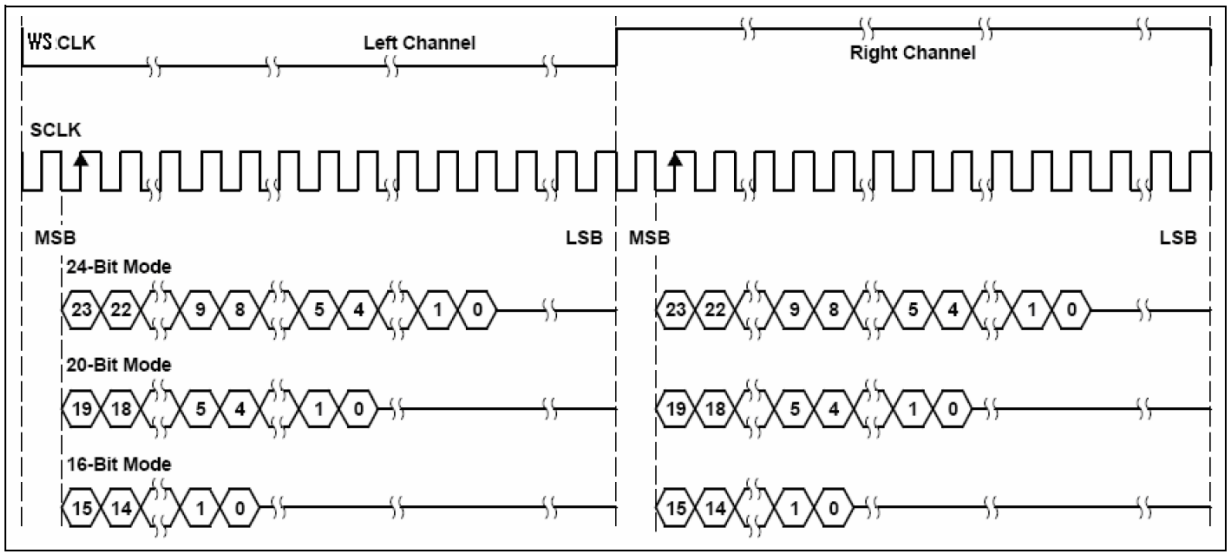
A 64xFs clock mode can accommodate higher bit depth audio samples typically used by high definition audio. High Definition Audio provides up to 7.1 surround audio with 192 KHz sampling rate and up to 32-bit resolution. For a given bit depth, depending on arrangement of audio data within the word clock period, 64xFs clock mode is classified as left-justified, right-justified, and delayed left-justified (also called I2S or Philips mode). The STDP4028 supports left-justified and I2S format within 64xFs clock mode. The description of supported formats is shown below.

Figure 15. Left-justified 64xFs format



The diagram above shows left-justified 64xFs format with sample bit depth of 24, 20, and 16 bits for a 2-channel audio. Note that, in the case of 8-channel audio, there are a total of four serial data lines, each of which carries 2-channel audio. SCLK is I2S bit clock running at 64xfs clocks rate. WS clock is HIGH when left-channel data is transmitted and LOW when right-channel data is transmitted. The first bit of data appears on the data lines at the same time WS toggles. The data is written MSB first and is valid on the rising edge of the bit clock.

Figure 16. I2S 64xFs format

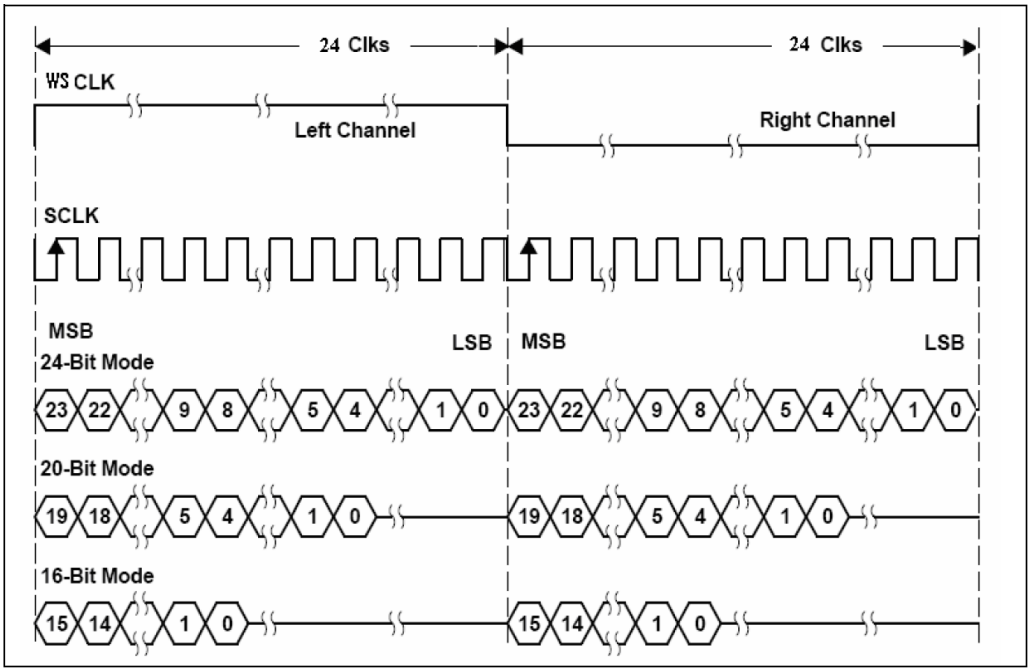


The diagram above is generally referred to as I2S format (also called Philips format). There is one SCLK clock delay from the time the WS clock signal changes state to the first bit of data on the data lines. Sample bit depth of 24, 20, and 16 bits for a 2-channel audio is shown in the diagram. The WS clock is LOW when left-channel data is transmitted and HIGH when right-channel data is transmitted. The data is written MSB first and is valid on the rising edge of the bit clock. SCLK is a bit clock running at 64xfs clocks rate.

48xFs clock mode

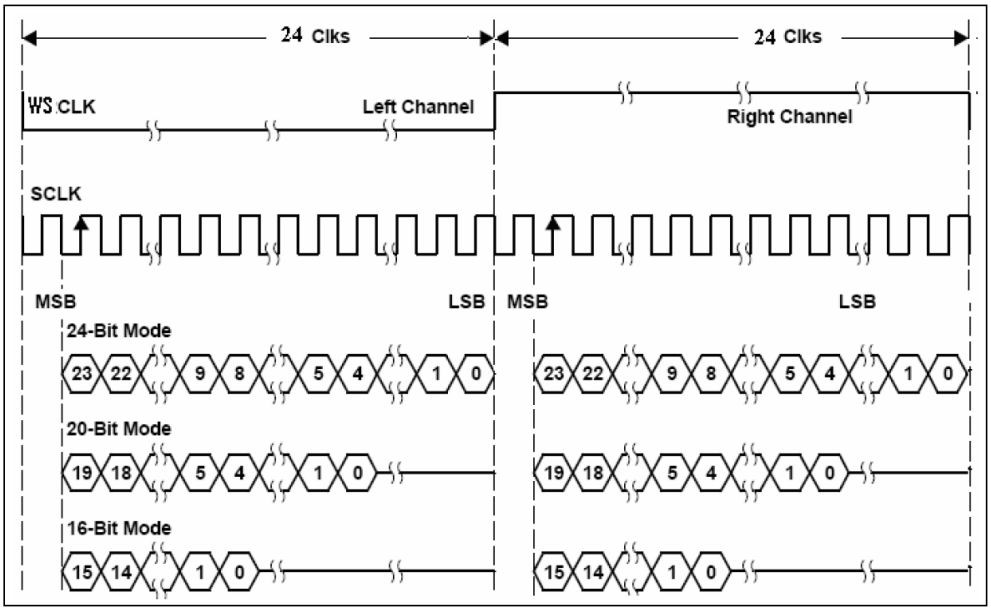
A 48xFs clock mode can accommodate audio bit depth of 24 bits-per-samples or below. This format is also used for High Definition Audio transportation (up to 7.1 surround audio with 192 kHz sampling rate and up to 24-bit resolution). For a given bit depth, depending on arrangement of audio data within the word clock period, the 48xFs clock mode is classified as left-justified, right-justified, and delayed left-justified (also called I2S or Philips mode). The STDP4028 supports left-justified and I2S format within 48xFs clock mode. The description of supported formats is shown below.

Figure 17. Left-justified 48xFs Format



The diagram above shows left-justified 48xFs format with sample bit depth of 24, 20, and 16 bits for a 2-channel audio. SCLK is I2S bit clock running at 48xFs clocks rate. WS clock is HIGH when left-channel data is transmitted and LOW when right-channel data is transmitted. The first bit of data appears on the data lines at the same time WS toggles. The data is written MSB first and is valid on the rising edge of the bit clock.

Figure 18. I2S 48xFs format



The diagram above is 48xFs I2S format (also referred to as Philips format). There is a one SCLK clock delay from the time the WS clock signal changes state to the first bit of data on the data lines. Sample bit depth of 24, 20, and 16 bits for a 2-channel audio is shown in the diagram. The WS clock is LOW when left-channel data is transmitted and HIGH when right-channel data is transmitted. The data is written MSB first and is valid on the rising edge of the bit clock. SCLK is a bit clock running at 48xFs clock rate.

32xFs clock mode

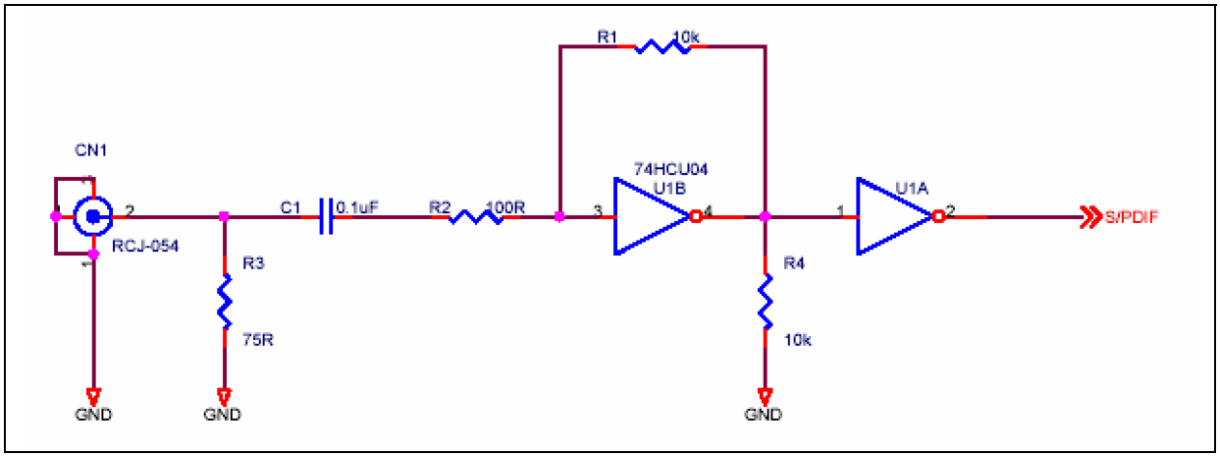
A 32xFs clock mode can accommodate audio bit depth of 16 bits-per-samples. This format is typically used for 2-channel audio transportation. For a given bit depth, depending on arrangement of audio data within the word clock period, the 32xFs clock mode is classified as left-justified and delayed left-justified (also called I2S or Philips mode).

Note: The timing diagrams are similar to 48xFs clock format, except the sample data structure is 16 bits only.

4.7.2 S/PDIF receiver input requirement

S/PDIF input is required to convert the original bi-phase S/PDIF signal to LVTTL signal for STDP4028 to sample the audio signal. An example circuit of this conversion is shown below.

Figure 19. S/PDIF input signal level conversion circuit



4.8 LVDS video input port

STDP4028 has an integrated 30-bit QLVDS receiver that supports the following:

- ingle pixel mode, dual pixel mode and quad pixel mode
- 30-bit mapping to the LVDS channels
- 24-bit mapping to the LVDS channels
- 18-bit mapping to the LVDS channels
- JEIDA/VESA/PSWG compliant data mapping from 30-/24-bit source
- Programmable even/odd channel swapping
- Programmable channel polarity (positive (D+) and negative (D-)) swapping
- Supports up to 100 Mpixels per channel

This device consists of four LVDS channels (EVEN0 [E0], EVEN1 [E1], ODD0 [O0] and ODD1[O1]) to receive data and timing information from LVDS source device.

STDP4028 can receive input from the standard LVDS interface sources, supporting all standard data formats-single, dual and quad bus formats with 6-bit, 8-bit, or 10-bit per color data input. The data clock at dual bus operation is DCLK/2 and the data clock at quad bus operation is DCLK/4. The default data format is compliant with PSWG type mapping. The following diagrams illustrate the default RGB, HSync, VSync, and Data Enable signal mapping in a single bus output configuration under various color depths. In addition to the default mapping, STDP4028 allows several data swapping options for board layout flexibility.

Table 10. Data transferring order quad LVDS configuration

Channel	Pixel	Pixel	Pixel
E1	0	4	8
E0	1	5	9
O0	2	6	10
O1	3	7	11

The following diagrams illustrate various input data-mapping options.

Figure 20. 10-bit PSWG (non-JEIDA) data-mapping

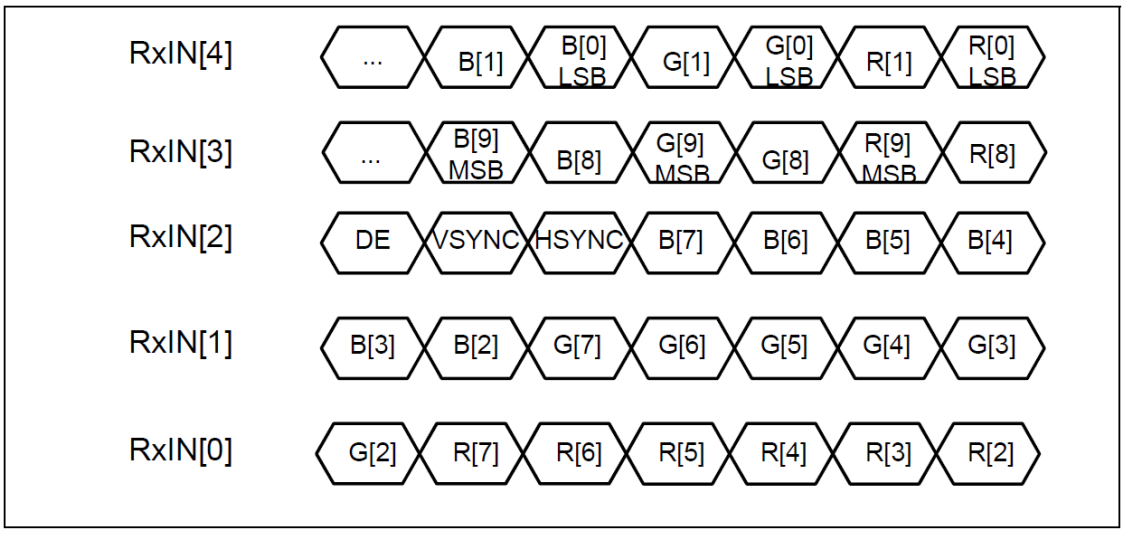


Figure 21. 8-bit PSWG (non-JEIDA) data-mapping

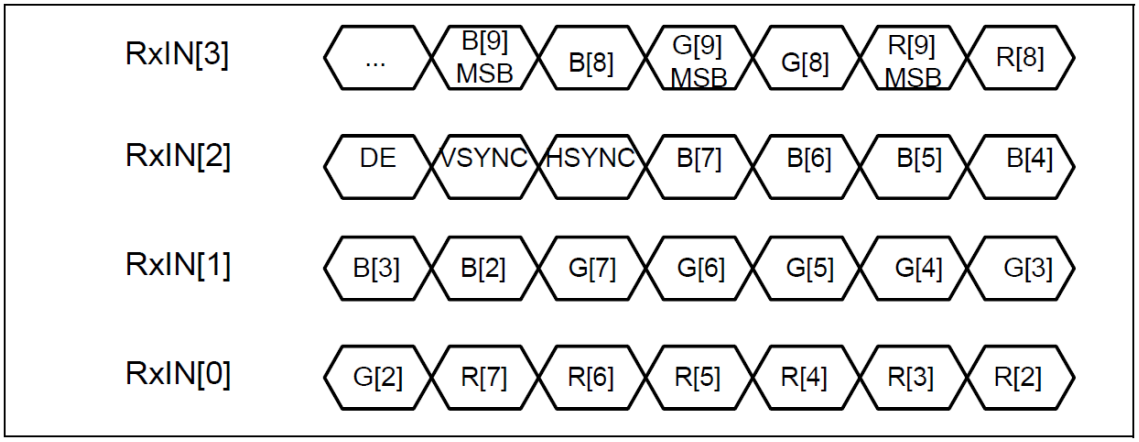
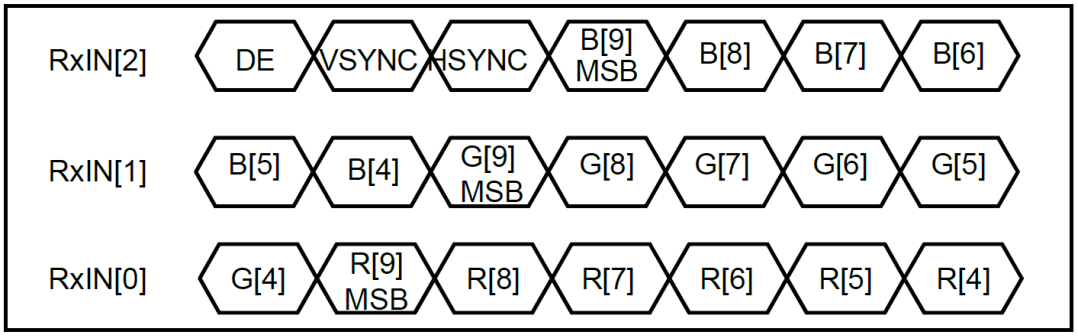


Figure 22. 6-bit PSWG (non-JEIDA) data-mapping



4.9 DisplayPort transmitter

The DisplayPort transmitter in STDP4028 encodes 24-bit audio and 30-bit video signals in parallel form into DisplayPort serial format. The DisplayPort transmitter output interface comprises four main lanes, an auxiliary channel, and an HPD input signal.

The main lanes are unidirectional, AC-coupled, doubly terminated differential pairs, to transport the audio-video streams. The transmitter supports three types of bit rates: 2.7 Gbps per lane (referred to as “high bit rate”) and 1.62 Gbps per lane (referred to as “low bit rate” or “reduced bit rate”) and 3.2 Gbps (referred as “Turbo” bit rate). The transmitter locks to one of the bit rates after negotiating with the receiver (sink device).

The DisplayPort Aux channel is a half-duplex bidirectional, AC-coupled, doubly terminated differential pair. It is capable of transmitting and receiving bits at 1 Mbps. The AUX channel is used for link management and device control and handles the following functions:

- Link training
- Exchanging AUX and I2C communication

The HPD line is used to detect the presence of sink device and to receive the interrupt requests from a DisplayPort sink device. The transmitter monitors the activity on HPD line and responds to the receivers interrupt request by initiating the Aux channel transaction. The HPD line remains low when sink device is not present and high when sink device is ready to receive DisplayPort signals. An active low short pulse on HPD line indicates an interrupt request from sink device for AUX transaction.

The DisplayPort transmitter supports High-Bandwidth Digital Content Protection, HDCP 1.3, for enhanced security of the digital content being transmitted over DisplayPort link.

The STDP4028 can receive up to eight channels of LPCM coded audio at maximum 192 kHz with a 24-bit sample size.

4.10 Highest video resolution modes supported

Table 11. Highest video resolution modes supported

Resolution	Refresh	Color depth	Reduced blanking	Freq.	Input port(s)	Output port DPTX	DPTX lane
1920 x 1080P	120 Hz	8 bpc	Extended Blanking	390 MHz	Quad LVDS	DP	4L
2560 x 1600	60 Hz	8 bpc	RB	268.5 MHz	QLVDS / DIPE and DIPO (combined)	DP	4L
1600 x 1200	60 Hz	8 bpc		162 MHz	LVDS / DIPE ON, DIPO OFF	DP	4L
1920 x 1080p	60 Hz	10 bpc		144 MHz	LVDS / DIPE and DIPO (combined)	DP	2L
1920 x 1080p	60 Hz	10 bpc		144 MHz	LVDS / DIPE ON, DIPO OFF	DP	2L
1920 x 1200	60 Hz	8 bpc	RB	154 MHz	LVDS / DIPE and DIPO (combined)	DP	2L
1920 x 1200	60 Hz	8 bpc	RB	154 MHz	LVDS / DIPE ON, DIPO OFF	DP	2L
1600 x 1200	60 Hz	8 bpc		162 MHz	LVDS / DIPE ON, DIPO OFF	DP	2L
1680 x 1050	60 Hz	6 bpc	RB	119 MHz	LVDS / DIPE and DIPO (combined)	DP	1L
1680 x 1050	60 Hz	6 bpc	RB	119 MHz	LVDS / DIPE ON, DIPO OFF	DP	1L

4.11 On-chip microcontroller (OCM)

The STDP4028 supports an on-chip microcontroller. When configured, the OCM executes a firmware program running from external Flash ROM. The chip supports an SPI interface to connect commercial serial Flash ROM devices. STDP4028 supports SPI Flash ROMs of sizes 512 KB to 4 MBits. Contact Kinetic for the list of SPI Flash devices supported in the ISP driver tool.

4.12 Serial peripheral interface for SPI Flash ROM

The SPI interface between STDP4028 and a serial Flash ROM is as follows:

SPI_CSn <-> CE# of SPI ROM

SPI_CLK <-> SCK of SPI ROM

SPI_DO <-> SI of SPI ROM

SPI_DI <-> SO of SPI ROM

Pins of WP# and HOLD# of SPI ROM are options for controlling the SPI ROM. WP# if pulled low will disable writing to the ROM. HOLD# is used when multiple devices are used in daisy-chain configuration. They can be pulled-high all the time to disable their functions or they can be controlled with GPIOs for

more flexibility. Refer to SPI ROM specifications for details. SPI port pins also share functionality with general-purpose input/output. During power up, the bootstrap selection SPI_FUNC_SEL decides whether the port pins are used as SPI interface or general purpose I/Os.

4.13 Test and debug

The following sections are useful for test and debug purposes. Some portions of this section are of relevance only for STDP4028 operating in standalone mode where the internal OCM is the system master and is executing firmware from an external SPI Flash device.

4.13.1 I2C (JTAG) debug interface

The STDP4028 has a I2C debug port. This port is intended for development/debug purposes from an external micro. This mode of operation is not recommended for a production environment. The OCM and its peripherals, such as UART and SPI blocks are not operational when the two-wire interface is active. Pin description of the two-wire interface is not shown in this document. Contact Kinetic for further details.

4.13.2 UART interface

The OCM has an integrated Universal Asynchronous Receiver and Transmitter (UART) port that can be used as a factory debug port. The UART interface is optional and described only to give information for developmental/debug purposes. In particular, the UART can be used to 1) read/write chip registers; 2) read/write to NVRAM, and 3) read/write to Flash ROM (In-System-Programming). The UART_RX and UART_TX pins also share functionality with GPIO. When unused these pins are available as GPIO pins. The UART baud rate is set to 115200 baud.

4.13.3 In-system-programming (ISP) of external Flash ROM

It is possible to program the serial ROM devices via the standard UART or by using DDC2Bi protocol. The embedded boot firmware performs the programming of external Flash ROM. However, ISP requires an external hardware and software tool (GProbe). Contact Kinetic for the ISP tool and procedure.

4.13.4 Internal test pattern generator

The STDP4028 has an on-chip test pattern generator that is useful for built-in self-test in the production line. The BIST patterns and sequence are configurable through the host controller. The STDP4028 includes some ofthe standard BIST patterns typically used in a production test environment.

5. BGA footprint and pin lists

5.1 Ball grid array diagram

The ball grid array (BGA) diagrams give the allocation of pins to the package, shown from the top looking down using the PCB footprint.

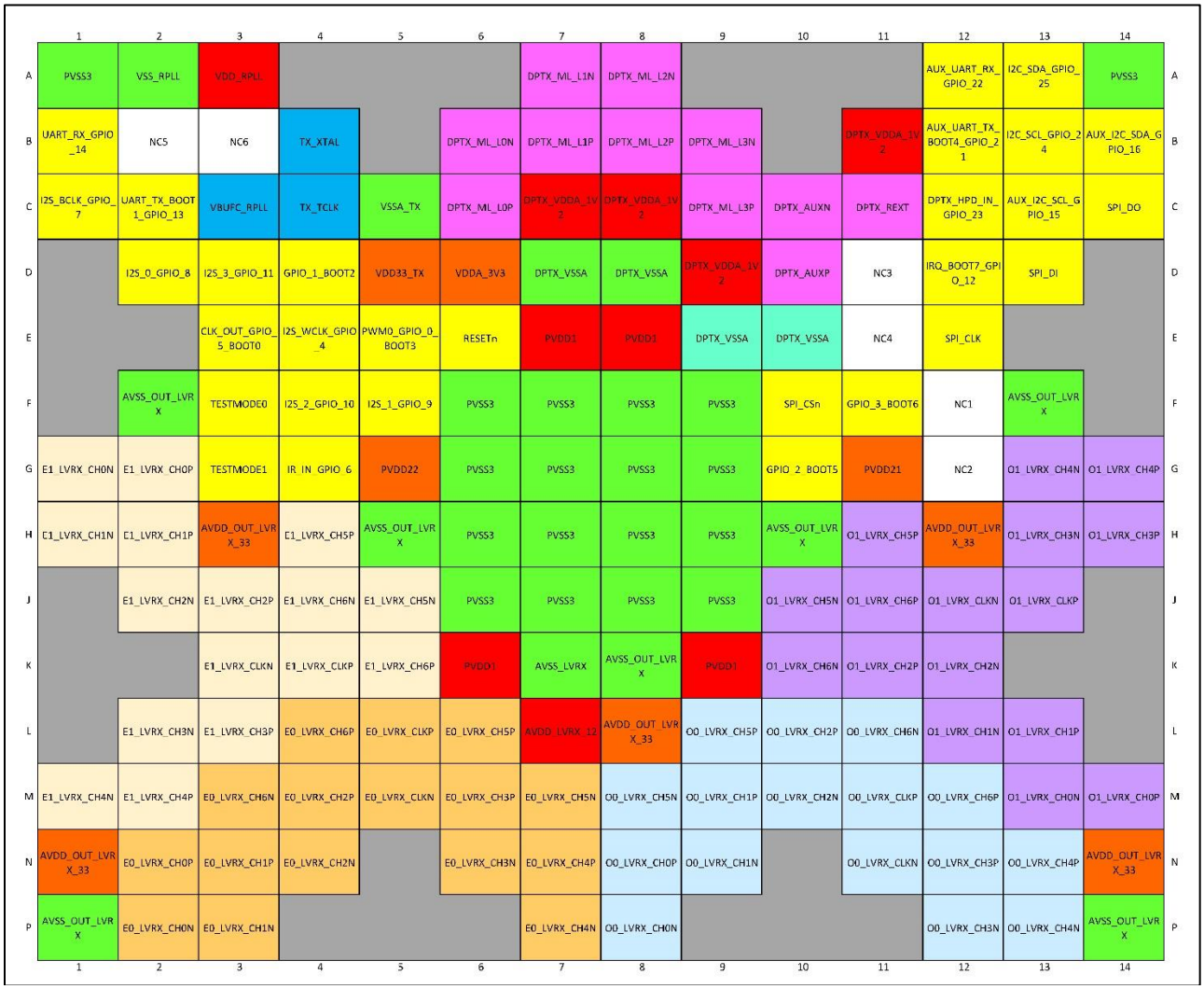
Some signal names in BGA diagrams have been abbreviated. Refer to*Table 13: Pin list on page 38* for full signal names sorted by pin number.

Table 12. Key to BGA diagrams

Function	Type	Key
DisplayPort input	SIG	
Reference clocks	SIG	
System controls	SIG	
Multi-function and system interface connections	SIG	
I2S/SPDIF audio output	SIG	
LVDS/TTL Output_Even-0	SIG	
LVDS/TTL Output_Even-1	SIG	
LVDS/TTL Output_Odd-0	SIG	
LVDS/TTL Output_Odd-1	SIG	
Analog power	VCC/VDD	
Analog ground	VSS/GND	
System power	VCC/VDD	
System ground	VSS/GND	
No connect/Do not connect	NC/DNC	
No ball		

The STDP4028 is available in 164-pin LFBGA package.

Figure 23. Pin Diagram



5.2 Full pin list sorted by pin number

Table 13. Pin list

Pin number	Net name
A1	PVSS3
A2	VSS_RPLL
A3	VDD_RPLL
A7	DPTX_ML_L1N
A8	DPTX_ML_L2N
A12	AUX_UART_RX_GPIO_22
A13	I2C_SDA_GPIO_25
A14	PVSS3
B1	UART_RX_GPIO_14
B2	NC
B3	NC
B4	TX_XTAL
B6	DPTX_ML_L0N
B7	DPTX_ML_L1P
B8	DPTX_ML_L2P
B9	DPTX_ML_L3N
B11	DPTX_VDDA_1V2
B12	AUX_UART_TX_BOOT4_GPIO_21
B13	I2C_SCL_GPIO_24
B14	AUX_I2C_SDA_GPIO_16
C1	I2S_BCLK_GPIO_7
C2	UART_TX_BOOT1_GPIO_13
C3	VBUFC_RPLL
C4	TX_TCLK
C5	VSSA_TX
C6	DPTX_ML_L0P
C7, C8	DPTX_VDDA_1V2
C9	DPTX_ML_L3P
C10	DPTX_AUXN
C11	DPTX_REXT
C12	DPTX_HDP_IN_GPIO_23
C13	AUX_I2C_SCL_GPIO_15
C14	SPI_DO

Table 13. Pin list (continue)

Pin number	Net name
D2	I2S_0_GPIO_8
D3	I2S_3_GPIO_11
D4	GPIO_1_BOOT2
D5	VDD33_TX
D6	VDDA_3V3
D7, D8	DPTX_VSSA
D9	DPTX_VDDA_1V2
D10	DPTX_AUXP
D11	NC
D12	IRQ_BOOT7_GPIO_12
D13	SPI_DI
E3	CLK_OUT_GPIO_5_BOOT0
E4	I2S_WCLK_GPIO_4
E5	PWM0_GPIO_0_BOOT3
E6	RESETn
E7, E8	PVDD1
E9, E10	DPTX_VSSA
E11	NC
E12	SPI_CLK
F2	AVSS_OUT_LVRX
F3	TESTMODE0
F4	I2S_2_GPIO_10
F5	I2S_1_GPIO_9
F6, F7, F8, F9	PVSS3
F10	SPI_CSn
F11	GPIO_3_BOOT6
F12	NC
F13	AVSS_OUT_LVRX
G1	E1_LVRX_CH0N
G2	E1_LVRX_CH0P
G3	TESTMODE1
G4	IR_IN_GPIO_6
G5	PVDD22
G6, G7, G8, G9	PVSS3
G10	GPIO_2_BOOT5

Table 13. Pin list (continue)

Pin number	Net name
G11	PVDD21
G12	NC
G13	O1_LVRX_CH4N
G14	O1_LVRX_CH4P
H1	E1_LVRX_CH1N
H2	E1_LVRX_CH1P
H3	AVDD_OUT_LVRX_33
H4	E1_LVRX_CH5P
H5	AVSS_OUT_LVRX
H6, H7, H8, H9	PVSS3
H10	AVSS_OUT_LVRX
H11	O1_LVRX_CH5P
H12	AVDD_OUT_LVRX_33
H13	O1_LVRX_CH3N
H14	O1_LVRX_CH3P
J2	E1_LVRX_CH2N
J3	E1_LVRX_CH2P
J4	E1_LVRX_CH6N
J5	E1_LVRX_CH5N
J6, J7, J8, J9	PVSS3
J10	O1_LVRX_CH5N
J11	O1_LVRX_CH6P
J12	O1_LVRX_CLKN
J13	O1_LVRX_CLKP
K3	E1_LVRX_CLKN
K4	E1_LVRX_CLKP
K5	E1_LVRX_CH6P
K6	PVDD1
K7	AVSS_LVRX
K8	AVSS_OUT_LVRX
K9	PVDD1
K10	O1_LVRX_CH6N
K11	O1_LVRX_CH2P
K12	O1_LVRX_CH2N
L2	E1_LVRX_CH3N

Table 13. Pin list (continue)

Pin number	Net name
L3	E1_LVRX_CH3P
L4	E0_LVRX_CH6P
L5	E0_LVRX_CLKP
L6	E0_LVRX_CH5P
L7	AVDD_LVRX_12
L8	AVDD_OUT_LVRX_33
L9	O0_LVRX_CH5P
L10	O0_LVRX_CH2P
L11	O0_LVRX_CH6N
L12	O1_LVRX_CH1N
L13	O1_LVRX_CH1P
M1	E1_LVRX_CH4N
M2	E1_LVRX_CH4P
M3	E0_LVRX_CH6N
M4	E0_LVRX_CH2P
M5	E0_LVRX_CLKN
M6	E0_LVRX_CH3P
M7	E0_LVRX_CH5N
M8	O0_LVRX_CH5N
M9	O0_LVRX_CH1P
M10	O0_LVRX_CH2N
M11	O0_LVRX_CLKP
M12	O0_LVRX_CH6P
M13	O1_LVRX_CH0N
M14	O1_LVRX_CH0P
N1	AVDD_OUT_LVRX_33
N2	E0_LVRX_CH0P
N3	E0_LVRX_CH1P
N4	E0_LVRX_CH2N
N6	E0_LVRX_CH3N
N7	E0_LVRX_CH4P
N8	O0_LVRX_CH0P
N9	O0_LVRX_CH1N
N11	O0_LVRX_CLKN
N12	O0_LVRX_CH3P

Table 13. Pin list (continue)

Pin number	Net name
N13	O0_LVRX_CH4P
N14	AVDD_OUT_LVRX_33
P1	AVSS_OUT_LVRX
P2	E0_LVRX_CH0N
P3	E0_LVRX_CH1N
P7	E0_LVRX_CH4N
P8	O0_LVRX_CH0N
P12	O0_LVRX_CH3N
P13	O0_LVRX_CH4N
P14	AVSS_OUT_LVRX

6. Connections

6.1 Pin list

I/O Legend: I = Input; O = Output; P = Power; G = Ground

Note: Some pins can have multiple functionalities, which are configured under register control. The alternate functionality for each pin is listed in the Description column.

Table 14. DisplayPort transmitter outputs

Pin	Assignment	I/O	Description
B6	DPTX_ML_L0N	O	Negative output of DPTX Main Link Lane0
C6	DPTX_ML_L0P	O	Positive output of DPTX Main Link Lane0
A7	DPTX_ML_L1N	O	Negative output of DPTX Main Link Lane1
B7	DPTX_ML_L1P	O	Positive output of DPTX Main Link Lane1
A8	DPTX_ML_L2N	O	Negative output of DPTX Main Link Lane2
B8	DPTX_ML_L2P	O	Positive output of DPTX Main Link Lane2
B9	DPTX_ML_L3N	O	Negative output of DPTX Main Link Lane3
C9	DPTX_ML_L3P	O	Positive output of DPTX Main Link Lane3
C10	DPTX_AUXN	I/O	Negative input/output of DPTX Aux Channel
D10	DPTX_AUXP	I/O	Positive input/output of DPTX Aux Channel
C12	DPTX_HPD_IN/GPIO_23	I/O	DisplayPort Receiver Hot Plug Detect Input
			General Purpose Schmitt Trigger Input / Tri-state Output 26 [5V Tolerant]
C11	DPTX_REXT	I	Termination calibration reference resistor; 240 ohm 1% resistor should be connected from this pin to 1.2 V analog power supply.

Table 15. Reference clocks

Pin	Assignment	I/O	Description
B4	TX_XTAL	I/O	Crystal Oscillator Input. Connect to external crystal.
C4	TX_TCLK	I/O	Reference Clock (TCLK) from a 27 MHz Crystal or TTL Oscillator. Connect to external crystal or oscillator.
C3	VBUFC_RPLL	O	Analog Test Pin for Internal Clocks. No connect.

Table 16. Digital video inputs

Pin	Assignment	I/O	Description
K4	E1_LVRX_CLKP	I	Positive input of LVDS RX E1 Clock Channel
			TTL Even Red Channel Data 4
K3	E1_LVRX_CLKN	I	Negative input of LVDS RX E1 Clock Channel
			TTL Even Red Channel Data 7
G2	E1_LVRX_CH0P	I	Positive input of LVDS RX E1 Channel 0
			TTL VSYNC
G1	E1_LVRX_CH0N	I	Negative input of LVDS RX E1 Channel 0
			TTL HSYNC
H2	E1_LVRX_CH1P	I	Positive input of LVDS RX E1 Channel 1
			TTL Even Red Channel Data 1
H1	E1_LVRX_CH1N	I	Negative input of LVDS RX E1 Channel 1
			TTL Even Red Channel Data 0
J3	E1_LVRX_CH2P	I	Positive input of LVDS RX E1 Channel 2
			TTL DE
J2	E1_LVRX_CH2N	I	Negative input of LVDS RX E1 Channel 2
			TTL Even Red Channel Data 9
L3	E1_LVRX_CH3P	I	Positive input of LVDS RX E1 Channel 3
			TTL Even Red Channel Data 6
L2	E1_LVRX_CH3N	I	Negative input of LVDS RX E1 Channel 3
			TTL Even Red Channel Data 5
M2	E1_LVRX_CH4P	I	Positive input of LVDS RX E1 Channel 4
			TTL Even Red Channel Data 2
M1	E1_LVRX_CH4N	I	Negative input of LVDS RX E1 Channel 4
			TTL Even Red Channel Data 3
J5	E1_LVRX_CH5N	I	TTL Even Red Channel Data 8
H4	E1_LVRX_CH5P	I	TTL Even Blue Channel Data 0
K5	E1_LVRX_CH6P	I	TTL Odd Red Channel Data 0
J4	E1_LVRX_CH6N	I	TTL Even Blue Channel Data 1
J12	O1_LVRX_CLKN	I	Negative input of LVDS RX O1 Clock Channel
			TTL Odd Blue Channel Data 8
J13	O1_LVRX_CLKP	I	Positive input of LVDS RX O1 Clock Channel
			TTL Odd Blue Channel Data 7

Table 16. Digital video inputs (continue)

Pin	Assignment	I/O	Description
M14	O1_LVRX_CH0P	I	Positive input of LVDS RX O1 Channel 0
			TTL Odd Green Channel Data 6
M13	O1_LVRX_CH0N	I	Negative input of LVDS RX O1 Channel 0
			TTL Odd Green Channel Data 5
L13	O1_LVRX_CH1P	I	Positive input of LVDS RX O1 Channel 1
			TTL Odd Green Channel Data 3
L12	O1_LVRX_CH1N	I	Negative input of LVDS RX O1 Channel 1
			TTL Odd Blue Channel Data 0
K11	O1_LVRX_CH2P	I	Positive input of LVDS RX O1 Channel 2
			TTL Odd Green Channel Data 4
K12	O1_LVRX_CH2N	I	Negative input of LVDS RX O1 Channel 2
			TTL Odd Green Channel Data 2
H14	O1_LVRX_CH3P	I	Positive input of LVDS RX O1 Channel 3
			TTL Odd Blue Channel Data 4
H13	O1_LVRX_CH3N	I	Negative input of LVDS RX O1 Channel 3
			TTL Odd Blue Channel Data 5
G14	O1_LVRX_CH4P	I	Positive input of LVDS RX O1 Channel 4
			TTL Odd Blue Channel Data 2
G13	O1_LVRX_CH4N	I	Negative input of LVDS RX O1 Channel 4
			TTL Odd Blue Channel Data 3
J10	O1_LVRX_CH5N	I	TTL Odd Green Channel Data 8
H11	O1_LVRX_CH5P	I	TTL Odd Blue Channel Data 6
K10	O1_LVRX_CH6N	I	TTL Odd Green Channel Data 9
J11	O1_LVRX_CH6P	I	TTL Odd Blue Channel Data 9
M5	E0_LVRX_CLKN	I	Negative input of LVDS RX E0 Clock Channel
			TTL Even Green Channel Data 2
L5	E0_LVRX_CLKP	I	Positive input of LVDS RX E0 Clock Channel
			TTL Even Green Channel Data 3
P2	E0_LVRX_CH0N	I	Negative input of LVDS RX E0 Channel 0
			TTL Even Green Channel Data 0
N2	E0_LVRX_CH0P	I	Positive input of LVDS RX E0 Channel 0
			TTL Even Green Channel Data 1
P3	E0_LVRX_CH1N	I	Negative input of LVDS RX E0 Channel 1
			TTL Even Green Channel Data 6

Table 16. Digital video inputs (continue)

Pin	Assignment	I/O	Description
N3	E0_LVRX_CH1P	I	Positive input of LVDS RX E0 Channel 1
			TTL Even Green Channel Data 7
N4	E0_LVRX_CH2N	I	Negative input of LVDS RX E0 Channel 2
			TTL Even Green Channel Data 4
M4	E0_LVRX_CH2P	I	Positive input of LVDS RX E0 Channel 2
			TTL Even Green Channel Data 5
N6	E0_LVRX_CH3N	I	Negative input of LVDS RX E0 Channel 3
			TTL Even Blue Channel Data 7
M6	E0_LVRX_CH3P	I	Positive input of LVDS RX E0 Channel 3
			TTL Even Blue Channel Data 8
P7	E0_LVRX_CH4N	I	Negative input of LVDS RX E0 Channel 4
			TTL Odd Red Channel Data 1
N7	E0_LVRX_CH4P	I	Positive input of LVDS RX E0 Channel 4
			TTL DCLK
M7	E0_LVRX_CH5N	I	TTL Even Blue Channel Data 6
L6	E0_LVRX_CH5P	I	TTL Even Blue Channel Data 9
M3	E0_LVRX_CH6N	I	TTL Even Green Channel Data 9
L4	E0_LVRX_CH6P	I	TTL Even Green Channel Data 8
N11	O0_LVRX_CLKN	I	Negative input of LVDS RX O0 Clock Channel
			TTL Odd Red Channel Data 8
M11	O0_LVRX_CLKP	I	Positive input of LVDS RX O0 Clock Channel
			TTL Odd Red Channel Data 7
P8	O0_LVRX_CH0N	I	Negative input of LVDS RX O0 Channel 0
			TTL Odd Green Channel Data 0
N8	O0_LVRX_CH0P	I	Positive input of LVDS RX O0 Channel 0
			TTL Odd Green Channel Data 1
N9	O0_LVRX_CH1N	I	Negative input of LVDS RX O0 Channel 1
			TTL Even Blue Channel Data 4
M9	O0_LVRX_CH1P	I	Positive input of LVDS RX O0 Channel 1
			TTL Even Blue Channel Data 3
M10	O0_LVRX_CH2N	I	Negative input of LVDS RX O0 Channel 2
			TTL Even Blue Channel Data 2
L10	O0_LVRX_CH2P	I	Positive input of LVDS RX O0 Channel 2
			TTL Odd Red Channel Data 2

Table 16. Digital video inputs (continue)

Pin	Assignment	I/O	Description
P12	O0_LVRX_CH3N	I	Negative input of LVDS RX O0 Channel 3
			TTL Odd Red Channel Data 6
N12	O0_LVRX_CH3P	I	Positive input of LVDS RX O0 Channel 3
			TTL Odd Red Channel Data 5
P13	O0_LVRX_CH4N	I	Negative input of LVDS RX O0 Channel 4
			TTL Odd Red Channel Data 4
13	O0_LVRX_CH4P	I	Positive input of LVDS RX O0 Channel 4
			TTL Odd Blue Channel Data 1
M8	O0_LVRX_CH5N	I	TTL Even Blue Channel Data 5
L9	O0_LVRX_CH5P	I	TTL Odd Red Channel Data 9
L11	O0_LVRX_CH6N	I	TTL Odd Green Channel Data 7
M12	O0_LVRX_CH6P	I	TTL Odd Red Channel Data 3

Table 17. Multi-function - digital audio output, general purpose input/output, bootstrap pins

Pin	Assignment	I/O	Description
E4	I2S_WCLK_GPIO_4	I/O	I2S_WCLK
			GPIO_4
C1	I2S_BCLK_GPIO_7	I/O	I2S_BCLK
			GPIO_7
D2	I2S_0_GPIO_8	I/O	I2S_0
			GPIO_8
F5	I2S_1_GPIO_9	I/O	I2S_1
			GPIO_9
F4	I2S_2_GPIO_10	I/O	I2S_2
			GPIO_10
D3	I2S_3_GPIO_11	I/O	I2S_3
			GPIO_11

Table 18. Multi-function and system interface connections

Pin	Assignment	I/O	Description
E6	RESETn	I/O	Reset (active low) signal. Connect to digital 3.3 V with a 2.7 K ohm pull-up resistor.
F3	TESTMODE0	I	Reserve for testing. Must be connected to system ground (GND)
G3	TESTMODE1	I	
D13	SPI_DI	I/O	SPI ROM Data Input.
C14	SPI_DO	I/O	SPI ROM Data Output.
E12	SPI_CLK	I/O	SPI ROM Clock
F10	SPI_CSn	I/O	SPI ROM Chip Select.
E5	PWM0_GPIO_0_BOOT3	I/O	PWM0
			BOOTSTRAP[3] Please refer to Bootstrap configuration table for description
			General Purpose Schmitt Trigger Input / Tri-state Output 0 [5V Tolerant]
D4	GPIO_1_BOOT2	I/O	General Purpose Schmitt Trigger Input / Tri-state Output 1 [5V Tolerant]
			BOOTSTRAP[2] Please refer to Bootstrap configuration table for description
G10	GPIO_2_BOOT5	I/O	General Purpose Schmitt Trigger Input / Tri-state Output 2 [5V Tolerant]
			BOOTSTRAP[5] Please refer to Bootstrap configuration table for description
F11	GPIO_3_BOOT6	I/O	BOOTSTRAP[6] Please refer to Bootstrap configuration table for description
			General Purpose Schmitt Trigger Input / Tri-state Output 3 [5V Tolerant]
E3	CLK_OUT_GPIO_5_BOOT0	I/O	CLK_OUT
			General Purpose Schmitt Trigger Input / Tri-state Output 5 [5V Tolerant]
			BOOTSTRAP[0] Please refer to Bootstrap configuration table for description
G4	IR_IN_GPIO_6	I/O	Infra-red Receiver Data Input
			General Purpose Schmitt Trigger Input / Tri-state Output 6 [5V Tolerant]
D12	IRQ_BOOT7_GPIO_12	I/O	IRQ
			BOOTSTRAP[7] Please refer to Bootstrap configuration table for description
			General Purpose Schmitt Trigger Input / Tri-state Output 12 [5V Tolerant]
C2	UART_TX_BOOT1_GPIO_13	I/O	UART Transmit Data Output.
			BOOTSTRAP[1] Please refer to Bootstrap configuration table for description
			General Purpose Schmitt Trigger Input / Tri-state Output 13 [5V Tolerant]

Table 18. Multi-function and system interface connections (continue)

Pin	Assignment	I/O	Description
B1	UART_RX_GPIO_14	I/O	UART Receive Data Input. Pull up with 4.7K ohm resistor.
			General Purpose Schmitt Trigger Input / Tri-state Output 14 [5V Tolerant]
C13	AUX_I2C_SCL_GPIO_15	I/O	I²C Serial Clock for DP AUX channel. This pin, along with AUX_I2C_SDA, creates external serial interface for DP AUX channel. Connect to digital 3.3V with 4.7K ohm resistor.
			General Purpose Schmitt Trigger Input / Tri-state Output 15 [5V Tolerant]
B14	AUX_I2C_SDA_GPIO_16	I/O	I²C Data Clock for DP AUX channel. This pin, along with AUX_I2C_SCL, creates external serial interface for DP AUX channel. Connect to digital 3.3V with 4.7K ohm resistor.
			General Purpose Schmitt Trigger Input / Tri-state Output 16 [5V Tolerant]
B12	AUX_UART_TX_BOOT4_GPIO_21	I/O	UART Transmit Data Output for DP AUX channel
			BOOTSTRAP[4] Please refer to Bootstrap configuration table for description
			General Purpose Schmitt Trigger Input / Tri-state Output 21 [5V Tolerant]
A12	AUX_UART_RX_GPIO_22	I/O	UART Receive Data Input for DP AUX channel. Pull up with 4.7K ohm resistor.
			General Purpose Schmitt Trigger Input / Tri-state Output 22 [5V Tolerant]
B13	I2C_SCL_GPIO_24	I/O	I²C_SCL. Pull up to 3.3V with 4.7K ohm resistor.
			General Purpose Schmitt Trigger Input / Tri-state Output 24 [5V Tolerant]
A13	I2C_SDA_GPIO_25	I/O	I²C_SDA. Pull up to 3.3V with 4.7K ohm resistor.
			General Purpose Schmitt Trigger Input / Tri-state Output 25 [5V Tolerant]

Table 19. No connects

Pin	Assignment	I/O	Description
F12	NC1	-	No connection.
G12	NC2	-	
D11	NC3	-	
E11	NC4	-	
B2	NC5	-	
B3	NC6	-	

Table 20. System power and ground

Pin	Assignment	I/O	Description
D6	VDDA_3V3	P	Analog 3.3V VDD. Connect to analog 3.3V with 0.1µF bypass capacitor to analog ground plane on board.
E7, E8, K6, K9	PVDD1	P	Digital 1.2V VDD. Connect to digital 1.2V with 0.1µF bypass capacitor.
G11	PVDD21	P	Digital 3.3V VDD. Connect to digital 3.3V with 0.1µF bypass capacitor. Must be connected at same voltage level.
G5	PVDD22		
A1, A14, F6, F7, F8, F9, G6, G7, G8, G9, H6, H7, H8, H9, J6, J7, J8, J9	PVSS3	G	Digital Ground. Each pin must be connected directly to digital ground plane.
B11, C7, C8, D9	DPTX_VDDA_1V2	P	DisplayPort Transmitter Analog 1.2V Power Supply. Must be bypassed with a 0.1µF capacitor to analog ground plane on board.
D7, D8, E9, E10	DPTX_VSSA	G	DisplayPort Transmitter VSS. Must be directly connected to analog ground plane on board.
D5	VDD33_TX	P	Analog 3.3V VDD. Connect to analog 3.3V with 0.1µF bypass capacitor to analog ground plane on board.
C5	VSSA_TX	G	Analog ground. Must connect directly to analog ground plane on board
H3, H12, L8, N1, N14	AVDD_OUT_LVRX_33	P	Analog 3.3V VDD. Connect to analog 3.3V with 0.1µF bypass capacitor to analog ground plane on board.
L7	AVDD_LVRX_12	P	Analog 1.2V VDD. Connect to analog 1.2V with 0.1µF bypass capacitor to analog ground plane on board.
K7	AVSS_LVTX	G	Analog ground. Must connect directly to analog ground plane on board.
F2, F13, H5, H10, K8, P1, P14	AVSS_OUT_LVRX	G	Analog ground. Must connect directly to analog ground plane on board.
A2	VSS_RPLL	G	Analog Ground for the DDS Reference PLL and Digital Core. Must be directly connected to analog ground plane on board.
A3	VDD_RPLL	P	Analog 1.2V Power Supply for RCLK PLL and Digital Core. Must be bypassed with a 0.1µF capacitor to analog ground plane on board.

Note: 1 PVDD21 and PVDD22 must be connected to same power supply.

2 Add 47 K pull-down resistor for HPD_IN signal.

6.2 Bootstrap configuration

During hardware reset, on the rising edge of RESETn, logic high or low configuration on Bootstrap pins are latched and stored. 4.7 K pull-up or pull-down resistors must be installed to indicate logic '1' or '0' status on the bootstrap pins. Bootstrap operation is only guaranteed with external pull-up or pull-down resistors. There are eight Bootstrap pins available on STDP4028. Some bootstraps may not be available for normal use.

Table 21. Bootstrap configuration

Pin #	Assignment	Function
E3	BOOT[0]	Set to 1 (Pull High to Vdd)
C2	BOOT[1]	Set to 0 (Pull Low to GND)
D4	BOOT[2]	Set to 0 (Pull Low to GND) for normal operation
E5	BOOT[3]	TTL_LVDS_OUT TTL/LVDS output mode selection 0 = Output is in LVDS format 1 = Output is in TTL format
B12	BOOT[4]	OCM_BOOT_SEL 0 = OCM boot will be from internal ROM code. (Internal ROM is 'ON' and mapped to top 32K of OCM address range) 1 = OCM boot is from external ROM/Flash code (Internal ROM is 'OFF' and external ROM/Flash mapped to top 512K of OCM address range)
G10	BOOT[5]	WIDE_NARROW_BUS Selects wide or narrow LVDS or TTL bus LVDS 0 = DUAL LVDS 1 = QUAD LVDS TTL 0 = Single 1 = Dual
F11	BOOT[6]	ASSR_ENABLE Selects whether ASSR is enabled 0 = Disabled 1 = Enabled
D12	BOOT[7]	I2C_DEV_ID I2C slave Device ID select for RD/WR access. 0: 0xE6, 0xE7 1: 0xE4, 0xE5

6.3 General purpose input/output (GPIO) pins

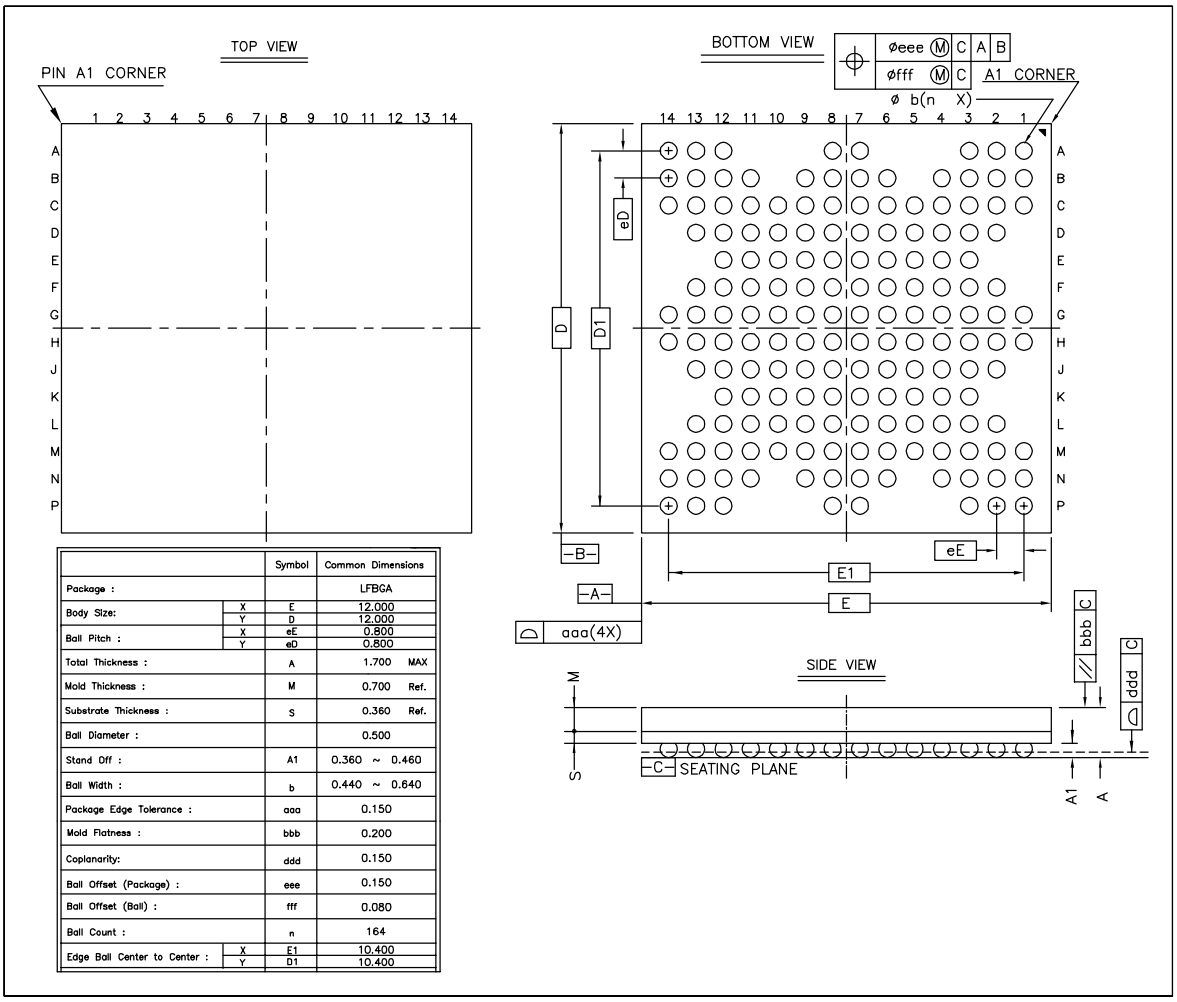
The STDP4028 contains 25 general-purpose input/output (GPIO) pins for system configuration purpose. GPIO_0, GPIO_1 are dedicated general-purpose IO pins and the rest have shared functionality. Each GPIO has independent direction control and open drain enable for reading and writing.

Note: The GPIO functionality is available only for custom applications. Default settings allow configuration of dedicated GPIO pins (GPIO_0 and GPIO_1) through host interface and the rest of the GPIO configuration requires over-riding the default feature using external firmware.

7. Package

Package type: 164 LFBGA (12 x 12 mm / ball pitch 0.8 mm)

Figure 24. Package specification

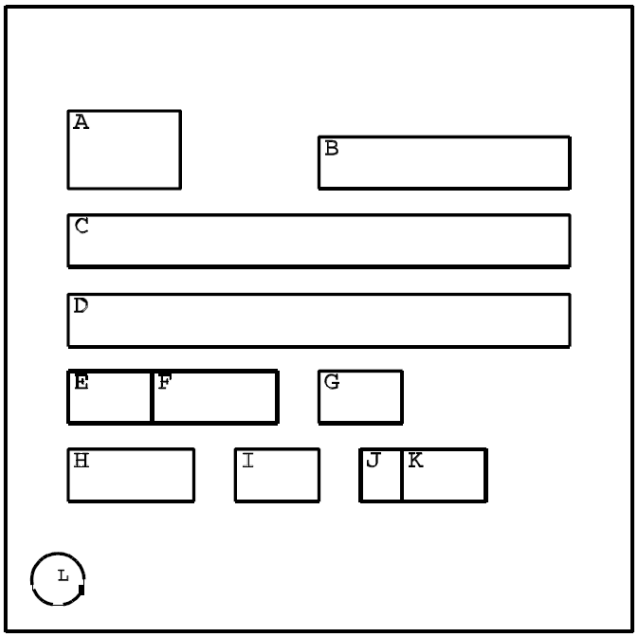


		Symbol	Common Dimensions
Package :			LFBGA
Body Size:	X	E	12.000
	Y	D	12.000
Ball Pitch :	X	eE	0.800
	Y	eD	0.800
Total Thickness :		A	1.700 MAX
Mold Thickness :		M	0.700 Ref.
Substrate Thickness :		S	0.360 Ref.
Ball Diameter :			0.500
Stand Off :		A1	0.360 ~ 0.460
Ball Width :		b	0.440 ~ 0.640
Package Edge Tolerance :		aaa	0.150
Mold Flatness :		bbb	0.200
Coplanarity:		ddd	0.150
Ball Offset (Package) :		eee	0.150
Ball Offset (Ball) :		fff	0.080
Ball Count :		n	164
Edge Ball Center to Center :	X	E1	10.400
	Y	D1	10.400

7.1 Marking field template and descriptors

The STDP4028 marking template is shown below.

Figure 25. Marking template



Field descriptors are shown below.

Table 22. Field descriptors

Field	Description	Marking
A	Company logo	
B	2-character version code	AB
C	Product code	STDP4028
D	8-character diffusion code	9R”ABCDEF”
E	2-character assembly plant code	AA
F	3-character BE sequence code	“XYZ”
G	2-character diffusion plant code	9R
H	3-character country of origin code	TWN
I	2-character test plant code	AA
J	1-digit assembly year	“Y”
K	2-digit assembly week	“WW”
L	Ball A1 identifier	a DOT

8. Electrical specification

8.1 Absolute maximum ratings

Applied conditions greater than those listed under “Absolute maximum ratings” may cause permanent damage to the device. The device should never exceed absolute maximum conditions since it may affect device reliability.

Table 23. Absolute maximum ratings

Parameter	Symbol	Min	Typ	Max	Units
3.3 V supply voltages (1,2)	$V_{VDD\_3.3}$	-0.3	3.3	3.6	V
1.2 V supply voltages (1.2)	$V_{VDD\_1.2}$	-0.3	1.2	1.26	V
Input voltage (5V tolerant inputs) (1,2)	$V_{IN5Vtol}$	-0.3	-	5.5	V
Input voltage (non 5V tolerant inputs) (1,2)	V_{IN}	-0.3	-	3.6	V
ESD - Human Body Model (HBM)(4)	V_{ESD}	-	-	±2.0	kV
ESD - Machine Model (MM)(4)	V_{ESD}	-	-	±200	V
ESD - Charged Device Model (CDM)(4)	V_{ESD}	-	-	±500	V
Latch-up	I_{LA}	-	-	±100	mA
Ambient operating temperature	T_A	0	-	70	°C
Storage temperature	T_{STG}	-40	-	150	°C
Operating junction temperature	T_J	0	-	125	°C
Thermal resistance (Junction to Ambient)(3)	θ_{JA}	-	-	36.6	°C/W
Thermal resistance (Junction to Case)(3)	θ_{JC}	-	-	18.1	°C/W
Peak IR reflow soldering temperature (<10 sec.)	T_{SOL}	-	-	260	°C

Note (1): All voltages are measured with respect to GND.

Note (2): Absolute maximum voltage ranges are for transient voltage excursions.

Note (3): These are simulated results under the following conditions - Four layer JEDEC PCB, no heat spreader, Air flow = 0 m/s

Note (4): The ESD result shown is not applicable for reserved pins.

8.2 Maximum speed of operation

System clocks

Crystal clock = 27 MHz typical

SPI_CLK = 50 MHz

I2C CLK = 400 kHz

Internal OCM clock = 100 MHz max

LVTTL input clocks

Video input: Single bus clocking

165 MHz max

Video input: Dual bus clocking

165 MHz max

LVDS input clocks

Single LVDS channel

Channel E0/O0: 150 MHz

Dual LVDS channel

Channel E0/O0: 150 MHz

Quad LVDS channel

Channel E0/O0/E1/O1: 100 MHz

Audio input

SPDIF LVTTL input = 12.288 MHz

I2S WS input = 192 kHz

I2S SCLK input = 12.288 MHz

DisplayPort transmitter bit rate

Main link

Min: 1.62 Gbps/lane Max:

3.24 Gbps/lane Auxiliary

channel: 1 Mbps

8.3 DC characteristics

Table 24. DC characteristics

Parameter	Symbol	Min	Typ	Max	Units
3.3 V supply voltages (analog and digital)	$V_{VDD\_3.3}$	3.0	3.3	3.6	V
1.2 V supply voltages (analog and digital)	$V_{VDD\_1.2}$	1.14	1.2	1.26	V
Power					
TTL input					
Power consumption: 2560 x 1600 / 60 Hz test pattern: ON-OFF dot Moire	4L	-	330	-	mW
Power consumption: 1920 x 1200 / 60 Hz test pattern: ON-OFF dot Moire	2L	-	270	-	mW
Power consumption: 1440 x 900 / 60 Hz test pattern: ON-OFF dot Moire	1L	-	230	-	mW
Standby		-	18	-	mW
Supply Current					
Measurement conditions: 2560 x 1600 / 60 Hz test pattern: ON-OFF dot Moire VDD (analog and digital power) = 3.3V DDA analog and digital power) =1.2V In all configuration, 8 bits input is used.		-	20 218	-	mA
Power					
LVDS input					
Power consumption: 1920 x 1080 / 120 Hz test pattern: ON-OFF dot Moire	4L	-	604	-	mW
Power consumption: 1920 x 1200 / 60 Hz test pattern: ON-OFF dot Moire	2L	-	400	-	mW
Power consumption: 1440 x 900 / 60 Hz test pattern: ON-OFF dot Moire	1L	-	312	-	mW
Standby		-	18	-	mW
Supply Current					
Measurement conditions: 1920 x 1080 / 120 Hz test pattern: ON-OFF dot Moire VDD (analog and digital power) = 3.3V DDA analog and digital power) =1.2V In all configuration, 8 bits input is used.		-	101 226	-	mA
Inputs					
High voltage	V_{IH}	2.0	-	VDD	V
Low voltage	V_{IL}	GND	-	0.8	V
High current (V_{IN} = 5.0 V)	I_{IH}	-25	-	25	µA
Low current (V_{IN} = 0.8 V)	I_{IL}	-25	-	25	µA
Capacitance (V_{IN} = 2.4 V)	C_{IN}	-	-	8	pF
Outputs					
High voltage (I_{OH} = 7 mA)	V_{OH}	2.4	-	VDD	V
Low voltage (I_{OL} = -7 mA)	V_{OL}	GND	-	0.4	V
Tri-state leakage current	I_{OZ}	-25	-	25	µA

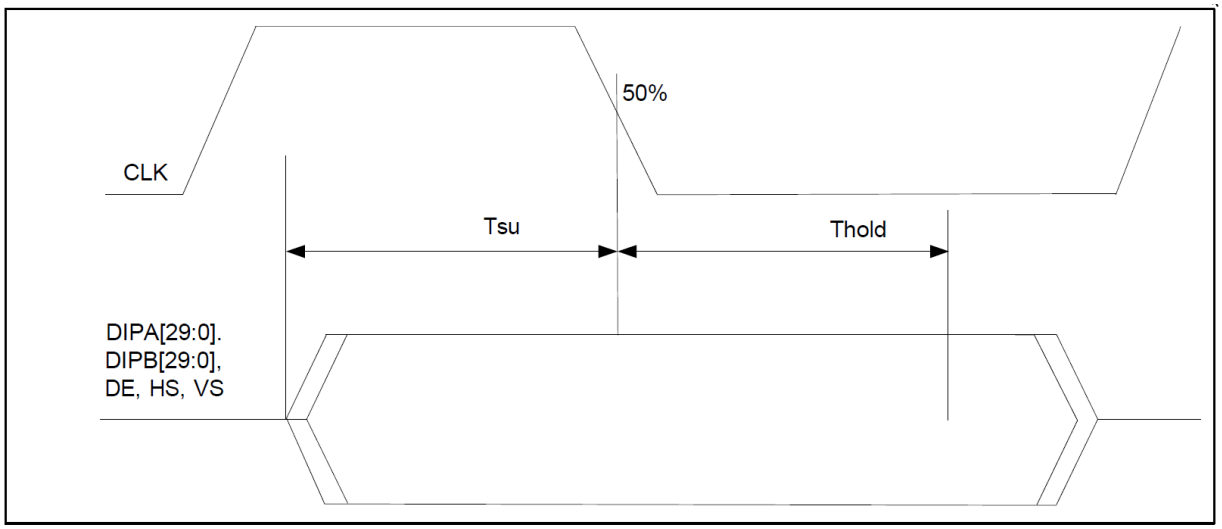
8.4 AC characteristics

8.4.1 Digital video input port DC characteristics

Table 25. Digital video input port DC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Low level input voltage		GND	-	+0.8	V
V_{IH}	High level input voltage		2.0	-	$V_{DD\_3.3}$	V
$I_{LI/O}$	I/O leak current		-	-	10	µA
Ci	Input capacitance	I/O at high impedance	-	-	4	pF
tcyc	DIP Clock cycle time		6	-	125	ns
Tsu	DIPE[29:0], DIPO[29:0], HS, VS, DE setup time		2	-	-	ns
Thold	DIPE[29:0], DIPO[29:0], HS, VS, DE hold time		2	-	-	ns

Figure 26. Digital video input timing



8.4.2 LVDS video input DC/AC characteristics

Table 26. LVDS video input DC/AC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	Differential input high voltage threshold	V_{CM} = 1.2V, *Figure 27*	-	-	100	mV
V_{IL}	Differential input low voltage threshold		-100	-	-	mV
V_{CM}	Common-mode Input voltage	*Note 1*	0.1	-	2.35	V
V_{ID}	Differential Input voltage		200	-	600	mV
$I_{IN-LEAK}$	Input leakage current	V_{IN} = 2.4V or V_{IN} = 0V, termination disabled	-	-	±10	µA
R_{TERM}	Integrated termination resistor		80	100	130	Ω
t_{TXBIT0}	Receiver LVDS input strobe position	Bit 0, *Figure 28*	0.61	-	1.33	ns
t_{TXBIT1}		Bit 1, *Figure 28*	2.54	-	3.26	ns
t_{TXBIT2}		Bit 2, *Figure 28*	4.47	-	5.19	ns
t_{TXBIT3}		Bit 3, *Figure 28*	6.4	-	7.12	ns
t_{TXBIT4}		Bit 4, *Figure 28*	8.33	-	9.05	ns
t_{TXBIT5}		Bit 5, *Figure 28*	10.26	-	10.98	ns
t_{TXBIT6}		Bit 6, *Figure 28*	12.19	-	12.91	ns
t_{PHD}	Phase delay time		-	241	-	ps
t_{DATA}	Data period	f_{CLOCK} = 74 MHz	-	1.93	-	ns
t_{RCVR_MARGIN}	Receiver margin	*Figure 29*, *Note 2*	-	370	-	ps
t_{STROBE}	Minimum strobe timing	*Figure 29*, f_{CLOCK} = 74 MHz, *Note 2*	720	800	-	ps
$t_{TXBITMIN}$	Clock to data skew margin	*Figure 29*	-200	-	-	ps
$t_{TXBITMAX}$		*Figure 29*	-	-	+200	ps

Note: 1 The common-mode range is guaranteed by design. The LVDS receiver is tested with V_{CM} = 1.2V.

2 The LVDS receiver inputs can tolerate jitter added within the receiver margin (t_{RCVR_MARGIN}) specification.

Figure 27. LVDS single-ended waveform

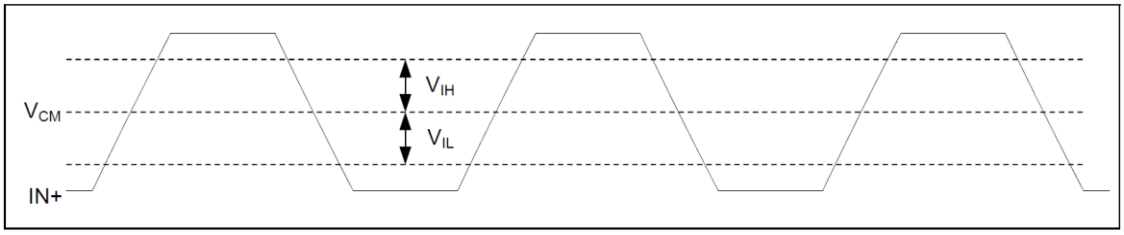


Figure 28. Receiver strobe positions LVDS input

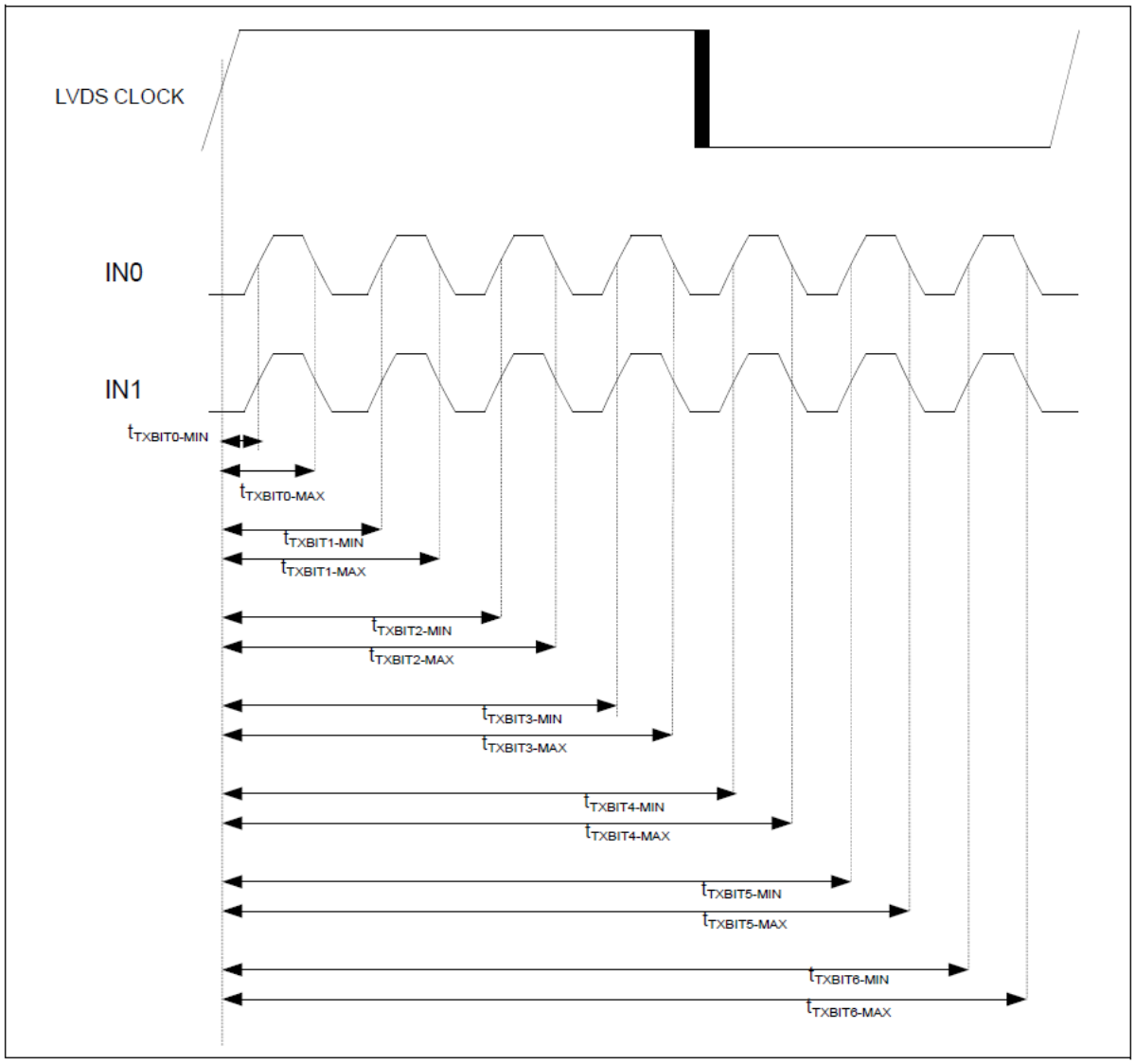
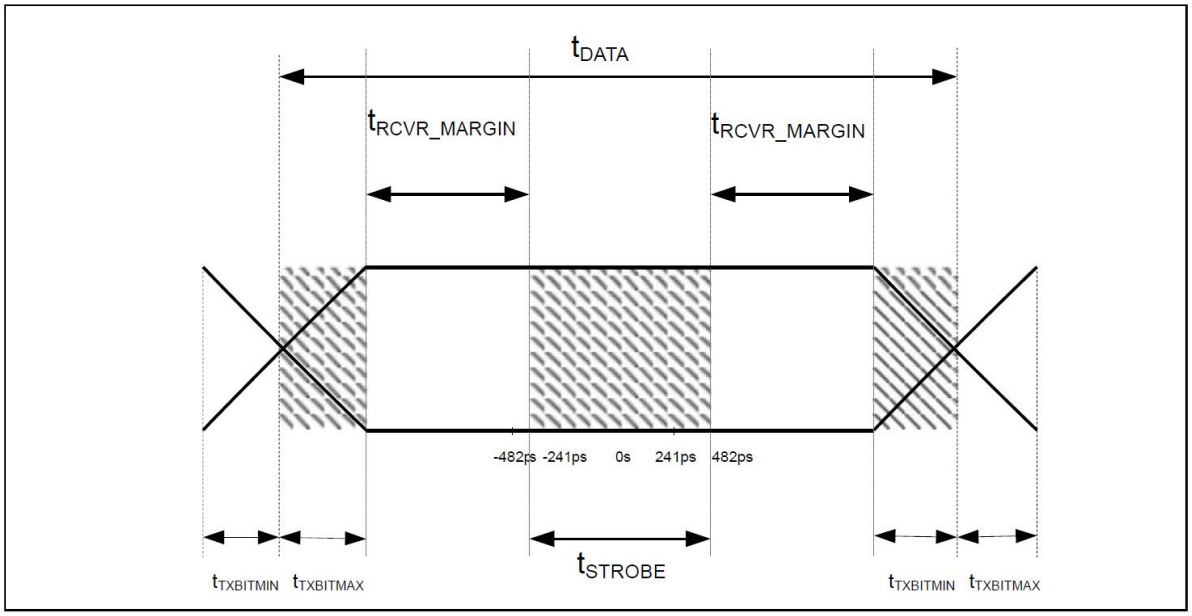


Figure 29. Receiver margins

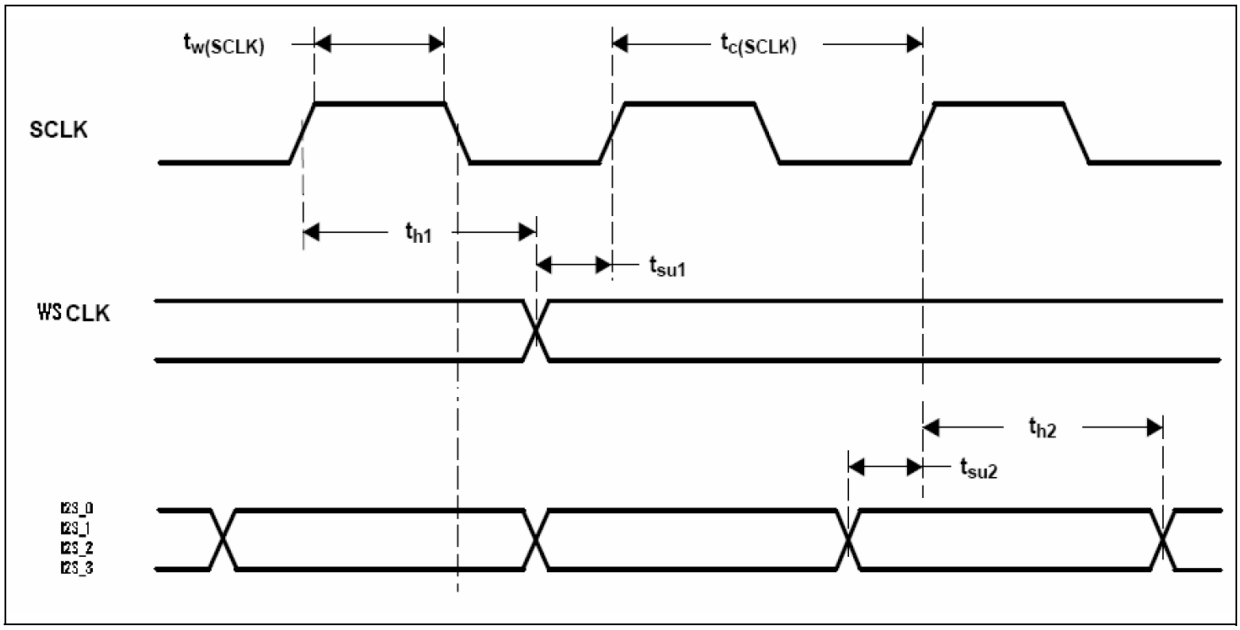


8.4.3 Digital audio input I2S timing

Table 27. Digital audio input I2S timing

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
fs	Sample frequency		32	-	192	kHz
$t_{c(sclk)}$	SCLK cycle time		-	81.38	-	ns
$t_{w(sclk)}$	SCLK pulse duration, SCLK high time		$0.4t_{c(sclk)}$	$0.5t_{c(sclk)}$	$0.6t_{c(sclk)}$	ns
f_{sclk}	SCLK (bit clock) frequency = rate x sample frequency (fs)	Maximum bit clock freq.	-	-	9.216	MHz
		64 x 32 kHz (32 kHz)	-	2.048	-	MHz
		6 4x 44.1 kHz (44.1kHz)	-	2.822	-	MHz
		64 x 48 kHz (48 kHz)	-	3.072	-	MHz
		64 x 96 kHz (96 kHz)	-	6.144	-	MHz
		64 x 192 kHz (192 kHz)	-	12.288	-	MHz
t_{su1}	Hold time, WS clock from SCLK rising edge		$0.5\ t_{c(sclk)}$	-	-	ns
t_{h1}	Setup time, WS clock to SCLK rising edge		10	-	-	ns
t_{su2}	Setup time, I2S data in to SCLK rising edge		10	-	-	ns
t_{h2}	Hold time, I2S data in to SCLK rising edge		10	-	-	ns

Figure 30. Digital audio I2S input timing



8.4.4 DisplayPort transmitter

Table 28. DisplayPort transmitter characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Comments
UI_High_Rate	Unit interval for high bit rate (2.7 Gbps/lane)	-	370	-	ps	Range is nominal +/- 300ppm. UI does not account for down-spread dictated variations.
UI_Low_Rate	Unit interval for reduced bit rate (1.62 Gbps/lane)	-	617	-	ps	
UI_Rate_3.24Gbps	Unit interval for high bit rate (3.24 Gbps/lane)	-	3.24	-	Gbps	
Down_Spread_Amplitude	Link clock down spreading	0	-	0.5	%	
Down_Spread_Frequency	Link clock down-spreading frequency	30	-	33	kHz	
VTX-DIFFp-p-Level1	Differential peak-to-peak output voltage Level 1	0.34	0.4	0.46	V	Refer to DisplayPort Specification for definition of differential voltage.
VTX-DIFFp-p-Level2	Differential peak-to-peak output voltage Level 2	0.51	0.6	0.68	V	
VTX-DIFFp-p-Level3	Differential peak-to-peak output voltage Level 3	0.69	0.8	0.92	V	
VTX-DIFFp-p-Level4	Differential peak-to-peak output voltage Level 4	1.01	1.2	1.38	V	
VTX-PREEMP-RATIO	No pre-emphasis	0.0	-	9.5	dB	Refer to DisplayPort Specification for definition of differential voltage. Support of no pre-emphasis, 3.5- and 6.0-dB pre-emphasis mandatory. 9.5-dB level optional.
	3.5 dB pre-emphasis level	2.8	3.5	4.2	dB	
	6.0 dB pre-emphasis level	4.8	6.0	7.2	dB	
	9.5 dB pre-emphasis level	7.6	9.5	11.4	dB	
Tx horizontal eye specification for high bit rate						
TTX-EYE_CHIP_High_Rate	Minimum transmitter eye width at Tx package pins	0.74	-	-	UI	
TTX-EYE-MEDIAN-to-MAX-JITTER_CHIP_High_Rate	Maximum time between the jitter median and maximum deviation from the median at Tx package pins	-	-	0.13	UI	
Tx horizontal eye specification for reduced bit rate						
TTX-EYE_CHIP_Low_Rate	Minimum transmitter eye width at Tx package pins	0.84	-	-	UI	
TTX-EYE-MEDIAN-to-MAX-JITTER_CHIP_Low_Rate	Maximum time between the jitter median and maximum deviation from the median at Tx package pins	-	-	0.08	UI	

Table 28. DisplayPort transmitter characteristics (continue)

Symbol	Parameter	Min	Typ	Max	Unit	Comments
TTX-RISE_CHIP, TTX-FALL_CHIP	D+/D- TX output rise/fall time at Tx package pins	50	-	130	ps	At 20-to-80%
VTX-DC-CM	TX DC common mode voltage	0	-	VDD	V	Common mode voltage is equal to Vbias_Tx voltage. VDD is the output driver power supply voltage and 3.6 V maximum.
ITX-SHORT	TX short circuit current limit	-	-	90	mA	Total drive current of the transmitter when it is shorted to its ground.
RLTX-DIFF	Differential return loss at 0.675 GHz	-	-	12	dB	Straight loss line between 0.675 GHz and 1.35 GHz
	Differential return loss at 1.35 GHz	-	-	9	dB	
LTX-SKEW-INTER_CHIP	Lane-to-lane skew at TX package pins	-	-	2	UI	
LTX-SKEW-INTRA_CHIP	Lane intra-pair output skew at Tx package pins	-	-	20	ps	
CTX	AC coupling capacitor	75	-	200	nF	All DisplayPort Main Link lanes as well as AUX CH shall be AC coupled. AC coupling capacitors shall be placed on the transmitter side. Placement of AC coupling capacitors on the receiver side is optional.
FTX-REJECTION-BW	Clock jitter rejection bandwidth	-	-	4	MHz	

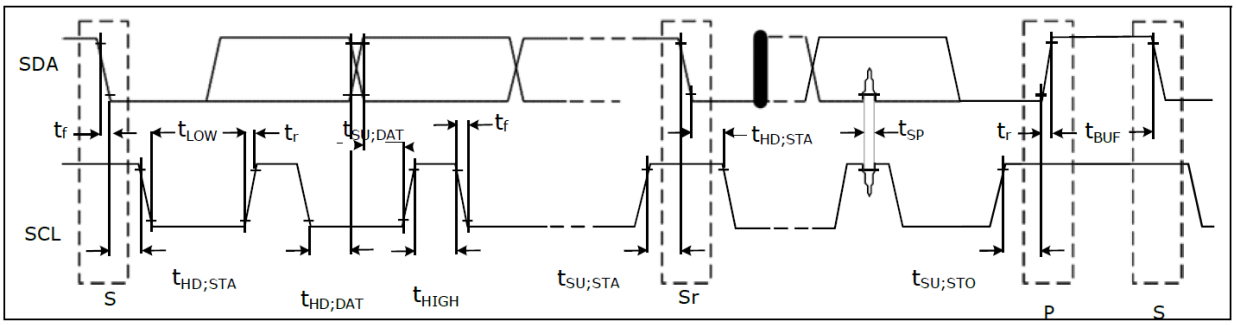
8.4.6 I2C interface timing

Table 29. I2C interface timing

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCL}	SCL clock rate	Fast mode	0	-	400	kHz
t_{HD-STA}	Hold time START	After this period, the 1st clock starts	0.6	1.1	-	µs
t_{LOW}	Low period of clock	SCL	1.3	1.12	-	µs
t_{HIGH}	High period of clock	SCL	0.6	1.0	-	µs
$T_{su;STA}$	Setup time for a repeated START		0.6	1.4	-	µs
$t_{HD;DAT}$	Data hold time	For master	0	0.72	0.9(1)	µs
$t_{SU;DAT}$	Data setup time		100	400	-	ns
T_{BUF}	Bus free time between STOP and START		1.3	140	-	µs
C_b	Capacitance load for each bus line		-	-	400	pF
t_r	Rise time		20	195	300	ns
t_f	Fall time		20	10	300	ns
V_{nh}	Noise margin at high level		0.2 VDD	0.34	-	V
V_{nl}	Noise margin at low level		0.1 VDD	0.16	-	

Note: *The maximum $t_{HD;DAT}$ only has to be met if the device does not stretch the low period t_{LOW} of the SCL signal. In the diagram below, S = start, P = stop, Sr = Repeated start, and SP= Repeated stop conditions.*

Figure 31. I2C Timing



8.4.7 SPI interface timing

Table 30. SPI interface timing, VDD = 3.3V

Symbol	Parameter	Min	Max	Units
F_{CLK}	Serial clock frequency	-	50	MHz
T_{SCKH}	Serial clock high time	9	-	ns
T_{SCKL}	Serial clock low time	9	-	ns
T_{SCKR}	Serial clock rise time (slew rate)	0.1	-	V/ns
T_{SCKF}	Serial clock fall time (slew rate)	0.1	-	V/ns
T_{CES}	CE# active setup time	5	-	ns
T_{CEH}	CE# active hold time	5	-	ns
T_{CHS}	CE# not active setup time	5	-	ns
T_{CHH}	CE# not active hold time	5	-	ns
T_{CPH}	CE# high time	50	-	ns
T_{CHZ}	CE# high to high-Z output	-	8	ns
T_{CLZ}	SCK low to low-Z output	0	-	ns
T_{DS}	Data in setup time	5	-	ns
T_{DH}	Data in hold time	5	-	ns
T_{OH}	Output hold from SCK change	0	-	ns
T_V	Output valid from SCK	-	8	ns

Figure 32. SPI output or serial interface SPI ROM input timing

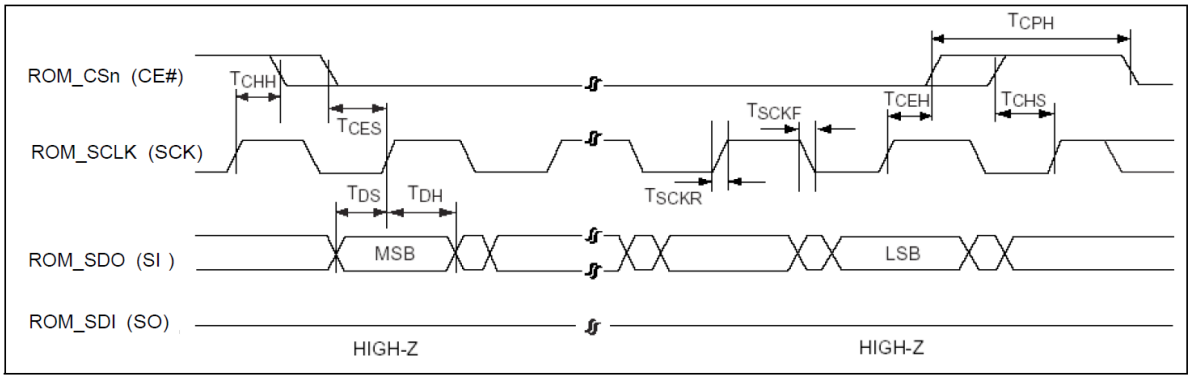
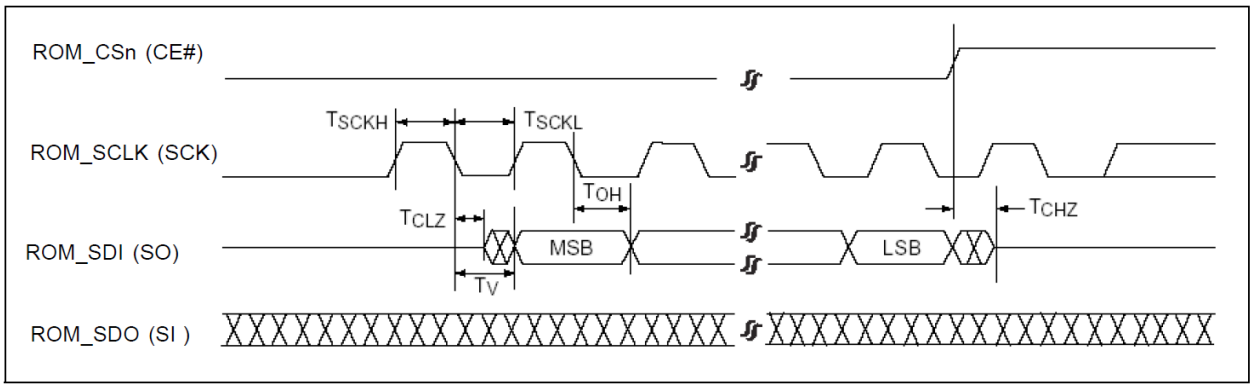


Figure 33. SPI input or serial interface SPI ROM output timing



9. Ordering information

Table 31. Order codes

Part Number	Operating Temperature	Package
STDP4028-AB	0°C to +70°C	164 LFBGA (12 x 12 mm)

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Kinetic Technologies:

STDP4028-AB RD2-4028